

Dual Channel, Ultra-Low Resistance Load Switch

General Description

The EM5209 is a small, ultra-low RON, dual channel load switch with controlled turn on. The device contains two N-channel MOSFETs that can operate over an input voltage range of 0.8V to 5.5V and can support a maximum continuous current of 6A per channel. Each switch is independently controlled by an on/off input (ON1 and ON2), which is capable of interfacing directly with low-voltage control signals. In EM5209, a 220-Ω on-chip load resistor is added for quick output discharge when switch is turned off.

The EM5209 is available in a small, space-saving DFN3X2 package with integrated thermal pad allowing for high power dissipation.

Ordering Information

Part Number	Package	Remark
EM5209VF	DFN3X2-14L	

Features

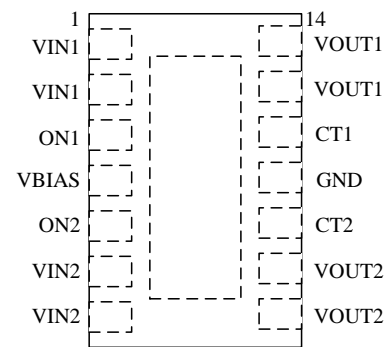
- Integrated dual channel load switch
- Input voltage range : 0.8V to 5.5V
- Ultra low R_{ON} resistance 20mΩ per channel
- 6A maximum continuous switch current per channel
- Low quiescent current 75uA (dual channel)
- Adjustable output rising time
- Quick Output Discharge (QOD)
- DFN3X2 14-pin package with Thermal Pad
- Bias voltage supports : 2.5V and 5.5V
- Over Temperature Protection

Applications



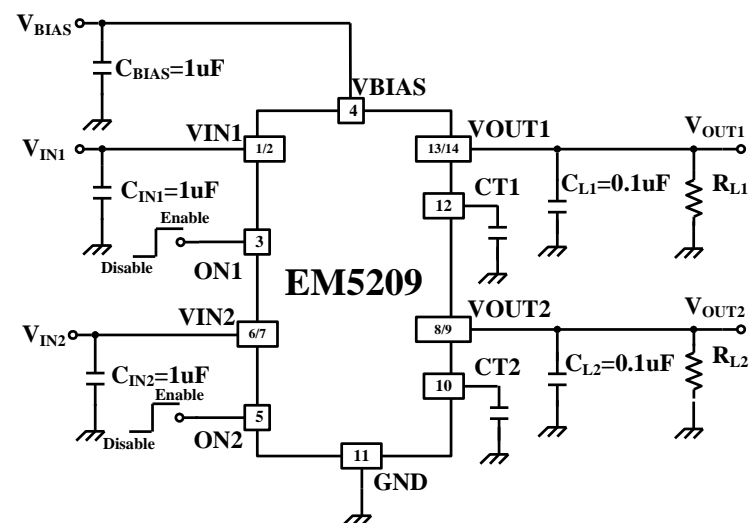
- Ultrabook
- Notebooks & Netbooks
- Tablet PC
- Consumer electronics
- Set-top boxes/Residential gateway
- Telecom systems
- Solid State Drives (SSD)

Pin Configuration



DFN3X2 14L
TOP VIEW

Typical Application Circuit

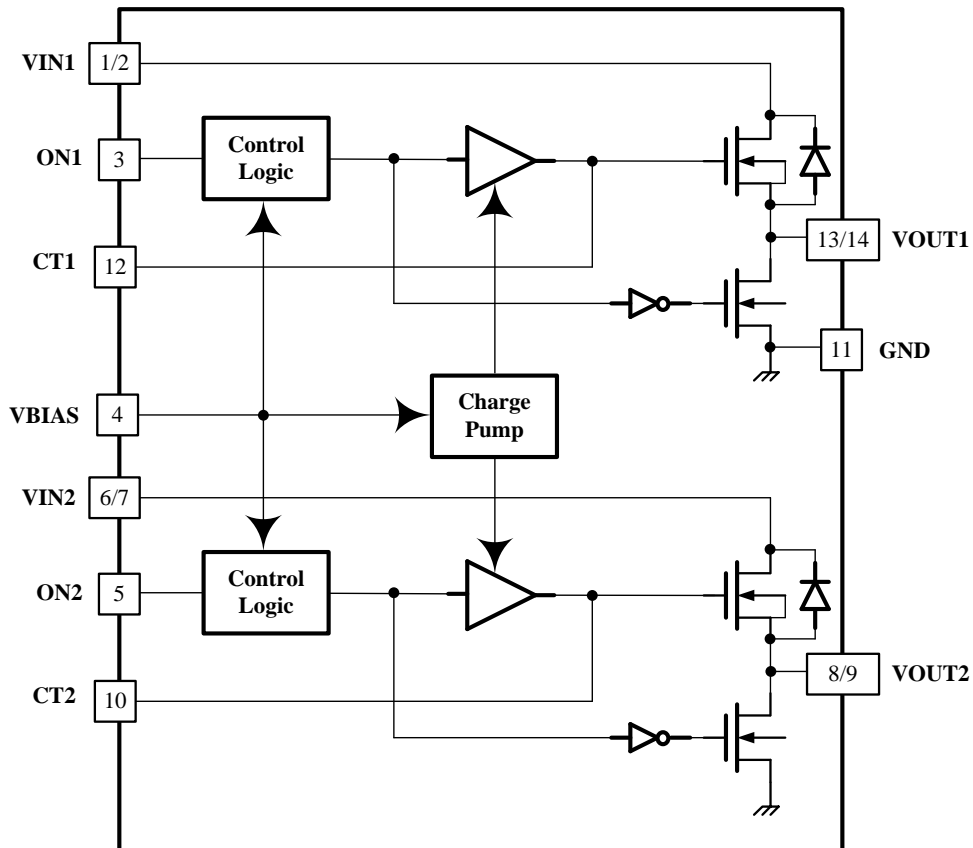




Pin Assignment

Pin Name	Pin No.	Pin Function
VIN1	1 / 2	Switch #1 input. Bypass this input with a ceramic capacitor to GND. Recommended voltage range for this pin for optimal R_{ON} performance is 0.8V to VBIAS. ($VIN1 \leq VBIAS$)
ON1	3	Active high switch #1 control input. Do not leave floating.
VBIAS	4	Bias voltage. Power supply to the device. Recommended voltage range for this pin is 2.5V to 5.5V.
ON2	5	Active high switch #2 control input. Do not leave floating.
VIN2	6 / 7	Switch #2 input. Bypass this input with a ceramic capacitor to GND. Recommended voltage range for this pin for optimal R_{ON} performance is 0.8V to VBIAS. ($VIN2 \leq VBIAS$)
VOUT2	8 / 9	Switch #2 output.
CT2	10	Switch #2 slew rate control. Can be left floating.
GND	11	Ground
CT1	12	Switch #1 slew rate control. Can be left floating.
VOUT1	13 / 14	Switch #1 output.
Thermal PAD	15	Thermal pad (exposed center pad) to alleviate thermal stress. Tie to GND.

Function Block Diagram



Absolute Maximum Ratings (Note1)

- $V_{IN1,2}$ ----- -0.3V to +6.0V
- $V_{OUT1,2}$ ----- -0.3V to +6.0V
- V_{BIAS} ----- -0.3V to +6.0V
- $V_{ON1,2}$ ----- -0.3V to +6.0V
- Maximum Peak Switch Current Per Channel, Pulse<300uS, 2% Duty-----8A
- Maximum Switch Current Per Channel, I_{MAX} ----- 6A
- Power Dissipation, P_D @ $T_A = 25^\circ C$, DFN3X2 ----- 1.53W
- Package Thermal Resistance, θ_{JA} , DFN3X2 (Note 2)----- 65°C/W
- Junction Temperature----- 150°C
- Lead Temperature (Soldering, 10 sec.)----- 260°C
- Storage Temperature ----- -65°C to 150°C
- ESD susceptibility (Note3)
 - HBM (Human Body Mode) ----- 2KV
 - MM (Machine Mode) ----- 200V
 - CDM (Charged-Device Model) ----- 1KV

Recommended Operating Conditions (Note4)

- Bias Voltage, V_{BIAS} ----- +2.5V to +5.5V
- Supply Input Voltage, $V_{IN1,2}$ ----- +0.8V to V_{BIAS}
- ON Voltage $V_{ON1,2}$ High-level input voltage ----- +1.2V to +5.5V
 $V_{ON1,2}$ Low-level input voltage ----- +0V to +0.6V
- Junction Temperature ----- -40°C to 125°C
- Ambient Temperature ----- -40°C to 85°C
- Input capacitor $C_{IN1,2}$ ----- $\geq 1\mu F$

Electrical Characteristics
 $V_{BIAS} = 5V$, $T_A = 25^\circ C$, unless otherwise specified

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units	
Power Supplies and Currents Section							
VBIAS Quiescent current (both channels)	$I_{BIAS-ON-both}$	$I_{OUT1} = I_{OUT2} = 0$, $V_{IN1,2} = V_{ON1,2} = V_{BIAS} = 5V$		75	100	uA	
VBIAS Quiescent current (single channel)	$I_{BIAS-ON-single}$	$I_{OUT1} = I_{OUT2} = 0$, $V_{ON2} = 0V$ $V_{IN1,2} = V_{ON1} = V_{BIAS} = 5V$		60		uA	
VBIAS Shutdown current	$I_{BIAS-OFF}$	$V_{OUT1,2} = 0V$, $V_{ON1,2} = 0V$ $V_{IN1,2} = V_{BIAS} = 5V$			2	uA	
$V_{IN1,2}$ Off state supply current (per channel)	$I_{VIN-OFF}$	$V_{OUT1,2} = 0V$, $V_{ON1,2} = 0V$	$V_{IN1,2} = 5.0V$		2	uA	
			$V_{IN1,2} = 3.3V$		2		
			$V_{IN1,2} = 1.8V$		2		
			$V_{IN1,2} = 0.8V$		1		
ON pin leakage current	I_{ON}	$V_{ON} = 5.5V$			1	uA	
Resistance Section							
ON-state Resistance	R_{ON}	$I_{OUT} = 200mA$, $V_{BAIS} = 5.0V$	$V_{IN} = 5.0V$		20	25	mΩ
			$V_{IN} = 3.3V$		20	25	
			$V_{IN} = 1.8V$		20	25	
			$V_{IN} = 1.5V$		20	25	
			$V_{IN} = 1.2V$		20	25	
			$V_{IN} = 0.8V$		20	25	

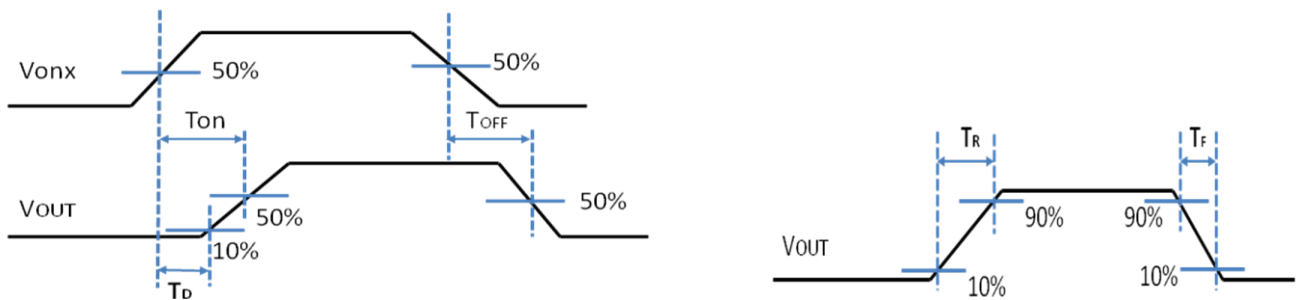


Output Pull-down Resistance	R_{PD}	$V_{IN} = 5.0V, V_{ON} = 0V, I_{OUT} = 15mA$		220	300	Ω
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$V_{BIAS} = 2.5V, T_A = 25^\circ C$, unless otherwise specified

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units	
Power Supplies and Currents Section							
VBIAS Quiescent current (both channels)	$I_{BIAS-ON-both}$	$I_{OUT1} = I_{OUT2} = 0,$ $V_{IN1,2} = V_{ON1,2} = V_{BIAS} = 2.5V$		25	37	μA	
VBIAS Quiescent current (single channel)	$I_{BIAS-ON-single}$	$I_{OUT1} = I_{OUT2} = 0, V_{ON2} = 0V$ $V_{IN1,2} = V_{ON1} = V_{BIAS} = 2.5V$		20		μA	
VBIAS Shutdown current	$I_{BIAS-OFF}$	$V_{OUT1,2} = 0V, V_{ON1,2} = 0V$ $V_{IN1,2} = V_{BIAS} = 2.5V$			2	μA	
$V_{IN1,2}$ Off state supply current (per channel)	$I_{VIN-OFF}$	$V_{OUT1,2} = 0V,$ $V_{ON1,2} = 0V$	$V_{IN1,2} = 2.5V$		2	μA	
			$V_{IN1,2} = 1.8V$		2		
			$V_{IN1,2} = 1.2V$		2		
			$V_{IN1,2} = 0.8V$		1		
ON pin leakage current	I_{ON}	$V_{ON} = 5.5V$			1	μA	
Resistance Section							
ON-state Resistance	R_{ON}	$I_{OUT} = 200mA,$ $V_{BIAS} = 2.5V$	$V_{IN} = 2.5V$		22	29	$m\Omega$
			$V_{IN} = 1.8V$		22	29	
			$V_{IN} = 1.5V$		22	29	
			$V_{IN} = 1.2V$		22	29	
			$V_{IN} = 0.8V$		22	29	
Output Pull-down Resistance	R_{PD}	$V_{IN} = 2.5V, V_{ON} = 0V, I_{OUT} = 1mA$		260	320	Ω	
ON Input Supply							
High-level input voltage	V_{ON-H}		1.2			V	
Low-level input voltage	V_{ON-L}				0.6	V	
Over Temperature Protection							
Over Temperature Protection	T_{OTP}			150		$^\circ C$	
Hysteresis	T_{HYS}			30		$^\circ C$	

Switching Timing Diagrams



Switching characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
$V_{IN} = V_{ON} = V_{BIAS} = 5V, T_A = 25^\circ C$						
Turn-on time	T_{ON}	$R_L = 10\Omega, C_L = 0.1\mu F, C_T = 1000pF$		1200		μS
Turn-off time	T_{OFF}	$R_L = 10\Omega, C_L = 0.1\mu F, C_T = 1000pF$		6		μS
Vout Rising time	T_R	$R_L = 10\Omega, C_L = 0.1\mu F, C_T = 1000pF$		1700		μS

Vout falling time	T_F	$R_L=10\Omega, C_L=0.1\mu F, C_T=1000pF$	7	μS
ON Delay time	T_D	$R_L=10\Omega, C_L=0.1\mu F, C_T=1000pF$	200	μS
$V_{IN}=0.8V, V_{ON}=V_{BIAS}=5V, T_A=25^\circ C$				
Turn-on time	T_{ON}	$R_L=10\Omega, C_L=0.1\mu F, C_T=1000pF$	360	μS
Turn-off time	T_{OFF}	$R_L=10\Omega, C_L=0.1\mu F, C_T=1000pF$	10	μS
Vout Rising time	T_R	$R_L=10\Omega, C_L=0.1\mu F, C_T=1000pF$	300	μS
Vout falling time	T_F	$R_L=10\Omega, C_L=0.1\mu F, C_T=1000pF$	4	μS
ON Delay time	T_D	$R_L=10\Omega, C_L=0.1\mu F, C_T=1000pF$	200	μS
$V_{IN}=V_{ON}=V_{BIAS}=3.3V, T_A=25^\circ C$				
Turn-on time	T_{ON}	$R_L=10\Omega, C_L=0.1\mu F, C_T=1000pF$	1900	μS
Turn-off time	T_{OFF}	$R_L=10\Omega, C_L=0.1\mu F, C_T=1000pF$	8	μS
Vout Rising time	T_R	$R_L=10\Omega, C_L=0.1\mu F, C_T=1000pF$	2300	μS
Vout falling time	T_F	$R_L=10\Omega, C_L=0.1\mu F, C_T=1000pF$	7	μS
ON Delay time	T_D	$R_L=10\Omega, C_L=0.1\mu F, C_T=1000pF$	500	μS
$V_{IN}=0.8V, V_{ON}=V_{BIAS}=3.3V, T_A=25^\circ C$				
Turn-on time	T_{ON}	$R_L=10\Omega, C_L=0.1\mu F, C_T=1000pF$	900	μS
Turn-off time	T_{OFF}	$R_L=10\Omega, C_L=0.1\mu F, C_T=1000pF$	10	μS
Vout Rising time	T_R	$R_L=10\Omega, C_L=0.1\mu F, C_T=1000pF$	700	μS
Vout falling time	T_F	$R_L=10\Omega, C_L=0.1\mu F, C_T=1000pF$	4	μS
ON Delay time	T_D	$R_L=10\Omega, C_L=0.1\mu F, C_T=1000pF$	500	μS

- Note 1.** Stresses listed as the above “Absolute Maximum Ratings” may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.
- Note 2.** θ_{JA} is measured in the natural convection at $T_A=25^\circ C$ on a 4-layers high effective thermal conductivity test board with minimum copper area of JEDEC 51-7 thermal measurement standard.
- Note 3.** Devices are ESD sensitive. Handling precaution is recommended.
- Note 4.** The device is not guaranteed to function outside its operating conditions.

Output Rising Time Control

The table as below contains rise time values measured on a typical device. Rise time shown below are only valid for the power-on sequence where V_{IN} and V_{BIAS} are already in steady state condition, and the V_{ON} is high.

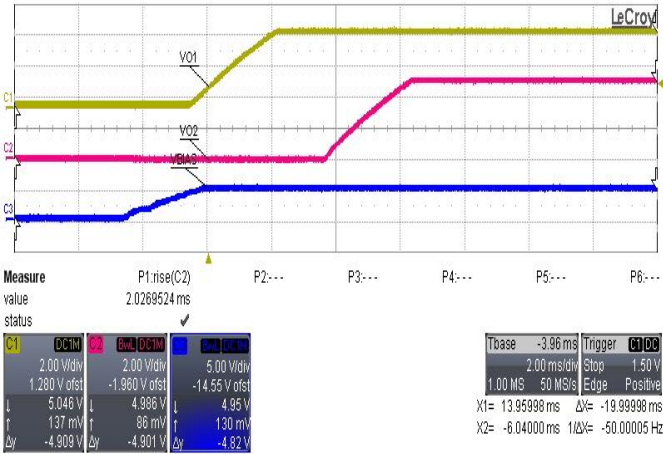
Rise Time (μs)		10%-90% V_o Rising Time, $V_{ON}=V_{BIAS}=5V, R_L=10\Omega, C_{IN}=1\mu F, C_L=0.1\mu F, T_A=25^\circ C$						
	CT (nF)	0.8V	1.05V	1.5V	1.8V	2.5V	3.3V	5V
EM5209VF	0	38.5	45.4	60.1	67.4	82.4	99.7	127.6
	0.22	101	123	169	189	273	343	501
	0.47	164	206	294	352	489	646	979
	1	315	398	526	651	861	1204	1890
	2.2	654	823	1140	1470	1930	2680	4180
	4.7	1370	1790	2590	3080	4280	5570	8680
	10	3080	4660	5290	6380	8930	12000	18100

Table1

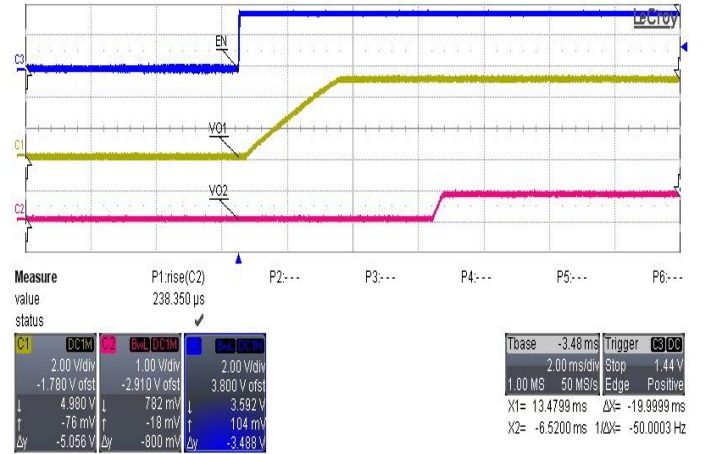
Typical Operating Characteristics

$V_{BIAS}=5V$; $C_{IN}=1\mu F$; $C_L=0.1\mu F$; $T_A=25^\circ C$

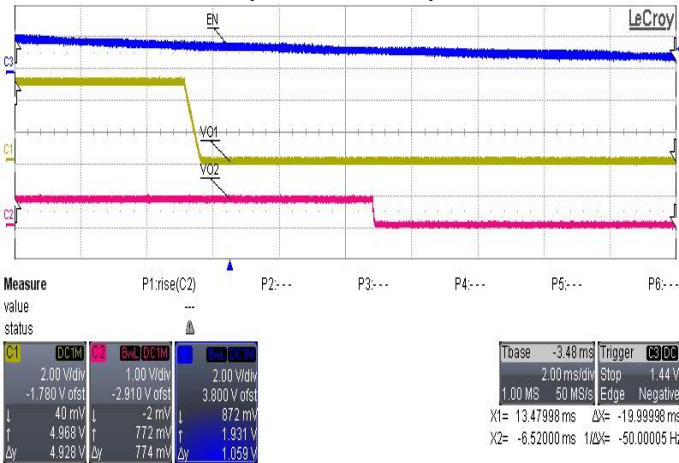
**Turn-ON from V_{BIAS}
(Both Channel)**



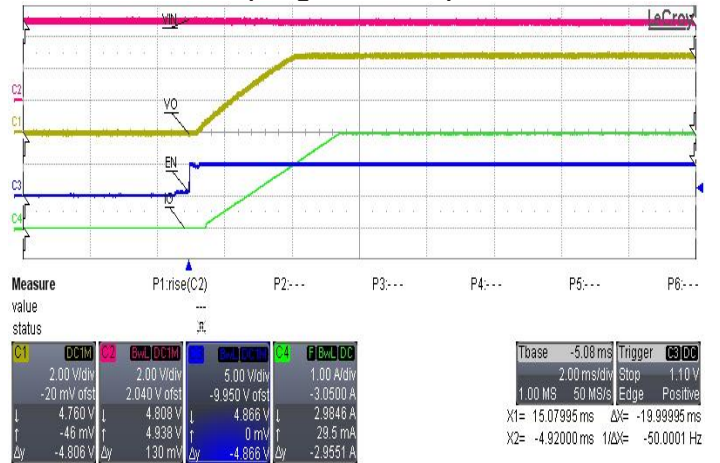
**Turn-ON from $V_{ON1}&V_{ON2}$
(Both Channel)**



**Turn-OFF from $V_{ON1}&V_{ON2}$
(Both Channel)**

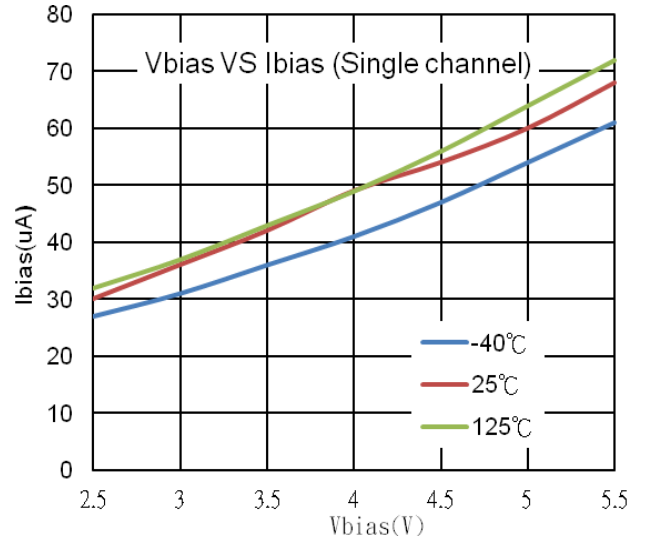
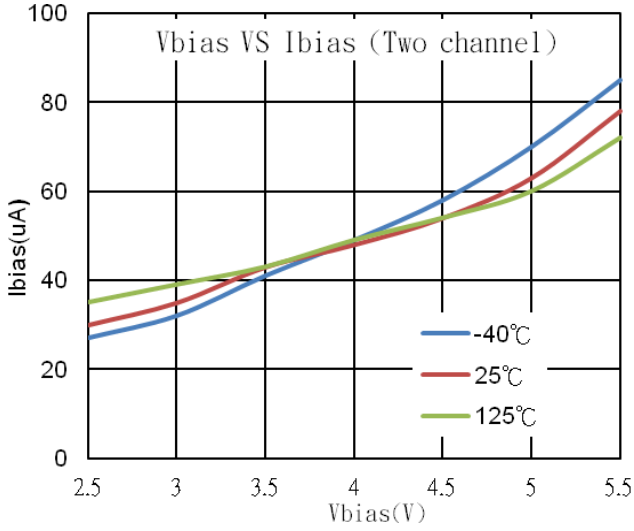


**Turn-ON when Heavy load (3A)
(Single Channel)**



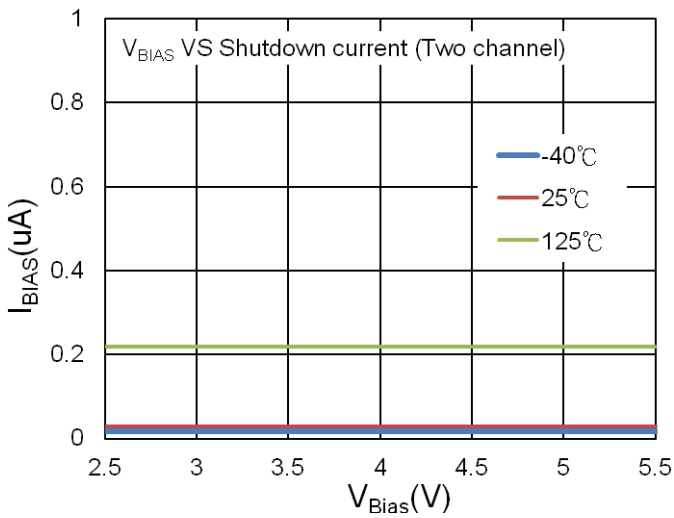
**V_{BIAS} vs. Quiescent Current
(Two Channel)**

**V_{BIAS} vs. Quiescent Current
(Single Channel)**

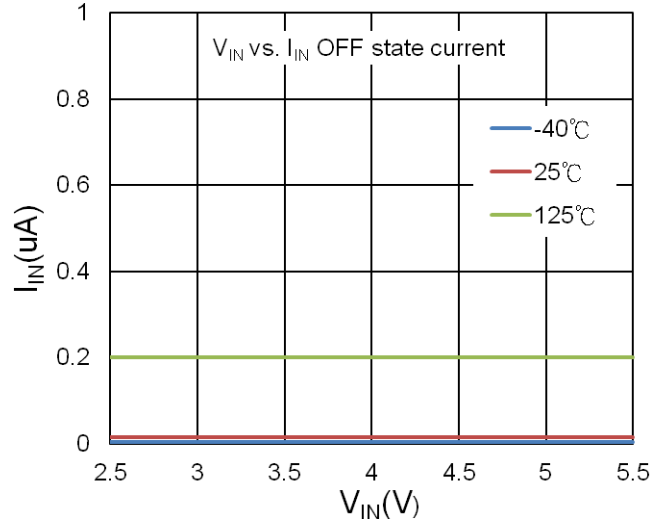


Typical Operating Characteristics

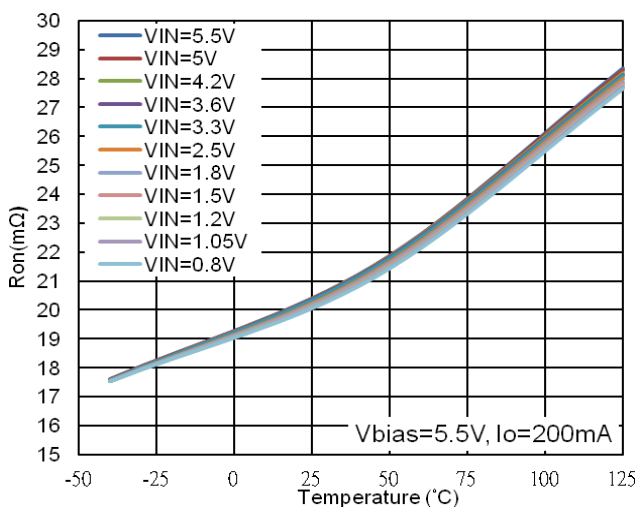
V_{BIAS} vs. Shutdown Current (Two Channel)



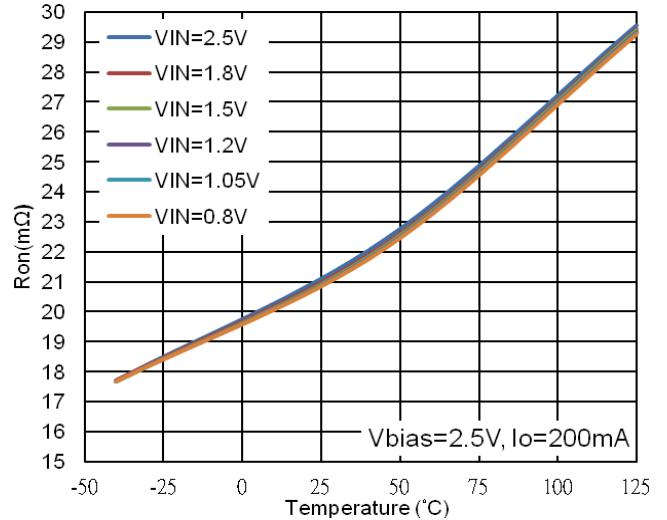
V_{IN} vs. OFF-State Supply Current



R_{ON} vs. Temperature (V_{BIAS}=5.5V)

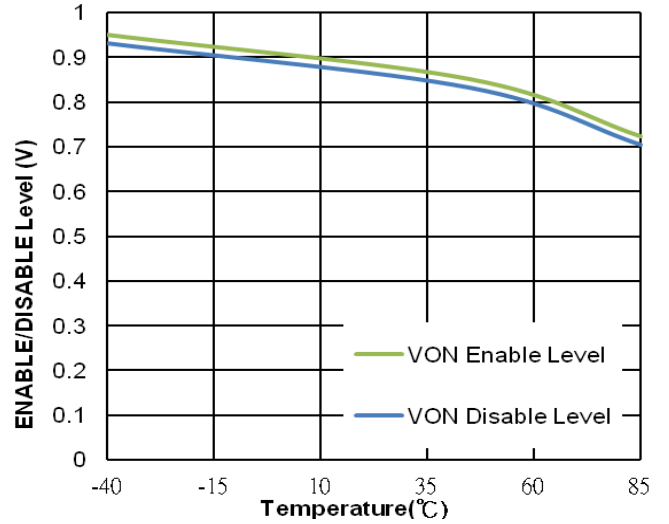
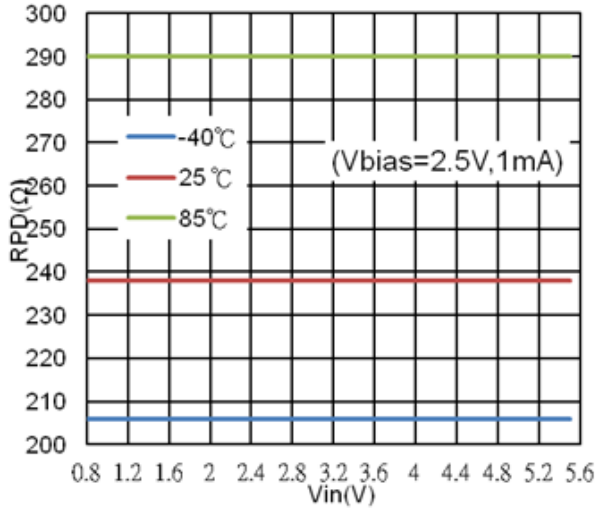


R_{ON} vs. Temperature (V_{BIAS}=2.5V)



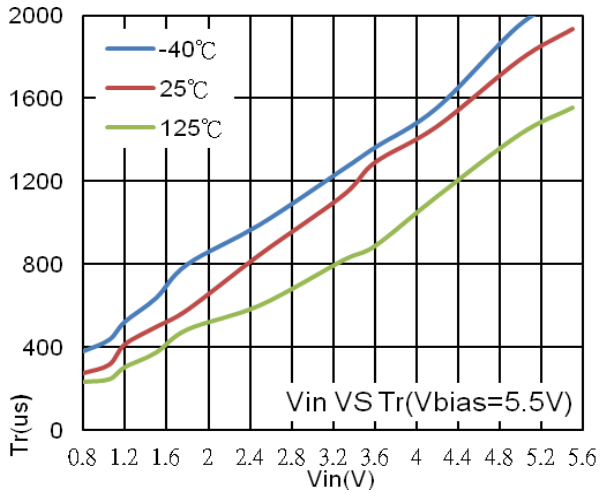
V_{IN} vs. RPD (V_{BIAS}=2.5V)

V_{ON} Threshold vs. Temperature

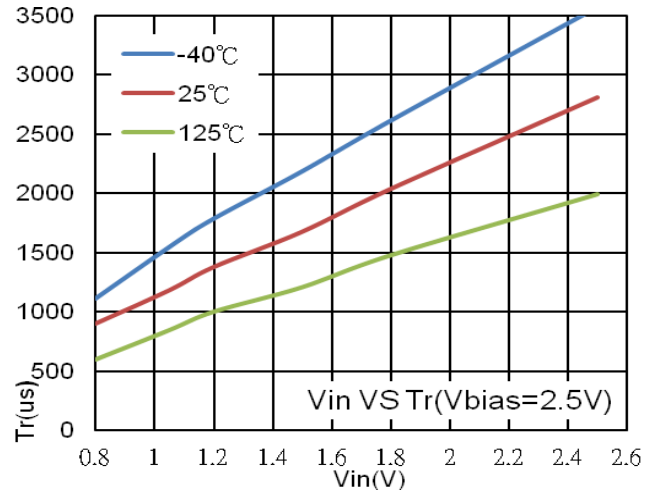


Typical Operating Characteristics

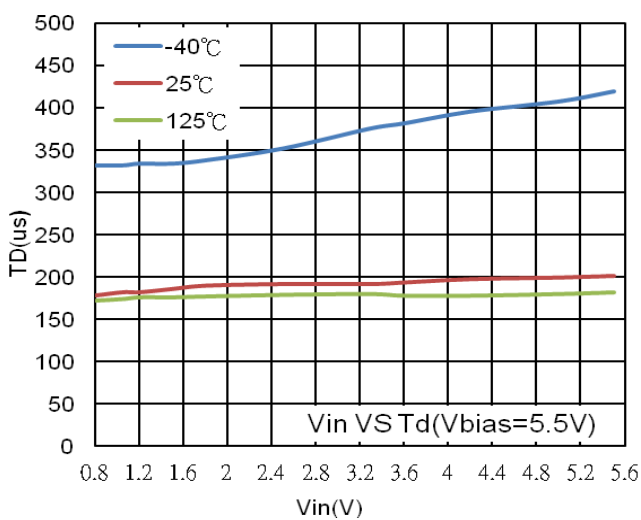
V_{IN} vs. TR (CT=1nF, V_{BIAS}=5.5V)



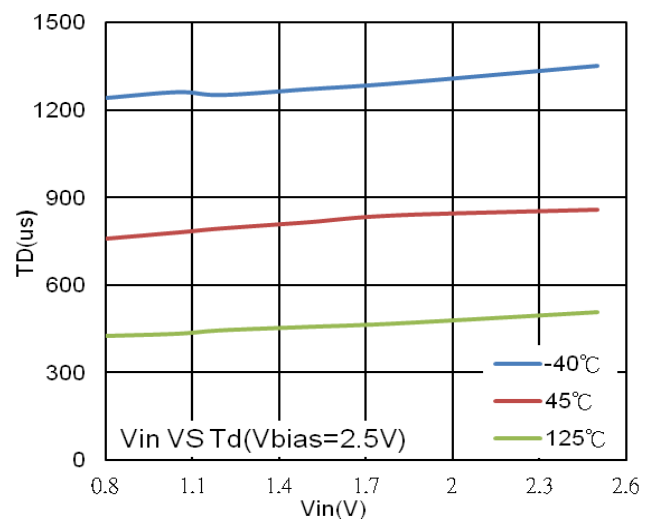
V_{IN} vs. TR (CT=1nF, V_{BIAS}=2.5V)



V_{IN} vs. TD (CT=1nF, V_{BIAS}=5.5V)



V_{IN} vs. TD (CT=1nF, V_{BIAS}=2.5V)



Functional Description

On-Resistance

The MOSFET gate voltage in the EM5209 is driven by an internal charge pump. The output voltage of the charge pump is dependent on the voltage on VBIAS pin. Care must be taken to ensure a sufficient VBIAS is used to keep the desired R_{ON} when given the anticipated input voltage.

ON/OFF Control

EM5209 is enabled if the voltage of the Von pin is greater than logic high level and the VBIAS voltage has an adequate applied. If the voltage of the ON pin is less than logic low level, the device will be disabled.

Input Capacitor

The EM5209 do not require an input capacitor. In order to limit the voltage drop on the input supply caused by transient inrush current, an input bypass capacitor is recommended. A 1uF ceramic capacitor should be placed as closed as possible to the V_{IN} pin. Higher values capacitor can help to further reduce the voltage drop.

Output Capacitor

Due to the integrated body diode in the NMOS switch, the C_{IN} greater than C_L is highly recommended. A C_{IN} to C_L ratio of 10 to 1 is recommended for minimizing V_{IN} drop caused by inrush during startup. It also helps to prevent parasitic inductance forces V_{OUT} below GND when switching off. Output capacitor has minimal affect on device's turn on slew rate time.

Slew Rate Control

The slew rate of each channel output voltage can be controlled by the capacitor on the CT pin to GND which provides soft start functionality. This limits the inrush current caused by capacitor charging.

Thermal and Layout Consideration

EM5209 is designed to maintain a constant output load current. Due to physical limitations of the chip layout and assembly of the device the maximum switch current is 6A for each channel, the figure below show an example of typical PCB layout. All copper traces for the V_{IN} and V_{OUT} pin should be widely and short to carry the maximum continuous current and obtain the best effect. The input and output capacitor (option) should be close to the device as possible to minimize the parasitic trace inductances and prevents the voltage drop when load transient.

The maximum IC junction temperature should be restricted to 125 °C under normal operating conditions. To calculate the maximum allowable dissipation, P_{D(MAX)} for a given output current and ambient temperature, used the following equation:

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{\theta_{JA}}$$

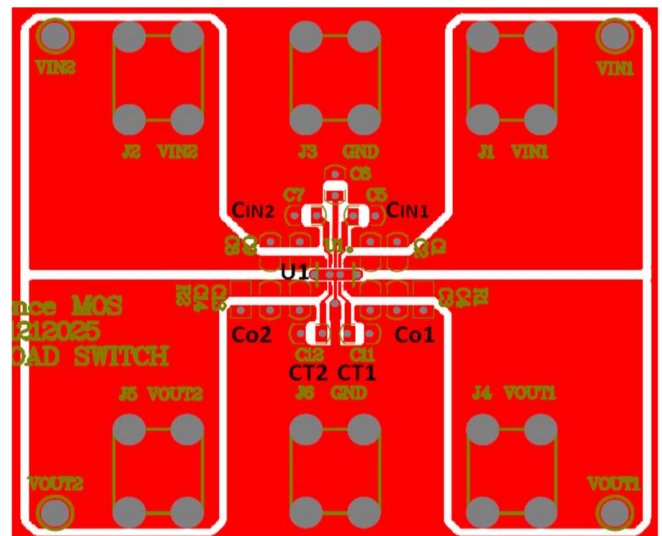
Where:

P_{D(MAX)}=Maximum allowable power dissipation

T_{J(MAX)}=Maximum allowable junction temperature (125 °C for the EM5209)

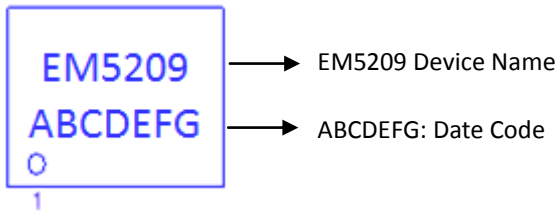
T_A=Ambient Temperature of the device

θ_{JA}= Junction to air thermal impedance. This parameter is also dependent upon PCB layout.

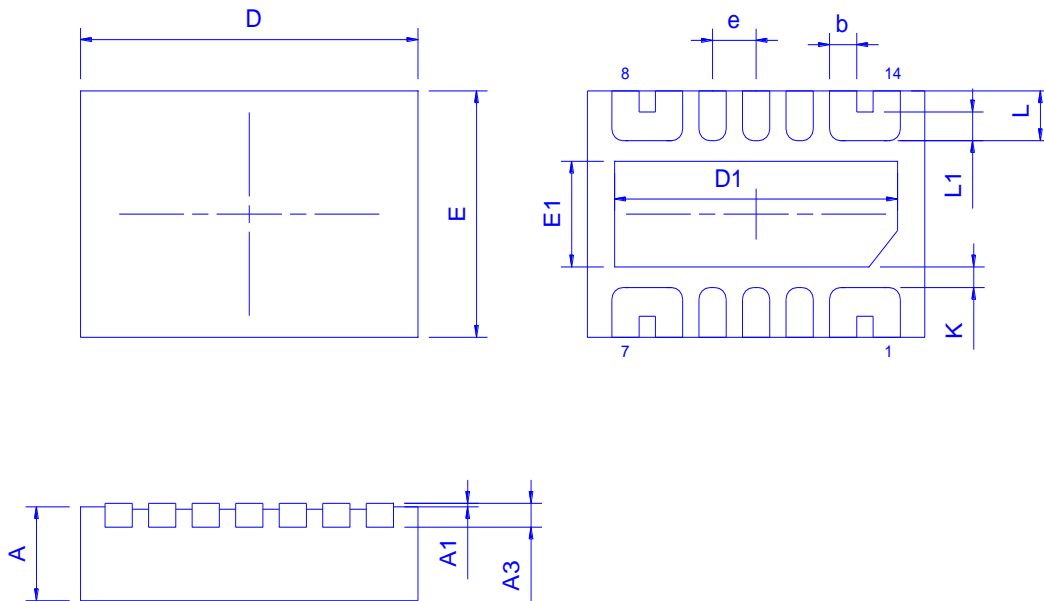


Marking Information

Device Name: EM5209VF for DFN3X2-14L



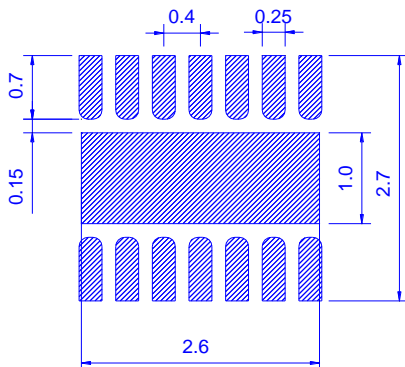
Outline Drawing



Dimension in mm

Dimension	A	A1	A3	b	D	E	D1	E1	e	L	K
Min.	0.7	0.00		0.13	2.9	1.9	2.4	0.7	0.3	0.200	0.15
Typ.			0.203		3.0	2.0					
Max.	0.8	0.05		0.25	3.1	2.1	2.6	1.0	0.5	0.426	0.35

Recommended minimum pads



◆ Tape&Reel Information:3000pcs/Reel(Dimension in millimeter)

