杰力科技股份有限公司
Excelliance MOS Corporation

EM5305

12V Synchronous Buck controller

General Description

The EM5305 series are compact synchronous -rectified buck controllers specifically designed to operate from 5V or 12V supply voltage. The output voltage is tightly regulated to the external reference voltage from 0.4V to 3.0V. These devices operate at fixed 300 kHz frequency and provide an optimal level of integration to redwuce size and cost of the power supply.

The controllers integrate internal MOSFET drivers that support 12V+12V bootstrapped voltage for high efficiency power conversion. The bootstrap diode is built-in to simplify the circuit design and minimize external part count.

Other features include internal soft-start, under-voltage protection, over-voltage protection, over-current protection and shutdown function. With aforementioned functions, these parts provide customers a compact, high efficiency, well-protected and cost-effective solutions. These parts are available in DFN3x3-10L package.

Ordering Information

Part Number	Package	Remark
EM5305VT	DFN3x3-10L Lead-Free	

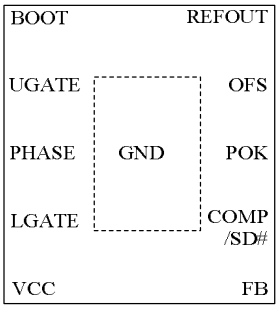
Applications

- Power Supplies for Microprocessors or Subsystem Power Supplies
- Cable Modems, Set Top Boxes, and xDSL Modems
- 5V or 12V Input DC-DC Regulators
- Graphics Cards

Features

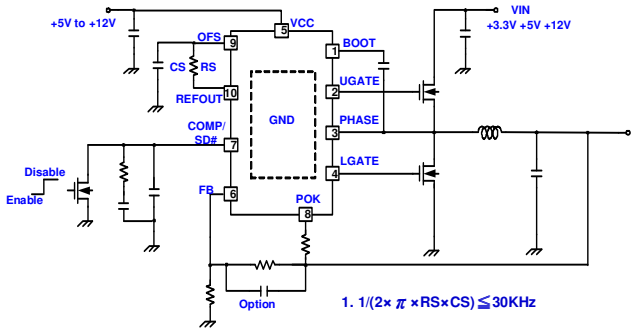
- Tracking mode
- 300 kHz fixed frequency operation.
- Voltage mode PWM control with external compensation (GM)
- Internal soft start
- Integrated bootstrap diode
- Low side MOS OC protection
- OUT UV protection
- OUT OV protection
- Power Good Indicator
- 0.8V Reference Output

Pin Configuration



EM5305

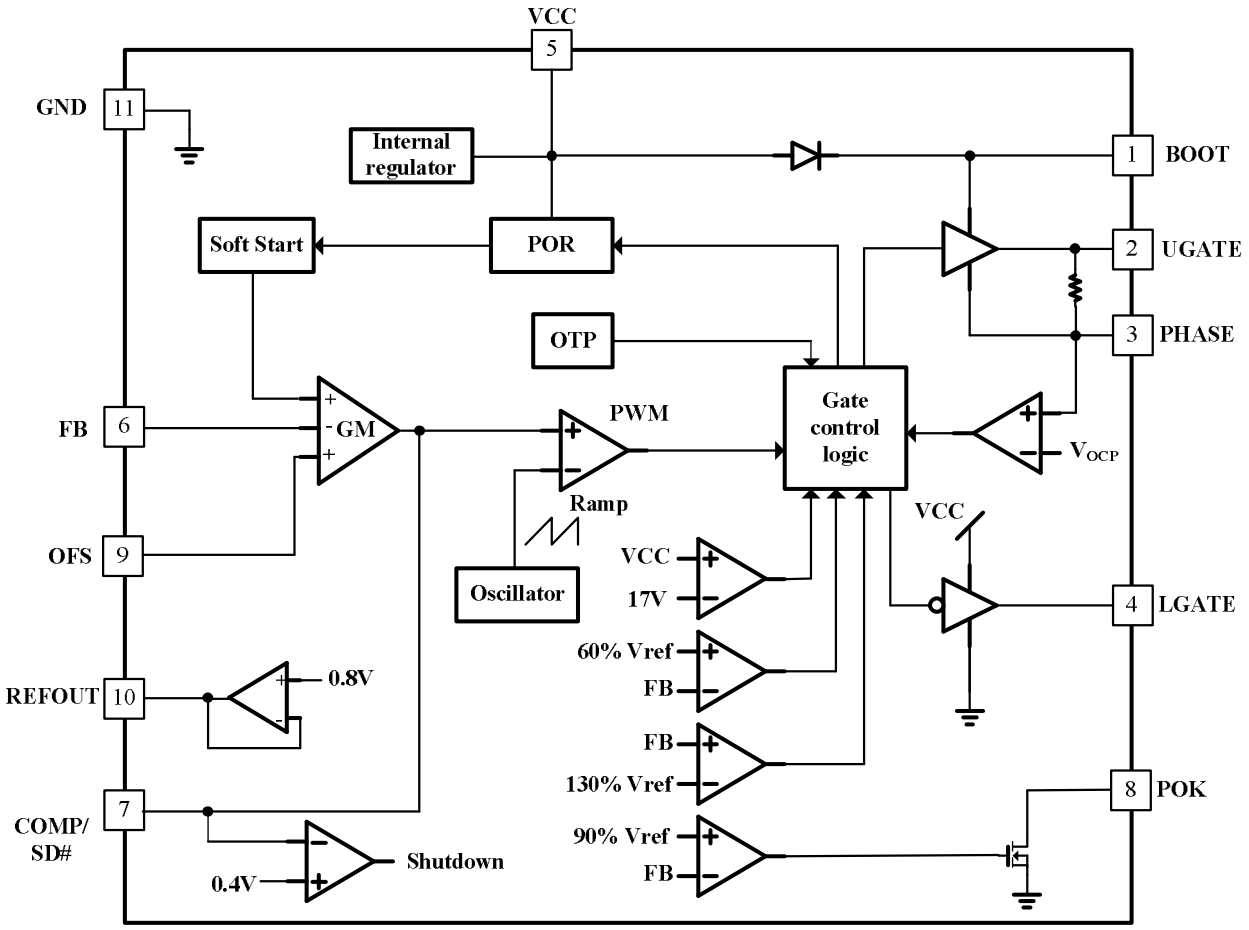
Typical Application Circuit



Pin Assignment

Pin Name	Pin No.	Pin Function
BOOT	1	**Bootstrap Supply** for the floating upper gate driver. Connect the bootstrap capacitor C_{BOOT} between BOOT pin and the PHASE pin to form a bootstrap circuit. The bootstrap capacitor provides the charge to turn on the upper MOSFET. Typical values for C_{BOOT} range from 0.1uF to 0.47uF. Ensure that C_{BOOT} is placed near the IC.
UGATE	2	**Upper Gate Driver Output.** Connect this pin to the gate of upper MOSFET. This pin is monitored by the adaptive shoot-through protection circuitry to determine when the upper MOSFET has turned off.
PHASE	3	**PHASE Switch Node.** Connect this pin to the source of the upper MOSFET and the drain of the lower MOSFET. This pin is used as the sink for the UGATE driver, and to monitor the voltage drop across the lower MOSFET for over current protection. This pin is also monitored by the adaptive shoot-through protection circuitry to determine when the upper MOSFET has turned off. A Schottky diode between this pin and ground is recommended to reduce negative transient voltage which is common in a power supply system.
LGATE	4	**Lower Gate Driver Output.** Connect this pin to the gate of lower MOSFET. This pin is monitored by the adaptive shoot-through protection circuitry to determine when the lower MOSFET has turn off.
VCC	5	**Supply Voltage.** This pin provides the bias supply for the EM5305 and the lower gate driver. The supply voltage is internally regulated to 5VDD for internal control circuit. Connect a well-decoupled 4.5V to 13.2V supply voltage to this pin. Ensure that a decoupling capacitor is placed near the IC.
FB	6	**Feedback Voltage.** This pin is the inverting input to the error amplifier. A resistor divider from the output to GND is used to set the regulation voltage.
COMP/ SD#	7	**Error Amplifier Output.** This pin is the output of error amplifier and the non-inverting input of the PWM comparator. Use this pin in combination with the FB pin to compensate the voltage control feedback loop of the converter. Pulling this pin lower than 0.4V disables the controller and causes the oscillator to stop, the UGATE and LGATE outputs to be held low.
POK	8	**Power OK Indicator**
OFS	9	**External Reference Input.** This pin receives a voltage with range from 0.4V to 3.0V as the reference voltage at the non-inverting input of the error amplifier. Pulling this pin lower than 0.3V or higher than 3.3V disables the controller and causes the oscillator to stop, the UGATE and LGATE outputs to be held low.
REFOUT	10	**0.8V Reference Voltage Output**
GND	Thermal PAD	**Signal and Power Ground for the IC.** All voltages levels are measured with respect to this pin. Tie this pin to the ground island/plane through the lowest impedance connection available.

Function Block Diagram



Absolute Maximum Ratings (Note1)

- Supply voltage, VCC---------- -0.3V to 16V
- PHASE to GND
  - DC---------- -5V to 16V
  - <200ns---------- -10V to 30V
- BOOT to PHASE---------- 16V
- BOOT to GND
  - DC---------- -0.3V to PHASE+16V
  - <200ns---------- -0.3V to 40V
- UGATE
  - DC ---------- V_{PHASE} -0.3V to V_{BOOT} + 0.3V
  - <200ns---------- V_{PHASE} -5V to V_{BOOT} +5V
- LGATE
  - DC---------- -0.3V to VCC + 0.3V
  - <200ns---------- -5V to VCC+5V
- COMP/SD# & FB & OFS & REFOUT & POK---------- -0.3V to 7V
- Power Dissipation, PD @ TA = 25℃, DFN3x3-10L---------- 1.67W
- Package Thermal Resistance, Θ_{JA}, DFN3x3-10L (Note 2)---------- 60℃/W
- Junction Temperature---------- 150℃
- Lead Temperature (Soldering, 10 sec.)---------- 260℃
- Storage Temperature Range---------- -65℃ to 150℃
- ESD susceptibility (Note3)
  - HBM (Human Body Mode)---------- 2KV
  - MM (Machine Mode)---------- 200V

Recommended Operating Conditions (Note4)

- Supply voltage, VCC---------- 4.5V to 13.2V
- Junction Temperature Range---------- –40°C to 125°C
- Ambient Temperature Range---------- –40°C to 85°C

Electrical Characteristics

V_{CC}=12V, T_A=25℃, unless otherwise specified

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Supply Input Section						
Supply Voltage	V_{CC}		4.5		13.2	V
Supply Current	I_{CC}	LGATE, UGATE open, Switching.		1.5		mA
Shutdown Current					0.4	mA
Power on Reset Threshold	V_{CCRTH}		3.8	4.05	4.3	V
Power on Reset Hysteresis	V_{CCHYS}		0.3	0.45	0.6	V

Internal Oscillator						
Free Running Frequency	f_{OSC}		270	300	330	kHz
Ramp Amplitude	$\triangle V_{OSC}$			1.5		V_{p-p}
Max. Duty Cycle	D_{MAX}		80	85	90	%
Error Amplifier						
Trans-conductance	Gm			700		uA/V
Max. Comp Source Current			100	200		uA
Max. Comp Sink Current			100	200		uA
PWM Controller Gate Drivers						
Upper Gate Sourcing Current	I_{UG_SRC}	V_{BOOT} - V_{PHASE} = 12V, V_{BOOT} - V_{UGATE} = 6V		1.2		A
Upper Gate $R_{DS(ON)}$ Sinking	R_{UG_SNK}	V_{BOOT} - V_{PHASE} = 12V, V_{UGATE} – V_{PHASE} = 0.1V		3		Ω
Lower Gate Sourcing Current	I_{LG_SRC}	V_{CC} – V_{LGATE} = 6V		1.2		A
Lower Gate $R_{DS(ON)}$ Sinking	R_{LG_SNK}	V_{LGATE} = 0.1V		1.8		Ω
PHASE Falling to LGATE Rising Delay		V_{CC} = 12V; (V_{UGATE} - V_{PHASE})< 1.2V to V_{LGATE} > 1.2V		30	90	ns
LGATE Falling to UGATE Rising Delay		V_{CC} = 12V; V_{LGATE} < 1.2V to (V_{UGATE} - V_{PHASE}) > 1.2V		30	90	ns
Reference Voltage						
Feedback Voltage	V_{FB}	V_{OFS}= 0.8V	0.792	0.8	0.808	V
Reference Output	V_{REFOUT}		0.792	0.8	0.808	V
Reference Output Source/Sink	I_{REFOUT}			5		mA
Protection section						
FB Under Voltage Protection	V_{FB_UVP}	FB falling	50	60	70	%
UVP delay time				7.5	10	us
FB Over Voltage Protection	V_{FB_OVP}	FB rising	120	130	140	%
OVP delay time				7.5	10	us
LGATE OC Setting Current	I_{OCSET}		8.5	10	11.5	uA
Built in Max. OCP Threshold				-630		mV
Soft-Start Interval	T_{SS}		1	2	3	ms
COMP Shutdown Threshold	$V_{COMP/SD\#}$				0.4	V
POK Threshold	V_{POK}		88	90	92	%
POK Delay			1	2	3	ms
Power Good Leakage Current					1	uA
Temperature Shutdown	T_{SD}			140		℃
Temperature Shutdown Hysteresis	T_{SD_Hys}			40		℃

Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

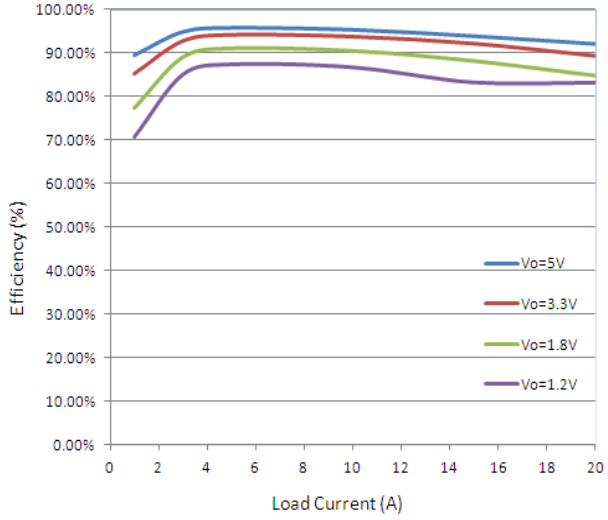
Note 2. θ_{JA} PSOP-8 packages is 52°C /W on JEDEC 51-7 (4 layers,2S2P) thermal test board with 50mm^2 copper area.

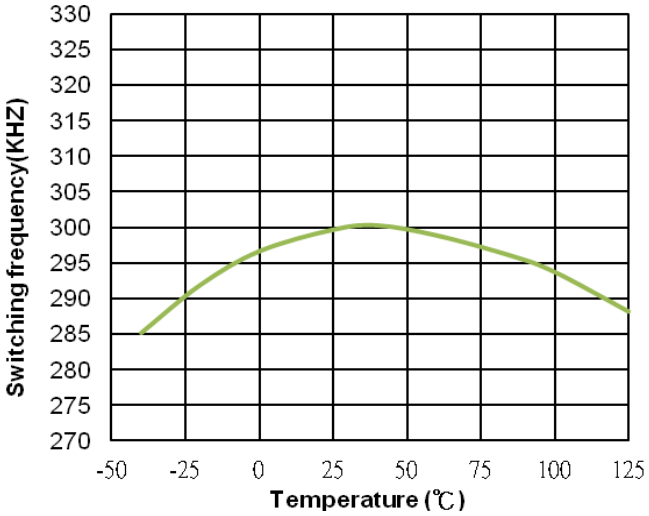
Note 3. Devices are ESD sensitive. Handling precaution is recommended.

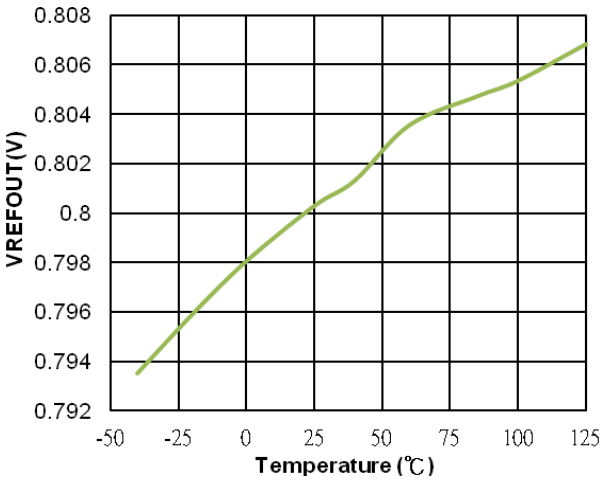
Note 4. The device is not guaranteed to function outside its operating conditions.

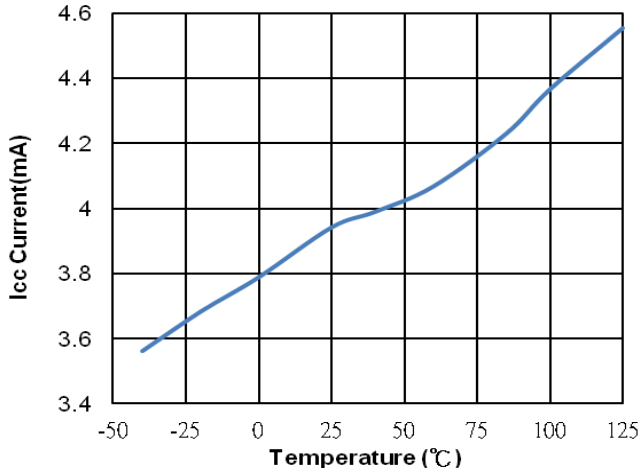
Typical Operating Characteristics

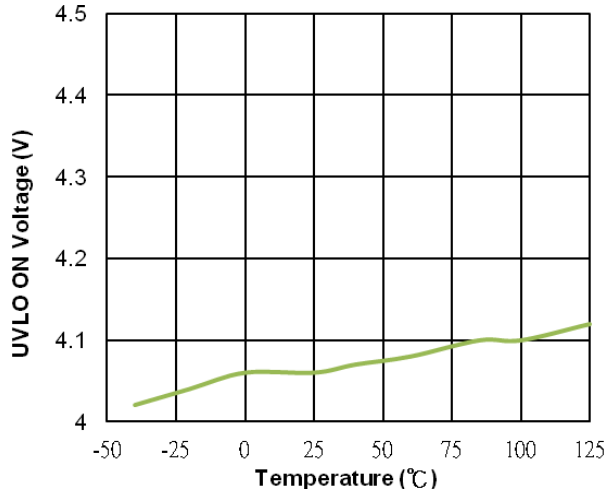
(VIN = VCC=12V, TA = +25, unless otherwise noted.)

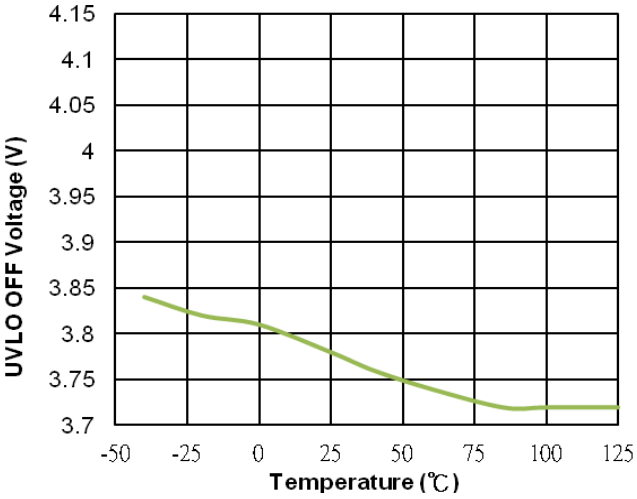


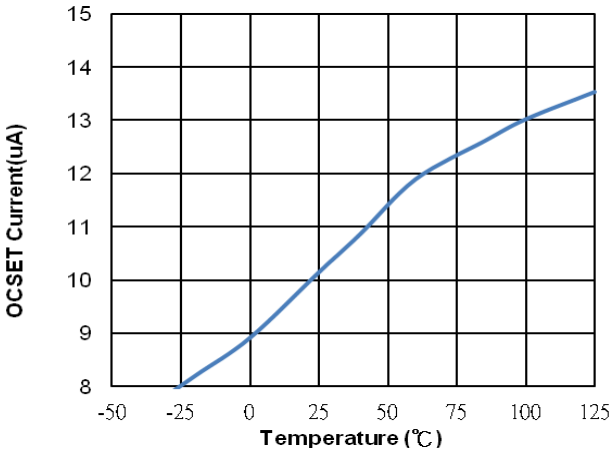




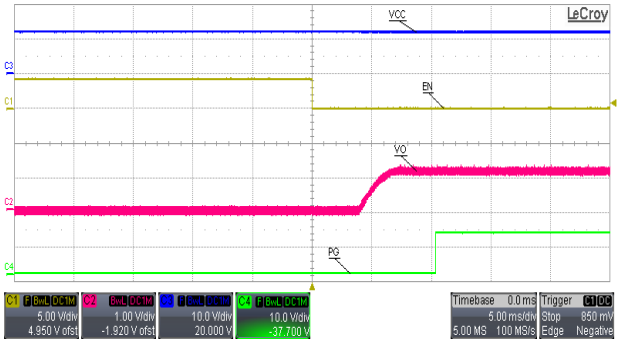






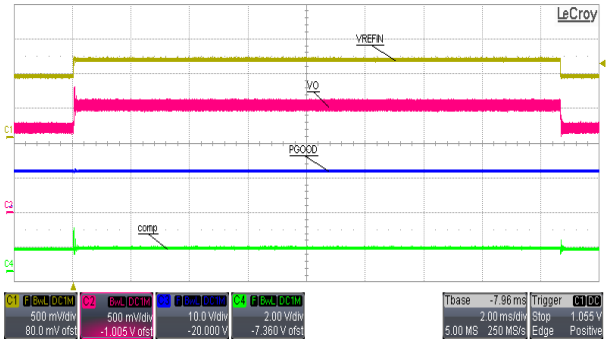


Power on-off from EN signal



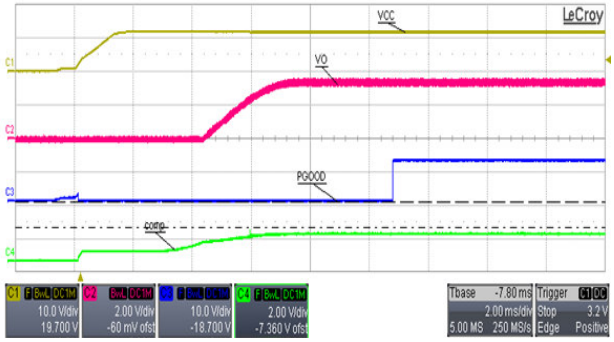
CH1:VCC, CH2:EN, CH3:Vo, CH4:COMP

Dynamic Vo Transition 1.1V to 1.5V



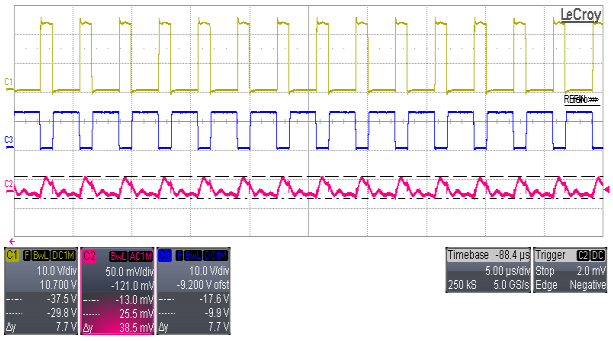
CH1:OFS, CH2:Vo, CH3:POK, CH4:COMP

Power on from VCC



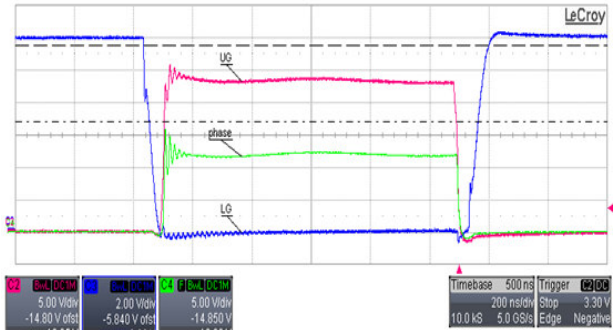
CH1:VCC, CH2:Vo, CH3:POK, CH4:COMP

Vo Ripple



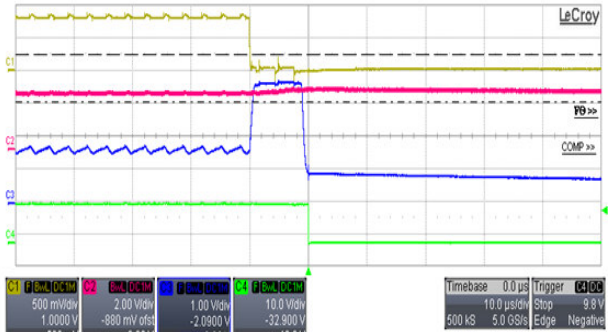
CH1:UGATE, CH2:LGATE, CH3:Vo(ac)

UGATE AND LGATE Dis-overlap



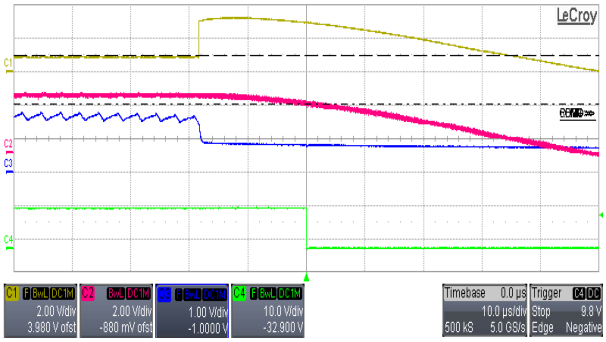
CH1:UGATE, CH2:LGATE, CH3:PHASE

Under feedback voltage protection



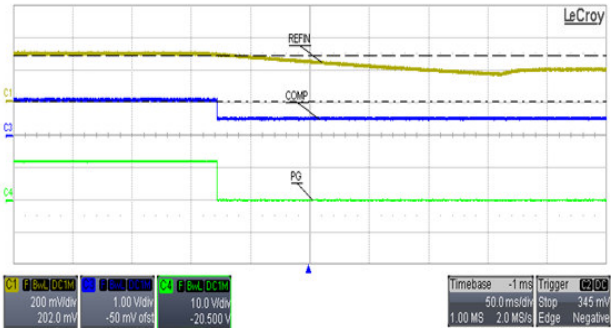
CH1:FB, CH2:Vo, CH3:Comp, CH4:POK

Over feedback voltage protection



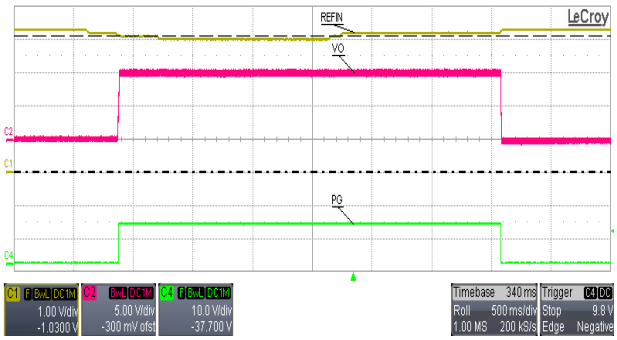
CH1:FB, CH2:Vo, CH3:Comp, CH4:POK

Under OFS voltage protection



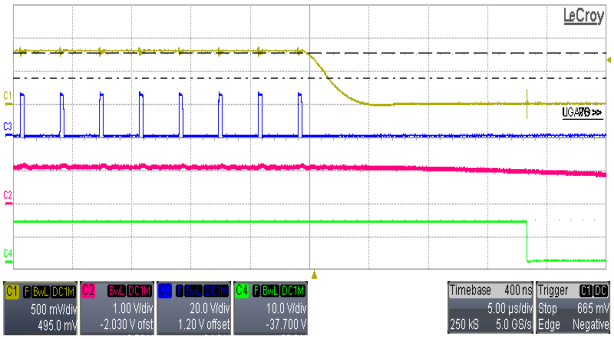
CH1:OFS, CH2:Comp, CH3:POK

Over OFS voltage protection



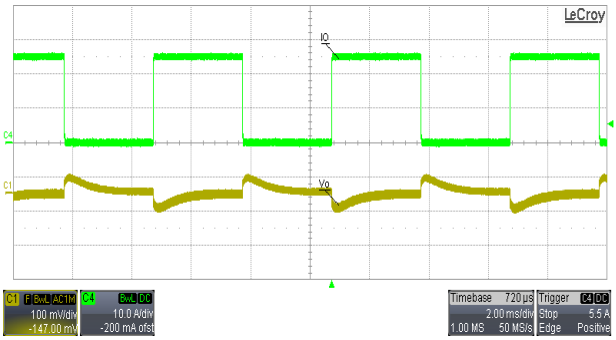
CH1:OFS, CH2:Vo, CH3:POK

REFOUT short to GND protection



CH1:REFOUT, CH2:UGATE, CH3:Vo, CH4:POK

Load transient response (0.1A to 25A)



CH1:Vo(ac), CH2:Io

Functional Description

EM5305 is a voltage mode synchronous buck PWM controller. This device provides complete protection function such as over current protection, under voltage protection and over voltage protection.

Supply Voltage

The V_{CC} pin provides the bias supply of EM5305 control circuit, as well as lower MOSFET's gate and the BOOT voltage for the upper MOSFET's gate. A minimum 0.1uF ceramic capacitor is recommended to bypass the supply voltage.

Power ON Reset

To let EM5305 start to operation, V_{CC} voltage must be higher than its POR voltage even when the COMP/SD# voltage is pulled higher than enable high voltage. Typical POR voltage is 4.05V.

Shutdown

The COMP/SD# pin can be used to enable or disable EM5305. Pull down COMP/SD# pin below 0.4V can disable the controller.

Soft Start

EM5305 provides soft start function internally. The FB voltage will track the internal soft start signal, which ramps up from zero during soft start period.

OCP, Over Current Protection

The over current function protects the converter from a shorted output by using lower MOSFET's on-resistance to monitor the current. The OCP level can be calculated as the following equation:

$$I_{OCP} = \frac{I_{OCSET} \bullet R_{OCSET}}{R_{DS(ON)}}$$

When OCP is triggered, EM5305 will shut down the converter and cycles the soft start function in a hiccup mode. If over current condition still exist after 3 times of hiccup, EM5305 will shut down the controller and latch.

UVP, Under Voltage Protection

The FB voltage is monitored for under voltage protection. The UVP threshold is typical 60% V_{OFS}. When UVP is triggered, EM5305 will shut down the converter and cycles the soft start function in a hiccup mode.

OVP, Over Voltage Protection

The FB voltage is monitored for over voltage protection. The OVP threshold is typical 130% V_{OFS}. When OVP is triggered, EM5305 will turn off upper MOSFET and turn on lower MOSFET.

REFOUT and OFS

The REFOUT pin provides the 0.8V voltage output with 5mA sourcing/sinking capability. The OFS pin is high impedance input and receives a voltage range from 0.4V to 3V as the reference voltage. Connecting a resistor between REFOUT pin and OFS pin can provide 0.8V as the reference input. By sourcing or sinking OFS pin through the resistor can adjust the input reference. Show as Fig.1

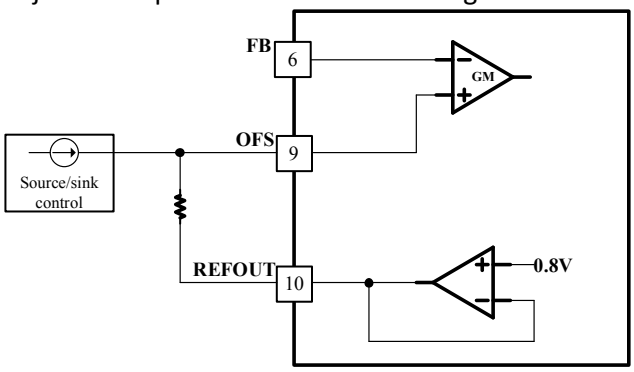


Fig.1 REFOUT and OFS application.

Feedback Compensation

If f_{ESR} is lower than fcross and close to fLC, the phase lead of the capacitor ESR zero almost cancels the phase loss of one of the complex poles of the LC filter around the crossover frequency. Use a Type II compensation network with a one zero and a high-frequency pole to stabilize the loop. In Figure 2, RF and CF introduce a one zero (fZ1). RF and CCF in the Type II compensation network provide a high-frequency pole (fP1), which mitigates the effects of the output high-frequency ripple.

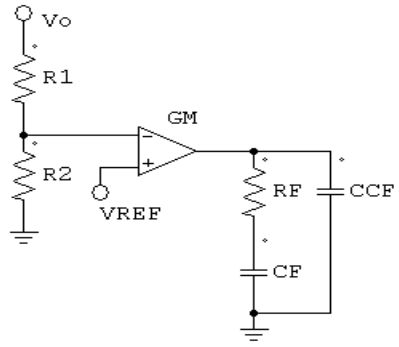


Fig.2 Compensation II for Voltage Mode Buck Converter

When using a low-ESR tantalum or OSCON type, the ESR-induced zero frequency is usually above the targeted zero crossover frequency (fcross). Use Type III compensation Fig3.Type III compensation provides two zeros to cancel the pair of complex poles introduced by LC filter.

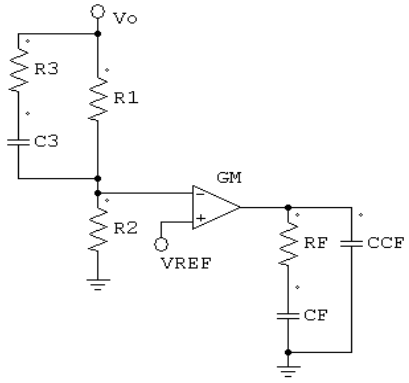


Fig.2 Compensation III for Voltage Mode Buck Converter

Fig.3 shows the Bode plot for the control loop. The compensation gain uses external impedance networks Z_{IN} and Z_{FB} to provide a stable loop. A stable control loop has a gain crossing with -20db/decade slope and phase margin greater than 45 degrees.

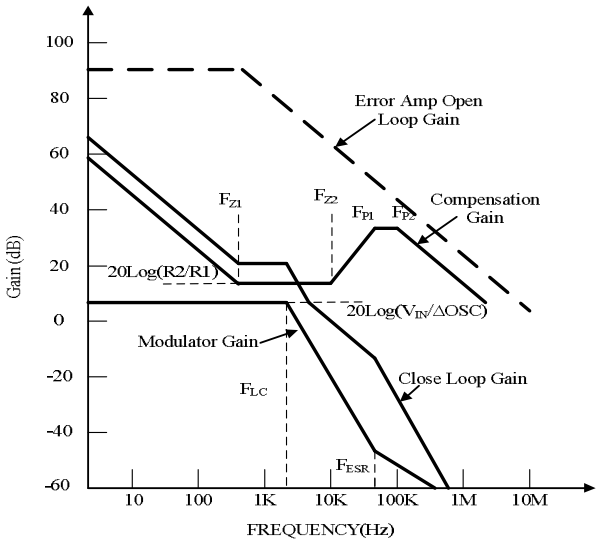


Fig.3 Bode Plot of Voltage Mode Buck Converter

Output Inductor Selection

The output inductor is selected to meet the output voltage ripple requirements and minimize the response time to the load transient. The inductor value determines the current ripple and voltage ripple. The ripple current is approximately the following equation:

$$\Delta I_L = \frac{V_{IN} - V_{OUT}}{L} * \frac{V_{OUT}}{V_{IN} * F_{SW}}$$

Output Capacitor Selection

An output capacitor is required to filter the output and supply the load transient. The selection of output capacitor depends on the output ripple voltage. The output ripple voltage is approximately bounded by the following equation:

$$\Delta V_{OUT} = \Delta I_L * (ESR + \frac{1}{8 * F_{SW} * C_{OUT}})$$

Input Capacitor Selection

Use a mix of input bypass capacitors to control the voltage overshoot across the MOSFET. Use small ceramic capacitors for high frequency decoupling and bulk capacitors to supply the current needed each time the upper MOSFET turn on. Place the small ceramic capacitors physically close to the MOSFETs and between the drain of the upper MOSFET and the source of the lower MOSFET. The important parameters of the input capacitor are the voltage rating and the RMS current rating. The capacitor voltage rating should be at least 1.25 times greater than the maximum input voltage and a voltage rating of 1.5 times is a conservative guideline. The RMS current rating requirement can be expressed as the following equation:

$$I_{RMS} = I_{OUT}\sqrt{D(1-D)}$$

For a through hole design, several electrolytic capacitors may be needed. For surface mount designs, solid tantalum capacitors can also be used but caution must be exercised with regard to the capacitor surge current rating. These capacitors must be capable of handling the surge current at power-up. Some capacitor series available from reputable manufacturers are surge current tested.

Power MOSFET Selection

The EM5305 requires two N-Channel power MOSFETs. These should be selected based upon on-resistance, breakdown voltage, gate supply requirement, and thermal management requirements.

In high current applications, the MOSFET power dissipation, package selection and heat sink are the dominate design factor. The power dissipation includes two loss components: conduction loss and switching loss. The conduction losses are the largest component of power dissipation for both the upper and lower MOSFETs. These losses are distributed between the two MOSFETs according to duty factor.

The power dissipations in the two MOSFETs are approximately the following equation:

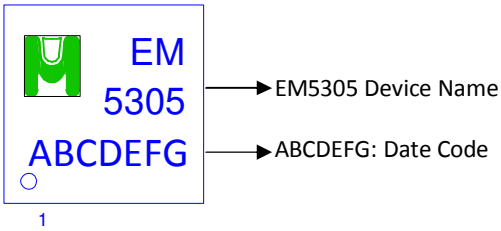
$$PD_{UPPER} = I^2_{OUT} * R_{DS(ON)} * D + 0.5 * I_{OUT} * V_{IN} * F_{SW} * t_{SW}$$

$$PD_{LOWER} = I^2_{OUT} * R_{DS(ON)} * (1-D)$$

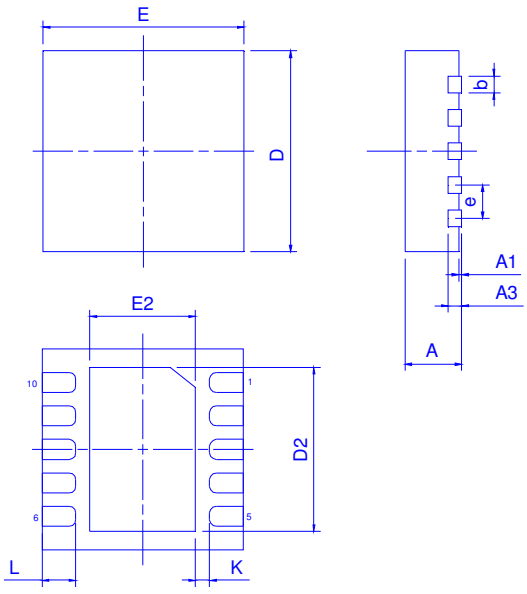
Where D is the duty cycle, t_{SW} is the combined switch ON and OFF time.

Marking Information

Device Name: EM5305VT for DFN3X3-10L



Outline Drawing



Dimension in mm

Dimension	A	A1	A3	b	D	E	D2	E2	e	L	K
Min.	0.7	0.00		0.18			2.20	1.40		0.30	0.20
Typ.	0.75	0.02	0.2	0.25	3.0	3.0			0.50	0.40	
Max.	0.80	0.05		0.30			2.70	1.75		0.50	