

**GENERAL DESCRIPTION**

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The EM6128K800V is a 1,048,576-bit low power CMOS static random access memory organized as 131,072 words by 8 bits. It is fabricated using very high performance, high reliability CMOS technology. Its standby current is stable within the range of operating temperature.

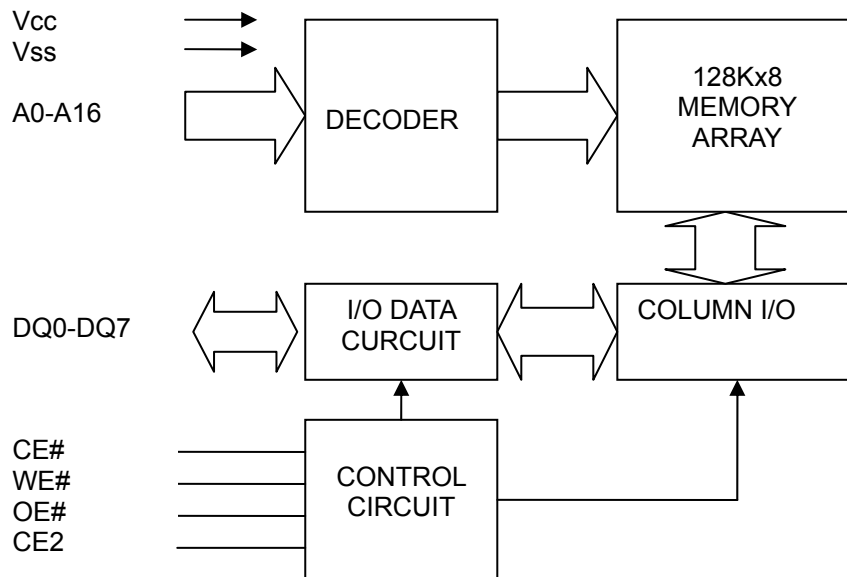
The EM6128K800V is well designed for low power application, and particularly well suited for battery back-up nonvolatile memory application.

The EM6128K800V operates from a single power supply of 2.7V ~ 3.6V and all inputs and outputs are fully TTL compatible

**FEATURES**

- Fast access time: 35/55/70ns
- Low power consumption:  
Operating current: 12/10/7mA (TYP.)  
Standby current: -L/-LL version 20/1µA (TYP.)
- Single 2.7V ~ 3.6V power supply
- All inputs and outputs TTL compatible
- Fully static operation
- Tri-state output
- Data retention voltage: 1.5V (MIN.)
- Package:  
32-pin 450 mil SOP  
32-pin 600 mil P-DIP  
32-pin 8mm x 20mm TSOP-I  
32-pin 8mm x 13.4mm STSOP  
36-ball 6mm x 8mm TFBGA

**FUNCTIONAL BLOCK DIAGRAM**

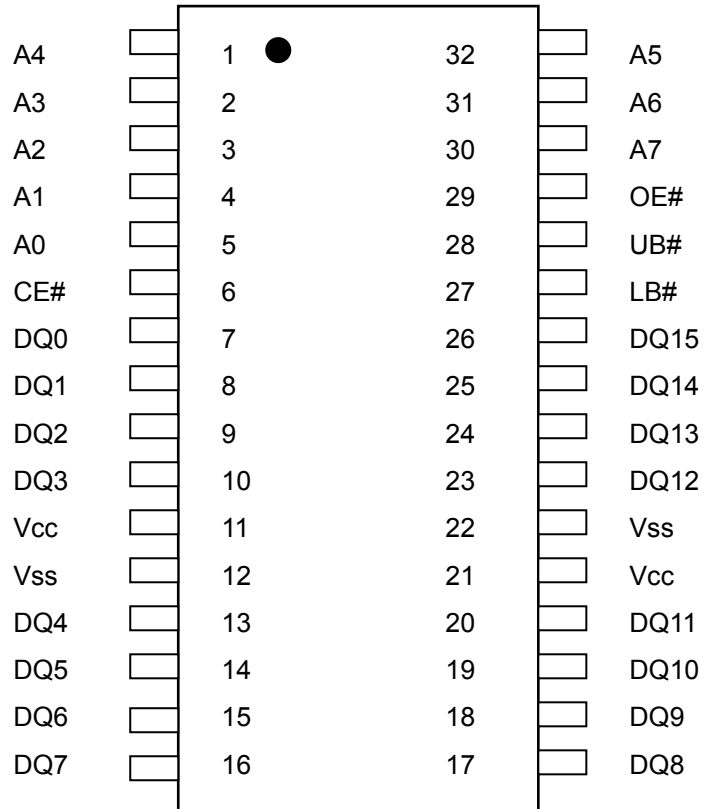


**PIN DESCRIPTION**

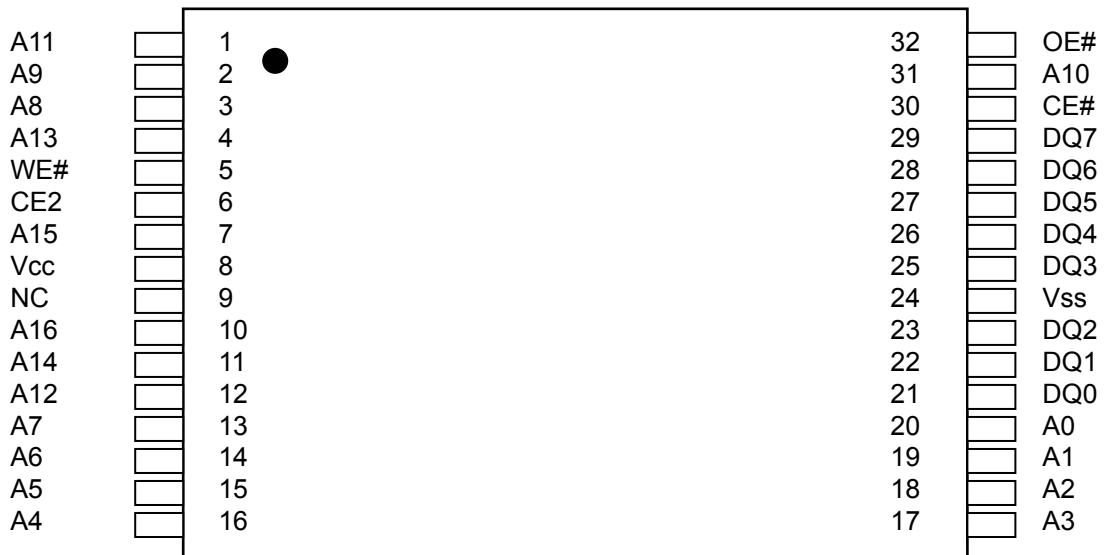
SYMBOL	DESCRIPTION
A0 - A16	Address Inputs
DQ0 - DQ7	Data Inputs/Outputs
CE#, CE2	Enable Input
WE#	Write Enable Input
OE#	Output Enable Input
Vcc	Power Supply
Vss	Ground

PIN CONFIGURATION

SOP/P-DIP



TSOP-I/STSOP



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**TFBGA**

<b>A</b>	<b>A0</b>	<b>A1</b>	<b>CE2</b>	<b>A3</b>	<b>A6</b>	<b>A8</b>
<b>B</b>	<b>DQ4</b>	<b>A2</b>	<b>WE#</b>	<b>A4</b>	<b>A7</b>	<b>DQ0</b>
<b>C</b>	<b>DQ5</b>		<b>NC</b>	<b>A5</b>		<b>DQ1</b>
<b>D</b>	<b>Vss</b>					<b>Vcc</b>
<b>E</b>	<b>Vcc</b>					<b>Vss</b>
<b>F</b>	<b>DQ6</b>		<b>NC</b>	<b>NC</b>		<b>DQ2</b>
<b>G</b>	<b>DQ7</b>	<b>OE#</b>	<b>CE#</b>	<b>A16</b>	<b>A15</b>	<b>DQ3</b>
<b>H</b>	<b>A9</b>	<b>A10</b>	<b>A11</b>	<b>A12</b>	<b>A13</b>	<b>A14</b>
	<b>1</b>	<b>2</b>	<b>3</b>	<b>4</b>	<b>5</b>	<b>6</b>

**ABSOLUTE MAXIMUM RATINGS\***

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PARAMETER	SYMBOL	RATING	UNIT
Terminal Voltage with Respect to V <sub>SS</sub>	V <sub>TERM</sub>	-0.5 to 4.6	V
Operating Temperature	T <sub>A</sub>	0 to 70(C grade)	°C
		-20 to 80(E grade)	
		-40 to 85(I grade)	
Storage Temperature	T <sub>STG</sub>	-65 to 150	°C
Power Dissipation	P <sub>D</sub>	1	W
DC Output Current	I <sub>OUT</sub>	50	mA
Soldering Temperature (under 10 sec)	T <sub>SOLDER</sub>	260	°C

\*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

**TRUTH TABLE**

MODE	CE#	OE#	WE#	I/O OPERATION	SUPPLY CURRENT
Standby	H	X	X	High-Z	I <sub>SB</sub> , I <sub>SB1</sub>
Output Disable	L	H	H	High-Z	I <sub>CC</sub> , I <sub>CC1</sub>
Read	L	L	H	D <sub>OUT</sub>	I <sub>CC</sub> , I <sub>CC1</sub>
Write	L	X	L	D <sub>IN</sub>	I <sub>CC</sub> , I <sub>CC1</sub>

Note: H = V<sub>IH</sub>, L = V<sub>IL</sub>, X = Don't care.

**DC ELECTRICAL CHARACTERISTICS**

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP. *5	MAX.	UNIT	
Supply Voltage	V <sub>CC</sub>		2.7	3.0	3.6	V	
Input High Voltage	V <sub>IH</sub> *1		2.0	-	V <sub>CC</sub> +0.3	V	
Input Low Voltage	V <sub>IL</sub> *2		-0.2	-	0.6	V	
Input Leakage Current	I <sub>LI</sub>	V <sub>CC</sub> ≥ V <sub>IN</sub> ≥ V <sub>SS</sub>	-1	-	+1	μA	
Output Leakage Current	I <sub>LO</sub>	V <sub>CC</sub> ≥ V <sub>OUT</sub> ≥ V <sub>SS</sub> , Output Disabled	-1	-	1	μA	
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> = -1mA	2.2	2.7	-	V	
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> = 2mA	-	-	0.4	V	
Average Operating Power supply Current	I <sub>CC</sub>	Cycle time = Min. CE# = V <sub>IL</sub> , I <sub>I/O</sub> = 0mA	-35	-	12	35	mA
			-55	-	10	30	mA
			-70	-	7	25	mA
	I <sub>CC1</sub>	Cycle time = 1μs CE# ≤ 0.2V and I <sub>I/O</sub> = 0mA other pins at 0.2V or V <sub>CC</sub> -0.2V	-	1	5	mA	
Standby Power Supply Current	I <sub>SB</sub>	CE# = V <sub>IH</sub>	-	0.3	0.5	mA	
	I <sub>SB1</sub>	CE# V ≥ V <sub>CC</sub> - 0.2V	-L	-	20	80	μA
			-LL	-	1	10	μA

Notes:

1. V<sub>IH</sub>(max) = V<sub>CC</sub> + 3.0V for pulse width less than 10ns.
2. V<sub>IL</sub>(min) = V<sub>SS</sub> - 3.0V for pulse width less than 10ns.
3. Over/Undershoot specifications are characterized, not 100% tested.
4. 10μA for special request
5. Typical values are included for reference only and are not guaranteed or tested.  
Typical values are measured at V<sub>CC</sub> = V<sub>CC</sub>(TYP.) and T<sub>A</sub> = 25°C

**CAPACITANCE** ( $T_A = 25^\circ\text{C}$ ,  $f = 1.0\text{MHz}$ )

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PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Input Capacitance	$C_{IN}$	-	6	pF
Input/Output Capacitance	$C_{I/O}$	-	8	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

**AC TEST CONDITIONS**

Input Pulse Levels	0.2V to $V_{CC} - 0.2\text{V}$
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	$C_L = 30\text{pF} + 1\text{TTL}$ , $I_{OH}/I_{OL} = -1\text{mA}/2\text{mA}$

**AC ELECTRICAL CHARACTERISTICS****READ CYCLE**

PARAMETER	SYM.	-35		-55		70		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	$t_{RC}$	35	-	55	-	70	-	ns
Address Access Time	$t_{AA}$	-	35	-	55	-	70	ns
Chip Enable Access Time	$t_{ACE}$	-	35	-	55	-	70	ns
Output Enable Access Time	$t_{OE}$	-	25	-	30	-	35	ns
Chip Enable to Output in Low-Z	$t_{CLZ}^*$	10	-	10	-	10	-	ns
Output Enable to Output in Low-Z	$t_{OLZ}^*$	5	-	5	-	5	-	ns
Chip Disable to Output in High-Z	$t_{CHZ}^*$	-	15	-	20	-	25	ns
Output Disable to Output in High-Z	$t_{OHZ}^*$	-	15	-	20	-	25	ns
Output Hold from Address Change	$t_{OH}$	10	-	10	-	10	-	ns

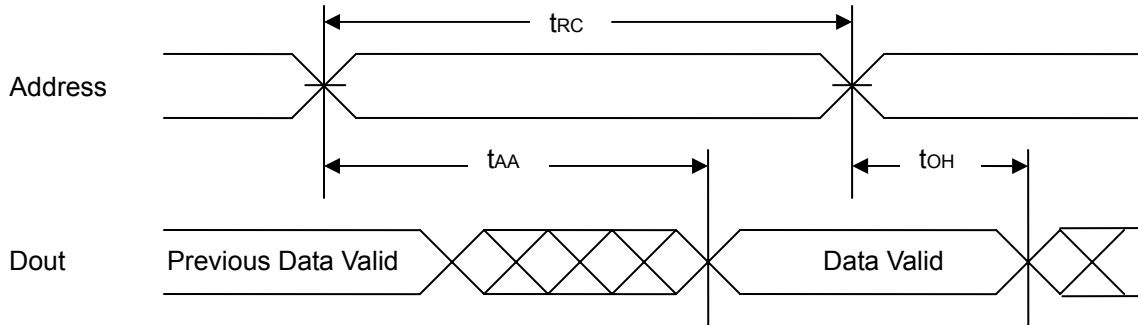
**WRITE CYCLE**

PARAMETER	SYM.	-35		-55		70		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	$t_{WC}$	35	-	55	-	70	-	ns
Address Valid to End of Write	$t_{AW}$	30	-	50	-	60	-	ns
Chip Enable to End of Write	$t_{CW}$	30	-	50	-	60	-	ns
Address Set-up Time	$t_{AS}$	0	-	0	-	0	-	ns
Write Pulse Width	$t_{WP}$	25	-	45	-	55	-	ns
Write Recovery Time	$t_{WR}$	0	-	0	-	0	-	ns
Data to Write Time Overlap	$t_{DW}$	20	-	25	-	30	-	ns
Data Hold from End of Write Time	$t_{DH}$	0	-	0	-	0	-	ns
Output Active from End of Write	$t_{OW}^*$	5	-	5	-	5	-	ns
Write to Output in High-Z	$t_{WHZ}^*$	-	15	-	20	-	25	ns

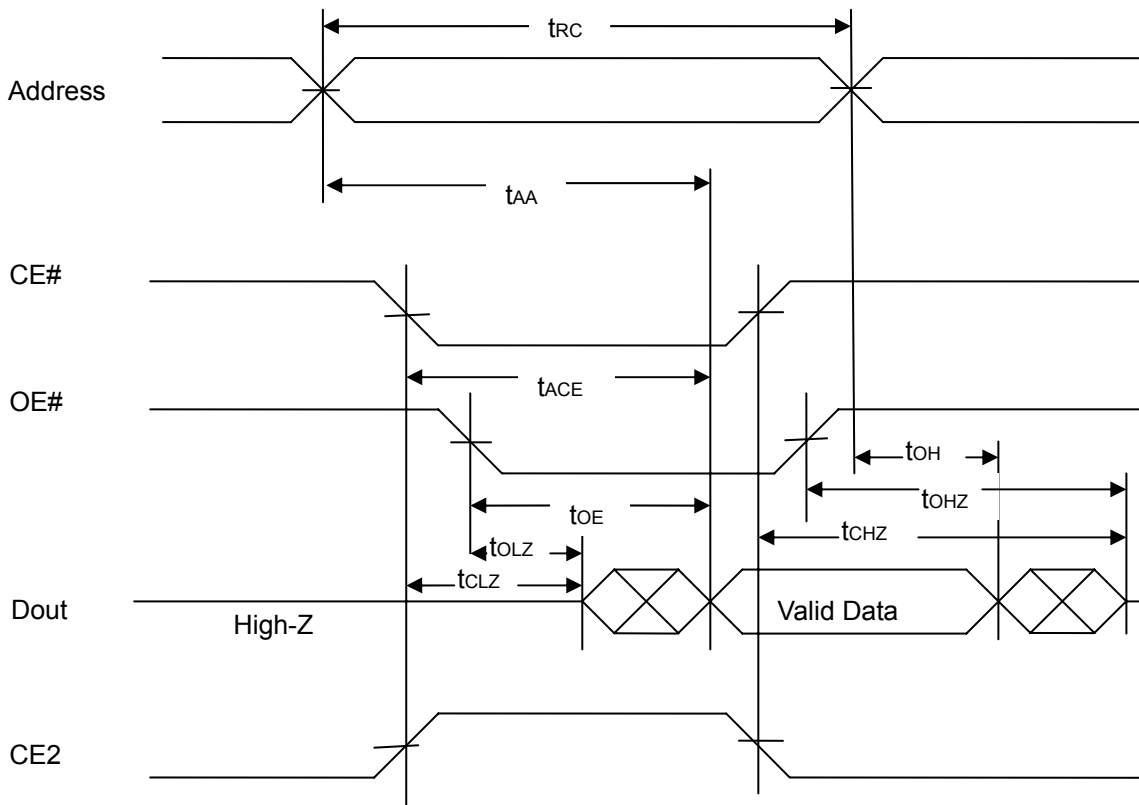
\*These parameters are guaranteed by device characterization, but not production tested.

TIMING WAVEFORMS

READ CYCLE 1 (Address Controlled) (1,2)



READ CYCLE 2 (CE#, CE2 and OE# controlled) (1,3,4,5)

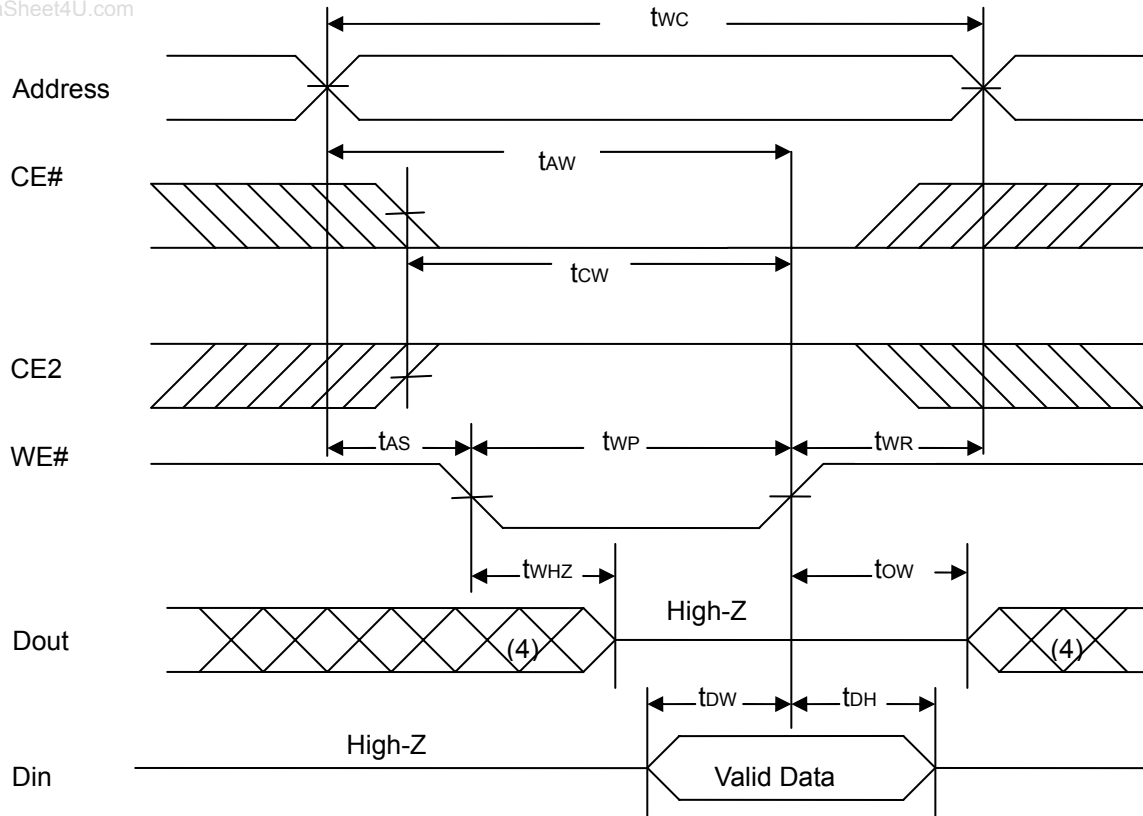


Notes :

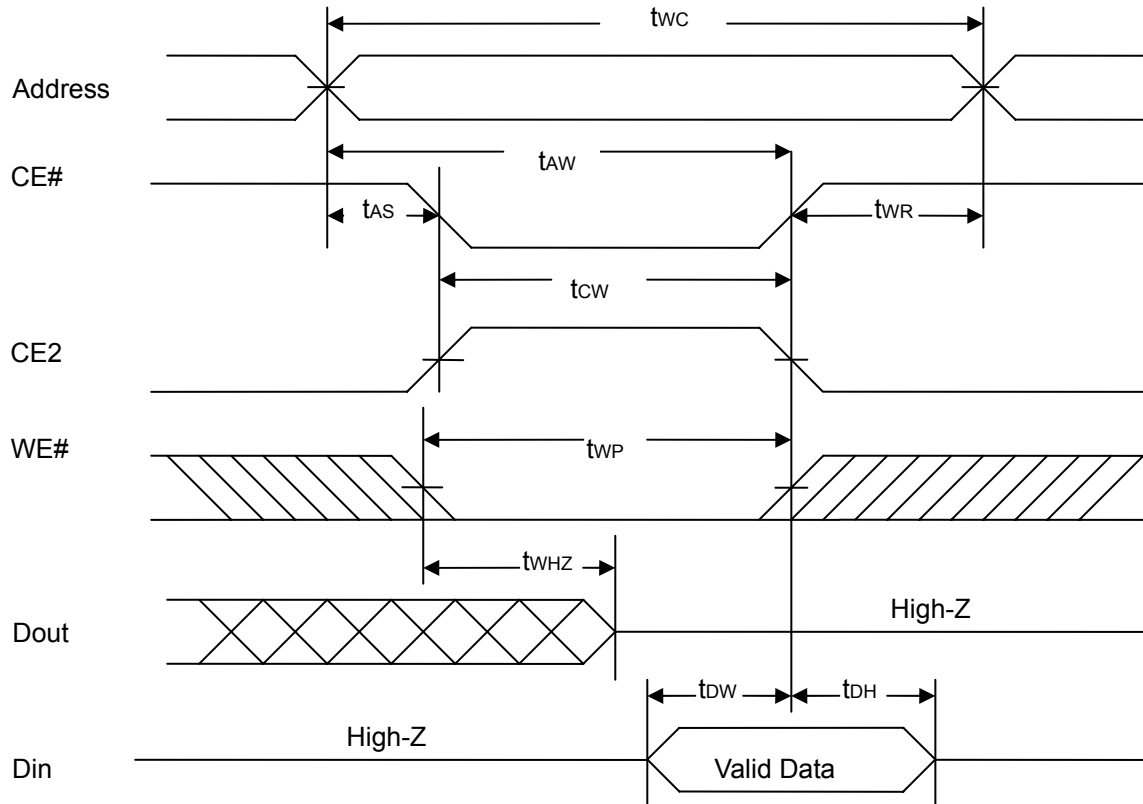
1. WE# is high for read cycle.
2. Device is continuously selected OE# = low, CE# = low, CE2 = high.
3. Address must be valid prior to or coincident with CE# = low, CE2 = high; otherwise  $t_{AA}$  is the limiting parameter.
4.  $t_{CLZ}$ ,  $t_{OLZ}$ ,  $t_{CHZ}$  and  $t_{OHZ}$  are specified with  $C_L = 5pF$ . Transition is measured  $\pm 500mV$  from steady state.
5. At any given temperature and voltage condition,  $t_{CHZ}$  is less than  $t_{CLZ}$ ,  $t_{OHZ}$  is less than  $t_{OLZ}$ .

**WRITE CYCLE 1 (WE# Controlled) (1,2,3,5,6)**

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**WRITE CYCLE 2 (CE# Controlled) (1,2,5,6)**



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1. WE#, CE# must be high during all address transitions.
2. A write occurs during the overlap of a low CE#, low WE#.
3. During a WE# controlled write cycle with OE# low, tWP must be greater than tWHZ + tDW to allow the drivers to turn off and data to be placed on the bus.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the CE# low transition occurs simultaneously with or after WE# low transition, the outputs remain in a high impedance state.
6. tOW and tWHZ are specified with CL = 5pF. Transition is measured  $\pm 500$ mV from steady state.



**DATA RETENTION CHARACTERISTICS**

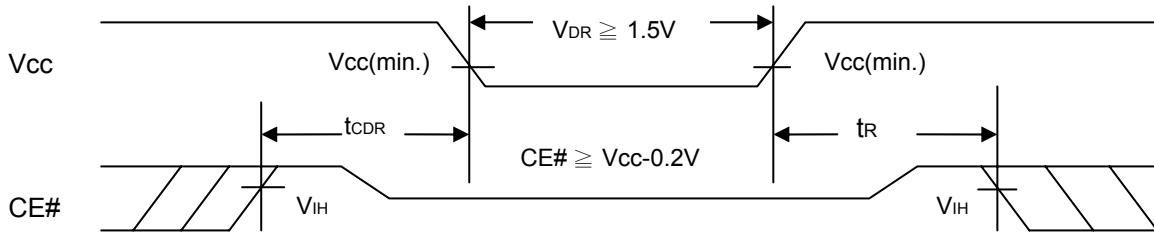
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PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT	
Vcc for Data Retention	V <sub>DR</sub>	CE# V ≥ V <sub>CC</sub> - 0.2V	1.5	-	3.6	V	
Data Retention Current	I <sub>DR</sub>	V <sub>CC</sub> = 1.5V CE# V ≥ V <sub>CC</sub> - 0.2V	-L	-	1	50	μA
			-LL	-	0.5	5	μA
			-LLE		0.5	10	μA
			-LLI				
Chip Disable to Data Retention Time	t <sub>CDR</sub>	See Data Retention Waveforms (below)	0	-	-	ns	
Recovery Time	t <sub>r</sub>		t <sub>RC</sub> *	-	-	ns	

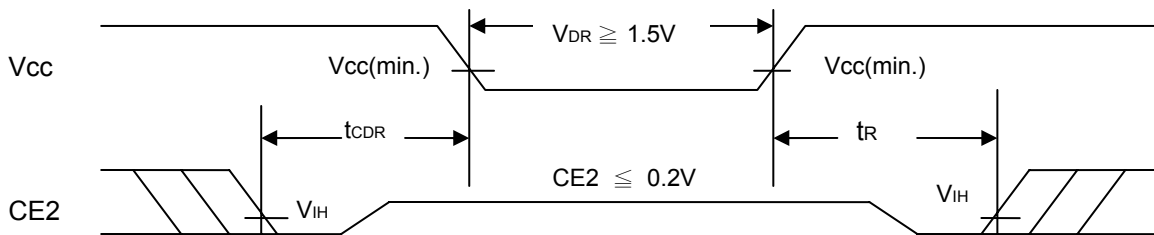
t<sub>RC</sub>\* = Read Cycle Time

**DATA RETENTION WAVEFORM**

**Low Vcc Data Retention Waveform (1) (CE# controlled)**



**Low Vcc Data Retention Waveform (2) (CE2 controlled)**

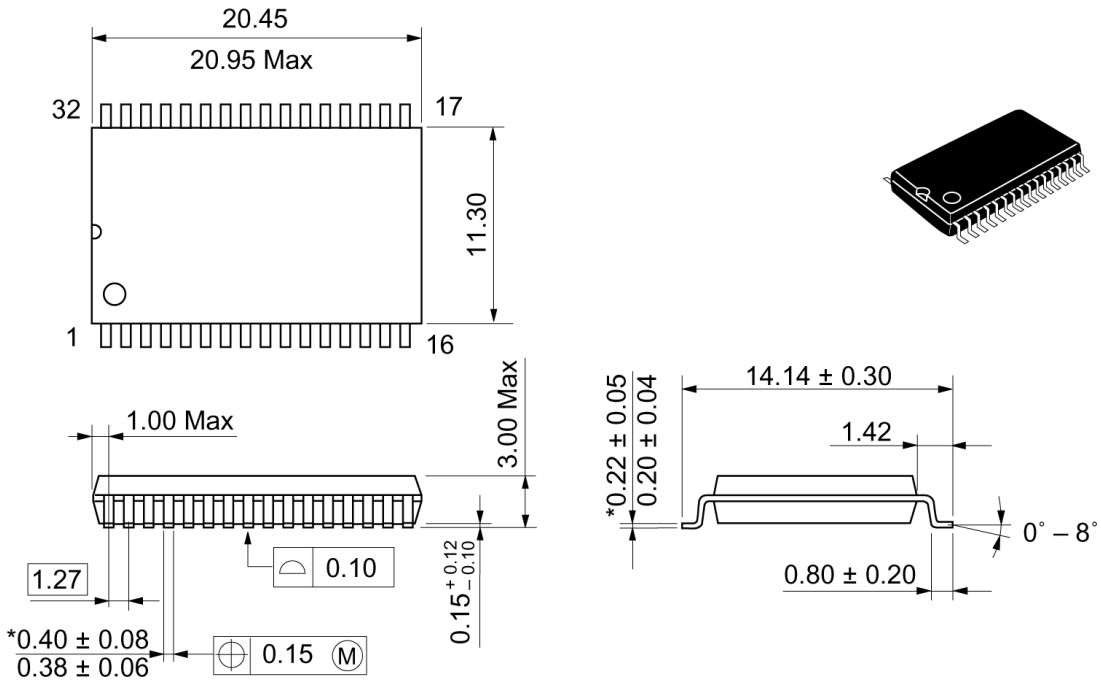


**PACKAGE OUTLINE DIMENSION**

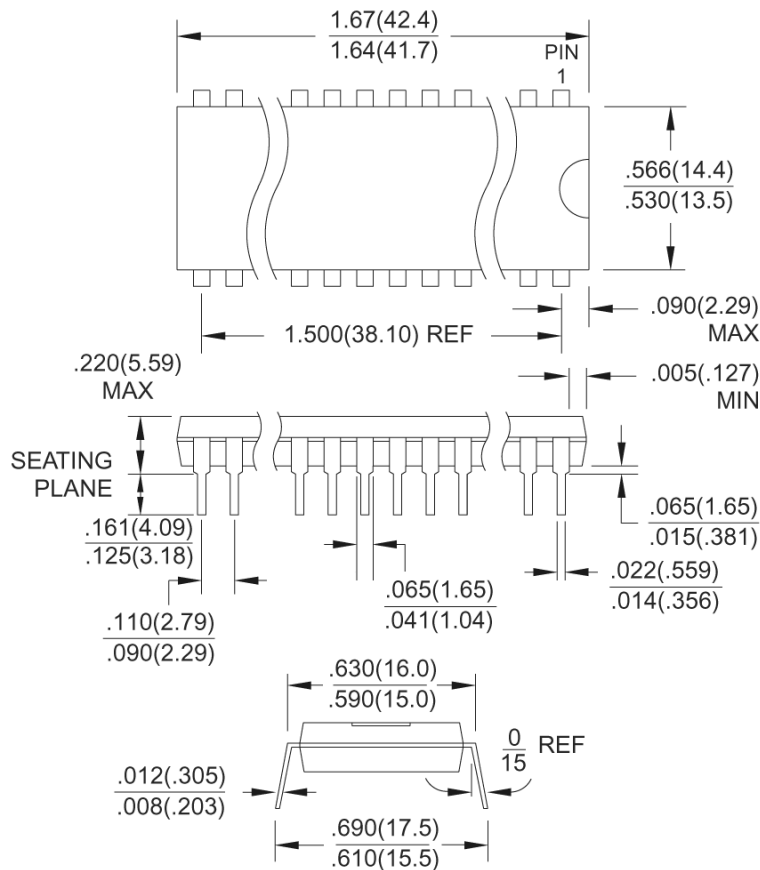
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**32 pin 450 mil SOP Package Outline Dimension**

Unit: mm

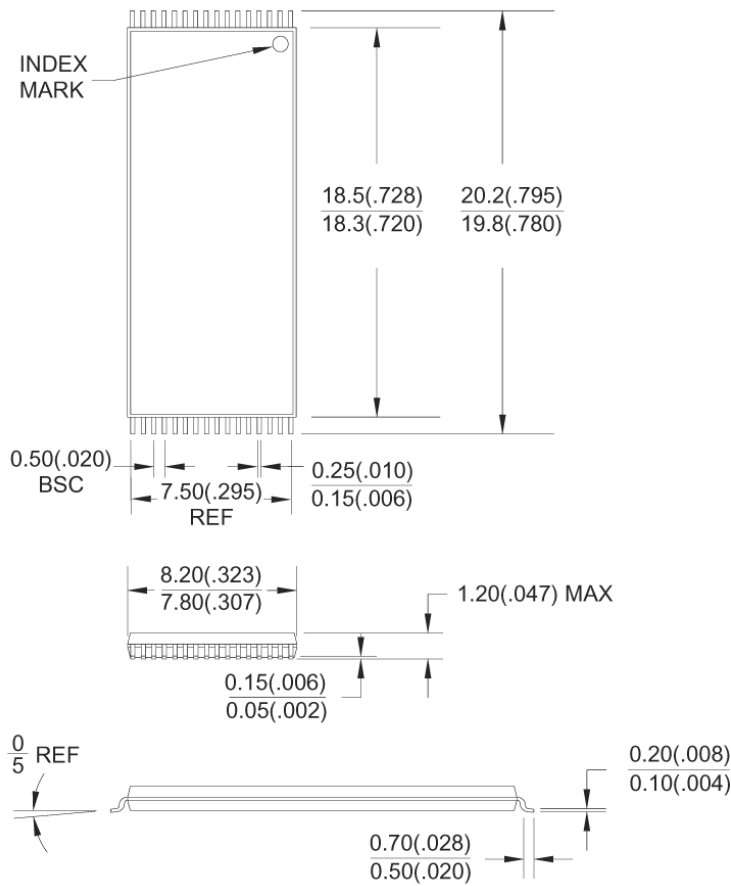


**32 pin 600 mil P-DIP Package Outline Dimension**

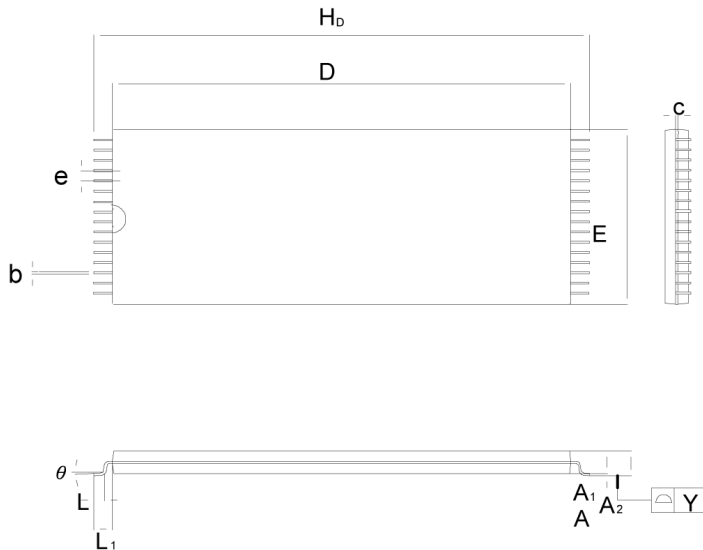


32 pin 8mm x 20mm TSOP-I Package Outline Dimension

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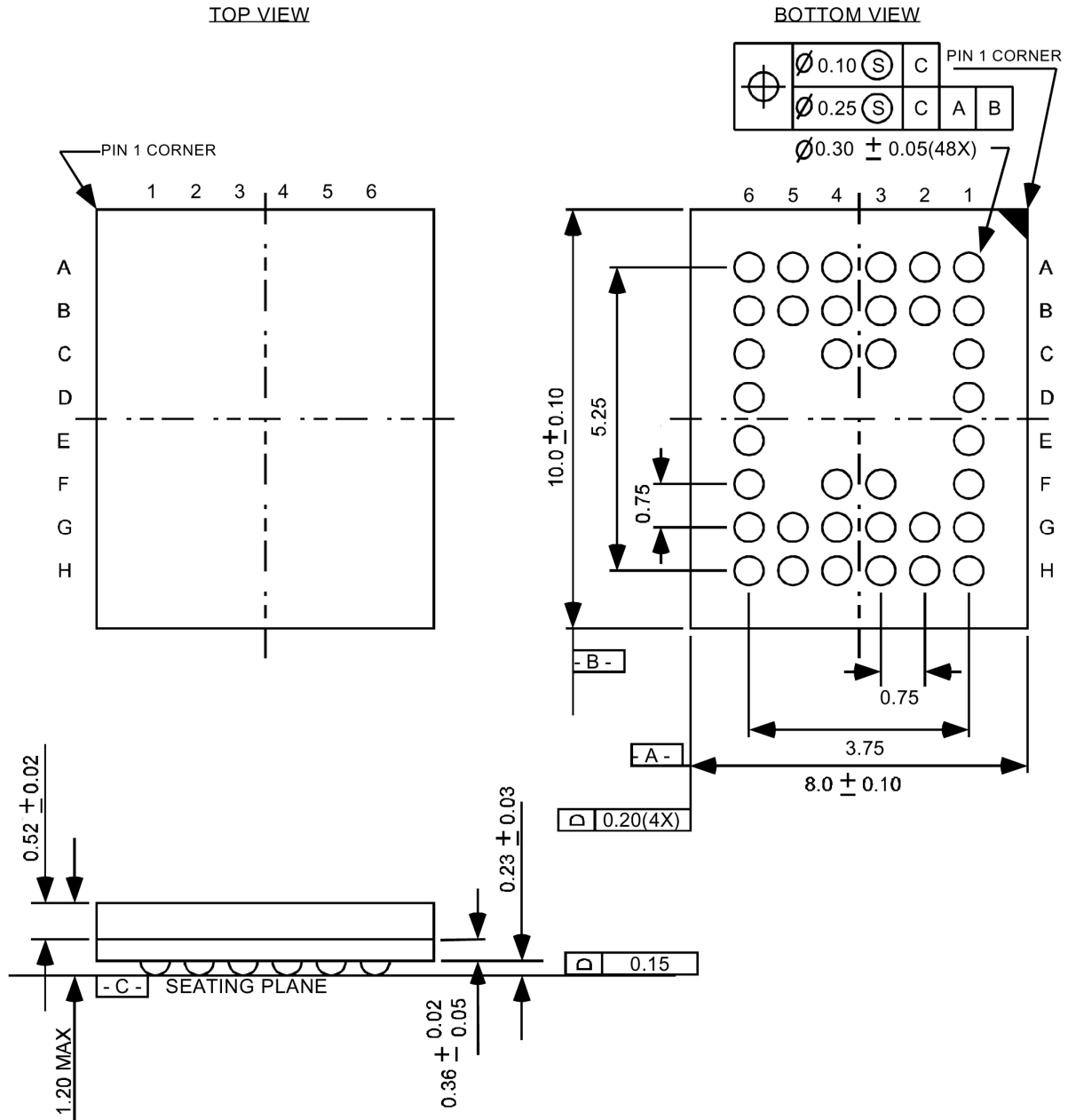


32 pin 8mm x 13.4mm STSOP Package Outline Dimension

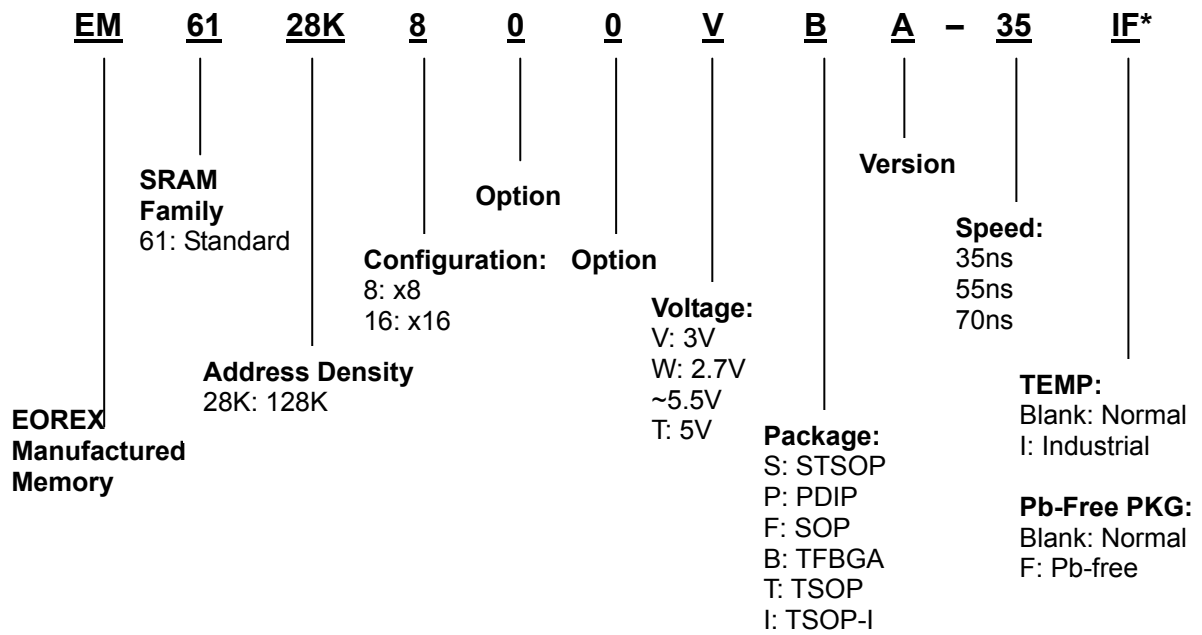


Symbol	Dimension in Inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A			0.047			1.20
A <sub>1</sub>	0.002		0.006	0.05		0.15
A <sub>2</sub>	0.035	0.040	0.041	0.95	1.00	1.05
b	0.007	0.009	0.010	0.17	0.22	0.27
c	0.004	-----	0.008	0.10	-----	0.21
D		0.488			12.40	
E		0.315			8.00	
H <sub>D</sub>		0.551			14.00	
e		0.020			0.50	
L	0.020	0.024	0.028	0.50	0.60	0.70
L <sub>1</sub>		0.031			0.80	
Y	0.000		0.004	0.00		0.10
θ	0	3	5	0	3	5

36-ball 6mm × 8mm TFBGA Package Outline Dimension



Product ID Information



\* Product ID example

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