

Document Title

512K x8 bit Super Low Power and Low Voltage Full CMOS Static RAM

Revision History

Revision No.	History	Draft Date	Remark
0.0	Initial Draft	October 24,2002	Preliminary
0.1	2' nd Draft Changed Icc, Icc1 value	November 11 , 2002	
0.2	3'rd Draft Changed I <sub>SB1</sub> test conditions, Changed VDR & IDR measurement condition	December 23 , 2002	
0.3	4' th Draft Add Pb-free part number	February 13 , 2004	

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The attached datasheets are provided by EMLSI reserve the right to change the specifications and products. EMLSI will answer to your questions about device. If you have any questions, please contact the EMLSI office.

**FEATURES**

- Process Technology : 0.18µm Full CMOS
- Organization : 512K x 8 bit
- Power Supply Voltage : 1.65V ~ 2.2V
- Low Data Retention Voltage : 1.0V(Min)
- Three state outputs
- Package Type : 36-FPBGA 6.0x7.0

**GENERAL DESCRIPTION**

The EM640FP8 families are fabricated by EMLSI's advanced full CMOS process technology. The families support industrial temperature range and Chip Scale Package for user flexibility of system design. The families also supports low data retention voltage for battery back-up operation with low data retention current.

**PRODUCT FAMILY**

Product Family	Operating Temperature	Vcc Range	Speed	Power Dissipation		PKG Type
				Standby (I <sub>SB1</sub> , Typ)	Operating (I <sub>CC1</sub> , Max)	
EM640FP8	Industrial (-40 ~ 85°C)	1.65~2.2V	70ns <sup>1)</sup>	1 µA	2 mA	36 FPBGA (6.0x7.0)

1. The parameter is measured with 30pF test load.

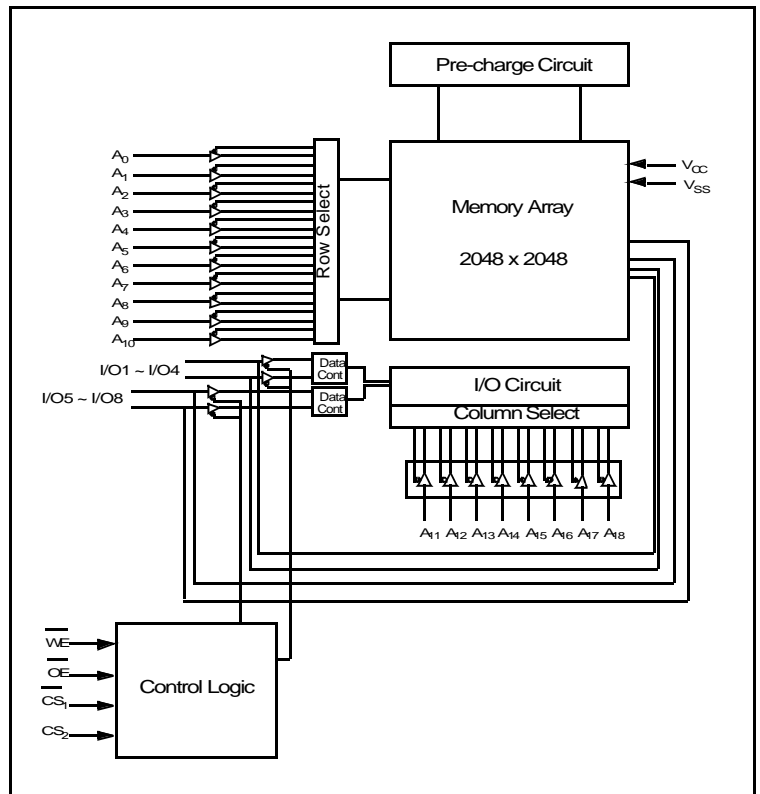
**PIN DESCRIPTION**

	1	2	3	4	5	6
A	A <sub>0</sub>	A <sub>1</sub>	CS <sub>2</sub>	A <sub>3</sub>	A <sub>6</sub>	A <sub>8</sub>
B	I/O <sub>5</sub>	A <sub>2</sub>	$\overline{WE}$	A <sub>4</sub>	A <sub>7</sub>	I/O <sub>1</sub>
C	I/O <sub>6</sub>		DNU	A <sub>5</sub>		I/O <sub>2</sub>
D	V <sub>SS</sub>					V <sub>CC</sub>
E	V <sub>CC</sub>					V <sub>SS</sub>
F	I/O <sub>7</sub>		A <sub>18</sub>	A <sub>17</sub>		I/O <sub>3</sub>
G	I/O <sub>8</sub>	$\overline{OE}$	$\overline{CS}_1$	A <sub>16</sub>	A <sub>15</sub>	I/O <sub>4</sub>
H	A <sub>9</sub>	A <sub>10</sub>	A <sub>11</sub>	A <sub>12</sub>	A <sub>13</sub>	A <sub>14</sub>

36-FPBGA : Top view (ball down)

Name	Function	Name	Function
$\overline{CS}_1, CS_2$	Chip select inputs	$\overline{WE}$	Write Enable input
$\overline{OE}$	Output Enable input	Vcc	Power Supply
A <sub>0</sub> -A <sub>18</sub>	Address Inputs	Vss	Ground
I/O <sub>1</sub> -I/O <sub>8</sub>	Data Inputs/outputs	DNU	Do Not Use

**FUNCTIONAL BLOCK DIAGRAM**



**ABSOLUTE MAXIMUM RATINGS \***

Parameter	Symbol	Ratings	Unit
Voltage on Any Pin Relative to V <sub>SS</sub>	V <sub>IN</sub> , V <sub>OUT</sub>	-0.5V to V <sub>CC</sub> +0.3V (Max.2.5V)	V
Voltage on V <sub>CC</sub> supply relative to V <sub>SS</sub>	V <sub>CC</sub>	-0.3V to 2.5V	V
Power Dissipation	P <sub>D</sub>	1.0	W
Operating Temperature	T <sub>A</sub>	-40 to 85	°C

\* Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**FUNCTIONAL DESCRIPTION**

$\overline{CS}_1$	CS <sub>2</sub>	$\overline{OE}$	$\overline{WE}$	I/O	Mode	Power
H	X	X	X	High-Z	Deselected	Stand by
X	L	X	X	High-Z	Deselected	Stand by
L	H	H	H	High-Z	Output Disabled	Active
L	H	L	H	Data Out	Read	Active
L	H	X	L	Data In	Write	Active

Note: X means don' t care. (Must be low or high state)

**RECOMMENDED DC OPERATING CONDITIONS**<sup>1)</sup>

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	$V_{CC}$	1.65	1.8	2.2	V
Ground	$V_{SS}$	0	0	0	V
Input high voltage	$V_{IH}$	1.4	-	$V_{CC} + 0.3^{2)}$	V
Input low voltage	$V_{IL}$	-0.3 <sup>3)</sup>	-	0.4	V

1.  $T_A = -40$  to  $85^\circ\text{C}$ , otherwise specified
2. Overshoot:  $V_{CC} + 1.0$  V in case of pulse width  $\leq 20$ ns
3. Undershoot:  $-1.0$  V in case of pulse width  $\leq 20$ ns
4. Overshoot and undershoot are sampled, not 100% tested.

**CAPACITANCE**<sup>1)</sup> ( $f = 1\text{MHz}$ ,  $T_A = 25^\circ\text{C}$ )

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	$C_{IN}$	$V_{IN} = 0\text{V}$	-	8	pF
Input/Output capacitance	$C_{IO}$	$V_{IO} = 0\text{V}$	-	10	pF

1. Capacitance is sampled, not 100% tested

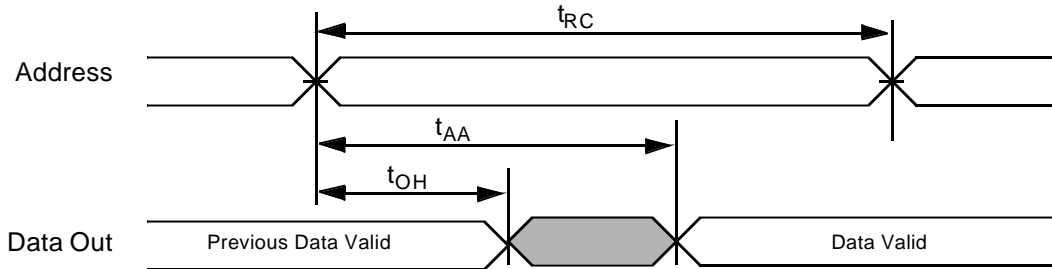
**DC AND OPERATING CHARACTERISTICS**

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit	
Input leakage current	$I_{LI}$	$V_{IN} = V_{SS}$ to $V_{CC}$	-1	-	1	$\mu\text{A}$	
Output leakage current	$I_{LO}$	$\overline{CS}_1 = V_{IH}$ , $CS_2 = V_{IL}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$ , $V_{IO} = V_{SS}$ to $V_{CC}$	-1	-	1	$\mu\text{A}$	
Operating power supply	$I_{CC}$	$I_{IO} = 0\text{mA}$ , $\overline{CS}_1 = V_{IL}$ , $CS_2 = \overline{WE} = V_{IH}$ , $V_{IN} = V_{IH}$ or $V_{IL}$	-	-	2	mA	
Average operating current	$I_{CC1}$	Cycle time = $1\mu\text{s}$ , 100% duty, $I_{IO} = 0\text{mA}$ , $\overline{CS}_1 \leq 0.2\text{V}$ , $CS_2 \geq V_{CC} - 0.2\text{V}$ , $V_{IN} \leq 0.2\text{V}$ or $V_{IN} \geq V_{CC} - 0.2\text{V}$	-	-	2	mA	
	$I_{CC2}$	Cycle time = Min, $I_{IO} = 0\text{mA}$ , 100% duty, $\overline{CS}_1 = V_{IL}$ , $CS_2 = V_{IH}$ , $V_{IN} = V_{IL}$ or $V_{IH}$	70ns	-	-	12	mA
Output low voltage	$V_{OL}$	$I_{OL} = 0.1\text{mA}$	-	-	0.2	V	
Output high voltage	$V_{OH}$	$I_{OH} = -0.1\text{mA}$	1.4	-	-	V	
Standby Current (CMOS)	$I_{SB1}$	$\overline{CS}_1 \geq V_{CC} - 0.2\text{V}$ , $CS_2 \geq V_{CC} - 0.2\text{V}$ ( $\overline{CS}_1$ controlled) or $0\text{V} \leq CS_2 \leq 0.2\text{V}$ ( $CS_2$ controlled), Other inputs = $0 \sim V_{CC}$ (Typ. condition : $V_{CC} = 1.8\text{V}$ @ $25^\circ\text{C}$ ) (Max. condition : $V_{CC} = 2.2\text{V}$ @ $85^\circ\text{C}$ )	LL LF	-	1	5	$\mu\text{A}$

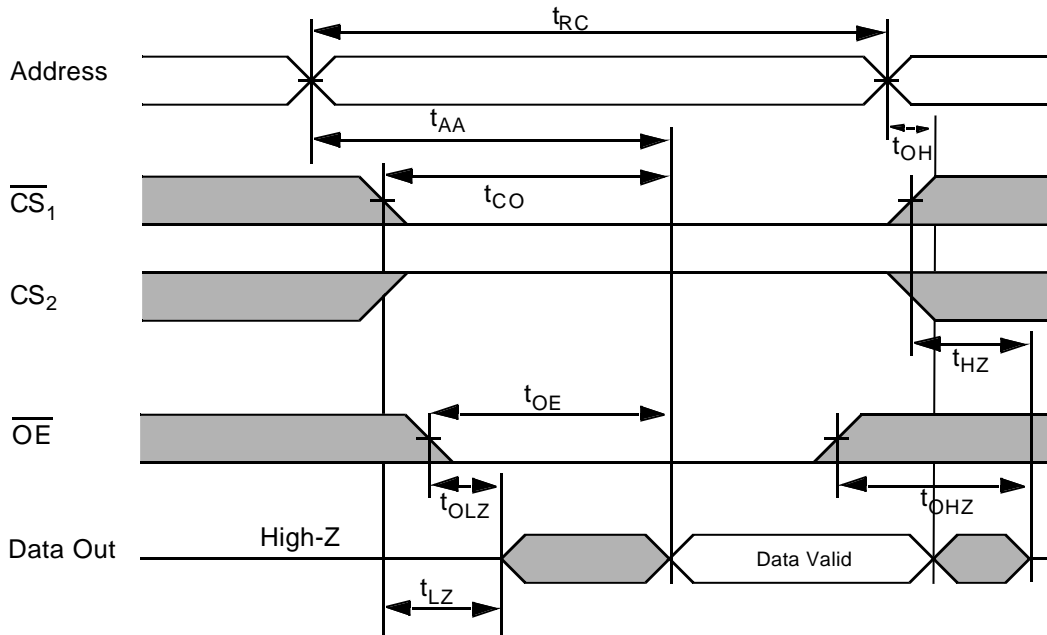


**TIMING DIAGRAMS**

**TIMING WAVEFORM OF READ CYCLE(1).** (Address Controlled,  $\overline{CS}_1 = \overline{OE} = V_{IL}$ ,  $CS_2 = \overline{WE} = V_{IH}$ )



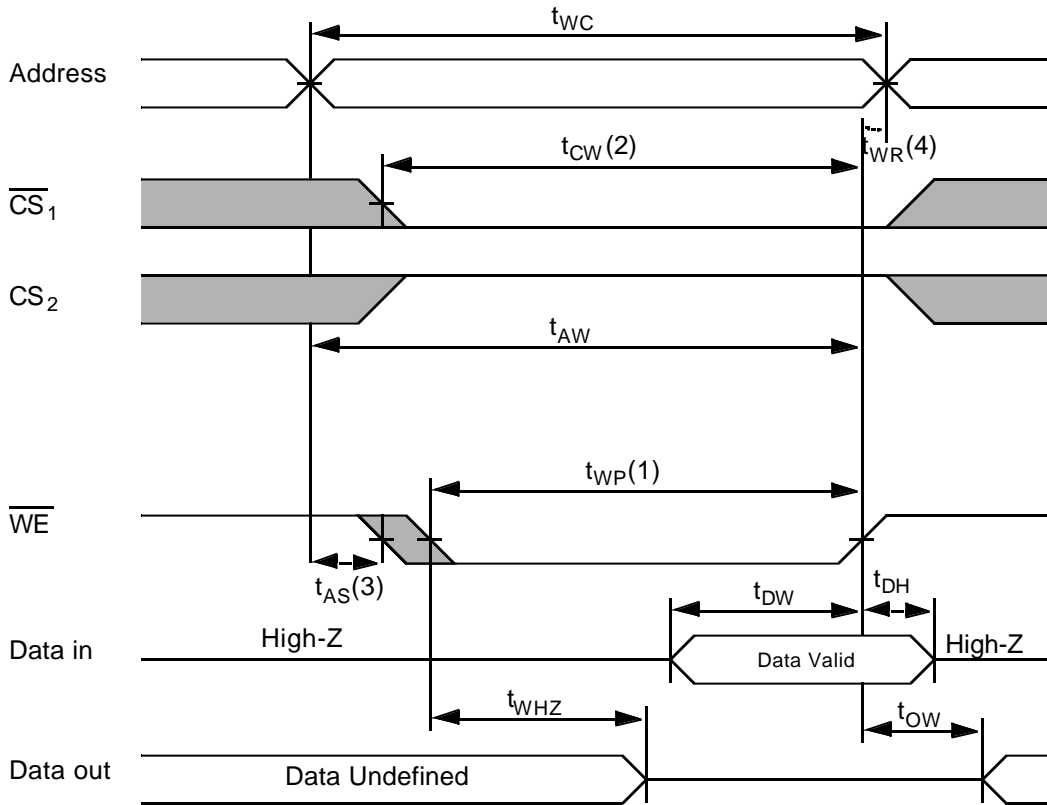
**TIMING WAVEFORM OF READ CYCLE(2)** ( $\overline{WE} = V_{IH}$ )



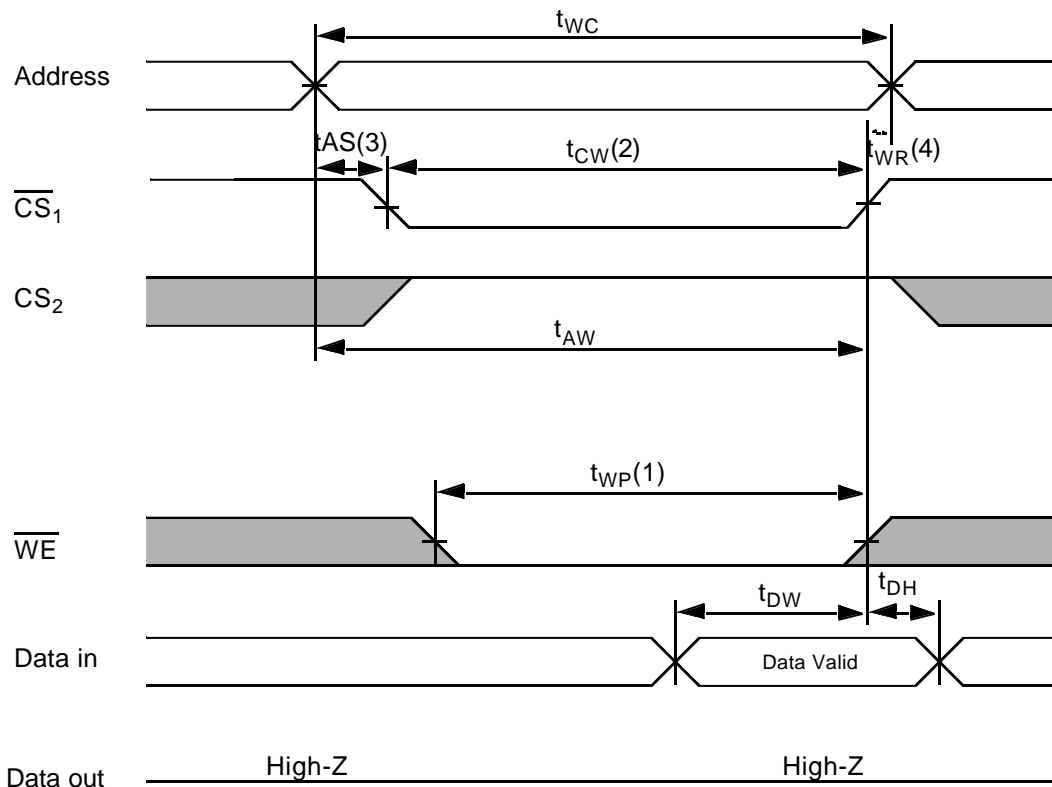
**NOTES (READ CYCLE)**

1.  $t_{HZ}$  and  $t_{OHZ}$  are defined as the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition,  $t_{HZ}(\text{Max.})$  is less than  $t_{LZ}(\text{Min.})$  both for a given device and from device to device interconnection.

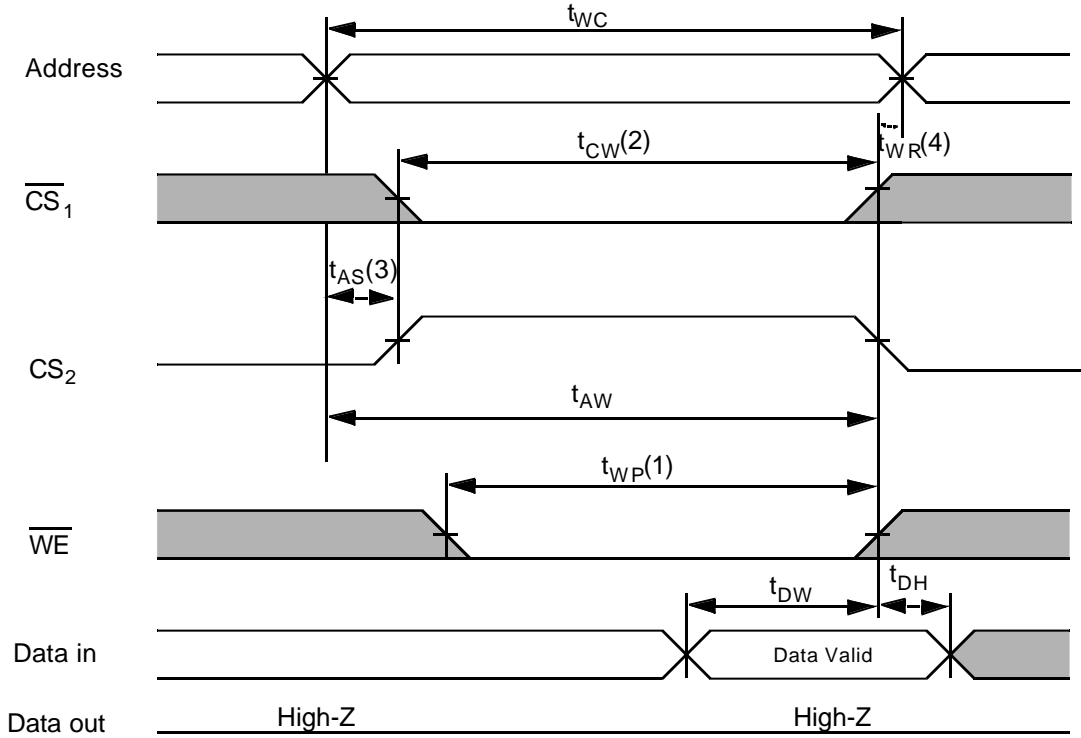
**TIMING WAVEFORM OF WRITE CYCLE(1) ( $\overline{WE}$  CONTROLLED)**



**TIMING WAVEFORM OF WRITE CYCLE(2) ( $\overline{CS}_1$  CONTROLLED)**



**TIMING WAVEFORM OF WRITE CYCLE(3) ( CS<sub>2</sub> CONTROLLED)**



**NOTES (WRITE CYCLE)**

1. A write occurs during the overlap(t<sub>WP</sub>) of low  $\overline{CS}_1$ , a high CS<sub>2</sub> and low  $\overline{WE}$ . A write begins at the latest transition among  $\overline{CS}_1$  goes low, CS<sub>2</sub> goes high and  $\overline{WE}$  goes low. A write ends at the earliest transition when  $\overline{CS}_1$  goes high, CS<sub>2</sub> goes high and  $\overline{WE}$  goes high. The t<sub>WP</sub> is measured from the beginning of write to the end of write.
2. t<sub>CW</sub> is measured from the  $\overline{CS}_1$  going low to end of write.
3. t<sub>AS</sub> is measured from the address valid to the beginning of write.
4. t<sub>WR</sub> is measured from the end of write to the address change. t<sub>WR</sub> applied in case a write ends as  $\overline{CS}_1$  or  $\overline{WE}$  going high.



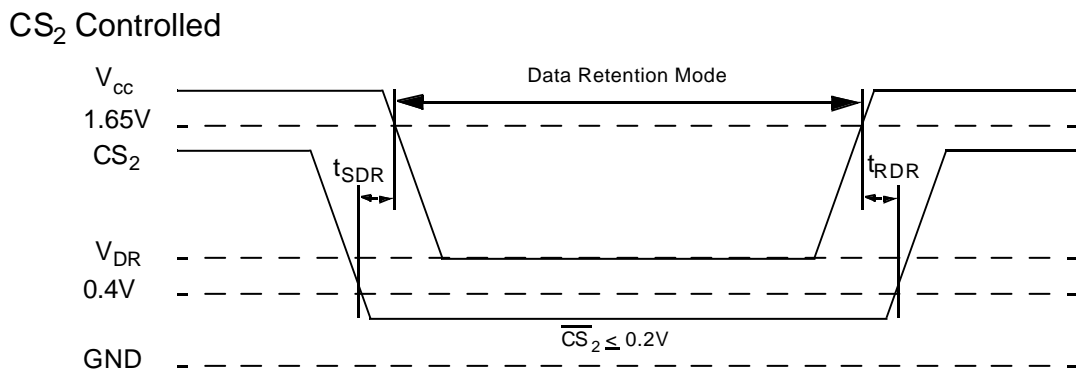
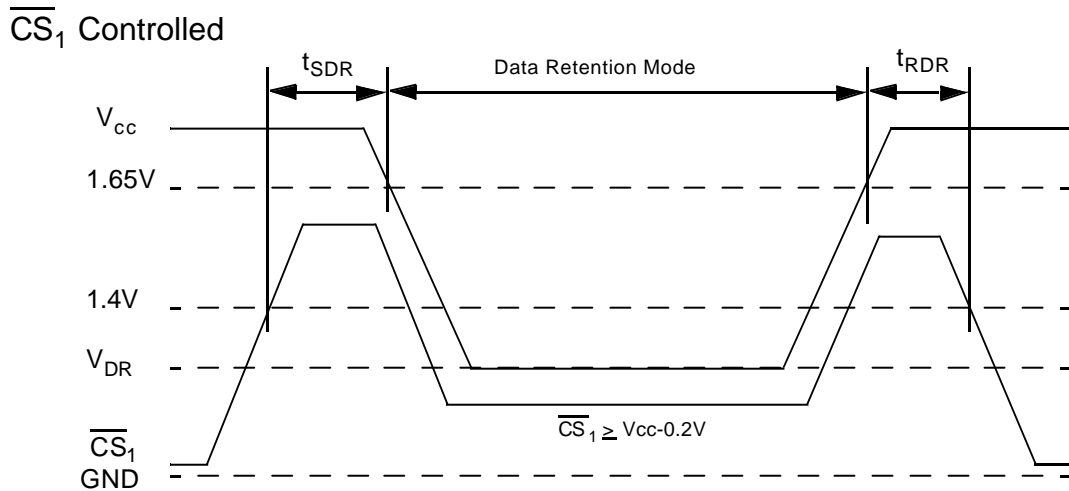
**DATA RETENTION CHARACTERISTICS**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
V <sub>CC</sub> for Data Retention	V <sub>DR</sub>	I <sub>SB1</sub> Test Condition (Chip Disabled) <sup>1)</sup>	1.0	-	2.2	V
Data Retention Current	I <sub>DR</sub>	V <sub>CC</sub> =1.2V, I <sub>SB1</sub> Test Condition (Chip Disabled) <sup>1)</sup>	-	0.5	2	μA
Chip Deselect to Data Retention Time	t <sub>SDR</sub>	See data retention wave form	0	-	-	ns
Operation Recovery Time	t <sub>RDR</sub>		t <sub>RC</sub>	-	-	

**NOTES**

1. See the I<sub>SB1</sub> measurement condition of datasheet page 4.

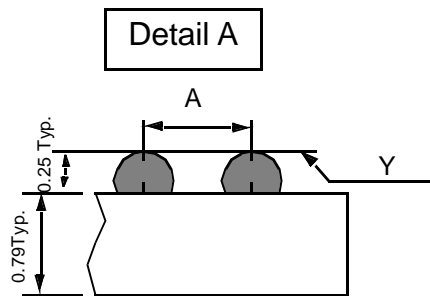
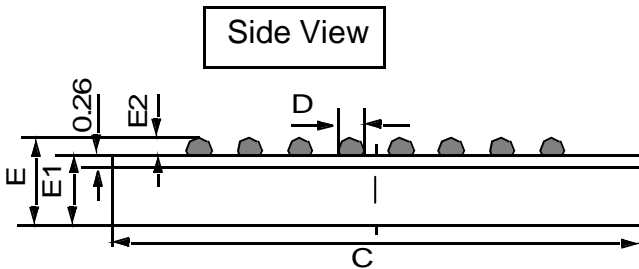
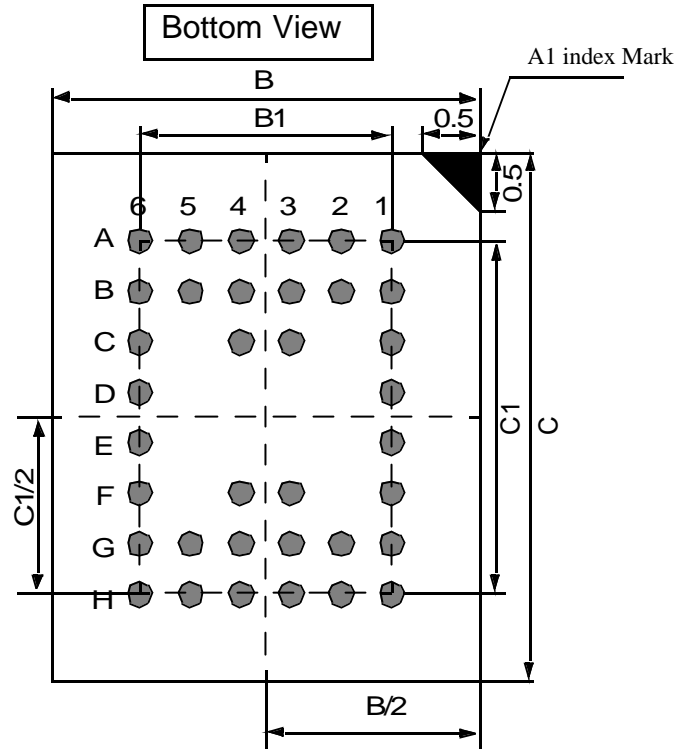
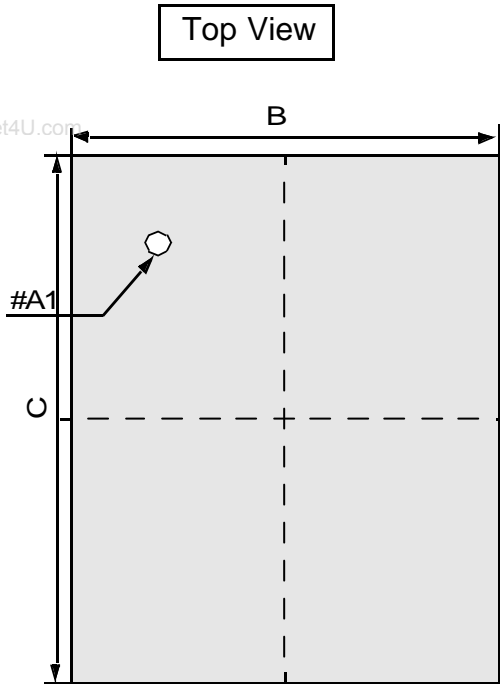
**DATA RETENTION WAVE FORM**



Unit: millimeters

**PACKAGE DIMENSION**

36 Ball Fine Pitch BGA (0.75mm ball pitch)

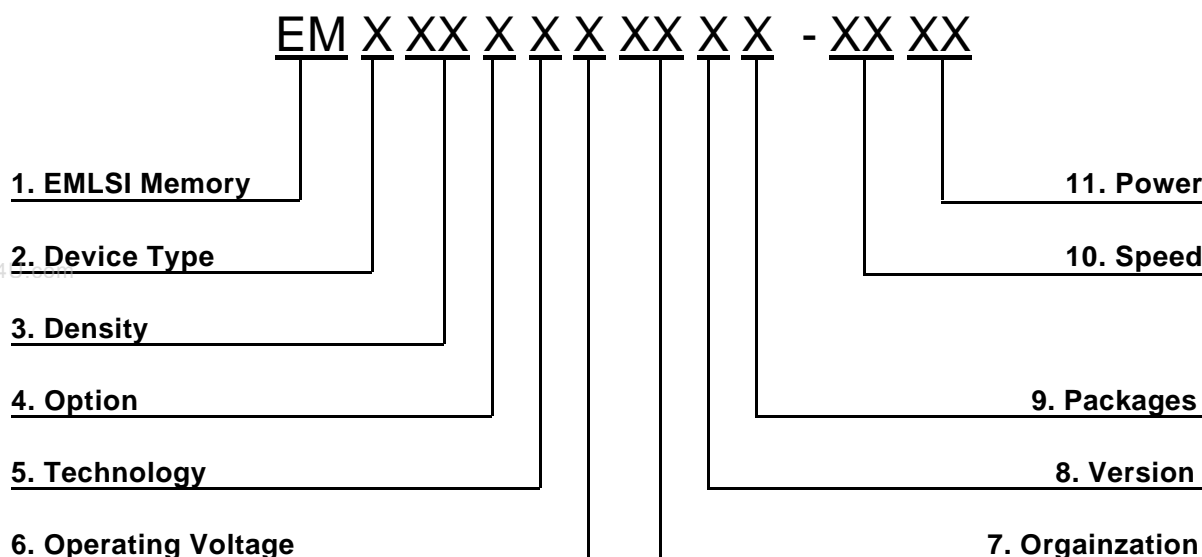


	Min	Typ	Max
A	-	0.75	-
B	5.95	6.00	6.05
B1	-	3.75	-
C	6.95	7.00	7.05
C1	-	5.25	-
D	0.30	0.35	0.40
E	1.00	1.04	1.10
E1	-	0.79	-
E2	-	0.25	-
Y	-	-	0.08

**NOTES.**

1. Bump counts : 36(8row x 6column)
2. Bump pitch : (x,y)=(0.75x0.75) (typ.)
3. All tolerance are +/-0.050 unless otherwise specified.
4. Typ : Typical
5. Y is coplanarity : 0.08(Max)

**MEMORY FUNCTION GUIDE**



- 1. Memory Component
- 2. Device Type
  - 6 ----- Low Power SRAM
  - 7 ----- STRAM
- 3. Density
  - 1 ----- 1M
  - 2 ----- 2M
  - 4 ----- 4M
  - 8 ----- 8M
  - 16 ----- 16M
  - 32 ----- 32M
  - 64 ----- 64M
- 4. Option
  - 0 ----- Dual CS
  - 1 ----- Single CS
- 5. Technology
  - Blank ----- CMOS
  - F ----- Full CMOS
- 6. Operating Voltage
  - Blank ----- 5V
  - V ----- 3.3V
  - U ----- 3.0V
  - S ----- 2.5V
  - R ----- 2.0V
  - P ----- 1.8V
- 7. Organization
  - 8 ----- x8 bit
  - 16 ----- x16 bit
  - 32 ----- x32 bit

- 8. Version
  - Blank ----- Mother Die
  - A ----- First revision
  - B ----- Second revision
  - C ----- Third revision
  - D ----- Fourth revision
- 9. Package
  - Blank ----- Package
  - W ----- Wafer
- 10. Speed
  - 45 ----- 45ns
  - 55 ----- 55ns
  - 70 ----- 70ns
  - 85 ----- 85ns
  - 10 ----- 100ns
  - 12 ----- 120ns
- 11. Power
  - LL ----- Low Low Power
  - LF ----- Low Low Power(Pb-Free)
  - L ----- Low Power
  - S ----- Standard Power