

Document Title

512K x8 bit Low Power Full CMOS Static RAM

Revision History

Revision No.	History	Draft Date	Remark
0.0	Initial Draft	Nov. 20, 2007	Preliminary
0.1	0.1 Revision I_{DR} Current from 1.5 μ A to 7 μ A t_{OE} from 25nsec to 30nsec with 55ns part	Dec. 5, 2007	

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512K x8 Bit Low Power CMOS Static RAM

FEATURES

- Very high speed : 45ns
- Process Technology : 0.15um Full CMOS
- Organization : 512K x8
- Power Supply Voltage
=> EM641FT8V : 4.5V~5.5V
- Low Data Retention Voltage : 1.5V (MIN)
- Three state output and TTL Compatible
- Packaged product designed for 45/55/70ns
- Package Type: 32L-SOP

GENERAL DESCRIPTION

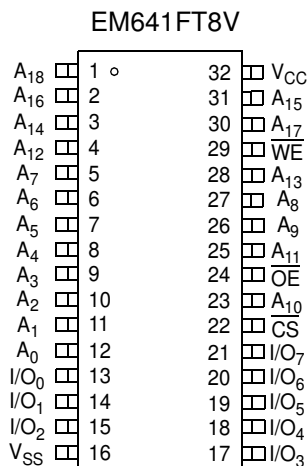
The EM641FT8V is fabricated by EMLSI's advanced full CMOS process technology. The families support industrial temperature range and Chip Scale Package for user flexibility of system design. The families also supports low data retention voltage for battery back-up operation with low data retention current.

The EM641FT8V is available in KGD, JEDEC standard 32 pin 450mil Plastic SOP package.

PRODUCT FAMILY

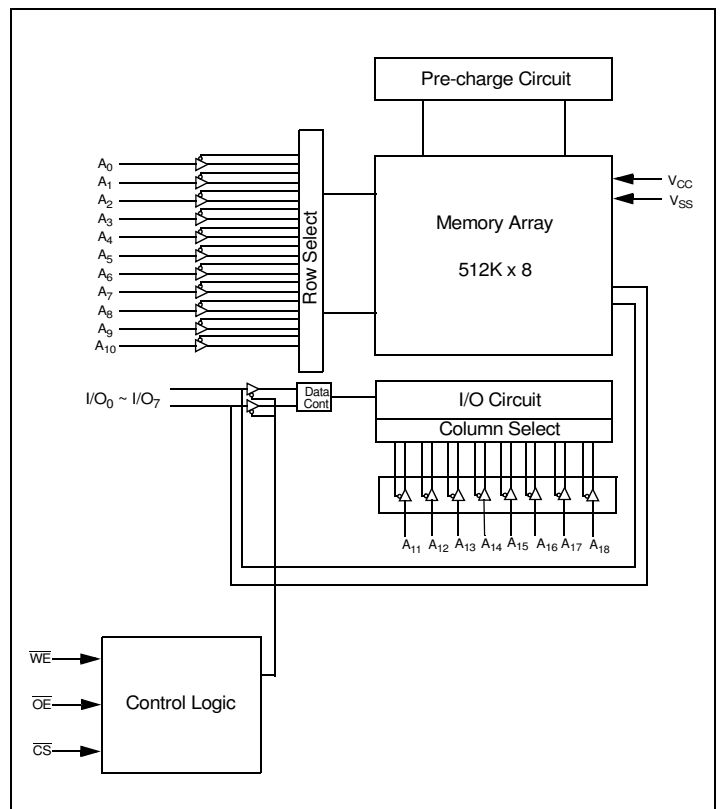
Product Family	Operating Temperature	Vcc Range	Speed	Power Dissipation		PKG Type
				Standby (I _{SB1} , Typ.)	Operating (I _{CC1} -Max)	
EM641FT8V-45LF	Industrial (-40 ~ 85°C)	4.5V~5.5V	45ns	1.5 μA	7mA	32-SOP
EM641FT8V-55LF	Industrial (-40 ~ 85°C)	4.5V~5.5V	55ns	1.5 μA	7mA	32-SOP
EM641FT8V-70LF	Industrial (-40 ~ 85°C)	4.5V~5.5V	70ns	1.5 μA	7mA	32-SOP

PIN DESCRIPTION



Name	Function	Name	Function
\overline{CS}	Chip select input	V _{CC}	Power Supply
\overline{OE}	Output Enable input	V _{SS}	Ground
\overline{WE}	Write Enable input		
A ₀ ~A ₁₈	Address Inputs		
I/O ₀ ~I/O ₇	Data Inputs/Outputs		

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Minimum	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	-0.5 to 6.0V	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	-0.5 to 6.0V	V
Power Dissipation	P_D	1.0	W
Operating Temperature	T_A	-40 to 85	°C

Note : Stresses greater than those listed above "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

FUNCTIONAL DESCRIPTION

\overline{CS}	\overline{OE}	\overline{WE}	I/O ₀₋₇	Mode	Power
H	X	X	High-Z	Deselected/ Power down	Stand by
L	L	H	Data Out	Read	Active
L	X	L	Data In	Write	Active
L	H	H	High-Z	Selected, Output Disabled	Active

Note : X means don't care. (Must be low or high state)

RECOMMENDED DC OPERATING CONDITIONS ¹⁾

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	$V_{CC}^{2)}$	4.5	-	5.5	V
Ground	V_{SS}	0	0	0	V
Input high voltage	V_{IH}	2.2	-	$V_{CC} + 0.5^{3)}$	V
Input low voltage	V_{IL}	-0.5 ⁴⁾	-	0.6	V

Notes :

1. $T_A = -40$ to 85°C , otherwise specified
2. Overshoot: $V_{CC} + 1.0$ V in case of pulse width $\leq 20\text{ns}$
3. Undershoot: -1.0 V in case of pulse width $\leq 20\text{ns}$
4. Overshoot and undershoot are sampled, not 100% tested.

CAPACITANCE ($f = 1\text{MHz}$, $T_A = 25^\circ\text{C}$)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C_{IN}	$V_{IN} = 0\text{V}$	-	8	pF
Input/Output capacitance	C_{IO}	$V_{IO} = 0\text{V}$	-	10	pF

Note : Capacitance is sampled, not 100% tested.

DC ELECTRICAL CHARACTERISTICS ($T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit			
Input leakage current	I_{LI}	$V_{IN} = V_{SS}$ to V_{CC}	-1	-	1	μA			
Output leakage current	I_{LO}	$\overline{CS} = V_{IH}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$ $V_{IO} = V_{SS}$ to V_{CC}	-1	-	1	μA			
Operating power supply	I_{CC}	$I_{IO} = 0\text{mA}$, $\overline{CS} = V_{IL}$, $V_{IN} = V_{IH}$ or V_{IL}	-	-	5	mA			
Average operating current	I_{CC1}	Cycle time = $1\mu\text{s}$, 100% duty, $I_{IO} = 0\text{mA}$, $\overline{CS} \leq 0.2\text{V}$, $V_{IN} \leq 0.2\text{V}$ or $V_{IN} \geq V_{CC} - 0.2\text{V}$	-	-	7	mA			
			I_{CC2}	Cycle time = Min, $I_{IO} = 0\text{mA}$, 100% duty, $\overline{CS} = V_{IL}$, $V_{IN} = V_{IL}$ or V_{IH}	45ns	-	-	65	mA
					55ns	-	-	55	
70ns	-	-	45						
Output low voltage	V_{OL}	$I_{OL} = 2.1\text{mA}$	-	-	0.4	V			
Output high voltage	V_{OH}	$I_{OH} = -1.0\text{mA}$	2.4	-	-	V			
Standby Current (TTL)	I_{SB}	$\overline{CS} = V_{IH}$, Other inputs = V_{IH} or V_{IL}	-	-	1	mA			
Standby Current (CMOS)	I_{SB1}	$\overline{CS} \geq V_{CC} - 0.2\text{V}$ Other inputs = $0 \sim V_{CC}$ (Typ. condition : $V_{CC} = 5\text{V}$ @ 25°C) (Max. condition : $V_{CC} = 5.5\text{V}$ @ 85°C)	LF	-	1.5 ¹⁾	20	μA		

NOTES :

1. Typical values are measured at $V_{CC} = 5\text{V}$, $T_A = 25^\circ\text{C}$ and not 100% tested.

AC OPERATING CONDITIONS

Test Conditions (Test Load and Test Input/Output Reference)

Input Pulse Level : 0V to V_{CC}

Input Rise and Fall Time : 1V/ns

Input and Output reference Voltage : $0.5V_{CC}$

Output Load (See right) : $CL^{(1)} = 100\text{pF} + 1 \text{ TTL (70ns)}$

$CL^{(1)} = 30\text{pF} + 1 \text{ TTL (45ns/55ns)}$

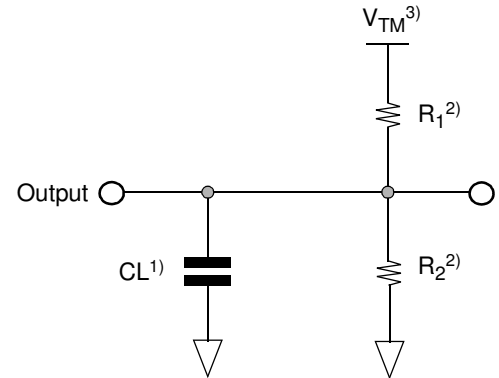
Notes :

1. Including scope and Jig capacitance

2. $R_1 = 1800 \text{ ohm}$, $R_2 = 990 \text{ ohm}$

3. $V_{TM} = V_{CC}$

4. $CL = 5\text{pF} + 1 \text{ TTL (measurement with tLZ, tOLZ, tHZ, tOHZ, tWHZ)}$



READ CYCLE ($V_{CC} = 4.5\text{V to } 5.5\text{V}$, $GND = 0\text{V}$, $T_A = -40^\circ\text{C to } +85^\circ\text{C}$)

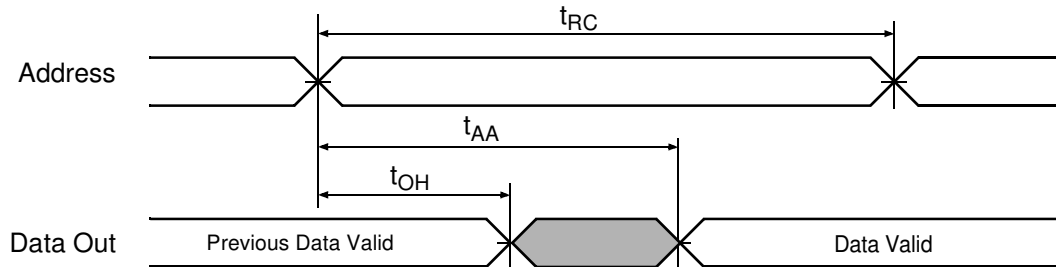
Parameter	Symbol	45ns		55ns		70ns		Unit
		Min	Max	Min	Max	Min	Max	
Read cycle time	t_{RC}	45	-	55	-	70	-	ns
Address access time	t_{AA}	-	45	-	55	-	70	ns
Chip select to output	t_{CO}	-	45	-	55	-	70	ns
Output enable to valid output	t_{OE}	-	25	-	30	-	35	ns
Chip select to low-Z output	t_{LZ}	10	-	10	-	10	-	ns
Output enable to low-Z output	t_{OLZ}	5	-	5	-	5	-	ns
Chip disable to high-Z output	t_{HZ}	0	20	0	20	0	25	ns
Output disable to high-Z output	t_{OHZ}	0	15	0	20	0	25	ns
Output hold from address change	t_{OH}	10	-	10	-	10	-	ns

WRITE CYCLE ($V_{CC} = 4.5\text{V to } 5.5\text{V}$, $GND = 0\text{V}$, $T_A = -40^\circ\text{C to } +85^\circ\text{C}$)

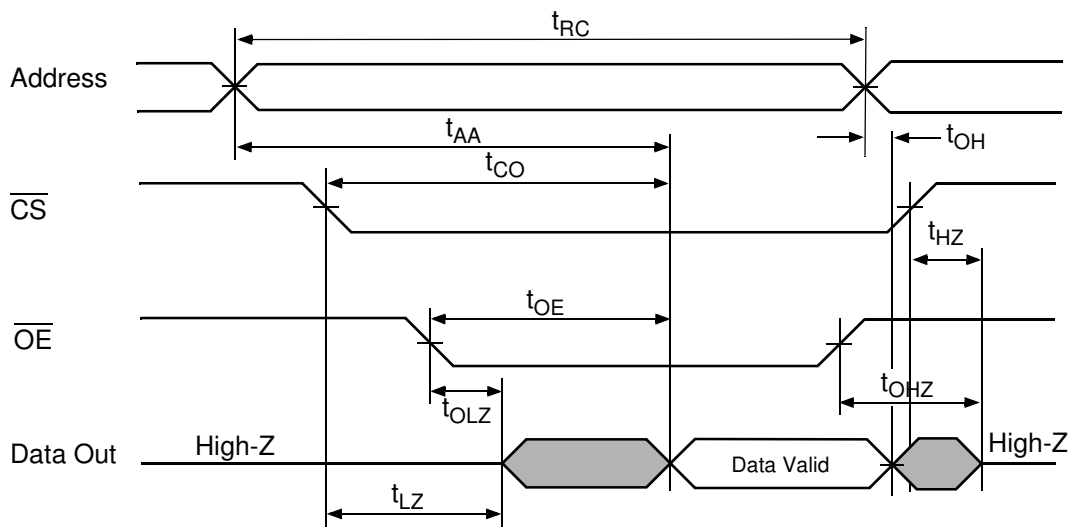
Parameter	Symbol	45ns		55ns		70ns		Unit
		Min	Max	Min	Max	Min	Max	
Write cycle time	t_{WC}	45	-	55	-	70	-	ns
Chip select to end of write	t_{CW}	45	-	45	-	60	-	ns
Address setup time	t_{AS}	0	-	0	-	0	-	ns
Address valid to end of write	t_{AW}	45	-	45	-	60	-	ns
Write pulse width	t_{WP}	35	-	40	-	50	-	ns
Write recovery time	t_{WR}	0	-	0	-	0	-	ns
Write to output high-Z	t_{WHZ}	0	15	0	20	0	20	ns
Data to write time overlap	t_{DW}	25		25		30		ns
Data hold from write time	t_{DH}	0	-	0	-	0	-	ns
End of write to output low-Z	t_{OW}	5	-	5	-	5	-	ns

TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Transition Controlled)



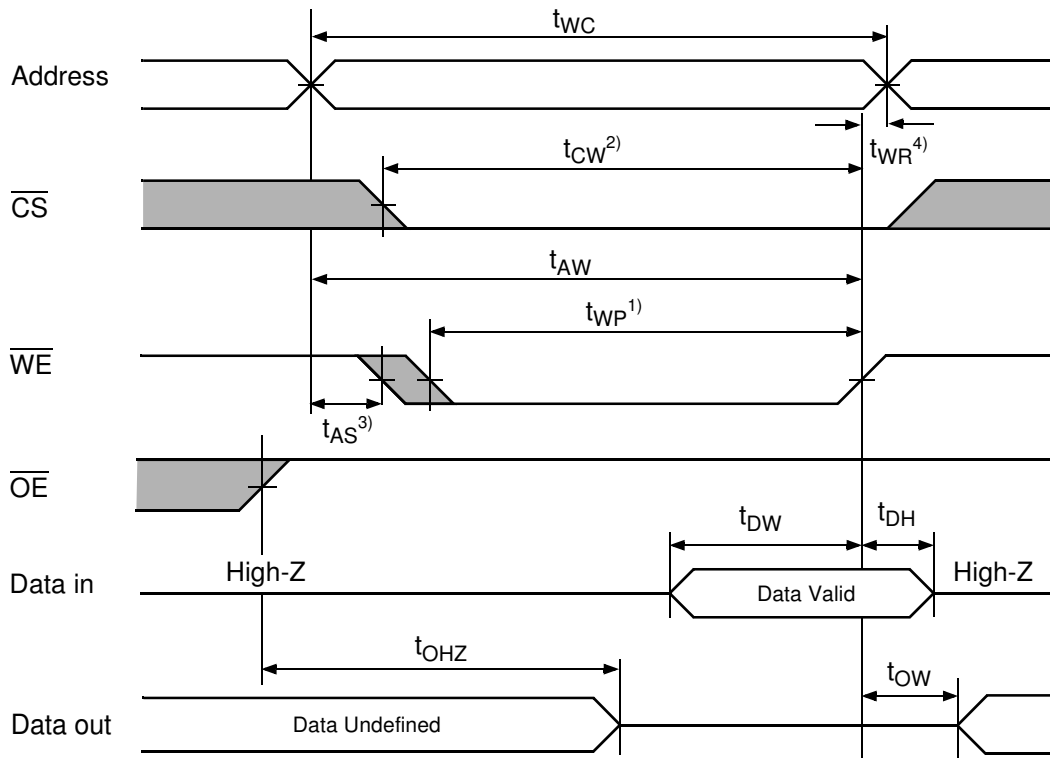
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{\text{OE}}$ Controlled)



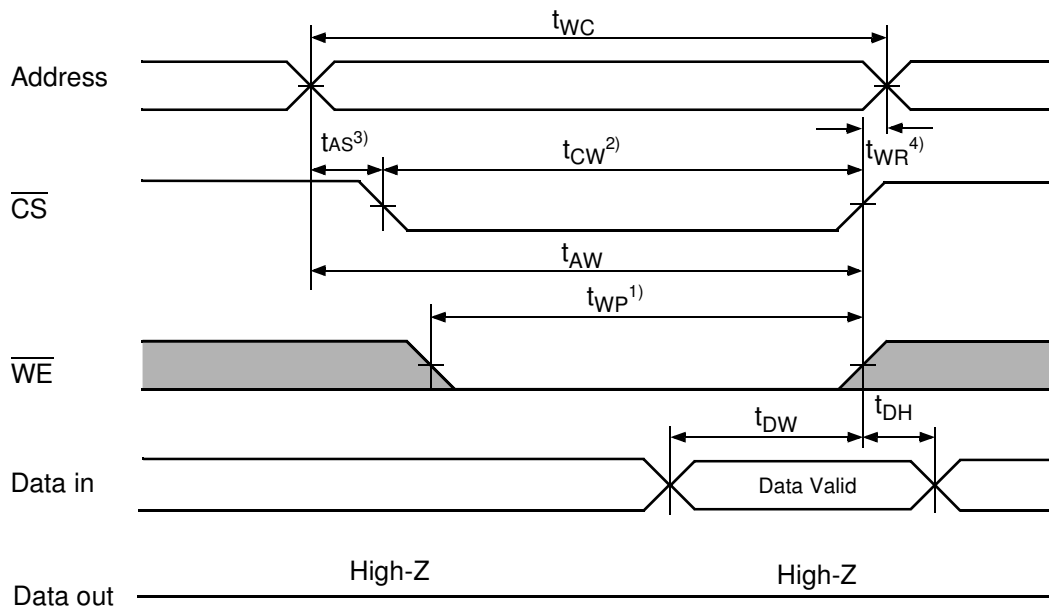
NOTES (READ CYCLE)

1. t_{HZ} and t_{OHZ} are defined as the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, $t_{\text{HZ}}(\text{Max.})$ is less than $t_{\text{LZ}}(\text{Min.})$ both for a given device and from device to device interconnection.

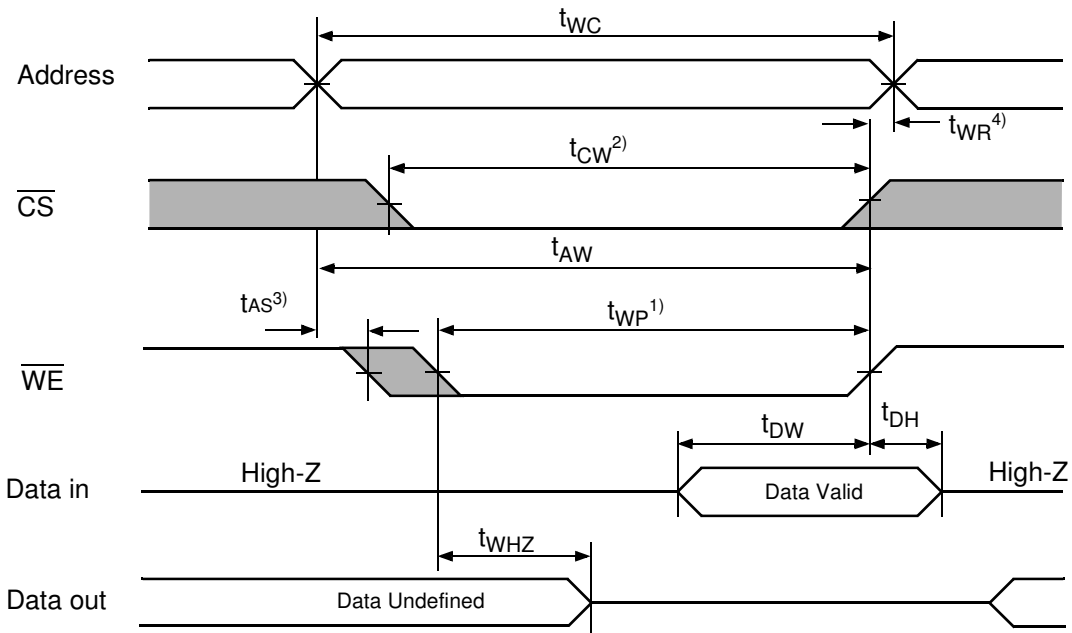
TIMING WAVEFORM OF WRITE CYCLE(1) (\overline{WE} Controlled, \overline{OE} High During WRITE)



TIMING WAVEFORM OF WRITE CYCLE(2) (\overline{CS} Controlled)



TIMING WAVEFORM OF WRITE CYCLE(3) (\overline{WE} Controlled, \overline{OE} LOW)



NOTES (WRITE CYCLE)

1. A write occurs during the overlap (t_{WP}) of low \overline{CS} and low \overline{WE} . A write begins at the latest transition among \overline{CS} goes low and \overline{WE} goes low. A write ends at the earliest transition when \overline{CS} goes high and \overline{WE} goes high. The t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the \overline{CS} going low to end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as \overline{CS} or \overline{WE} going high.

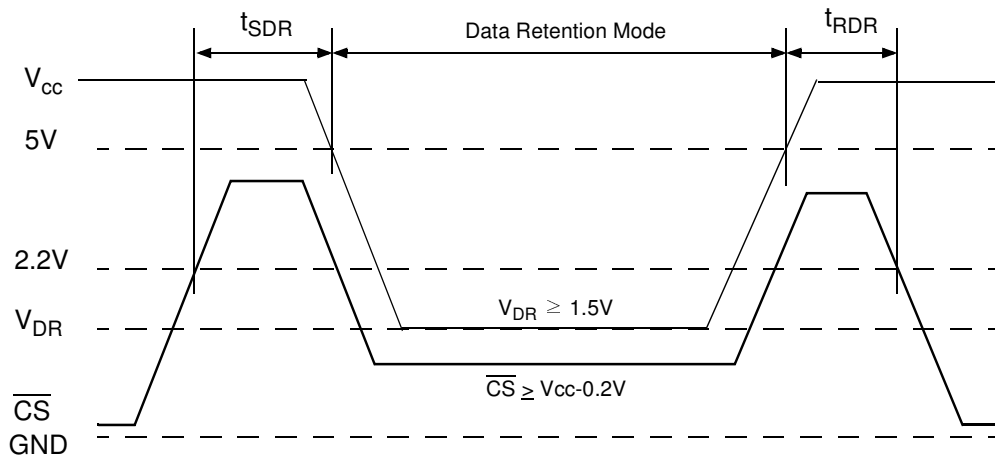
DATA RETENTION CHARACTERISTICS

Parameter	Symbol	Test Condition	Min	Typ ²⁾	Max	Unit
V _{CC} for Data Retention	V _{DR}	I _{SB1} Test Condition (Chip Disabled) ¹⁾	1.5	-	-	V
Data Retention Current	I _{DR}	I _{SB1} Test Condition (Chip Disabled) ¹⁾	-	1	7	μA
Chip Deselect to Data Retention Time	t _{SDR}	See data retention wave form	0	-	-	ns
Operation Recovery Time	t _{RDR}		t _{RC}	-	-	

NOTES :

1. See the ISB1 measurement condition of data sheet page 4.
2. Typical value is measured at TA=25°C and not 100% tested.

DATA RETENTION WAVE FORM

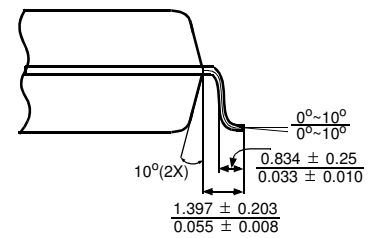
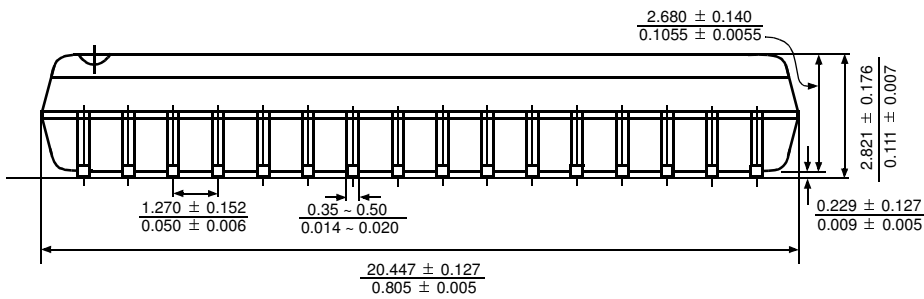
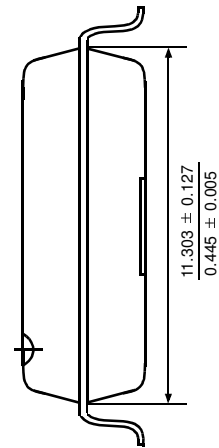
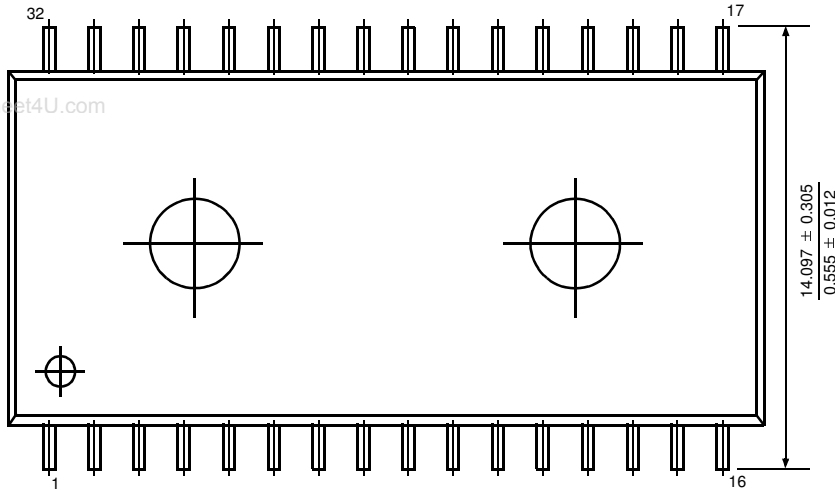


PACKAGE DIMENSIONS

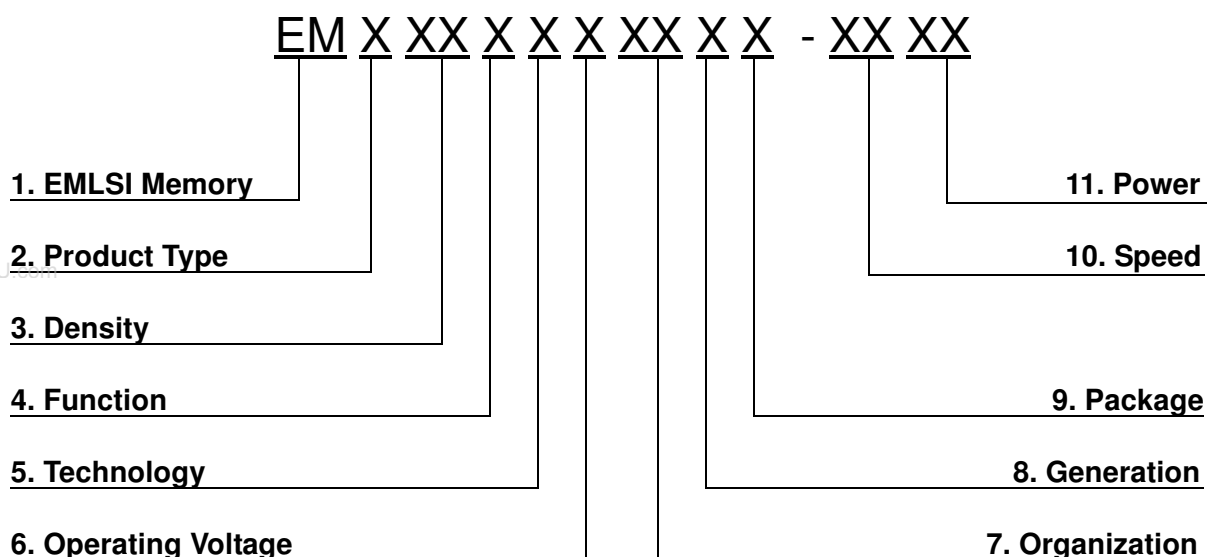
32Pin - SOP

Unit : millimeters/Inches

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SRAM PART CODING SYSTEM



1. Memory Component
EM ----- Memory

2. Product Type
6 ----- SRAM

3. Density
1 ----- 1M
2 ----- 2M
4 ----- 4M
8 ----- 8M

4. Function
0 ----- Dual CS
1 ----- Single CS
2 ----- Multiplexed
3 ----- Single CS / LBB, UBB(tBA=tOE)
4 ----- Single CS / LBB, UBB(tBA=tCO)
5 ----- Dual CS / LBB, UBB(tBA=tOE)
6 ----- Dual CS / LBB, UBB(tBA=tCO)

5. Technology
F ----- Full CMOS

6. Operating Voltage
T ----- 5.0V
V ----- 3.3V
U ----- 3.0V
S ----- 2.5V
R ----- 2.0V
P ----- 1.8V

7. Organization
8 ----- x8 bit
16 ----- x16 bit

8. Generation
Blank ----- 1st generation
A ----- 2nd generation
B ----- 3rd generation
C ----- 4th generation
D ----- 5th generation
E ----- 6th generation
F ----- 7th generation
G ----- 8th generation

9. Package
Blank ----- KGD, 48&36FpBGA
S ----- 32 sTSOP1
T ----- 32 TSOP1
U ----- 44 TSOP2
V ----- 32 SOP

10. Speed
45 ----- 45ns
55 ----- 55ns
70 ----- 70ns
85 ----- 85ns
10 ----- 100ns
12 ----- 120ns

11. Power
LL ----- Low Low Power
LF ----- Low Low Power(Pb-Free & Green)
L ----- Low Power
S ----- Standard Power