Etron 鈺創科技
Etron Technology, Inc.

Embedded Multi-Media Card (e.MMC)

Flash Storage Specification e.MMC 5.1 HS400

EM74I08HVAGB-H

Advance
Revision 1.01
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1 Introduction

The e.MMC products follow the JEDEC e.MMC 5.1 standards. It is an ideal universal storage solution for many electronic devices, including smart phones, tablets, PDAs, eBook readers, digital cameras, recorders, MP3, MP4 players, electronic learning products, digital TVs and set-top boxes. e.MMC encloses the MLC NAND and e.MMC controller inside as one JEDEC standard package, providing a standard interface to the host. The e.MMC controller directly manages NAND flash, including ECC, wear-leveling, IOPS optimization and read sensing.

1.1 Product Features

- **Packaged NAND flash memory with e.MMC 5.1 interface**
- **Backward compatible with all prior e.MMC specification revisions**
- **Operating Voltage Support:**
  - V_{CC}: (3.3V) 2.7V ~ 3.6V
  - V_{CCQ}: (1.8V) 1.7V ~ 1.95V / (3.3V) 2.7V ~ 3.6V
- **Temperature:**
  - Operating Temperature: TA = -25°C to +85°C
  - Storage without operation: -40°C to +85°C
- **Compliant with e.MMC 5.1 JEDEC Standard Number JESD84-B51**
- **Embedded Multi-Media storage in a single Multi-Chip package**
- **Package: 153-ball 11.5 x 13.0 x 0.95mm FBGA package**

Table 1-1. Product Information

Part Number	NAND Density	V_{CC}	V_{CCQ}	Package
EM74I08HVAGB-H	8 GB	3.3V	1.8V/3.3V	FBGA

1.2 e.MMC Specific Feature

- **JEDEC/e.MMC Standard version 5.1 Compatible (backward compatible to e.MMC 4.5)**
  - Supports a wide range of power supply voltage: 1.8 and 3.3V
  - Supports HS400 Mode
  - e.MMC production state awareness
  - e.MMC device health report
  - Supports Command Queue
  - Programmable bus width: 1/4/8 bits
  - Supports Boot operation in High Speed and DDR mode
  - Supports Boot mode and Alternative Boot mode
  - Replay Protection Memory Block (RPMB)
  - Enhanced Partition Attributes
  - High Priority Interrupt (HPI)
  - Background operations
  - Enhanced Reliable Write
  - Secure removal types
  - Enhance techniques: Sleep Notification in power off notification, data tagging, packed commands, discard, sanitize, RTC (real time clock)
- **LDPC ECC Engine**
  - Support multiple parity size with 1KB based codeword
  - Support low-power decoding mode and high-correction capability decoding with soft information
- **e.MMC Clock**
  - e.MMC I/F Clock Frequency : 0 ~ 200MHz
  - e.MMC I/F Boot Frequency : 0 ~ 52MHz
- **RoHS compliant**

2 Ball Assignment

2.1 Package Configuration

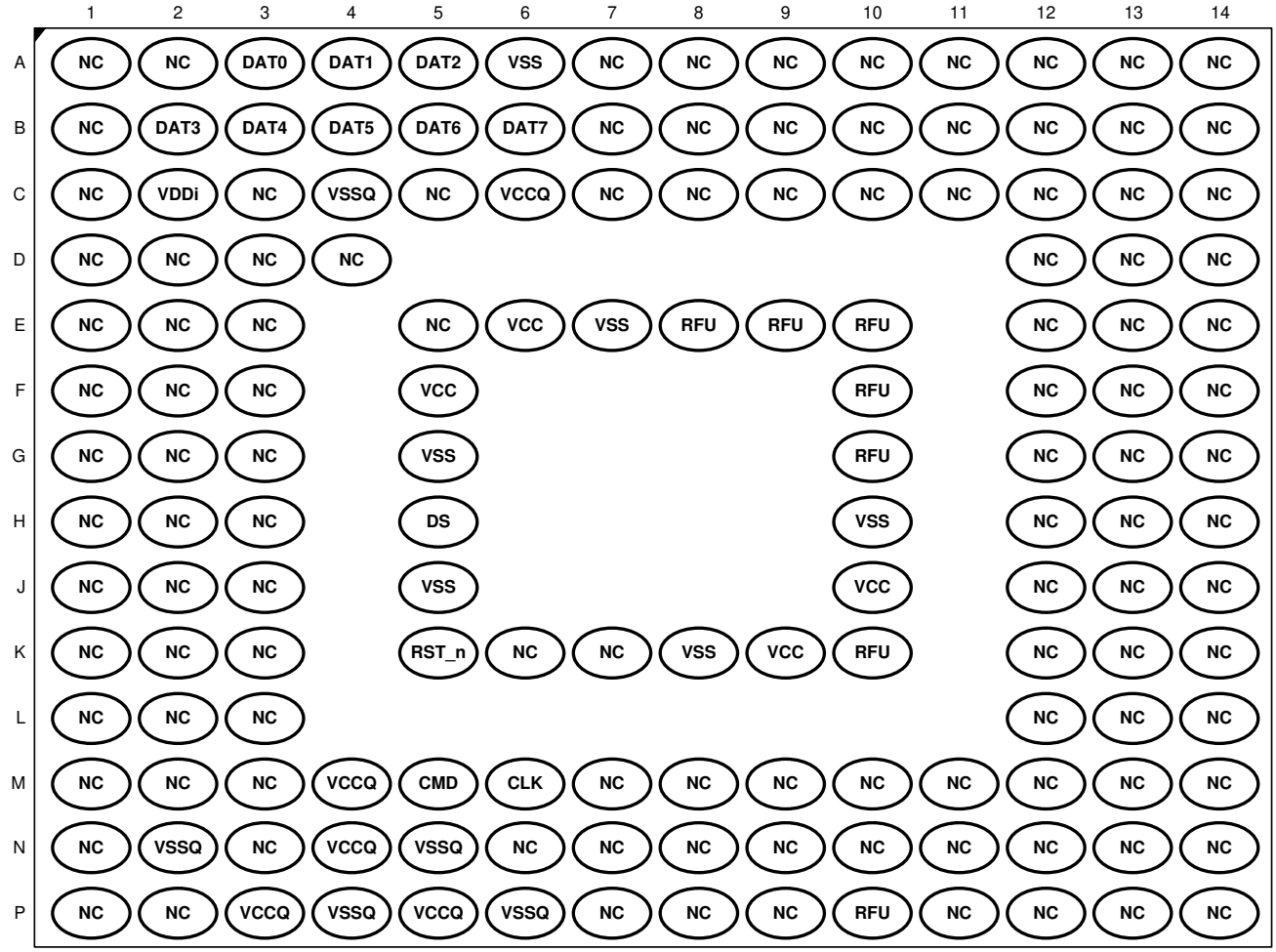


Figure 2-1. 153-FBGA Ball Assignment (Top View)

2.2 Pins and Signal Description

The e.MMC device transfers data via a configurable number of data bus signals. The communication signals are:

Table 2-1. Communication Interface

Name	Type	Description
CLK	I	**Clock:** Each cycle of this signal directs a one bit transfer on the command and either a one bit (1x) or a two bits transfer (2x) on all the data lines. The frequency may vary between zero and the maximum clock frequency.
DAT[7:0]	I/O/PP	**Data:** These are bidirectional data channels. The DAT signals operate in push-pull mode. Only the Device or the host is driving these signals at a time. By default, after power up or reset, only DAT0 is used for data transfer. A wider data bus can be configured for data transfer, using either DAT0-DAT3 or DAT0- DAT7, by the e.MMC host controller. The e.MMC device includes internal pull-ups for data lines DAT1-DAT7. Immediately after entering the 4-bit mode, the device disconnects the internal pull ups of lines DAT1, DAT2, and DAT3. Correspondingly, immediately after entering to the 8-bit mode, the device disconnects the internal pull-ups of lines DAT1-DAT7.
CMD	I/O/PP/OD	**Command:** This signal is a bidirectional command channel used for device initialization and transfer of commands. The CMD signal has two operation modes: open-drain for initialization mode, and push-pull for fast command transfer. Commands are sent from the e.MMC host controller to the e.MMC device and responses are sent from the device to the host.
RST_n	I	**Hardware Reset:** By default, hardware reset is disabled and must be enabled in the EXT_CSD register if used. Otherwise, it can be left un-connected.
VCC	S	Supply voltage for core
VCCQ	S	Supply voltage for I/O
VSS	S	Supply ground for core
VSSQ	S	Supply ground for I/O
DS	O/PP	**Data Strobe:** This signal is generated by the device and used for output in HS400 mode. The frequency of this signal follows the frequency of CLK. For data output each cycle of this signal directs two bits transfer(2x) on the data - one bit for positive edge and the other bit for negative edge. For CRC status response output and CMD response output (enabled only HS400 enhanced strobe mode), the CRC status is latched on the positive edge only, and don't care on the negative edge.
RFU	-	Reserved for future use: These pins are not internally connected. Leave floating
NC	-	Not Connected: These pins are not internally connected. Signals can be routed through these balls to ease printed circuit board design.
VDDi	-	Internal Voltage Node: Note that this is not a power supply input. This pin provides access to the output of an internal voltage regulator to allow for the connection of an external Creg capacitor.
Note: I=Input; O=Output; P=Push-Pull; OD=Open Drain; NC= No Connection and left floating; S=Power Supply		

2.3 Product Block Diagram

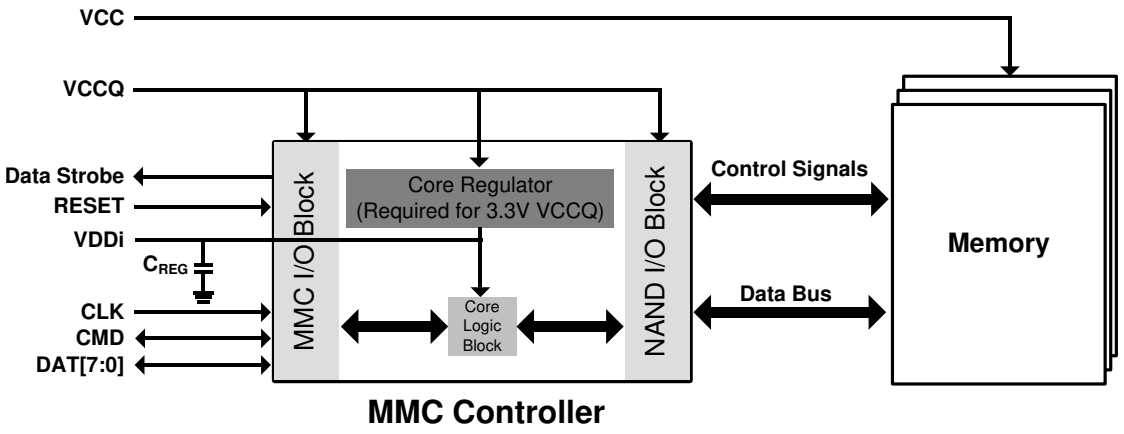


Figure 2-2. e.MMC Block Diagram

3 S/W Algorithm

3.1 Partition Management

e.MMC offers the possibility for the host to configure additional split local memory partitions with independent addressable space starting from logical address 0x00000000 for different usage models. Therefore memory block area can be classified as follows Factory configuration supplies two boot partitions implemented as enhanced storage media and one RPMB partitioning of 4MB in size.

Up to four General Purpose Area Partitions can be configured to store user data or sensitive data, or for other host usage models. The size of these partitions is a multiple of the write protect group.

3.2 Enhanced Partition (Area)

This e.MMC adopts Enhanced User Data Area as SLC Mode. Therefore when master adopts some portion as enhanced user data area in User Data Area, that area occupies triple size of original set up size. (For example, if master set 1MB for enhanced mode, total 3MB user data area is needed to generate 1MB enhanced area.)

Max Enhanced User Data Area size is defined as (MAX_ENH_SIZE_MULT x HC_WP_ GRP_SIZE x HC_ERASE_GRP_SIZE x 512kBytes)

3.3 User Density

Total User Density depends on device type. Different e.MMC part ID has different user density. The following diagram illustrates the memory space allocation within an e.MMC device.

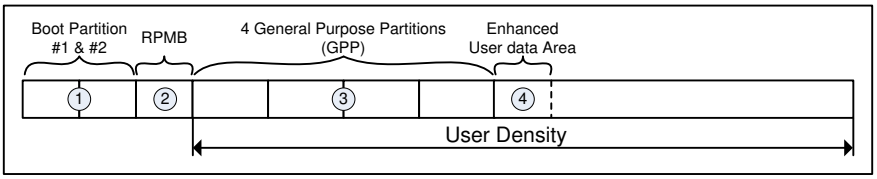


Figure 3-1. Space Allocation in e.MMC

Table 3-1. Capacity According to Partition

Capacity	Boot partition 1	Boot partition 2	RPMB
8GB	4096 KB	4096 KB	4096 KB

Table 3-2. User Density and Enhanced Partition Size

Capacity	User Density Size	Max. Enhanced Partition Size
8GB	7,650,410,496 Byte	3,825,205,248 Bytes

3.4 Typical Performance

The testing result is only for reference. Any change in testing environment may cause big difference in performance result.

Table 3-3. Typical Performance

Capacity	Read Sequential (MB/s)	Write Sequential (MB/s)
8GB	Up to 242	Up to 76

3.5 Power Consumption

3.5.1 Operating Current (RMS)

Table 3-4. Operating Current (RMS)

Capacity	Symbol	Read (mA)	Write (mA)
8GB	ICC	39	27
	ICCQ	64	40

Note 1. The measurement for current is the average RMS current consumption over a period of 100ms.
Note 2. Typical value is measured at TA = 25 °C.

3.5.2 Standby Power Consumption in auto power saving mode and standby state

Table 3-5. Standby Power Consumption

Capacity	State	ICC (uA)	ICCQ (uA)
8GB	Standby	32	79

Note 1. Power Measurement conditions: Bus configuration = x8, No CLK
Note 2. Typical value is measured at TA = 25 °C. Not 100% tested.

3.5.3 Sleep Power Consumption

Table 3-6. Sleep Power Consumption

Capacity	State	ICC (uA)	ICCQ (uA)
8GB	Sleep	0	79

Note 1. Power Measurement conditions: Bus configuration = x8, No CLK
Note 2. Enter sleep state by CMD5, VCC power is switched off. Not 100% tested.

4 e.MMC Features Overview

Table 4-1. e.MMC Features Overview

e.MMC	Device Features	Function	Support
NA	INTERFACE	Speed	HS400
NA	BUS SPEED	Max Speed	Up to 400MB/s
4.41	SECURE ERASE/TRIM	“True Wipe”	YES
4.41	BOOT AND MASS STORAGE	One storage device (reduced BOM)	YES
4.41	PARTITION & PROTECTION	Flexibility	YES
4.41	BACKGROUND OPERATIONS	Better user experience (low latency)	YES
4.41	POWER OFF NOTIFICATION	Faster Boot; Responsiveness	YES
4.41	HARDWARE RESET	Robust system design	YES
4.41	HPI	Control long Reads/Writes	YES
4.41	RPMB	Secure folders	YES
4.5	EXTENDED PARTITION ATTRIBUTE	Flexibility	YES
4.5	LARGE SECTOR SIZE	Potential performance	NO
4.5	PACKED COMMANDS	Reduce host overhead	YES
4.5	DISCARD	Improved performance on full media	YES
4.5	DATA TAG	Performance and/or Reliability	YES
4.5	CONTEXT MANAGEMENT	Performance and/or Reliability	YES
4.5	CACHE	Better sequential & random writes	YES
4.51	SANITIZE	“True Wipe”	YES
5.0	FIELD FIRMWARE UPGRADE (FFU)	Enables feature enhancement	YES
5.0	PRODUCTION STATE AWARENESS	Different operation during production	YES
5.0	DEVICE HEALTH	Vital NAND info	YES
5.1	ENHANCE STROBE	Sync Device and Host in HS400	YES
5.1	COMMAND QUEUE	Responsiveness	YES
5.1	RPMB THROUGHPUT	Faster RPMB write throughput	YES
5.1	CACHE FLUSH AND BARRIER	Order cache flushing	YES
5.1	BKOPS CONTROLLER	Host control on BLOPs	YES
5.1	SECURE WP	Secure write protect	YES
5.1	EUDA	Enhance User Data Area	YES

4.1 HS400 Interface

e.MMC supports HS400 signaling to achieve a bus speed of 400 MB/s via a 200MHz dual data rate clock frequency. HS400 mode supports 8 bits bus width and the 1.7 ~ 1.95 VCCQ option. Due to the speed, the host may need to have an adjustable sampling point to reliably receive the incoming data.

4.2 Field Firmware Upgrade (FFU)

Field Firmware Updates (FFU) enables features enhancement in the field. Using this mechanism, the host downloads a new version of the firmware to the e.MMC device and instructs the e.MMC device to install the new downloaded firmware into the device. The entire FFU process occurs in the background without affecting the user/OS data. During the FFU process, the host can replace firmware files or single/all file systems.

4.3 Cache

The e.MMC cache is dedicated volatile memory at the size of 512KB. Caching enables to improve e.MMC performance for both sequential and random access.

4.4 Discard

e.MMC supports discard command as defined in e.MMC 5.1 spec. This command allows the host to identify data which is not needed, without requiring the device to remove the data from the Media. It is highly recommended for use to guarantee optimal performance of e.MMC and reduce amount of housekeeping operation.

4.5 Power off Notification

e.MMC supports power off notifications as defined in e.MMC 5.1 spec. The usage of power off notifications allows the device to prepare itself to power off, and improve user experience during power-on. Note that the device may be set into sleep mode while power off notification is enabled.

Power off notification long allows the device to shutdown properly and save important data for fast boot time on the next power cycle.

4.6 Packed Commands

To enable optimal system performance, e.MMC supports packed commands as defined in e.MMC 5.1 spec. It allows the host to pack Read or Write commands into groups (of single type of operation) and transfer these to the device in a single transfer on the bus. Thus, it allows reducing overall bus overheads.

4.7 Sleep (CMD5)

e.MMC may be switched between a Sleep and a Standby state using the SLEEP/AWAKE (CMD5). In the Sleep state the power consumption of the memory device is minimized and the memory device reacts only to the commands RESET (CMD0) and SLEEP/AWAKE (CMD5). All the other commands are ignored by the memory device.

The VCC power supply may be switched off in Sleep state to enable even further system power consumption saving.

4.8 Enhanced Reliable Write

e.MMC supports enhanced reliable write as defined in e.MMC 5.1 spec. Enhanced reliable write is a special write mode in which the old data pointed to by a logical address must remain unchanged until the new data written to same logical address has been successfully programmed. This is to ensure that the target address updated by the reliable write transaction never contains undefined data. When writing in reliable write, data will remain valid even if a sudden power loss occurs during programming.

4.9 Sanitize

The Sanitize operation is used to remove data from the device. The use of the Sanitize operation requires the device to physically remove data from the unmapped user address space. The device will continue the sanitize operation, with busy asserted, until one of the following events occurs:

- Sanitize operation is complete
- HPI is used to abort the operation
- Power failure
- Hardware reset

After the sanitize operation is complete no data should exist in the unmapped host address space.

4.10 Secure Erase

For backward compatibility reasons, in addition to the standard erase command the e.MMC supports the optional Secure Erase command.

This command allows the host to erase the provided range of LBAs and ensure no older copies of this data exist in the flash.

4.11 Secure Trim

For backward compatibility reasons, e.MMC supports Secure Trim command. The Secure Trim command is similar to the Secure Erase command but performs a secure purge operation on write blocks instead of erase groups.

4.12 High Priority Interrupt (HPI)

The operating system usually uses demand-paging to launch a process requested by the user. If the host needs to fetch pages while in a middle of a write operation the request will be delayed until the completion of the write command.

The High Priority Interrupt (HPI), as defined in the e.MMC 5.1 specifications, allows for low-latency read operations by suspending a lower-priority task before its completion.

4.13 H/W Reset

Hardware reset may be used by host to reset the device, moving the device to a Pre-idle state and disabling the power-on period write protect on blocks that were power-on write protected before the reset was asserted.

4.14 Command Queue

e.MMC Command Queue enables device visibility of next commands and allows performance improvement. The protocol allows the host to queue up to 32 data-transfer commands in the device by implementing 5 new commands.

The benefits of command queuing are:

- Random Read performance improvement (higher IOPs)
- Reducing protocol overhead
- Command issuance allowed while data transfer is on-going
- Device order the tasks according to best access to/from flash

5 Register Settings

Within the Device interface six registers are defined: OCR, CID, CSD, EXT_CSD, RCA and DSR. These can be accessed only by corresponding commands. For more details, refer to the JEDEC Standard Specification JESD84-B51.

5.1 OCR Register

The 32-bit operation conditions register (OCR) stores the VDD voltage profile of the device and the access mode indication. In addition, this register includes a status information bit. This status bit is set if the device power up procedure has been finished. The OCR register shall be implemented by all devices.

Table 5-1. OCR Register Setting

OCR Register Definitions OCR bit	VDD voltage window	High Voltage Multi-Media Card	Dual voltage Multi-Media Card and e.MMC
[6:0]	Reserved	00 00000b	00 00000b
[7]	1.70 - 1.95V	0b	1b
[14:8]	2.0 - 2.6V	000 0000b	000 0000b
[23:15]	2.7 - 3.6V	1 1111 1111b	1 1111 1111b
[28:24]	Reserved	0 0000b	0 0000b
[30:29]	Access Mode	00b (byte mode) 10b (sector mode)	00b (byte mode) 10b (sector mode)
[31]	(Device power up status bit (busy)[1]		
Note1：This bit is set to LOW if the Device has not finished the power up routine.			

5.2 Card Identification Register (CID)

The Card Identification (CID) register is 128 bits wide. It contains the Device identification information used during the device identification phase (e.MMC protocol). For more details, refer to the JEDEC Standard Specification JESD84-B51.

Table 5-2. CID Register Setting

CID Fields Name	Field	Width	CID slice	Value
Manufacturer ID	MID	8	[127:120]	D5h
Reserved	-	6	[119:114]	0h
Device/BGA	CBX	2	[113:112]	01h
OEM/Application ID	OID	8	[111:104]	30h
Product name	PNM	48	[103:56]	(535437344948h) ST74IH
Product revision	PRV	8	[55:48]	01h
Product serial number	PSN	32	[47:16]	Random by Production
Manufacturing date	MDT	8	[15:8]	month, year
CRC7 checksum	CRC	7	[7:1]	CRC7 Generator
not used, always “1”	-	1	[0]	1h

5.3 Card Specific Data Register [CSD]

The Card-Specific Data (CSD) register provides information on how to access the contents stored in e.MMC. The CSD registers are used to define the error correction type, maximum data access time, data transfer speed, data format…etc. For more details, refer to the JEDEC Standard Specification JESD84-B51.

Table 5-3. CSD Register Setting

Name	Field	Width	CSD-slice	Value
CSD structure	CSD_STRUCTURE	2	[127:126]	3h
System specification version	SPEC_VERS	4	[125:122]	4h
Reserved	-	2	[121:120]	-
Data read access-time 1	TAAC	8	[119:112]	27h
Data read access-time 2 in CLK cycles (NSAC*100)	NSAC	8	[111:104]	01h
Max. bus clock frequency	TRAN_SPEED	8	[103:96]	32h
Device command classes	CCC	12	[95:84]	0F5h
Max. read data block length	READ_BL_LEN	4	[83:80]	9h
Partial blocks for read allowed	READ_BL_PARTIAL	1	[79:79]	0h
Write block misalignment	WRITE_BLK_MISALIGN	1	[78:78]	0h
Read block misalignment	READ_BLK_MISALIGN	1	[77:77]	0h
DSR implemented	DSR_IMP	1	[76:76]	0h
Reserved	-	2	[75:74]	-
Device size	C_SIZE	12	[73:62]	FFFh
Max. read current @ VDD min	VDD_R_CURR_MIN	3	[61:59]	7h
Max. read current @ VDD max	VDD_R_CURR_MAX	3	[58:56]	7h
Max. write current @ VDD min	VDD_W_CURR_MIN	3	[55:53]	7h
Max. write current @ VDD max	VDD_W_CURR_MAX	3	[52:50]	7h
Device size multiplier	C_SIZE_MULT	3	[49:47]	7h
Erase group size	ERASE_GRP_SIZE	5	[46:42]	1Fh
Erase group size multiplier	ERASE_GRP_MULT	5	[41:37]	1Fh
Write protect group size	WP_GRP_SIZE	5	[36:32]	Fh
Write protect group enable	WP_GRP_ENABLE	1	[31:31]	1h
Manufacturer default ECC	DEFAULT_ECC	2	[30:29]	0h
Write speed factor	R2W_FACTOR	3	[28:26]	2h
Max. write data block length	WRITE_BL_LEN	4	[25:22]	9h
Partial blocks for write allowed	WRITE_BL_PARTIAL	1	[21:21]	0h
Reserved	-	4	[20:17]	-
Content protection application	CONTENT_PROT_APP	1	[16:16]	0h
File format group	FILE_FORMAT_GRP	1	[15:15]	0h
Copy flag (OTP)	COPY	1	[14:14]	0h
Permanent write protection	PERM_WRITE_PROTECT	1	[13:13]	0h
Temporary write protection	TMP_WRITE_PROTECT	1	[12:12]	0h
File format	FILE_FORMAT	2	[11:10]	0h
ECC code	ECC	2	[9:8]	0h
CRC	CRC	7	[7:1]	CRC7 Generator
Not used, always'1'	-	1	[0:0]	-

5.4 Extended Card Specific Data Register [EXT_CSD]

The Extended CSD register defines the Device properties and selected modes. It is 512 bytes long. The most significant 320 bytes are the Properties segment, which defines the Device capabilities and cannot be modified by the host. The lower 192 bytes are the Modes segment, which defines the configuration the Device is working in. These modes can be changed by the host by means of the SWITCH command. For more details, refer to the JEDEC Standard Specification JESD84-B51.

Table 5-4. Extended CSD Register Setting

Name	Field	Size (Bytes)	CSD-slice	Value
Properties Segment				
Reserved	–	6	[511:506]	-
Extended Security Commands Error	EXT_SECURITY_ERR	1	[505]	0h
Supported Command Sets	S_CMD_SET	1	[504]	1h
HPI features	HPI_FEATURES	1	[503]	1h
Background operations support	BKOPS_SUPPORT	1	[502]	1h
Max packed read commands	MAX_PACKED_READS	1	[501]	3Fh
Max packed write commands	MAX_PACKED_WRITES	1	[500]	3Fh
Data Tag Support	DATA_TAG_SUPPORT	1	[499]	1h
Tag Unit Size	TAG_UNIT_SIZE	1	[498]	0h
Tag Resources Size	TAG_RES_SIZE	1	[497]	0h
Context management capabilities	CONTEXT_CAPABILITIES	1	[496]	78h
Large Unit size	LARGE_UNIT_SIZE_M1	1	[495]	1h
Extended partitions attribute support	EXT_SUPPORT	1	[494]	3h
Supported modes	SUPPORTED_MODES	1	[493]	1h
FFU features	FFU_FEATURES	1	[492]	0h
Operation codes timeout	OPERATION_CODE_TIME_OUT	1	[491]	17h
FFU Argument	FFU_ARG	4	[490:487]	FFFAFFF0h
Barrier support	BARRIER_SUPPORT	1	[486:486]	1h
Reserved	–	177	[485:309]	-
CMD Queuing Support	CMQ_SUPPORT	1	[308:308]	1h
CMD Queuing Depth	CMQ_DEPTH	1	[307:307]	1Fh
Reserved	Reserved	1	[306:306]	-
Number of FW sectors correctly programmed	NUMBER_OF_FW_SECTORS_ CORRECTLY_PROGRAMMED	4	[305:302]	0h
Vendor proprietary health report	VENDOR_PROPRIETARY_ HEALTH_REPORT	32	[301:270]	0h
Device life time estimation type B	DEVICE_LIFE_TIME_EST_TYP_B	1	[269]	01h
Device life time estimation type A	DEVICE_LIFE_TIME_EST_TYP_A	1	[268]	01h
Pre EOL information	PRE_EOL_INFO	1	[267]	01h
Optimal read size	OPTIMAL_READ_SIZE	1	[266]	40h
Optimal write size	OPTIMAL_WRITE_SIZE	1	[265]	40h
Optimal trim unit size	OPTIMAL_TRIM_UNIT_SIZE	1	[264]	7h
Device version	DEVICE_VERSION	2	[263:262]	3805h
Firmware version	FIRMWARE_VERSION	8	[261:254]	0000000000000010h
Power class for 200MHz, DDR at VCC=3.6V	PWR_CL_DDR_200_360	1	[253]	00h
Cache size	CACHE_SIZE	4	[252:249]	0400h
Generic CMD6 timeout	GENERIC_CMD6_TIME	1	[248]	05h

Power off notification(long) time out	POWER_OFF_LONG_TIME	1	[247]	64h
Background operations status	BKOPS_STATUS	1	[246]	Default = 0h
Number of correctly programmed sectors	CORRECTLY_PRG_SECTORS_NUM	4	[245:242]	Default = 0h
1st initialization time after partitioning	INI_TIMEOUT_AP	1	[241]	0Ah
Cache Flushing Policy	CACHE_FLUSH_POLICY	1	[240]	1h
Power class for 52MHz, DDR at 3.6V	PWR_CL_DDR_52_360	1	[239]	0h
Power class for 52MHz, DDR at 1.95V	PWR_CL_DDR_52_195	1	[238]	0h
Power class for 200MHz at 3.6V	PWR_CL_200_360	1	[237]	0h
Power class for 200MHz, at 1.95V	PWR_CL_200_195	1	[236]	0h
Minimum Write Performance for 8bit at 52MHz in DDR mode	MIN_PERF_DDR_W_8_52	1	[235]	0h
Minimum Read Performance for 8bit at 52MHz in DDR mode	MIN_PERF_DDR_R_8_52	1	[234]	0h
Reserved	–	1	[233]	-
TRIM Multiplier	TRIM_MULT	1	[232]	2h
Secure Feature support	SEC_FEATURE_SUPPORT	1	[231]	55h
Secure Erase Multiplier	SEC_ERASE_MULT	1	[230]	FFh
Secure TRIM Multiplier	SEC_TRIM_MULT	1	[229]	FFh
Boot information	BOOT_INFO	1	[228]	7h
Reserved	–	1	[227]	-
Boot partition size	BOOT_SIZE_MULTI	1	[226]	20h
Access size	ACC_SIZE	1	[225]	6h
High-capacity erase unit size	HC_ERASE_GRP_SIZE	1	[224]	1h
High-capacity erase timeout	ERASE_TIMEOUT_MULT	1	[223]	2h
Reliable write sector count	REL_WR_SEC_C	1	[222]	1h
High-capacity write protect group size	HC_WP_GRP_SIZE	1	[221]	10h
Sleep current (VCC)	S_C_VCC	1	[220]	7h
Sleep current (VCCQ)	S_C_VCCQ	1	[219]	7h
Production state awareness Timeout	PRODUCTION_STATE_AWARENESS_TIMEOUT	1	[218]	17h
Sleep/awake timeout	S_A_TIMEOUT	1	[217]	13h
Sleep Notification time out	SLEEP_NOTIFICATION_TIME	1	[216]	0Ch
Sector Count	SEC_COUNT	4	[215:212]	00E40000h
Reserved	–	1	[211]	1h
Minimum Write Performance for 8bit at 52MHz	MIN_PERF_W_8_52	1	[210]	0h
Minimum Read Performance for 8bit at 52MHz	MIN_PERF_R_8_52	1	[209]	0h
Minimum Write Performance for 8bit at 26MHz, for 4bit at 52MHz	MIN_PERF_W_8_26_4_52	1	[208]	0h
Minimum Read Performance for 8bit at 26MHz, for 4bit at 52MHz	MIN_PERF_R_8_26_4_52	1	[207]	0h
Minimum Write Performance for 4bit at 26MHz	MIN_PERF_W_4_26	1	[206]	0h
Minimum Read Performance for 4bit at 26MHz	MIN_PERF_R_4_26	1	[205]	0h
Reserved	–	1	[204]	-
Power class for 26MHz at 3.6V 1 R	PWR_CL_26_360	1	[203]	0h
Power class for 52MHz at 3.6V 1 R	PWR_CL_52_360	1	[202]	0h
Power class for 26MHz at 1.95V 1 R	PWR_CL_26_195	1	[201]	00h
Power class for 52MHz at 1.95V 1 R	PWR_CL_52_195	1	[200]	0h
Partition switching timing	PARTITION_SWITCH_TIME	1	[199]	06h
Out-of-interrupt busy timing	OUT_OF_INTERRUPT_TIME	1	[198]	05h

I/O Driver Strength	DRIVER_STRENGTH	1	[197]	1Fh
Device type	CARD_TYPE	1	[196:195]	57h
CSD structure version	CSD_STRUCTURE	1	[194]	2h
Reserved	–	1	[193]	-
Extended CSD revision	EXT_CSD_REV	1	[192]	8h
Modes Segment				
Command set	CMD_SET	1	[191]	Default = 0h Updated in runtime
Reserved	–	1	[190]	-
Command set revision	CMD_SET_REV	1	[189]	0h
Reserved	–	1	[188]	-
Power class	POWER_CLASS	1	[187]	0h
Reserved	–	1	[186]	-
High-speed interface timing	HS_TIMING	1	[185]	Default = 0h Updated in runtime by host
Strobe Support	STROBE_SUPPORT	1	[184]	0h
Bus width mode	BUS_WIDTH	1	[183]	Default = 0h Updated in runtime by host
Reserved	–	1	[182]	-
Erased memory content	ERASED_MEM_CONT	1	[181]	0h
Reserved	–	1	[180]	-
Partition configuration	PARTITION_CONFIG	1	[179]	Default = 0h Updated in runtime by host
Boot config protection	BOOT_CONFIG_PROT	1	[178]	Default = 0h Updated in runtime by host
Boot bus Conditions	BOOT_BUS_CONDITIONS	1	[177]	Default = 0h Updated in runtime by host
Reserved	–	1	[176]	-
High-density erase group definition	ERASE_GROUP_DEF	1	[175]	Default = 0h Updated in runtime by host
Boot write protection status registers	BOOT_WP_STATUS	1	[174]	Default = 0h Updated in runtime by host
Boot area write protection register	BOOT_WP	1	[173]	0h
Reserved	–	1	[172]	-
User area write protection register	USER_WP	1	[171]	0h
Reserved	–	1	[170]	-
FW configuration	FW_CONFIG	1	[169]	0h
RPMB Size	RPMB_SIZE_MULT		[168]	20h
Write reliability setting register	WR_REL_SET		[167]	1Fh
Write reliability parameter register	WR_REL_PARAM	1	[166]	15h
Start Sanitize operation	SANITIZE_START	1	[165]	Default = 0h Updated in runtime by host
Manually start background operation	BKOPS_START	1	[164]	Default = 0h Updated in runtime by host
Enable background operations handshake	BKOPS_EN	1	[163]	0h
H/W reset function	RST_n_FUNCTION	1	[162]	Default = 0h Updated by host
HPI management	HPI_MGMT	1	[161]	Default = 0h Updated by host
Partitioning Support	PARTITIONING_SUPPORT	1	[160]	7h
Max Enhanced Area Size	MAX_ENH_SIZE_MULT	3	[159:157]	0001C8h
Partitions attribute	PARTITIONS_ATTRIBUTE	1	[156]	Default = 0h Updated by host
Partitioning Setting	PARTITION_SETTING_COMPLETED	1	[155]	Default = 0h Updated by host

General Purpose Partition Size	GP_SIZE_MULT	12	[154:143]	0h
Enhanced User Data Area Size	ENH_SIZE_MULT	3	[142:140]	0h
Enhanced User Data Start Address	ENH_START_ADDR	4	[139:136]	0h
Reserved	–	1	[135]	-
Bad Block Management mode	SEC_BAD_BLK_MGMNT	1	[134]	0h
Production state awareness	PRODUCTION_STATE_AWARENESS	1	[133]	0h
Package Case Temperature is controlled	TCASE_SUPPORT	1	[132]	0h
Periodic Wake-up	PERIODIC_WAKEUP	1	[131]	0h
Program CID/CSD in DDR mode support	PROGRAM_CID_CSD_DDR_ SUPPORT	1	[130]	0h
Reserved	–	2	[129:128]	-
Vendor Specific Fields	VENDOR_SPECIFIC_FIELD	64	[127:64]	Reserved
Native sector size	NATIVE_SECTOR_SIZE	1	[63]	01h
Sector size emulation	USE_NATIVE_SECTOR	1	[62]	0h
Sector size	DATA_SECTOR_SIZE	1	[61]	0h
1st initialization after disabling sector size emulation	INI_TIMEOUT_EMU	1	[60]	Ah
Class 6 commands control	CLASS_6_CTRL	1	[59]	0h
Number of addressed group to be Released	DYNCAP_NEEDED	1	[58]	0h
Exception events control	EXCEPTION_EVENTS_CTRL	2	[57:56]	0h
Exception events status	EXCEPTION_EVENTS_STATUS	2	[55:54]	0h
Extended Partitions Attribute	EXT_PARTITIONS_ATTRIBUTE	2	[53:52]	0h
Context configuration	CONTEXT_CONF	15	[51:37]	Default = 0h
Packed command status	PACKED_COMMAND_STATUS	1	[36]	Default = 0h Updated in runtime
Packed command failure index	PACKED_FAILURE_INDEX	1	[35]	Default = 0h Updated in runtime
Power Off Notification	POWER_OFF_NOTIFICATION	1	[34]	Default = 0h Updated in runtime by host
Control to turn the Cache ON/OFF	CACHE_CTRL	1	[33]	0h
Flushing of the cache	FLUSH_CACHE	1	[32]	0h
Control to turn the Barrier ON/OF	BARRIER_CTRL	1	[31]	0h
Mode config	MODE_CONFIG	1	[30:30]	0h
Mode operation codes	MODE_OPERATION_CODES	1	[29:29]	0h
Reserved	–	2	[28:27]	-
FFU status	FFU_STATUS	1	[26:26]	0h
Per loading data size	PRE_LOADING_DATA_SIZE	4	[25:22]	0h
Max pre loading data size	MAX_PRE_LOADING_DATA_SIZE	4	[21:18]	00E40000h
Product state awareness enablement	PRODUCT_STATE_AWARENESS _ENABLEMENT	1	[17:17]	01h AUTO_PRE_SOL DERING
Secure removal type	SECURE_REMOVAL_TYPE	1	[16:16]	3Bh
Command Queue Mode enable	CMQ_MODE_EN	1	[15:15]	0h
Reserved	–	15	[14:0]	-

6 Electrical Characteristics

Within the Device interface six registers are defined: OCR, CID, CSD, EXT_CSD, RCA and DSR. These can be accessed only by corresponding commands. For more details, refer to the JEDEC Standard Specification JESD84-B51.

6.1 Supply Voltage

Permanent damage to e.MMC may occur if the supply voltages are exceeded. These are only stress ratings, and the functional operations should be restricted with the conditions detailed in the following table. Exposure to the absolute maximum rating conditions may also affect the reliability of the devices. The input and output negative voltage ratings may be exceeded if the input and output currents are not exceeded.

Table 6-1. Operating Voltage

Parameter	Symbol	Min	Max	Unit
Supply voltage	VCC	2.7	3.6	V
Supply voltage (1.8V)	VCCQ	1.7	1.95	V
Supply voltage (3.3V)	VCCQ	2.7	3.6	V
Supply voltage	VSS, VSSQ	-0.3	0.3	V

6.2 Bus Signal Levels

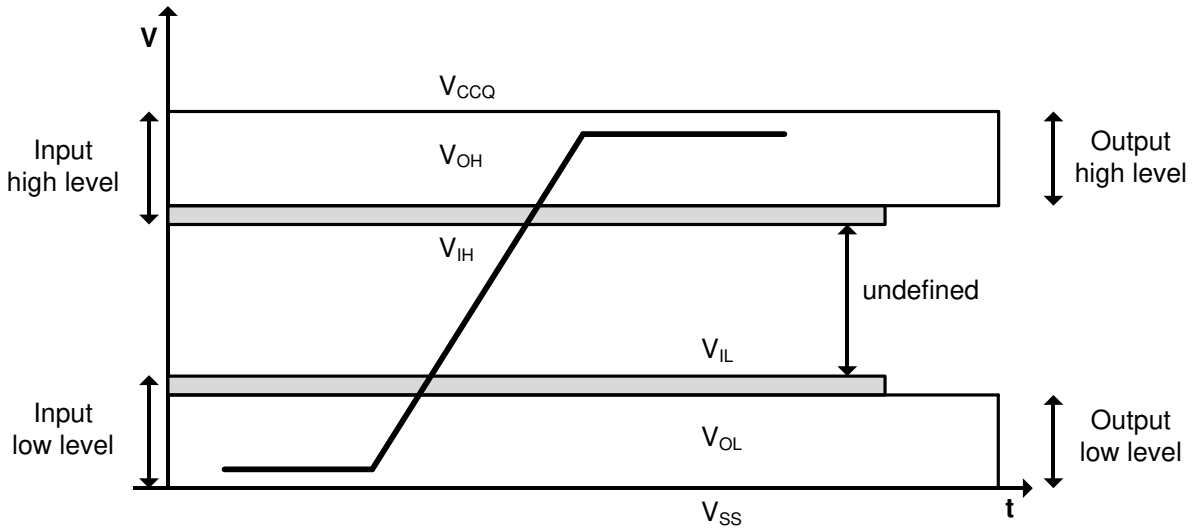


Figure 6-1. Bus Signal Levels

Table 6-2. Bus Signal Level

Parameter	Symbol	Min	Max	Unit	Conditions
Open-drain Bus Signal Level					
Output HIGH voltage	VOH	VCCQ - 0.2	-	V	
Output LOW voltage	VOL	-	0.3	V	IOL = 2 mA
Push-pull bus signal level (2.7V ~ 3.6V VCCQ)					
Output HIGH voltage	VOH	0.75 x VCCQ		V	IOH = -100 µA @ VCCQ min
Output LOW voltage	VOL		0.125 x VCCQ	V	IOL = 100 µA @ VCCQ min
Input HIGH voltage	VIH	0.625 x VCCQ	VCCQ + 0.3	V	
Input LOW voltage	VIL	VSS - 0.3	0.25 x VCCQ	V	
Push-pull bus signal level (1.7V ~ 1.95V VCCQ)					
Output HIGH voltage	VOH	VCCQ - 0.45	-	V	IOH = -2 mA
Output LOW voltage	VOL	-	0.45	V	IOL = 2 mA
Input HIGH voltage	VIH	0.65 x VCCQ	VCCQ + 0.3	V	
Input LOW voltage	VIL	VSS - 0.3	0.35 x VCCQ	V	

6.3 Bus Timing

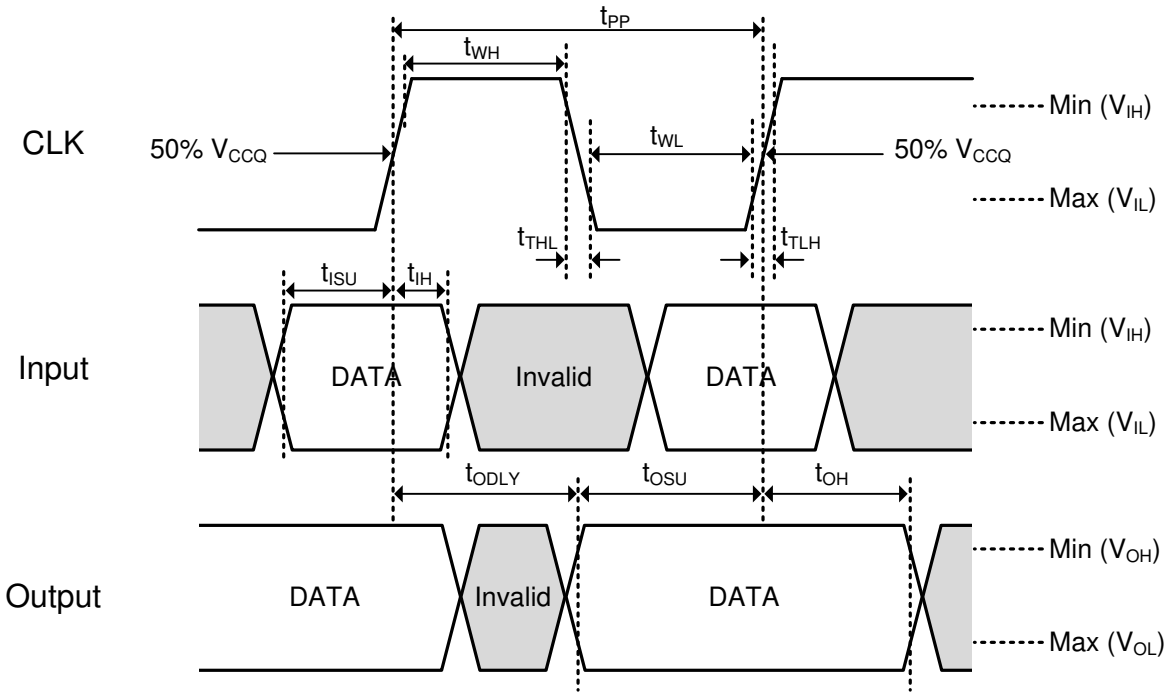


Figure 6-2. Timing Diagram

Table 6-3. High-speed Device Interface Timing

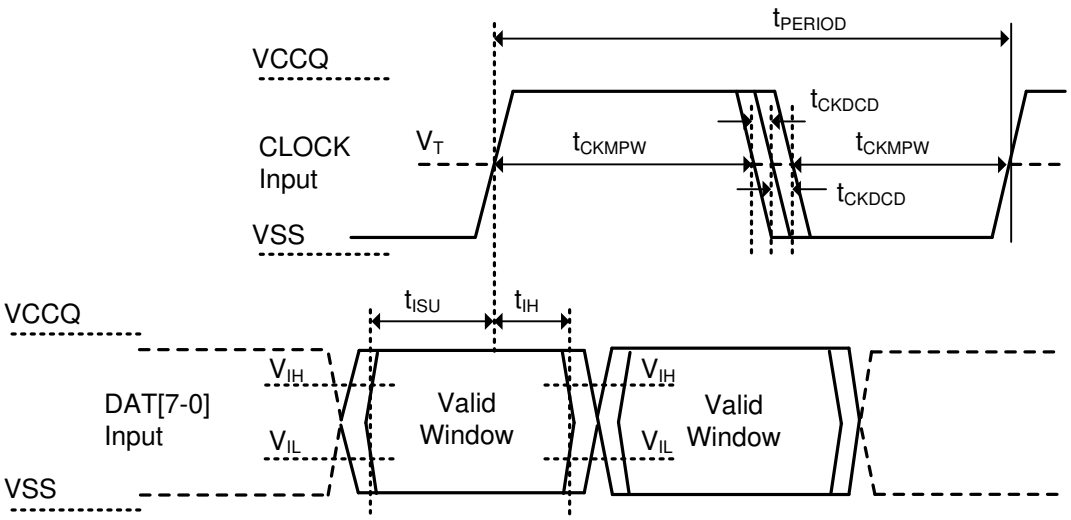
Parameter	Symbol	Min	Max	Unit	Conditions
Clock CLK					
Clock frequency Data Transfer Mode (PP)	fPP	0	52	MHz	CL ≤ 30 pF Tolerance:+100KHz
Clock frequency Identification Mode (OD)	fOD	0	400	kHz	Tolerance: +20KHz
Clock high time	tWH	6.5	-	ns	CL ≤ 30 pF
Clock low time	tWL	6.5	-	ns	CL ≤ 30 pF
Clock rise time	tTLH	-	3	ns	CL ≤ 30 pF
Clock fall time	tTHL	-	3	ns	CL ≤ 30 pF
Inputs CMD, DAT (referenced to CLK)					
Input setup time	tISU	3	-	ns	CL ≤ 30 pF
Input hold time	tIH	3	-	ns	CL ≤ 30 pF
Outputs CMD, DAT (referenced to CLK)					
Output delay time during data transfer	tODLY	-	13.7	ns	CL ≤ 30 pF
Output hold time	tOH	2.5	-	ns	CL ≤ 30 pF
Signal rise time	tRISE	-	3	ns	CL ≤ 30 pF
Signal fall time	tFALL	-	3	ns	CL ≤ 30 pF

Table 6-4. Backward-compatible Device Interface Timing

Parameter	Symbol	Min	Max	Unit	Conditions
Clock CLK					
Clock frequency Data Transfer Mode (PP)	fPP	0	26	MHz	CL ≤ 30 pF
Clock frequency Identification Mode (OD)	fOD	0	400	kHz	
Clock high time	tWH	10	-	ns	CL ≤ 30 pF
Clock low time	tWL	10	-	ns	CL ≤ 30 pF
Clock rise time	tTLH	-	10	ns	CL ≤ 30 pF
Clock fall time	tTHL	-	10	ns	CL ≤ 30 pF
Inputs CMD, DAT (referenced to CLK)					
Input setup time	tISU	3	-	ns	CL ≤ 30 pF
Input hold time	tIH	3	-	ns	CL ≤ 30 pF
Outputs CMD, DAT (referenced to CLK)					
Output setup time	tOSU	11.7	-	ns	CL ≤ 30 pF
Output hold time	tOH	8.3	-	ns	CL ≤ 30 pF

6.4 Bus Timing in HS400 mode

6.4.1 HS400 Device Input Timing



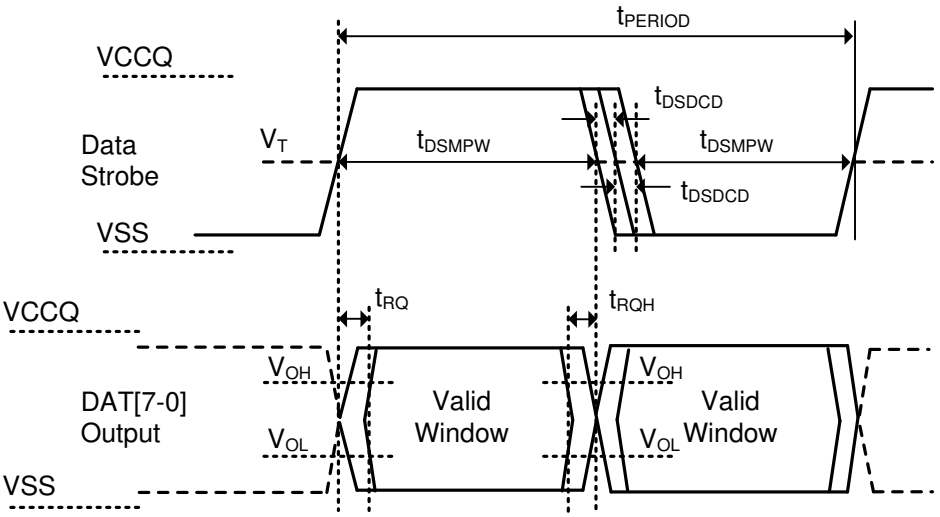
Note1: tISU and tIH are measured at VIL (max.) and VIH (min.)
Note2: VIH denotes VIH (min.) and VIL denotes VIL (max.)
Note3: VT = 50% of VCCQ, indicates clock reference point for timing measurements.

Figure 6-3. HS400 Device Data input timing

Table 6-5. HS400 Device input timing

Parameter	Symbol	Min	Max	Unit	Conditions
Input CLK					
Cycle time data transfer mode	tPERIOD	5	-	ns	200MHz (Max), between rising edges with respect to VT.
Slew rate	SR	1.125	-	V/ns	With respect to VIH/VIL.
Duty cycle distortion	tCKDCD	0.0	0.3	ns	Allowable deviation from an ideal 50% duty cycle. With respect to VT. Includes jitter, phase noise
Minimum pulse width	tCKMPW	2.2	-	ns	With respect to VT.
Input DAT (referenced to CLK)					
Input setup time	tISU	0.4	-	ns	CDevice ≤ 6pF With respect to VIH/VIL.
Input hold time	tIH	0.4	-	ns	CDevice ≤ 6pF With respect to VIH/VIL.
Slew rate	SR	1.125	-	V/ns	With respect to VIH/VIL.

6.4.2 HS400 Device Output Timing



Note1: VOH denotes VOH(min.) and VOL denotes VOL(max.)
Note2: VT = 50% of VCCQ, indicates clock reference point for timing measurements.

Figure 6-4. HS400 Device output timing

Table 6-6. HS400 Device output timing

Parameter	Symbol	Min	Max	Unit	Conditions
Data Strobe					
Cycle time data transfer mode	tPERIOD	5	-	ns	200MHz (Max), between rising edges with respect to VT.
Slew rate	SR	1.125	-	V/ns	With respect to VOH/VOL and HS400 reference load
Duty cycle distortion	tDSDCD	0.0	0.2	ns	Allowable deviation from the input CLK duty cycle distortion (tCKDCD) With respect to VT Includes jitter, phase noise
Minimum pulse width	tDSMPW	2.0	-	ns	With respect to VT.
Read pre-amble	tRPRE	0.4	-	tPERIOD	Max value is specified by manufacturer. Value up to infinite is valid
Read post-amble	tRPST	0.4	-	tPERIOD	Max value is specified by manufacturer. Value up to infinite is valid
Output DAT (referenced to Data Strobe)					
Output skew	tRQ	-	0.4	ns	With respect to VOH/VOL and HS400 reference load
Output hold skew	tRQH	-	0.4	ns	
Slew rate	SR	1.125	-	V/ns	

Table 6-7. HS400 Capacitance

Parameter	Symbol	Min	Max	Unit
Pull-up resistance for CMD	RCMD	4.7	100	kΩ
Pull-up resistance for DAT0-7	RDAT	10	100	kΩ
Pull-down resistance for Data Strobe	RDS	10	100	kΩ
Internal pull up resistance DAT1-DAT7	Rint	10	150	kΩ
Bus signal line capacitance	CL	-	13	pF
Single Device capacitance	CDevice	-	6	pF

7 Package Outline Information

Table 7-1. FBGA (11.5 x 13.0 x 0.95mm) Dimension Table

Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	0.033	0.035	0.037	0.85	0.90	0.95
A1	0.006	0.008	0.010	0.15	0.20	0.25
A2	--	--	0.028	--	--	0.70
D	0.449	0.453	0.457	11.40	11.50	11.60
E	0.508	0.512	0.516	12.90	13.00	13.10
D1	--	0.256	--	--	6.50	--
E1	--	0.256	--	--	6.50	--
D2	--	0.098	--	--	2.50	--
E2	--	0.098	--	--	2.50	--
SD	--	0.0098	--	--	0.25	--
SE	--	0.0098	--	--	0.25	--
e	--	0.020	--	--	0.50	--
b	0.010	0.012	0.014	0.25	0.30	0.35

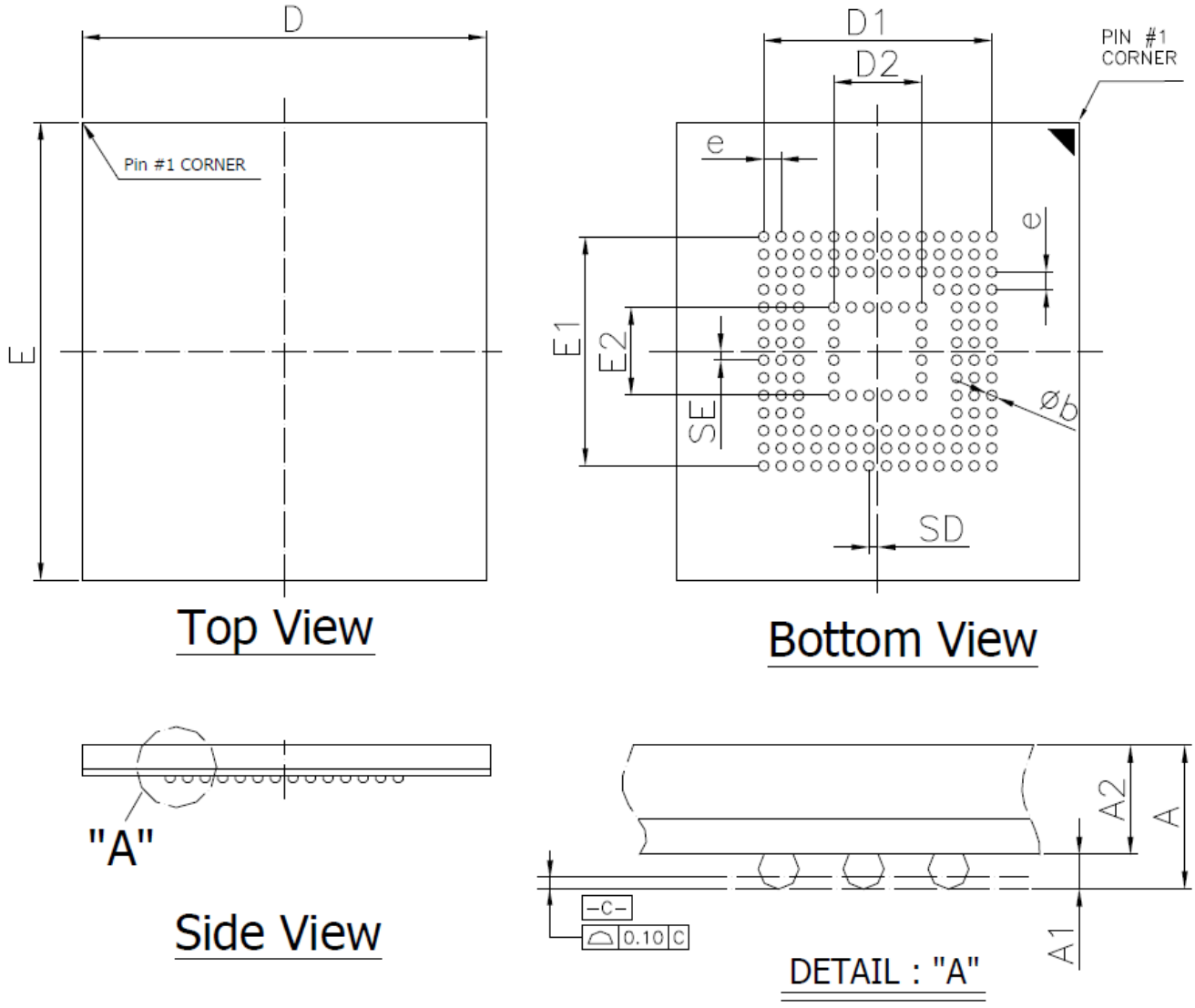


Figure 7-1. Package Outline Drawing Information