EM78452

8-Bit Microcontroller

Product Specification

DOC. VERSION 1.0

ELAN MICROELECTRONICS CORP.

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APPENDIX

Specification Revision History

Doc. Version	Revision Description	Date
1.0	Initial released version	2007/10/18

1 General Description

The EM78452 is an 8-bit microprocessor designed and developed with low-power, high-speed CMOS technology. It has 4K×13-bit on-chip ROM and 140×8-bit on-chip general purpose registers. Its operational kernel is implemented with RISC-like architecture and it is available in mask ROM version. The one time programmable (OTP) version is flexible, in both mass production and engineering test stages. OTP provides users with unlimited volume along with favorable price opportunities. This device is equipped with Serial Peripheral Interface (SPI) function, and it is suitable for wired communication. There are 58 easy-to-learn instructions and the user's program can be emulated with the EMC In-Circuit Emulator (ICE).

2 Features

- CPU configuration
  - 4K×13 bits on-chip ROM
  - 140×8 bits on chip general purpose registers
  - 11 special function registers
  - 5-level stacks for subroutine nesting
- Low power consumption:
  - Less than 3 mA at 5V/4MHz
  - Typically 10 μA during sleep mode
- I/O port configuration
  - 5 bidirectional I/O ports (35 I/O pins)
  - 12 Wake-up pins
  - 32 programmable pull-high input pins
  - 2 open-drain I/O pins
  - 2 R-option pins
- Operating voltage range: 1.8V ~ 5.5V
- Operating temperature range: 0°C ~70°C
- Operating frequency range (base on two clocks):
  - Crystal mode:
    DC ~ 20MHz @ 5V
    DC ~ 16MHz @ 2.2V
    DC ~ 4MHz @ 1.8V
- Serial Peripheral Interface (SPI)
- Four available interrupts:
  - External interrupt (/INT)
  - SPI transmission completed interrupt
  - TCC overflow interrupt
  - Timer 1 overflow interrupt
- Peripheral configuration
  - 8-bit real time clock/counter (TCC) with overflow interrupt
  - Power down mode
  - I/O ports have Programmable wake-up function from sleep mode
- 2 ~ 4 machine clocks for each instruction cycle
- 3 LED Direct sinking pins with internal serial resistors
- Built-in power-on reset
- Programmable free running on-chip watchdog timer
- Package Type:
  - 40-pin DIP 600mil : EM78452P
  - 40-pin SOP 450mil : EM78452WM
  - 44-pin QFP : EM78452AQ

3 Pin Assignment

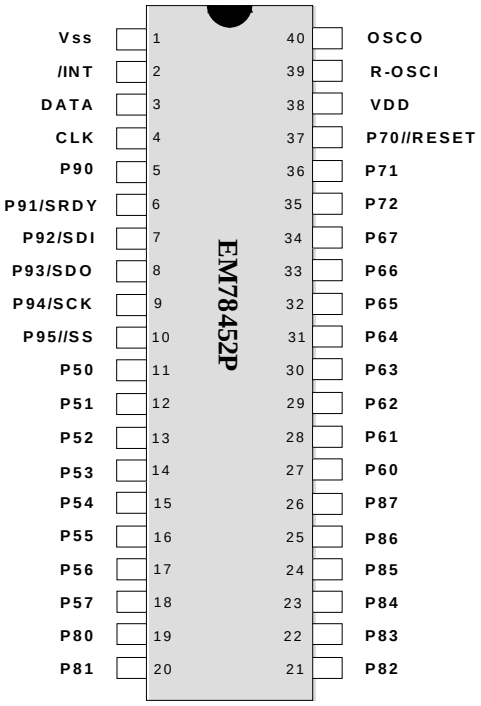


Fig. 3-1a 40-pin DIP EM78452P

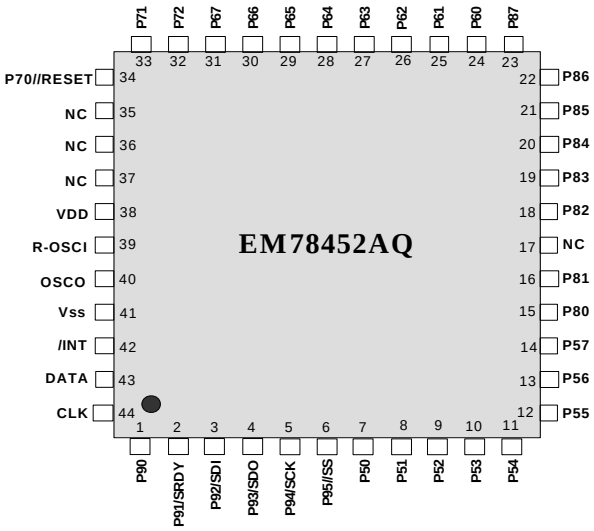


Fig. 3-1b 44-pin QFP EM78452AQ

Fig. 3-1 Pin Assignment

4 Pin Description

Symbol	Pin No.	Type	Function Description
P50~P57	11~18	I/O	8-bit bidirectional general-purpose I/O port. All of its pins can be pulled-high individually by software.
P60~P67	27~34	I/O	8-bit bidirectional general-purpose I/O port. All of its pins can be pulled-high by software, and pin-change wake-up pins.
P70~P72	37~35	I/O	LED direct-driving pins with internal serial resistor used as output and is software defined.
P80~P87	19~26	I/O	8-bit bidirectional general-purpose I/O port. All of its pins can be pulled-high by software. P80 and P81 are also used as R-option pins.
P90~P95	5~10	I/O	6-bit bidirectional general-purpose I/O port. All of its pins can be pulled-high by software. P90 and P91 are pin-change wake-up pins.
P70/ RESET	37	I/O	LED direct-driving pin with internal serial resistor used as output and is software defined. Code option Bit 3 (REN): reset enable REN=0 → for reset pin REN=1 → for general purpose I/O (P70) Internal pull high resistor 220KΩ
R-OSCI	39	I	Crystal input
OSCO	40	O	Crystal output
CLK	4	I/O	By connecting P74 and P76 together, P74 can be pulled-high by software and it is also a pin-change wake-up pin. P76 can be defined as an open-drain output.
DATA	3	I/O	By connecting P75 and P77 together, P75 can be pulled-high by software and it is also a pin-change wake-up pin. P77 can be defined as an open-drain output.
VDD	38	–	Power supply pin
VSS	1	–	Ground pin
/INT	2	I	Interrupt Schmitt trigger pin. The interrupt function is triggerred at a falling edge. Users can enable it by software.
SRDY	6	I/O	Slave Ready pin for SPI
SDI	7	I/O	Serial data in for SPI
SDO	8	I/O	Serial data out for SPI
SCK	9	I/O	Serial clock for SPI
/SS	10	I/O	/Slave select for SPI

5 Function Description

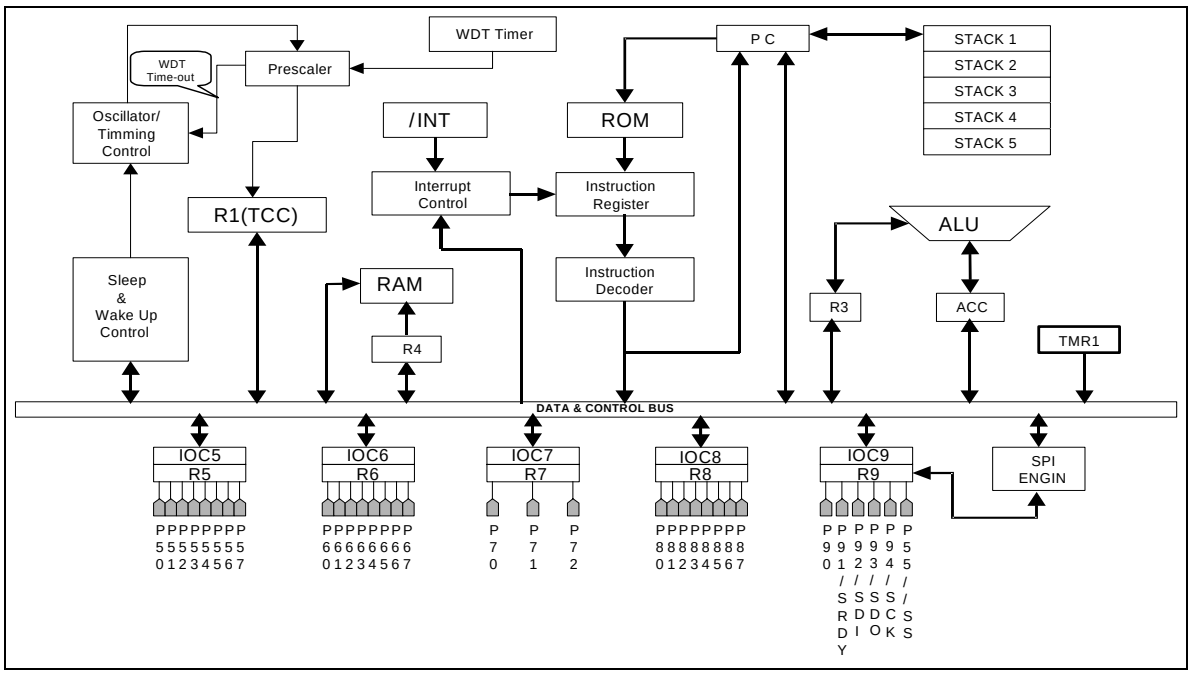


Fig. 5-1 Functional Block Diagram

5.1 Operational Registers

5.1.1 R0 (Indirect Address Register)

R0 is not a physically implemented register. It is used as an indirect addressing pointer. Any instruction using R0 as register actually accesses data pointed by the RAM Select Register (R4).

5.1.2 R1 (TCC)

- R1 is incremented by the instruction cycle clock.
- It is written and read by the program as any other register.

5.1.3 R2 (Program Counter) & Stack

- R2 and the hardware stacks are 12 bits wide.
- The structure is depicted in Fig. 5-2.
- Generates 4K × 13 on-chip ROM addresses to the relative programming instruction codes. One program page is 1024 words long.
- All the R2 bits are set to "1"s as a reset condition occurs.

- "JMP" instruction allows direct loading of the lower 10 program counter bits. Thus, "JMP" allows it to jump to any location on one page.
- "CALL" instruction loads the lower 10 bits of the PC, and then PC+1 is pushed into the stack. Thus, the subroutine entry address can be located anywhere within a page
- "RET" ("RETL k", "RETI") instruction loads the program counter with the contents at the top of the stack.
- "MOV R2, A" allows the loading of an address from the "A" register to the lower 8 bits of PC, and the ninth and tenth bits (A8~A9) of the PC are cleared.
- "ADD R2, A" allows a relative address to be added to the current PC, and the ninth and tenth bits of the PC are cleared.
- Any instruction that is written to R2 (e.g. "ADD R2, A", "MOV R2, A", "BC R2,6",·····) (except "TBL") will cause the ninth and tenth bits (A8~A9) of the PC to be cleared. Thus, the computed jump is limited to the first 256 locations of any program page.
- "TBL" allows a relative address to be added to the current PC (R2+A→R2), and contents of the ninth and tenth bits (A8~A9) of the PC are not changed. Thus, the computed jump can be on the second (or third, 4th) 256th locations on one program page.
- In the case of EM78452, the most significant bits (A10~A11) will be loaded with the contents of bits PS0~PS1 in the status register (R3) upon the execution of a "JMP", "CALL", or any other instructions which writes to R2.
- All instructions are single instruction cycle (fclk/2 or fclk/4 except for instructions that would change the contents of R2. Such instruction will need one more instruction cycle.

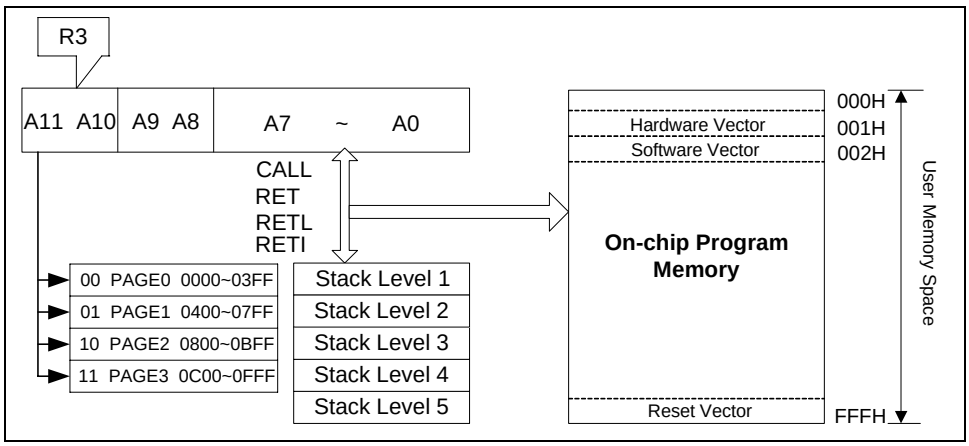


Fig. 5-2 Program Counter Organization

5.1.4 R3 (Status Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
GP	PS1	PS0	T	P	Z	DC	C

Bit 7 (GP): General read/write bit.

Bits 6 ~ 5 (PS1 ~ PS0): Page select bits. PS0~PS1 are used to pre-select a program memory page. When executing a "JMP", "CALL", or other instructions which causes the program counter to be changed (e.g. MOV R2, A), PS0~PS1 are loaded into the 11th and 12th bits of the program counter where it selects one of the available program memory pages. Note that RET (RETL, RETI) instruction does not change the PS0~PS1 bits. For this reason, the return will always be to the page from where the subroutine was called, regardless of the current settings of PS0~PS1 bits. PS1 bit is not used (read as "0") and cannot be modified in EM78452.

PS1	PS0	Program Memory Page [Address]
0	0	Page 0 [000-3FF]
0	1	Page 1 [400-7FF]
1	0	Page 2 [800-BFF]
1	1	Page 3 [C00-FFF]

Bit 4 (T): Time-out bit. Set to “1” with the "SLEP" and the "WDTC" commands, or during power up and reset to “0” with the WDT timeout.

Bit 3 (P): Power down bit. Set to “1” during power on or by a "WDTC" command and reset to “0” by a "SLEP" command.

Bit 2 (Z): Zero flag. Set to "1" if the result of an arithmetic or logic operation is zero.

Bit 1 (DC): Auxiliary carry flag

Bit 0 (C): Carry flag

5.1.5 R4 (RAM Select Register)

Bits 7~6: determines which bank is activated among the 4 banks.

Bits 5~0: are used to select the registers (Address: 00~3F) in the indirect addressing mode.

If indirect addressing is not used, the RSR is used as an 8-bit general-purpose read/writer register.

See the data memory configuration in Fig. 5-3.

5.1.6 R5~R8 (Port 5 ~ Port 8)

Four general 8 bits I/O registers

Both P74 and P76 reads or writes data from the DATA pin, while both P75 and P77 reads or writes data from the CLK pin.

5.1.7 R9 (Port9)

The general 6-bit I/O register. The values of the two most significant bits are read as "0".

Address	R PAGE registers	IOC PAGE registers
00	**R0** (Indirect Addressing Register)	Reserve
01	**R1** (Time Clock Counter)	**CONT** (Control Register)
02	**R2** (Program Counter)	Reserve
03	**R3** (Status Register)	Reserve
04	**R4** (RAM Select Register)	Reserve
05	**R5** (Port5)	**IOC5** (I/O Port Control Register)
06	**R6** (Port6)	**IOC6** (I/O Port Control Register)
07	**R7** (Port7)	**IOC7** (I/O Port Control Register)
08	**R8** (Port8)	**IOC8** (I/O Port Control Register)
09	**R9** (Port9)	**IOC9** (I/O Port Control Register)
0A	**RA** (SPI read buffer)	Reserve
0B	**RB** (SPI write buffer)	Reserve
0C	**RC** (SPI status buffer)	**IOCC** (Timer1 Control Register)
0D	**RD** (SPI control buffer)	**IOCD** (Pull_high Control Register)
0E	**RE** (Timer1 register)	**IOCE** (WDT Control Register)
0F	Reserve	**IOCF** (Interrupt Mask Register)
10 : 1F	General Registers	
20 : 3E	Bank0 / Bank1 / Bank2 / Bank3	
3F	**R3F** (Interrupt Status Register)	

Fig. 5-3 Data Memory Configuration

5.1.8 RA (SPIRB: SPI Read Buffer)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1
0X0A	SPIRB/RA	SRB7	SRB6	SRB5	SRB4	SRB3	SRB2	SRB1

SRB7~SRB0 are the 8-bit data when transmission is completed by SPI.

5.1.9 RB (SPIWB: SPI Write Buffer)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0B	SPIWB/RB	SWB7	SWB6	SWB5	SWB4	SWB3	SWB2	SWB1	SWB0

SWB7~SWB0 are the 8-bit data that are waiting for transmission by SPI.

5.1.10 RC (SPIS: SPI Status Register)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0C	SPIS/RC	DORD	TD1	TD0	TM1IF	OD3	OD4		RBF

Bit 7 (DORD): Data transmission order.

0 : Shift left (MSB first)

1 : Shift right (LSB first)

Bit 6~Bit 5: SDO Status output Delay times Options

TD1	TD0	Delay Time
0	0	8 CLK
0	1	16 CLK
1	0	24 CLK
1	1	32 CLK

Bit 4 (T1ROS): Timer 1 Read Out Buffer Select Bit

0 : Read Value from Timer 1 Preset Register

1 : Read Value from Timer 1 Counter Register

Bit 3 (OD3): Open-Drain Control bit

0 : Open-drain disable for SDO

1 : Open-drain enable for SDO

Bit 2 (OD4): Open-Drain Control bit

0 : Open-drain disable for SCK

1 : Open-drain enable for SCK

Bit 1: not used, read as “0”

Bit 0 (RBF): Read Buffer Full flag

0 : Receiving not completed, and SPIRB has not fully exchanged.

1 : Receiving completed; SPIRB is fully exchanged.

5.1.11 RD (SPIC: SPI Control Register)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0D	SPIC/RD	CES	SPIE	SRO	SSE	SDOC	SBRS2	SBRS1	SBRS0

Bit 7 (CES): Clock Edge Select bit

0 : Data shifts out on a rising edge, and shifts in on a falling edge. Data is on hold during low-level.

1 : Data shifts out on a falling edge, and shifts in on a rising edge. Data is on hold during high-level.

Bit 6 (SPIE): SPI Enable bit

0 : Disable SPI mode

1 : Enable SPI mode

Bit 5 (SRO): SPI Read Overflow bit

0 = No overflow

1 = A new data is received while the previous data is still being held in the SPIB register. In this situation, the data in the SPIS register will be destroyed. To avoid setting this bit, users are required to read the SPIRB register although only the transmission is implemented.

Note that this can only occur in slave mode.

Bit 4 (SSE): SPI Shift Enable bit

0 = Reset as soon as shifting is completed, and the next byte is ready to be shifted.

1 = Start to shift, and keep at "1" while the current byte is still being transmitted.

It should be noted that this bit will be reset to 0 at every 1-byte transmission by the hardware.

Bit 3 (SDOC): SDO output status control bit:

0 : After the Serial data output, the SDO remains high.

1 : After the Serial data output, the SDO remains low.

Bit 2~Bit 0 (SBRS): SPI Baud Rate Select bits

Refer to the SPI baud rate table illustration under the section "SPI" on the subsequent pages.

5.1.12 RE (TMR1: Timer 1 Register)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0X0E	TMR1/RE	TMR17	TMR16	TMR15	TMR14	TMR13	TMR12	TMR11	TMR10

TMR17~TMR10 are the set of bits of Timer 1 register and such are incremented until the value matches PWP and then it resets to 0.

5.1.13 RF (PWP: Pulse Width Preset Register)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0F	PWP/RF	PWP7	PWP6	PWP5	PWP4	PWP3	PWP2	PWP1	PWP0

PWP7~PWP0 are the set of bits with pulse width preset in advance for the desired width of the baud clock.

5.1.14 R20~R3E (General-purpose Register)

RA~R1F, and R20~R3E (including Banks 0~3) are general-purpose registers.

5.1.15 R3F (Interrupt Status Register)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x3F	ISR/R3F	-	-	-	-	TM1IF	SPIIF	EXIF	TCIF

Bits 7~4: not used, read as “0”.

Bit 3 (TM1IF): Timer 1 interrupt flag. Set by the comparator at Timer 1 application, flag is cleared by software.

Bit 2 (SPIIF): SPI interrupt flag. Set during data transmission completed, flag is cleared by software.

Bit 1 (EXIF): External interrupt flag. Set by a falling edge on the /INT pin, flag is cleared by software

Bit 0 (TCIF): TCC overflow interrupt flag. Set as TCC overflows; flag is cleared by software.

0 : means no interrupt occurs

1 : means with interrupt request

R3F can be cleared by instruction, but cannot be set by instruction.

IOCF is the interrupt mask register.

Note that when reading R3F it will result to "logic AND" of R3F and IOCF.

PSR2	PSR1	PSR0	TCC Rate	WDT Rate
0	0	0	1:2	1:1
0	0	1	1:4	1:2
0	1	0	1:8	1:4
0	1	1	1:16	1:8
1	0	0	1:32	1:16
1	0	1	1:64	1:32
1	1	0	1:128	1:64
1	1	1	1:256	1:128

5.2 Special Purpose Registers

5.2.1 A (Accumulator)

Internal data transfer operation, or instruction operand holding usually involves the temporary storage function of the Accumulator, which is not an addressable register.

5.2.2 CONT (Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/PHEN	/INT	-	-	PAB	PSR2	PSR1	PSR0

Bit 7 (/PHEN) I/O pin pull-high enable flag.

0: For P60~P67, P74~P75 and P90~P95, the pull-high function is enabled.

1: The pull-high function is disabled.

Bit 6 (INT) An interrupt enable flag cannot be written to by the CONTW instruction.

0: interrupt masked by the DISI instruction.

1: interrupt enabled by the ENI or RETI instruction.

Bits 5 and 4: Not used, read as "0".

Bit 3 (PAB) Prescaler assignment bit.

0: TCC

1: WDT

Bit 2 (PSR2) ~ Bit 0 (PSR0) TCC/WDT prescaler bits.

Bits 0~3, and 7 of the CONT register are readable and writable.

5.2.3 IOC5 ~ IOC9 (I/O Port Control Register)

0: puts the relative I/O pin as output

1: puts the relative I/O pin into high impedance

- Both P74 and P76 should not be defined as output pins at the same time. This also applies to both P75 and P77.
- Only the lower 6 bits of the IOC9 register are used.

5.2.4 IOCC (T1CON: Timer 1 Control Register)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0C	T1CON/IOCC	0	0	0	0	0	TM1E	TM1P1	TM1P0

Bit 2 (TM1E): Timer 1 Function Enable bit

0 : Disable Timer 1 function as default

1 : Enable Timer 1 function

Bit 1~Bit 0 (TM1P): Timer 1 Prescaler bit

Refer to the Timer 1 prescaler table for FOSC illustration under the section “Timer 1” on the subsequent pages.

5.2.5 IOCD (Pull-high Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
S7	-	-	-	/PU9	/PU8	/PU6	/PU5

- The default values of /PU5, /PU6, /PU8, and /PU9 are “1”, which means that the pull-high function is disabled.
- /PU6 and /PU9 are “AND” gating with /PHEN, that is, when each one is written with a “0”, pull high is enabled.
- S7 defines the driving ability of the P70-P72.

  0: Normal output

  1: Enhances the driving ability of the LED

5.2.6 IOCE (WDT Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	ODE	WDTE	SLPC	ROC	-	-	/WUE

Bits 7, and 1~2 are not used.

Bit 6 (ODE) Open-drain control bit.

0 : Both P76 and P77 are normally I/O pins.

1 : Both P76 and P77 pins have the open-drain function inside.

The ODE bit can be read and written to.

Bit 5 (WDTE) Control bit used to enable the Watchdog timer.

The WDTE bit can be used only if ENWDT, the Code Option bit, is "1." If the ENWDT bit is "1," then WDT can be disabled / enabled by the WDTE bit.

0: Disable WDT

1: Enable WDT

The WDTE bit is not used if ENWDT, the Code Option bit ENWD is "0". That is, if the ENWDT bit is "0", WDT is always disabled no matter what the WDTE bit is.

The WDTE bit can be read and written to.

Bit 4 (SLPC) This bit is set by hardware at a falling edge of the wake-up signal and is cleared by software. The SLPC is used to control the oscillator operation. The oscillator is disabled (oscillator stops, and the controller enters the Sleep 2 mode) on the high-to-low transition and is enabled (the controller is awakened from Sleep 2 mode) on a low-to-high transition.

In order to ensure a stable output of the oscillator, once the oscillator is enabled again, there is a delay of approximately 18 ms (oscillator start-up timer (OST)) before the next program instruction is executed. The OST is always activated by wake-up from sleep mode whether the Code Option bit ENWDT is "0" or not. After waking up, the WDT is enabled if the Code Option ENWDT is "1". The block diagram of Sleep 2 mode and wake-up caused by the input trigger is depicted in Fig. 5-4. The SLPC bit can be read and written to.

Bit 3 (ROC) ROC is used for the R-option. Setting ROC to "1" will enable the status of the R-option pins (P80, P81) to be read by the controller. Clearing ROC will disable the R-option function. Otherwise, the R-option function is introduced. Users must connect the P81 pin and/or P80 pin to VSS by a 560KΩ external resistor (Rex). If Rex is connected/disconnected with VDD, the status of P80 (P81) will be read as "0"/"1" (refer to Fig. 7(b)). The ROC bit can be read and written to.

Bit 0 (/WUE) This control bit is used to enable the wake-up function of P60~P67, P74~P75, and P90~P91.

0 : Enable the wake-up function

1 : Disable the wake-up function

The /WUE bit can be read and written to.

5.2.7 IOCF (Interrupt Mask Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	TM1IE	SPIIE	EXIE	TCIE

Bits 4~7 Not used.

Individual interrupt is enabled by setting its associated control bit in IOCF to "1".

The IOCF Register could be read and written to.

Bit 3 (TM1IE) TM1IE interrupt enable bit.

0 : disable TM1IE interrupt

1 : enable TM1IE interrupt

Bit 2 (SPIIE) SPI interrupt enable bit.

0 : disable SPI interrupt

1 : enable SPI interrupt

Bit 1 (EXIE) EXIF interrupt enable bit.

0 : disable EXIF interrupt

1 : enable EXIF interrupt

Bit 0 (TCIE) TCIF interrupt enable bit.

0 : disable TCIF interrupt

1: enable TCIF interrupt

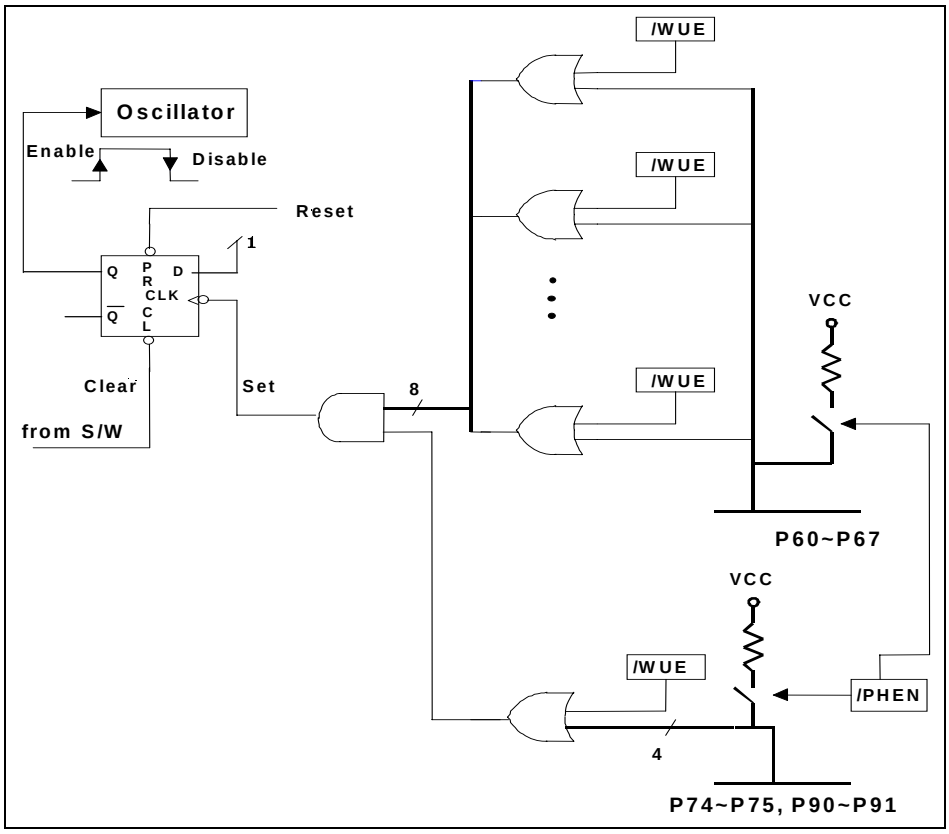


Fig. 5-4 Block Diagram of Sleep Mode and Wake-up Circuits on the I/O Ports

5.3 TCC/WDT Presacler

An 8-bit counter is available as prescaler for the TCC or WDT. The prescaler is available for either the TCC or WDT at any given time, and the PAB bit of CONT register is used to determine the prescaler assignment. The PSR0~PSR2 bits determine the prescaler ratio. The prescaler is cleared each time the instruction is written to TCC in TCC mode. The WDT and prescaler, when assigned to WDT mode, are cleared by the WDTC or SLEP instructions. Fig. 5-5 depicts the circuit diagram of TCC/WDT.

- R1 (TCC) is an 8-bit timer/counter. TCC will increase by one at every instruction cycle (without prescaler).
- The watchdog timer is a free running on-chip RC oscillator. The WDT will keep running even when the oscillator driver has been turned off (i.e. in sleep mode). During normal or sleep mode operation, a WDT time-out (if enabled) will cause the device to reset. The WDT can be enabled or disabled any time during normal mode by software programming (if Code Option bit ENWDT is "1"). Refer to the WDTE bit of the IOCE register. Without presacler, the WDT time-out period is approximately 18 ms[1].

5.4 I/O Ports

The I/O registers, from Port 5 to Port 9, are bidirectional tri-state I/O ports. P60~P67, P74~P75, and P90~P91 provides internal pull-high. P60~P67, P74~P75, and P90~P95 provides programmable wake-up function through software. P76~P77 can have an open-drain output by software control. P80~P81 are the R-option pins which are enabled by software. When the R-option function is used, it is recommended that P80 and P81 be used as output pins. During R-option enabled state, P80 and P81 must be programmed as input pins. If an external resistor is connected to P80 (P81) for the R-option function, the current consumption should be taken as an important factor in the applications for low power consideration.

The I/O ports can be defined as "input" or "output" pins by the I/O control registers (IOC5~IOC9) under program control. The I/O registers and I/O control registers are both readable and writable. The I/O interface circuit is shown in Fig. 5-6. Note that the reading path source of input and output pins is different when reading the I/O port.

[1] Vdd = 5V, set up time period = 16.2ms ± 30%
Vdd = 3V, set up time period = 18.0ms ± 30%

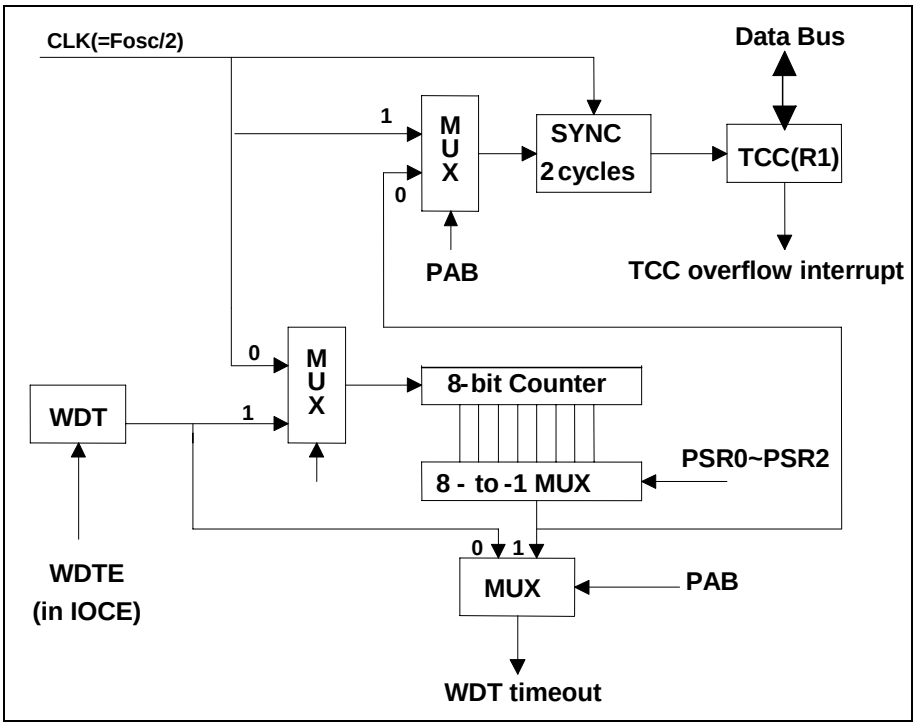


Fig. 5-5 Block Diagram of TCC WDT

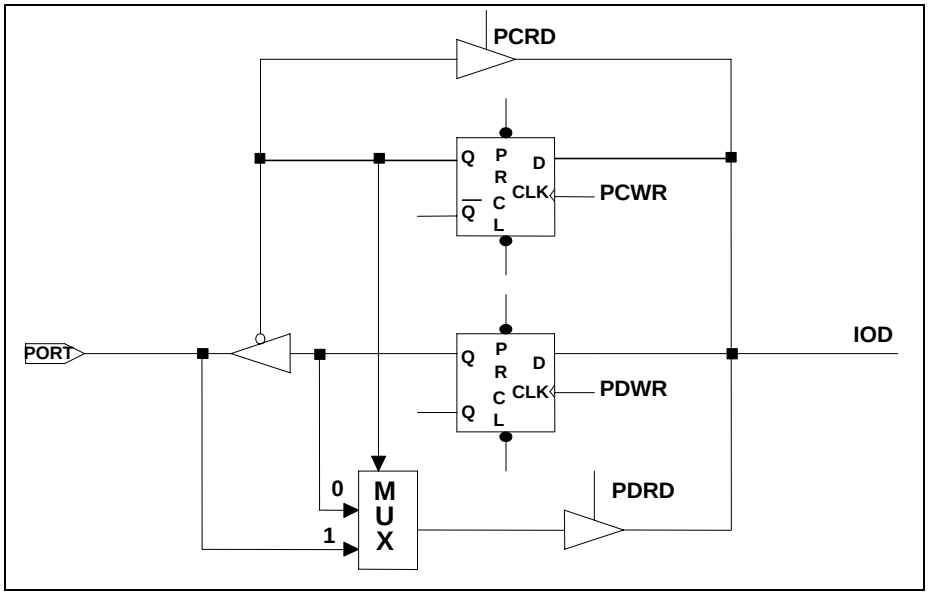


Fig. 5-6 (a) I/O Port and I/O Control Register Circuit

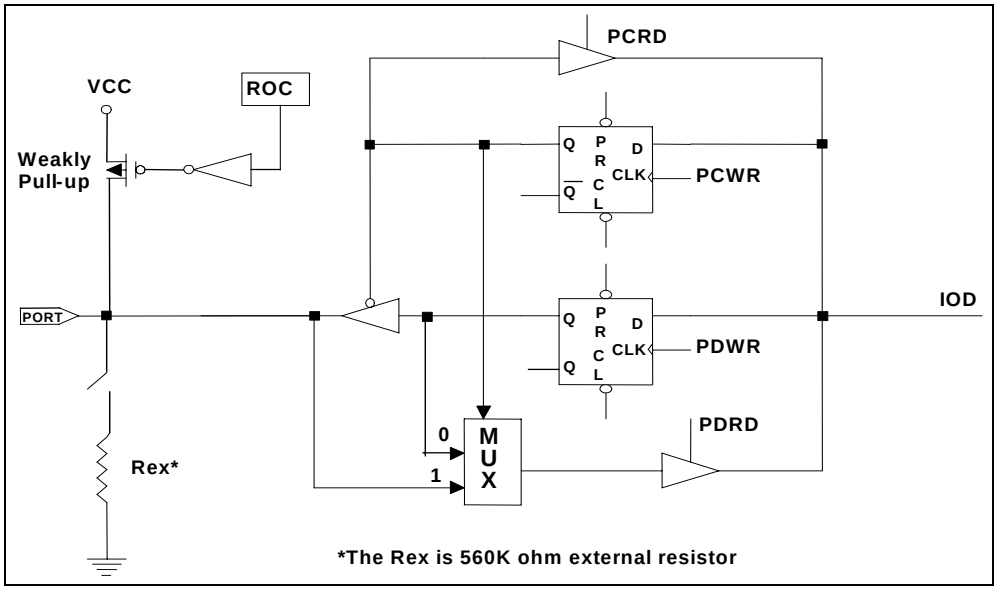


Fig. 4-6(b) The Circuit of I/O Port with R-option (P80, P81)

5.5 Serial Peripheral Interface Mode

5.5.1 Overview & Features

Overview:

Figures 4-7, 4-8, and 4-9 shows how the EM78452 communicates with other devices through SPI module. If EM78452 is a master controller, it sends clock through the SCK pin. A couple of 8-bit data are transmitted and received at the same time. However, if EM78452 is defined as a slave, its SCK pin could be programmed as an input pin. Data will continue to be shifted based on both the clock rate and the selected edge. In Slave mode when code option bit 7 (SPIHSK) is set to 0, the P91 (HSK) pin will be set to high after SPI enable and SSE bit set to 1. You can also set SPIS bit 7(DORD) to decide the SPI transmission order, SPIC bit3 (SDOC) to control SDO pin after serial data output status and SPIS bit 6 (TD1), bit 5 (TD0) decides the SDO status output delay times. Those three functions mentioned can work however; it must be based on code option bit5 (SDOS) set to 0.

Features:

- Operation in either Master mode or Slave mode
- Three-wire or four-wire synchronous communication; that is, full duplex
- Programmable baud rates of communication
- Programming clock polarity, (RD bit7)
- Interrupt flag available for the read buffer full
- SPI transmission order

- After serial data output SDO status select
- SDO status output delay times
- SPI handshake pin
- Up to 8 MHz (maximum) bit frequency

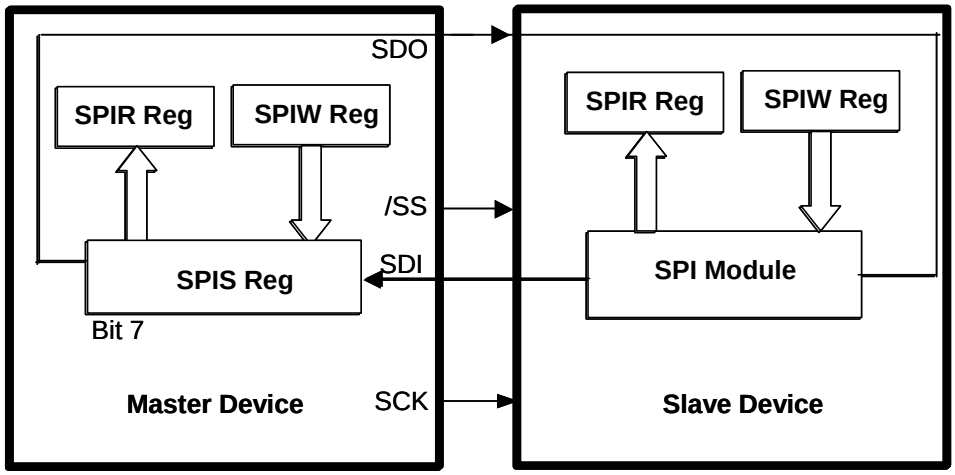


Fig. 5-7 SPI Master/Slave Communication

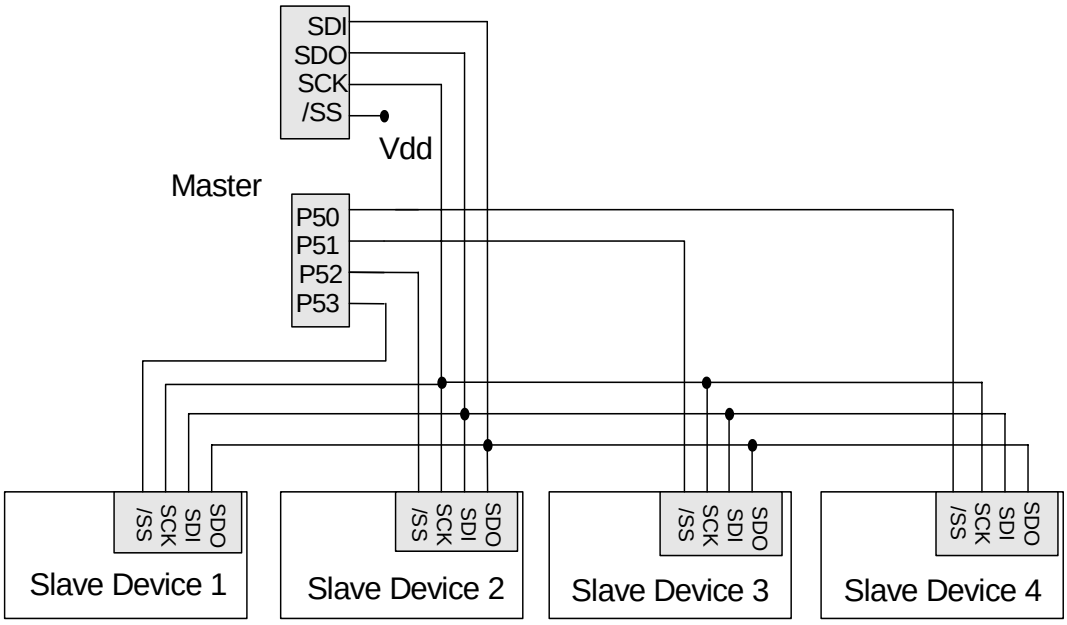


Fig. 5-8 SPI Configuration of Single-Master and Multi-Slave

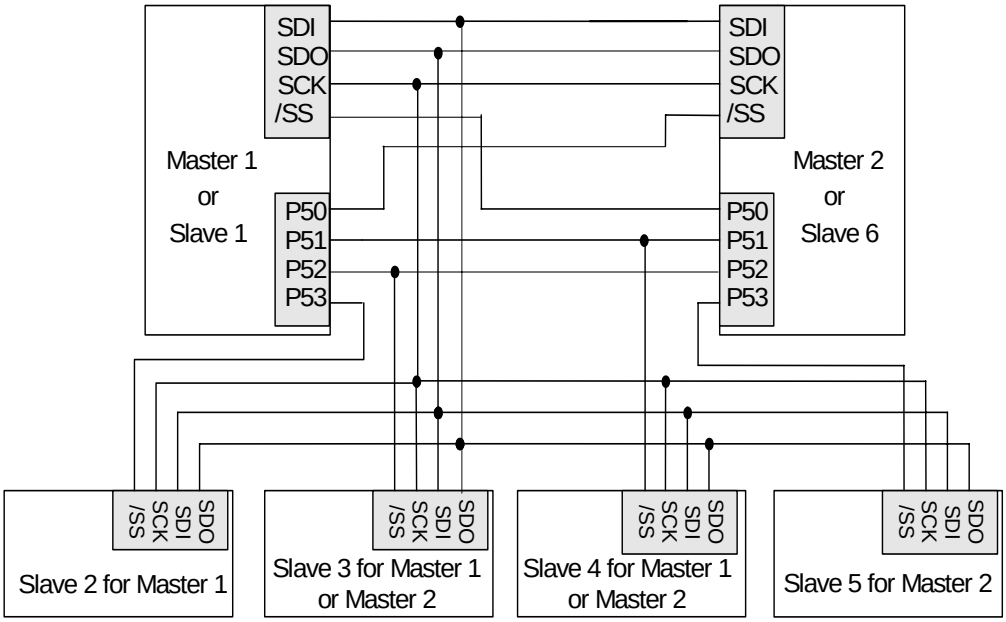


Fig. 5-9 SPI Configuration of Single-Master and Multi-Slave

5.5.2 SPI Function Description

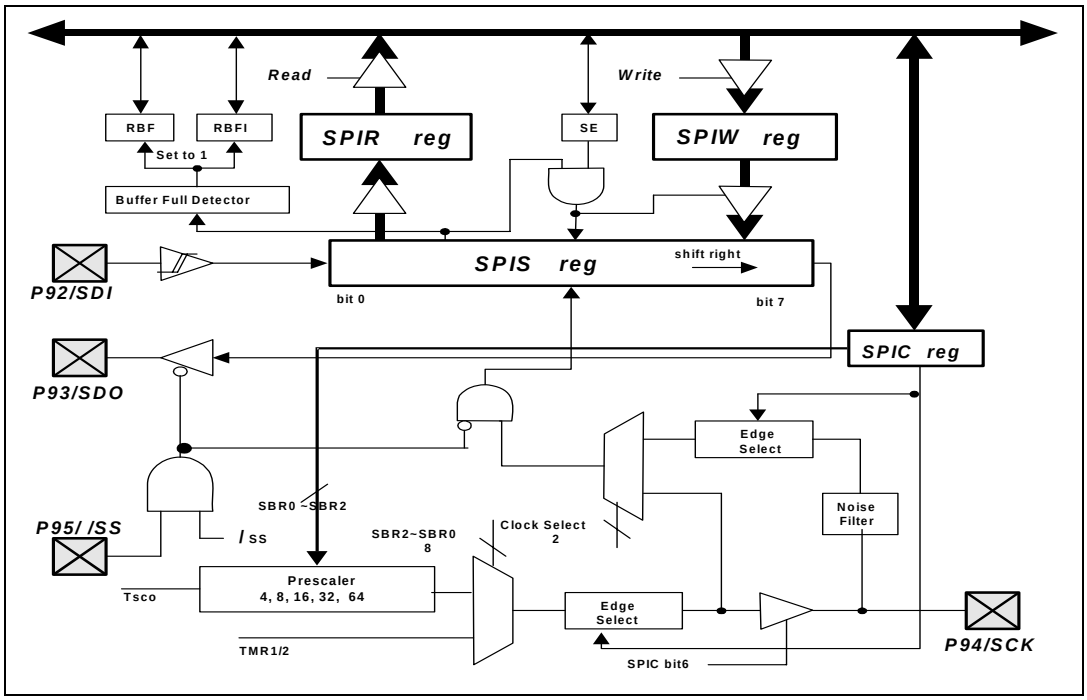


Fig. 5-10 SPI Block Diagram

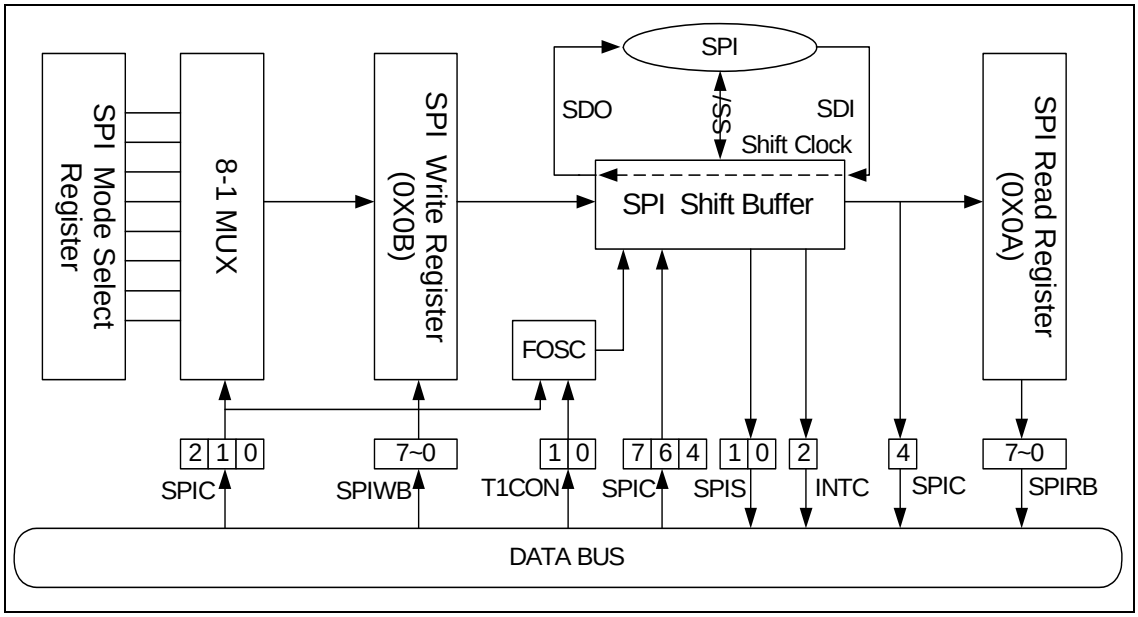


Fig. 5-11 The Function Block Diagram of SPI Transmission

Below are the functions of each block and explanations on how to carry out the SPI communication with the signals depicted in Fig.4-10 and Fig.4-11:

- P91/SRDY : Slave Ready pin
- P92/SDI : Serial Data In
- P93/SDO : Serial Data Out
- P94/SCK : Serial Clock
- P95//SS:/Slave Select (Option). This pin (/SS) may be required during slave mode.
- RBF : Set by Buffer Full Detector, and reset by software.
- Buffer Full Detector : Set to 1 when an 8-bit shifting is completed.
- SSE : Loads the data in SPIS register, and begin to shift
- SPIS reg. : Shifting byte in and out. The MSB is shifted first. Both the SPIS and the SPIW registers are loaded at the same time. Once data are written, SPIS starts transmission / reception. The data received will be moved to the SPIR register as the shifting of the 8-bit data is completed. The RBF (Read Buffer Full) flag and the RBFI (Read Buffer Full Interrupt) flag are then set.
- SPIR reg. : Read buffer. The buffer will be updated as the 8-bit shifting is completed. The data must be read before the next reception is completed. The RBF flag is cleared as the SPIR register reads.
- SPIW reg. : Write buffer. The buffer will deny any attempts to write until the 8-bit shifting is completed.

The SSE bit will be kept in “1“ if the communication is still undergoing. This flag must be cleared as the shifting is completed. Users can determine if the next write attempt is available.

- SBRS2~SBRS0: Programming the clock frequency/rates and sources.
- Clock Select:Selects either the internal or the external clock as the shifting clock.
- Edge Select: Selects the appropriate clock edges by programming the CES bit

5.5.3 SPI Signal & Pin Description

The detailed functions of the four pins, SDI, SDO, SCK, and /SS, which are shown in Fig. 5-8.

SRDY/P92 (Pin 6):

- Slave ready pin
- In Slave mode when code option bit 7 (SPIHSK) set to 0, P91 (SRDY) this pin will be set to high after SPI enable and SSE bit set to 1.

SDI/P92 (Pin 7):

- Serial Data In,
- Receive sequentially, the Most Significant Bit (MSB) first, Least Significant Bit (LSB) last,
- Defined as high-impedance, if not selected,
- Program the same clock rate and clock edge to latch on both the master and slave devices,
- The byte received will update the transmitted byte,
- Both the RBF and RBFIF bits (located in Register 0x0C) will be set as the SPI operation is completed.
- Timing is shown in Fig. 5-12 and 5-13.

SDO/P93 (Pin 8):

- Serial Data Out,
- Transmit sequentially; the Most Significant Bit (MSB) first, Least Significant Bit (LSB) last,
- Program the same clock rate and clock edge to latch on both the master and slave devices,
- The received byte will update the transmitted byte,
- The CES (located in Register 0x0D) bit will be reset, as the SPI operation is completed.
- Timing is shown in Fig. 5-12 and 5-13.

SCK/P94 (Pin 9):

- Serial Clock
- Generated by a master device
- Synchronize the data communication on both the SDI and SDO pins
- The CES (located in Register 0x0D) is used to select the edge to communicate.
- The SBR0~SBR2 (located in Register 0x0D) is used to determine the baud rate of communication
- The CES, SBR0, SBR1, and SBR2 bits have no effect in slave mode
- Timing is shown in Fig. 5-12 and Fig. 5-13

/SS/P95 (Pin 10):

- Slave Select; negative logic
- Generated by a master device to signify the slave(s) to receive data
- Goes low before the first cycle of SCK appears, and remains low until the last (eighth) cycle is completed
- Ignores the data on the SDI and SDO pins while /SS is high, because the SDO is no longer driven.
- Timing is shown in Fig. 5-12 and Fig. 5-13.

5.5.4 Programmed the Related Registers

As the SPI mode is defined, the related registers of this operation are shown in Table 2 and Table 3.

Table 1 Related Control Registers in SPI Mode

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0D	*SPIC/RD	CES	SPIE	SRO	SSE	SDOC	SBR2	SBR1	SBR0
0x0F	INTC/IOCF	--	--	--	--	TM1IE	SPIIE	EXIE	TCIE

SPIC: SPI Control Register.

Bit 7 (CES): Clock Edge Select bit

0 : Data shifts out on rising edge, and shifts in on falling edge. Data is on hold during the low level.

1 : Data shifts out on falling edge, and shifts in on rising edge. Data is on hold during the high level.

Bit 6 (SPIE): SPI Enable bit

0 : Disable SPI mode

1 : Enable SPI mode

Bit 5 (SRO): SPI Read Overflow bit

0 : No overflow.

1 : A new data is received while the previous data is still being on hold in the SPIB register. Under this condition, the data in the SPIS register will be destroyed. To avoid setting this bit, users should read the SPIRB register even if the transmission is implemented only.

Note that this can only occur in slave mode.

Bit 4 (SSE): SPI Shift Enable bit

0 : Reset as soon as the shifting is completed and the next byte is ready to shift.

1 : Start to shift, and stays on 1 while the current byte continues to transmit.

Note that this bit can be reset by hardware only.

Bit 3 (SDOC): SDO output status control bit:

1 : After Serial data output SDO keep low.

0 : After Serial data output SDO keep High

Bits 2~0 (S BRS): SPI Baud Rate Select Bits

SBRS2 (Bit 2)	SBRS1 (Bit 1)	SBRS0 (Bit 0)	Mode	Baud Rate
0	0	0	Master	Fosc/2
0	0	1	Master	Fosc/4
0	1	0	Master	Fosc/8
0	1	1	Master	Fosc/16
1	0	0	Master	Fosc/32
1	0	1	Slave	/SS enable
1	1	0	Slave	/SS disable
1	1	1	Master	TMR1/2

Note: In Mater mode, the /SS pin is disabled.

INTC: Interrupt control register

Bit 3 (TM1IE) TM1IE interrupt enable bit.

0 : disable TM1IE interrupt

1 : enable TM1IE interrupt

Bit 2 (SPIIE) SPI interrupt enable bit.

0 : disable SPI interrupt

1 : enable SPI interrupt

Bit 1 (EXIE) EXIF interrupt enable bit.

0 : disable EXIF interrupt

1 : enable EXIF interrupt

Bit 0 (TCIE) TCIF interrupt enable bit.

0 : disable TCIF interrupt

1 : enable TCIF interrupt

Table 2 Related Status/Data Registers of the SPI Mode

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0X0A	SPIRB/RA	SRB7	SRB6	SRB5	SRB4	SRB3	SRB2	SRB1	SRB0
0x0B	SPIWB/RB	SWB7	SWB6	SWB5	SWB4	SWB3	SWB2	SWB1	SWB0
0x0C	SPIS/RC	DORD	TD1	TD0	TM1IF	OD3	OD4	-	RBF

SPIRB: SPI Read Buffer. Once the serial data is received completely, it will be loaded to SPIRB from SPISR. The RBF bit and the RBFIF bit in the SPIS register will also be set.

SPIWB: SPI Write Buffer. As transmitted data is loaded, the SPIS register stands by and start to shift the data when sensing SCK edge with SSE set to "1".

SPIS: SPI Status register

Bit 7 (DORD): Read Buffer Full Interrupt flag

0 : Shift left (MSB first)

1 : Shift right (LSB first)

Bit 6~Bit 5: SDO Status Output Delay Times Options

TD1	TD0	Delay Time
0	0	8 CLK
0	1	16 CLK
1	0	24 CLK
1	1	32 CLK

T1ROS (Bit 4): Timer 1 Read Outbuffer Select Bit

0 : Read Value from Timer 1 Preset Register

1 : Read Value from Timer 1 Counter Register

Bit 4 (TM1IF): Timer 1 interrupt flag

Bit 3 (OD3) Open-Drain Control bit (P93)

0 : Open-drain disable for SDO

1 : Open-drain enable for SDO

Bit 2 (OD4): Open Drain-Control bit (P94)

0 : Open-drain disable for SCK

1 : Open-drain enable for SCK

Bit 0 (RBF): Read Buffer Full flag

0 = Receive is ongoing, SPIB is empty.

1 = Receive is completed, SPIB is full.

5.5.5 SPI Mode Timing

The edge of SCK is selected by programming bit CES. The waveform shown in Fig. 5-12 is applicable regardless whether the EM78452 is in master or slave mode with /SS disabled. However, the waveform in Fig. 5-13 can only be implemented in slave mode with /SS enabled.

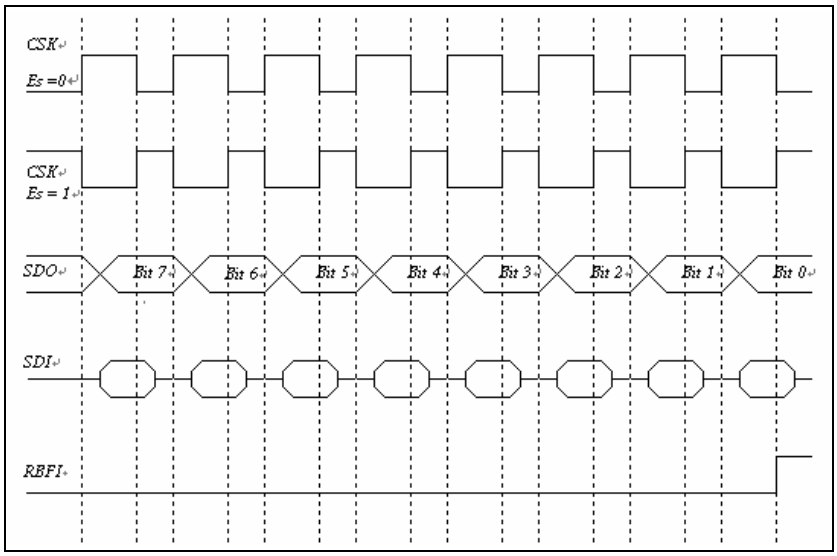


Fig. 5-12 SPI Mode with /SS Disabled

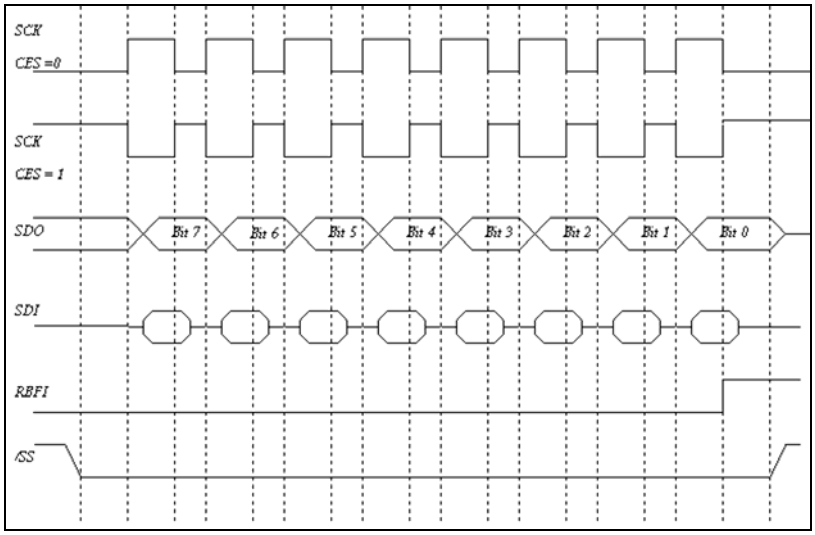


Fig. 4-13 SPI Mode with /SS Enable

5.5.6 Software Application of SPI

Example for SPI:

For Master

ORG 0X0

Setting:

```
CLRA
IOW 0X05                ; Set Port 5 output
IOW 0X06                ; Set Port 6 output
MOV 0X05,A
MOV A,@0B11001111       ; Set prescaler for WDT
CONTW
MOV A,@0B00010001       ; Disable wake-up function
IOW 0X0E
MOV A,@0B00000000       ; Disable interrupt
IOW 0X0F
MOV A,@0x07             ; SDI input and SDO, SCK output
IOW 0x09
MOV A,@0B10000000       ; Clear RBF and RBFIF flag
MOV 0x0C,A
MOV A,@0B11100000       ; Select clock edge and enable SPI
MOV 0X0D,A
```

Start:

```
  WDTC
  BC 0X0C,1                ; Clear RBFIF flag
  MOV A,@0XFF
  MOV 0X05,A               ; Show a signal at Port 5
  MOV 0X0A,A               ; Move FF at read buffer
  MOV A,@0XAA              ; Move AA at write buffer
  MOV 0X0B,A
  BS 0X0D,4                ; Start to shift SPI data
  NOP
  JMP SETTING              ; Polling loop for checking SPI
  JMP $-2                  ; transmission completed
  BC 0X03,2
  CALL DELAY               ; To catch the data from slaver
  MOV A,0X0A
  XOR A,@0X5A              ; Compare the data from slaver
  JBS 0X03,2
  JMP START
FLAG:
  MOV A,@0X55              ; Show the signal when receiving
  MOV 0X05,A               ; correct data from slaver
  CALL DELAY
  JMP START
DELAY:
                           ; (user's program)

  EOP
  ORG 0XFFF
  JBC 0X0D,4
```

For Slaver

```
ORG 0X0
INITI:
  JMP INIT
  ORG 0X2
INTERRUPT:            ; Interrupt address
  MOV A,@0X55
  MOV 0X06,A          ; Show a signal at Port 6 when entering
                      ; interrupt
  MOV A,@0B11100110   ; Enable SPI, /SS disabled
  MOV 0X0D,A
  BS 0X0D,4           ; Keep SSE at 1 to wait for SCK signal in
                        order to shift data
  MOV A,@0X00         ; Move 00 to write buffer in order to keep
                      ; master's read buffer as 00
  MOV 0X0B,A
  BS 0X0D,4           ; Keep SSE at 1 to wait for SCK signal in
                      ; order to shift data
  NOP
  JBC 0X0D,4          ; Polling loop for checking SPI
                      ; transmission completed
  JMP $-2
  BS 0X0D,4           ; Keep SSE at 1 to wait for SCK signal in
                      ; order to shift data
  BC  0X03,2
  MOV A,0X0A
  MOV 0X06,A          ; Read master's data from read buffer
  XOR A,@0XAA         ; Check pass signal from read buffer
  JBS 0X03,2
  JMP SPI
  JMP $-6
```

```
ORG 0X30

INIT:
  CLRA
  IOW 0X05
  IOW 0X06
  MOV 0x05,A
  MOV 0X06,A
  MOV A,@0XFF
  IOW 0X08
  MOV A,@0B11001111   ; Set prescaler for WDT
  CONTW
  MOV A,@0B00010001   ; Disable wakeup function
  IOW 0X0E
  MOV A,@0B00000010   ; Enable external interrupt
  IOW 0XF
  ENI
  MOV A,@0B00110111
  IOW 0x09
  BC  0X3F,1          ; Clear RBFIF flag
  NOP
  JBS 0X3F,1          ; Polling loop for checking interrupt
                      ; occurrences
  JMP $-2
  JMP INTERRUPT
SPI:
  BS 0X0D,4           ; Keep SSE enabled as long as possible
  WDTC
  MOV A,@0X0F         ; Show a signal when entering SPI loop
  MOV 0X06,A
  JBC 0X08,1          ; Choose P81 as a signal button
  JMP SPI
  MOV A,@0X5A         ; Move 5A into write buffer when P81 button
                      ; is pushed
  MOV 0X0B,A
  NOP
  JBC 0X0D,4          ; Polling loop for checking SPI
                      ; transmission completed
  JMP $-2
  BS 0XD,4
  NOP
  NOP
  MOV A,@0XF0         ; Display at Port6 when P81 button is pushed
```

```
  MOV 0X06,A
  MOV A,@0X00          ; Send a signal to master to prevent
                       ; infinite loop
  MOV 0X0B,A
  NOP
  JBC 0X0D,4
  JMP $-2
  BS 0X0D,4
  JMP INITI
  BC 0x0C,1
  NOP
  JMP SPI
DELAY:                 ; (user's program)


  EOP
  ORG 0XFFF
  BS 0x0C,7
```

5.6 Timer 1

5.6.1 Overview

Timer 1 (TMR1) is an 8-bit clock counter with programmable prescaler. The TMR1 is in SPI baud rate clock generator mode (SBRS0, SBRS1and SBRS2 a1l set to 1) and then SPI control register Bit 4 (SSE) is set to "1". Timer 1 will be enabled automatically without setting TM1E. TMR1 can be read and written to, and cleared on any reset conditions.

5.6.2 Function Description

Fig. 5-14 shows Timer 1 block diagram. Each signal and block is described as follows:

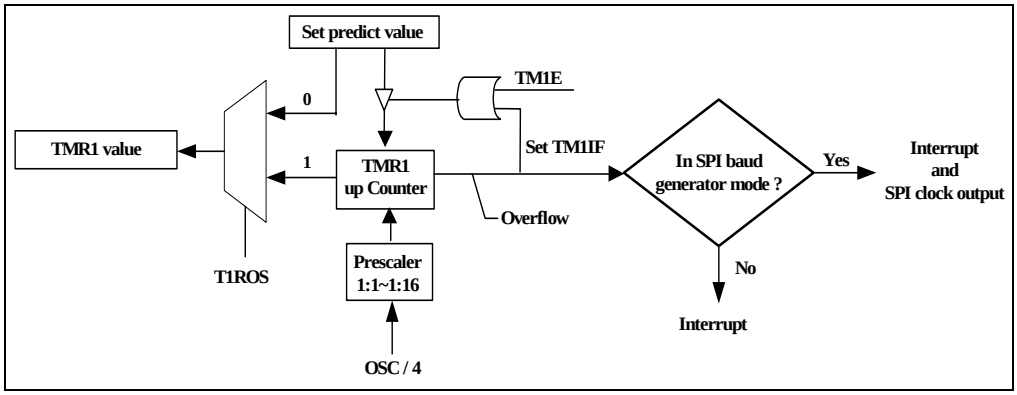


Fig. 5-14 Timer 1 Block Diagram

- OSC/4: Input clock.
- Prescaler: Option of 1:1, 1:4, 1:8, and 1:16 defined by T1P1 and T1P2 (T1CON<1, 0>). It is cleared when a value is written to TMR1 or T1CON, and during any kind of reset as well.
- TMR1: Timer 1 register. TMR1 increases until it overflows, and then resets to 0. If it is in the SPI baud rate generator mode, its output is fed as a shifting clock. TMR1 register; increases until it overflows, and then reloads the predicted value. If a value is written to Timer 1, the predicted value and TMR1 value will be the set value. However, If TRIOS is set to "1" and value is read from TMR1, the value will be TMR1 direct value. Or else, TRIOS is set to "0" and the value is read from TMR1, the value will be TMR1 predicted value.

5.6.3 Programming the Related Registers

The related registers of the defining TMR1 operation are shown in Table 4 and Table 5

Table 3 Related Control Registers of the TMR1

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0C	SPIS/RC	DORD	TD1	TD0	T1ROS	OD3	OD4	-	RBF
0x0F	INTC/IOCF	0	0	0	0	TM1IE	SPIIE	EXIE	TCIE

Table 4 Related Status/Data Registers ofTMR1

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0X0E	TMR1/RE	TMR17	TMR16	TMR15	TMR14	TMR13	TMR12	TMR11	TMR10
0x0C	T1CON/IOCC	0	0	0	0	0	TM1E	TM1P1	TM1P0

- TMR1: Timer 1 Register

  TMR17~TMR10 are bit set of Timer1 register and it increases until the value matches PWP and then it resets to 0.

- T1ROS (Bit 3): Timer Read Buffer Select Bit

  0: Read Value from Timer 1 Preset Register

  1: Read Value from Timer 1 Counter Register.

- T1CON: Timer 1 Control Register

  Bit 2 (TM1E): Timer1 enable bit

  Bit 1 (TM1P1) and Bit 0 (TM1P): Timer 1 prescaler for FSCO

TM1P1	TM1P0	Prescaler Rate
0	0	1:1
0	1	1:4
1	0	1:8
1	1	1:16

5.7 Reset and Wake-up

A reset is initiated by

(1) Power-on reset, or

(2) /RESET pin input “low”, or

(3) WDT timeout. (if enabled)

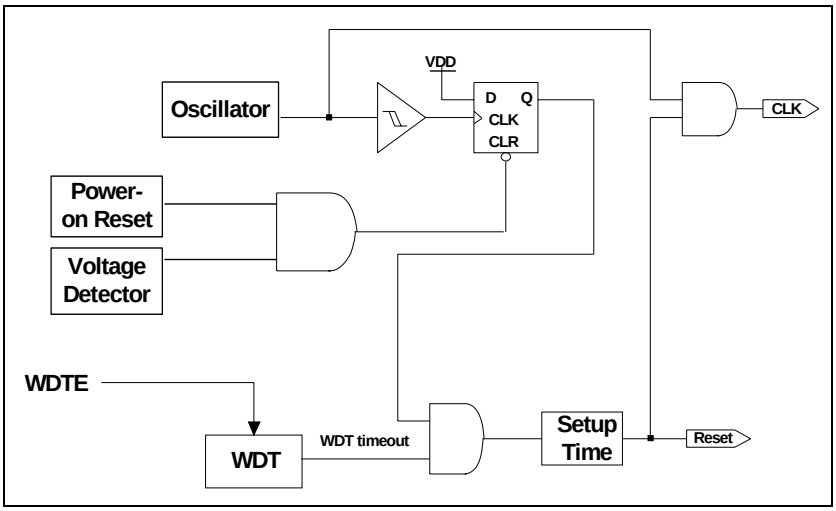


Fig. 5-15 Block Diagram of Reset

The EM78452 POR voltage range is between 1.2V~2.0V. Under customer application, when power is OFF, the Vdd must drop below 1.2V and remains OFF for 10μs before power can be switched ON again. This way, the EM78452 will reset and work normally. The extra external reset circuit will work well if Vdd can rise at very fast speed (50 ms or less). However, in most cases where critical applications are involved, extra devices are required to assist in solving the power-up problem.

The device is kept in a RESET condition for a period of approx. 18ms[2] (one oscillator start-up timer period) after the reset is detected and Fig. 5-15 is the block diagram of reset. Once the RESET occurs, the following functions are performed.

- The oscillator is running, or will be started.
- The Program Counter (R2) is set to all "1".
- When power is switched on, Bits 5~6 of R3 and the upper 2 bits of R4 are cleared.
- All I/O port pins are configured as input mode (high-impedance state).
- The Watchdog timer and prescaler are cleared.

[2] Vdd = 5V, set up time period = 16.20ms ± 30%
Vdd = 3V, set up time period = 18.0ms ±30%

- The Watchdog timer is enabled if the Code Option bit ENWDT is "1".
- The CONT register is set to all "1" except for Bit 6 (INT flag).
- Bits 3 and 6 of the IOCE register are cleared, Bits 0, 4~5 of the IOCE register are set to "1".
- Bit 0 of R3F and Bit 0 of the IOCF registers are cleared.

The sleep mode (power down) is achieved by executing the SLEP instruction (named as Sleep 1 MODE). While entering sleep mode, the WDT (if enabled) is cleared but keeps on running. The controller is awakened by WDT timeout (if enabled), and it will cause the controller to reset. The T and P flags of R3 are used to determine the source of the reset (wake-up).

In addition to the basic Sleep 1 Mode, the EM78452 has another sleep mode (caused by clearing "SLPC" bit of IOCE register, designated as Sleep 2 Mode). In the Sleep 2 Mode, the controller can be awakened by:

(a) Any of the wake-up pin(s) is set to “0.” (Refer to Fig. 5-16). Upon waking, the controller will continue to execute the program in-line. In this case, before entering Sleep 2 Mode, the wake-up function of the trigger sources (P60~P67, P74~P75, and P90~P91) should be selected (e.g. input pin) and enabled (e.g. pull-high, wake-up control). One caution should be noted is that after waking up, the WDT is enabled if the Code Option bit ENWDT is "1". The WDT operation (to be enabled or disabled) should be appropriately controlled by software after waking up.

(b) WDT time-out (if enabled) or external reset input on /RESET pin will trigger a controller reset.

Table 5 Usage of Sleep and Sleep 2 Mode

Usage of Sleep and Sleep2 Mode	
SLEEP2	**SLEEP**
(a) Before Sleep 1. Set Port6 or P74 or P75 or P90 or P91 Input 2. Enable Pull-high and set WDT prescaler over 1:1 (Set CONT.7 and CONT.3 ~ CONT.0) 3. Enable Wake-up (IOCE.0) 4. Execute Sleep 2 (Set IOCE.4)	(a) Before Sleep 1. Execute SLEP instruction
(b) After Wake-up 1. Next instruction 2. Disable Wake-up 3. Disable WDT (Set IOCE.5)	(b) After Wake-up 1. Reset

If Port6 Input Status Changed Wake-up is used to wake-up the EM78452 (Case [a] above), the following instructions must be executed before entering Sleep 2 mode:

```
MOV       A, @11111111b   ; Set Port 6 input
IOW       IOC6
MOV       A, @0xxx1010b   ; Set Port6 pull-high, WDT prescaler,
                          ; prescaler must set over 1:1
CONTW
MOV       A, @xx00xxx0b   ; Enable Port 6 wake-up function, Enable
IOW       IOCE            ; Sleep 2

After
Wake-up

NOP
MOV       A, @ xx01xxx1b  ; Disable Port 6 wake-up function;
IOW       IOCE            ; Disable WDT
```

After waking up from the Sleep 2 mode, WDT is automatically enabled. The WDT enabled/disabled operation after waking up from Sleep 2 mode should be properly defined in the software.

To avoid a reset from occurring when the Port 6 “Input Status Changed Interrupt” enters into an interrupt vector or is used to wake-up the MCU, the WDT prescaler must be set above the ratio of 1:1.

Table 6 Summary of the Initialized Values for Registers

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
N/A	IOC5	Bit Name	C57	C56	C55	C54	C53	C52	C51	C50
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOC6	Bit Name	C67	C66	C65	C64	C63	C62	C61	C60
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOC7	Bit Name	C77	C76	C75	C74	C73	C72	C71	C70
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOC8	Bit Name	C87	C86	C85	C84	C83	C82	C81	C80
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOC9	Bit Name	C97	C96	C95	C94	C93	C92	C91	C90
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	CONT	Bit Name	/PHEN	/INT	-	-	PAB	PSR2	PSR1	PSR0
		Power-on	1	0	1	1	1	1	1	1
		/RESET and WDT	1	P	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x00	R0 (IAR)	Bit Name	-	-	-	-	-	-	-	-
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x01	R1 (TCC)	Bit Name	-	-	-	-	-	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x02	R2 (PC)	Bit Name	-	-	-	-	-	-	-	-
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	**P	**P	**P	**P	**P	**P	**P	**P
0x03	R3 (SR)	Bit Name	GP	PS1	PS0	T	P	Z	DC	C
		Power-on	0	0	0	t	t	U	U	U
		/RESET and WDT	0	0	0	t	t	P	P	P
		Wake-up from Pin Change	P	P	P	t	t	P	P	P
0x04	R4 (RSR)	Bit Name	RSR.1	RSR.0	-	-	-	-	-	-
		Power-on	0	0	U	U	U	U	U	U
		/RESET and WDT	0	0	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x05	R5 (P5)	Bit Name	P57	P56	P55	P54	P53	P52	P51	P50
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x06	R6 (P6)	Bit Name	P67	P66	P65	P64	P63	P62	P61	P60
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x07	R7 (P7)	Bit Name	P77	P76	P75	P74	P73	P72	P71	P70
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x08	R8 (P8)	Bit Name	P87	P86	P85	P84	P83	P82	P81	P80
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x09	R9 (P9)	Bit Name	P97	P96	P95	P94	P93	P92	P91	P90
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x0A	RA (SPIRB)	Bit Name	SRB7	SRB6	SRB5	SRB4	SRB3	SRB2	SRB1	SRB0
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x0B	RB (SPIWB)	Bit Name	SWB7	SWB6	SWB5	SWB4	SWB3	SWB2	SWB1	SWB0
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x0C	RC (SPIS)	Bit Name	DORD	TD1	TD2	T1ROS	OD3	OD4	-	RBF
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x0D	RD (SPIC)	Bit Name	CES	SPIE	SRO	SPISE	SDOC	SBRS2	SBRS1	SBRS0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x0E	RE (TMR1)	Bit Name	TMR17	TMR16	TMR15	TMR14	TMR13	TMR12	TMR11	TMR10
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x3F	R3F (ISR)	Bit Name	-	-	-	-	T1IF	SPIIF	EXIF	TCIF
		Power-on	U	U	U	U	0	0	0	0
		/RESET and WDT	U	U	U	U	0	0	0	0
		Wake-up from Pin Change	U	U	U	U	P	P	P	P

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0C	IOCC	Bit Name	-	-	-	-	-	T1E	T1P1	T1P0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x0D	IOCD	Bit Name	S7	-	-	-	/PU9	/PU8	/PU6	/PU5
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x0E	IOCE	Bit Name	-	ODE	WTE	SLPC	ROC	-	-	/WUE
		Power-on	U	0	1	1	0	U	U	1
		/RESET and WDT	U	0	1	1	0	U	U	1
		Wake-up from Pin Change	U	P	1	1	P	U	U	P
0x0F	IOCF	Bit Name	-	-	-	-	T1IE	SPIIE	EXIE	TCIE
		Power-on	U	U	U	U	0	0	0	0
		/RESET and WDT	U	U	U	U	0	0	0	0
		Wake-up from Pin Change	U	U	U	U	P	P	P	P
0x0F~0x3E	GPR	Bit Name	-	-	-	-	-	-	-	-
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P

**To execute the next instruction after the "SLPC" bit status of IOCE register being on high-to-low transition.

U: Unknown or don't care **X:** Not used **–:** Not defined

P: Previous value before reset **t:** Check Table 7

5.7.1 The Status of RST, T, and P of STATUS Register

A reset condition is initiated by the following events:

1. Power-on condition
2. Watchdog timer time-out

The values of T and P, listed in Table 7 are used to check how the processor wakes up.

Table 8 shows the events that may affect the status of T and P.

Table 7 The Values of RST, T and P After RESET

Reset Type	T	P
Power on	1	1
WDT during Operating mode	0	P
WDT wake-up during Sleep 1 mode	0	0
WDT wake-up during Sleep 2 mode	0	P
Wake-Up on pin change during Sleep 2 mode	P	P

*P: Previous value before reset

Table 8 The Status of RST, T and P Being Affected by Events

Event	T	P
Power on	1	1
WDTC instruction	1	1
WDT time-out	0	*P
SLEP instruction	1	0
Wake-up on pin change during Sleep 2 mode	P	P

*P: Previous value before reset

5.8 Interrupt

The EM78452 has the following interrupts.

1. /TCC overflow interrupt

2. External interrupt (/INT)

3. Serial Peripheral Interface (SPI) transmission completed interrupt.

4. Timer 1 overflow interrupt.

R3F is the interrupt status register, which records the interrupt request in flag bit. IOCF is the interrupt mask register. Global interrupt is enabled by ENI instruction and is disabled by DISI instruction. When one of the interrupts (if enabled) is generated, it will cause the next instruction to be fetched from address 001H. Once in the interrupt service routine the source of the interrupt can be determined by polling the flag bits in the R3F register. The interrupt flag bit must be cleared by software before leaving the interrupt service routine and enabling interrupts to avoid recursive interrupts.

The flag in the Interrupt Status Register (R3F) is set regardless of the status of its mask bit or the execution of ENI instruction. Note that reading R3F will obtain the output of logic AND of R3F and IOCF (refer to Fig. 5-16). The RETI instruction exits the interrupt routine and enables the global interrupt (execution of ENI instruction).

When an interrupt is generated by INT instruction (if enabled), it causes the next instruction to be fetched from address 002H.

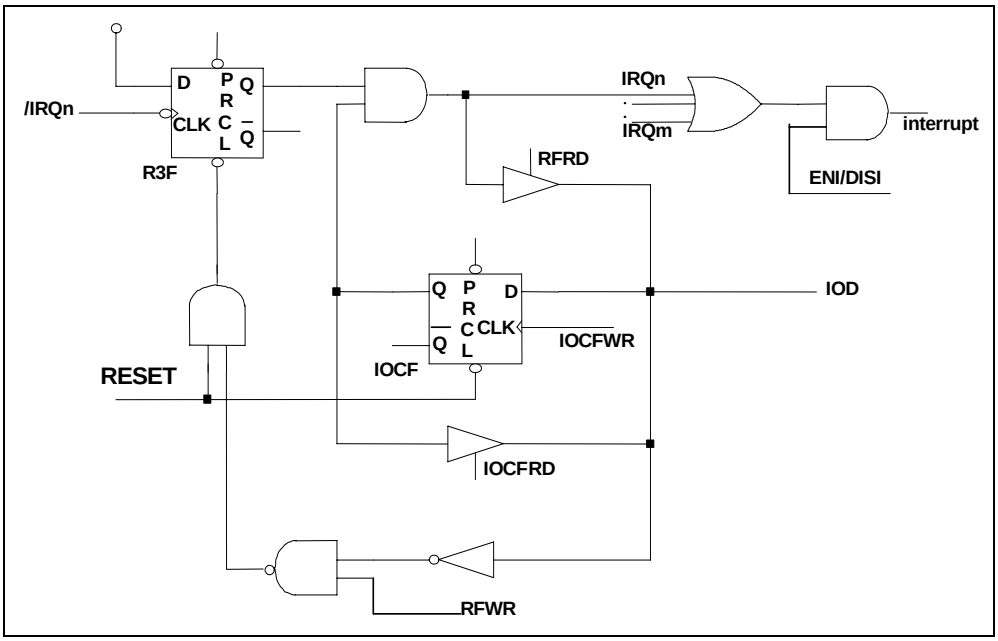


Fig. 5-16 Interrupt Input Circuit

5.9 Oscillator

5.9.1 Oscillator Modes

The EM78452 can only operate in high Crystal oscillator mode.

5.9.2 Crystal Oscillator/Ceramic Resonators (Crystal)

EM78452 can be driven by an external clock signal through the OSCI pin as shown in Fig 5-18. In most applications, pin OSCI and pin OSCO is connected with a crystal or ceramic resonator to generate oscillation. Fig. 5-18 depicts such circuit. Table 9 provides the recommended values of C1 and C2. Since each resonator has its own attribute, user should refer to its specification for appropriate values of C1 and C2. RS, a serial resistor may be necessary for AT strip cut crystal or low frequency mode.

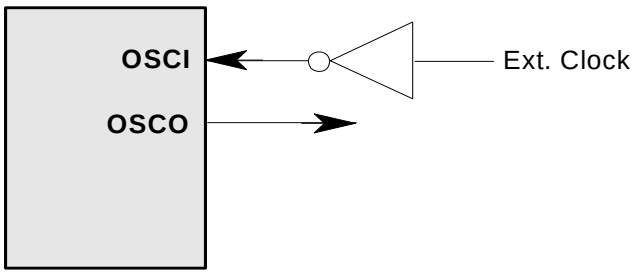


Fig. 5-17 Circuit for External Clock Input

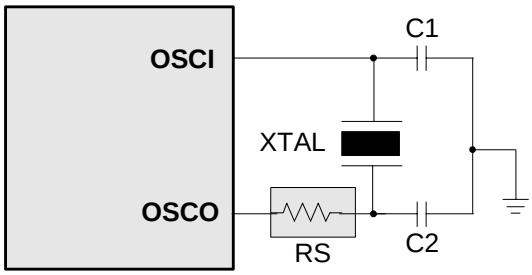


Fig. 5-18 Circuit for Crystal/Resonator

Table 10 Capacitor Selection Guide for Crystal Oscillator Ceramic Resonators

Oscillator Type	Frequency Mode	Frequency	C1 (pF)	C2 (pF)
Ceramic Resonator	HXT		10~150	10~150
		1.0 MHz	40~80	40~80
		2.0 MHz	20~40	20~40
		4.0 MHz	10~30	10~30
Crystal Oscillator	HXT		20~40	20~150
		1.0 MHz	15~30	15~30
		2.0 MHz	15	15

Fig. 5-19 Circuit for External R, Internal C Oscillator Mode

5.10 Code Option Register :

Word 0

Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ENWDT	CLKS	SPIHSK	REN	SDOS	WUTT

Bit 5 (ENWDT): Watchdog Timer enabled.

0: Enable

1: Disable

Bit 4 (CLKS): Clocks of each instruction cycle.

0: Two clocks

1: Four clocks

Bit 3 (SPIHSK): SPI handshake enable bit

0: enable SPI handshake function. When this bit is set to “0.” In SPI Slave mode, after SPI control register bit 4(SSE) is set to “1” it will send a high level through P91 (SRDY). Inform the “master” that the “Slave” is ready.

1: disable SPI handshake function

Bit 2 (REN): reset pin enable bit

0: enable, P70/reset → reset pin

1: disable, P70/reset → P70

Bit 1(SDOS): Serial data output status select bit

0: enable, SDOC Function enable.,

1: disable, SPI Function, the same as EM78452 waveform.

Bit 0 (WUTT): Wake up Trigger Type

0: Wake up trigger method as EM78P156 (Edge Trigger)

1: Wake up trigger as before (Low Level Trigger).

5.11 Instruction Set

Each instruction in the instruction set is a 13-bit word divided into an OP code and it includes one or more operands. All instructions are executed within one single instruction cycle (consisting of 2 oscillator periods), unless the program counter is changed by:

(a) Executing the instruction "MOV R2,A", "ADD R2,A", "TBL", or any other instructions that write to R2 (e.g. "SUB R2,A", "BS R2,6", "CLR R2", ····).

(b) execute CALL, RET, RETI, RETL, JMP, Conditional skip (JBS, JBC, JZ, JZA, DJZ, DJZA) which were tested to be true.

Under these cases, the execution takes two instruction cycles.

In addition, the instruction set has the following features:

(1). Every bit of any register can be set, cleared, or tested directly.

(2). The I/O register can be regarded as general register. That is, the same instruction can operate on I/O register.

Convention:

R = Register designator that specifies which one of the registers (including operation and general purpose registers) is to be utilized by the instruction.

b = Bit field designator that selects the value for the bit located in the register R and which affects the operation.

k = 8 or 10-bit constant or literal value

Binary Instruction	Hex	Mnemonic	Operation	Status Affected
0 0000 0000 0000	0000	NOP	No Operation	None
0 0000 0000 0001	0001	DAA	Decimal Adjust A	C
0 0000 0000 0010	0002	CONTW	A → CONT	None
0 0000 0000 0011	0003	SLEP	0 → WDT, Stop oscillator	T, P
0 0000 0000 0100	0004	WDTC	0 → WDT	T, P
0 0000 0000 rrrr	000r	IOW R	A → IOCR	None [1]
0 0000 0001 0000	0010	ENI	Enable Interrupt	None
0 0000 0001 0001	0011	DISI	Disable Interrupt	None
0 0000 0001 0010	0012	RET	[Top of Stack] → PC	None
0 0000 0001 0011	0013	RETI	[Top of Stack] → PC, Enable Interrupt	None
0 0000 0001 0100	0014	CONTR	CONT → A	None
0 0000 0001 rrrr	001r	IOR R	IOCR → A	None [1]
0 0000 0010 0000	0020	TBL	R2+A → R2, Bits 8~9 of R2 unchanged	Z, C, DC
0 0000 01rr rrrr	00rr	MOV R,A	A → R	None
0 0000 1000 0000	0080	CLRA	0 → A	Z
0 0000 11rr rrrr	00rr	CLR R	0 → R	Z
0 0001 00rr rrrr	01rr	SUB A,R	R-A → A	Z, C, DC
0 0001 01rr rrrr	01rr	SUB R,A	R-A → R	Z, C, DC
0 0001 10rr rrrr	01rr	DECA R	R-1 → A	Z
0 0001 11rr rrrr	01rr	DEC R	R-1 → R	Z
0 0010 00rr rrrr	02rr	OR A,R	A ∨ VR → A	Z
0 0010 01rr rrrr	02rr	OR R,A	A ∨ VR → R	Z
0 0010 10rr rrrr	02rr	AND A,R	A & R → A	Z
0 0010 11rr rrrr	02rr	AND R,A	A & R → R	Z
0 0011 00rr rrrr	03rr	XOR A,R	A ⊕ R → A	Z
0 0011 01rr rrrr	03rr	XOR R,A	A ⊕ R → R	Z
0 0011 10rr rrrr	03rr	ADD A,R	A + R → A	Z, C, DC
0 0011 11rr rrrr	03rr	ADD R,A	A + R → R	Z, C, DC
0 0100 00rr rrrr	04rr	MOV A,R	R → A	Z
0 0100 01rr rrrr	04rr	MOV R,R	R → R	Z

Binary Instruction	Hex	Mnemonic	Operation	Status Affected
0 0100 10rr rrrr	04rr	COMA R	/R → A	Z
0 0100 11rr rrrr	04rr	COM R	/R → R	Z
0 0101 00rr rrrr	05rr	INCA R	R+1 → A	Z
0 0101 01rr rrrr	05rr	INC R	R+1 → R	Z
0 0101 10rr rrrr	05rr	DJZA R	R-1 → A, skip if zero	None
0 0101 11rr rrrr	05rr	DJZ R	R-1 → R, skip if zero	None
0 0110 00rr rrrr	06rr	RRCA R	R(n) → A(n-1), R(0) → C, C → A(7)	C
0 0110 01rr rrrr	06rr	RRC R	R(n) → R(n-1), R(0) → C, C → R(7)	C
0 0110 10rr rrrr	06rr	RLCA R	R(n) → A(n+1), R(7) → C, C → A(0)	C
0 0110 11rr rrrr	06rr	RLC R	R(n) → R(n+1), R(7) → C, C → R(0)	C
0 0111 00rr rrrr	07rr	SWAPA R	R(0-3) → A(4-7), R(4-7) → A(0-3)	None
0 0111 01rr rrrr	07rr	SWAP R	R(0-3) ↔ R(4-7)	None
0 0111 10rr rrrr	07rr	JZA R	R+1 → A, skip if zero	None
0 0111 11rr rrrr	07rr	JZ R	R+1 → R, skip if zero	None
0 100b bbrr rrrr	0xxx	BC R,b	0 → R(b)	None [2]
0 101b bbrr rrrr	0xxx	BS R,b	1 → R(b)	None [3]
0 110b bbrr rrrr	0xxx	JBC R,b	if R(b)=0, skip	None
0 111b bbrr rrrr	0xxx	JBS R,b	if R(b)=1, skip	None
1 00kk kkkk kkkk	1kkk	CALL k	PC+1 → [SP], (Page, k) → PC	None
1 01kk kkkk kkkk	1kkk	JMP k	(Page, k) → PC	None
1 1000 kkkk kkkk	18kk	MOV A,k	k → A	None
1 1001 kkkk kkkk	19kk	OR A,k	A ∨ k → A	Z
1 1010 kkkk kkkk	1Akk	AND A,k	A & k → A	Z
1 1011 kkkk kkkk	1Bkk	XOR A,k	A ⊕ k → A	Z
1 1100 kkkk kkkk	1Ckk	RETL k	k → A, [Top of Stack] → PC	None
1 1101 kkkk kkkk	1Dkk	SUB A,k	k-A → A	Z, C, DC
1 1110 0000 0010	1E02	INT	PC+1 → [SP], 002H → PC	None
1 1111 kkkk kkkk	1Fkk	ADD A,k	k+A → A	Z, C, DC

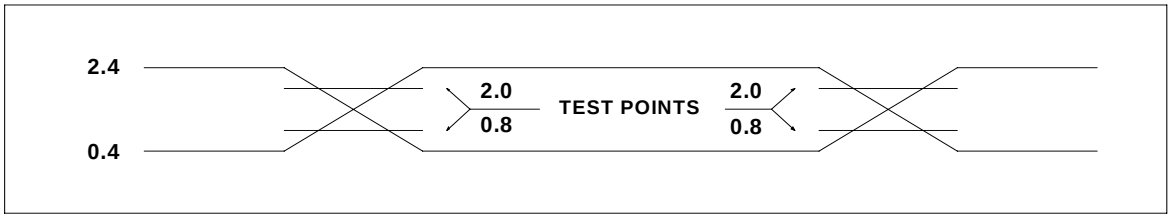
Note: [1] This instruction is applicable to IOC5~IOC9, IOCD ~ IOCF only.

[2] This instruction is not recommended for RF operation.

[3] This instruction cannot operate on R3F.

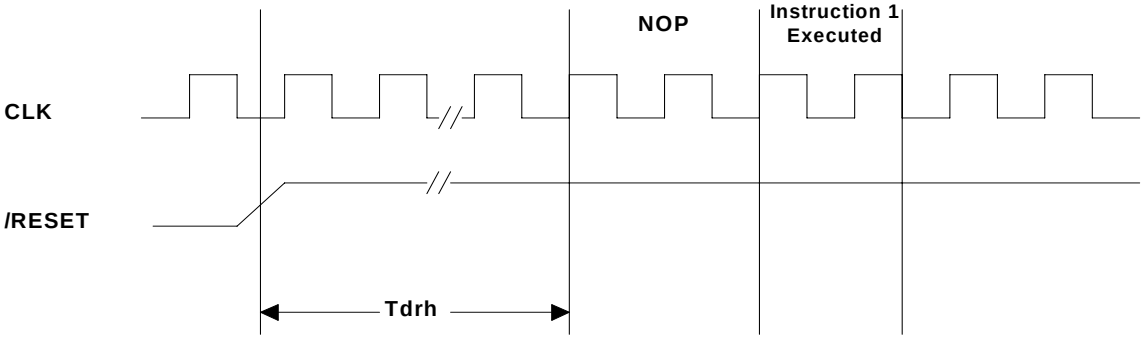
5.12 Timing Diagrams

AC Test Input/Output Waveform

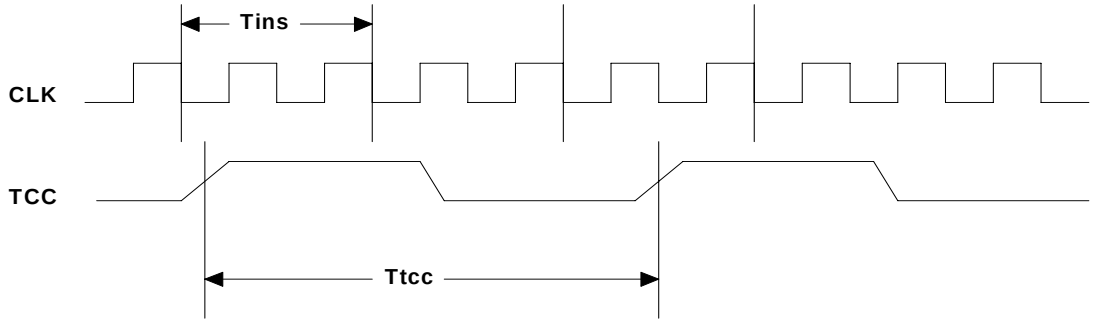


AC Testing : Input is driven at 2.4V for logic "1",and 0.4V for logic "0".Timing measurements are made at 2.0V for logic "1",and 0.8V for logic "0".

RESET Timing (CLK="0")



TCC Input Timing (CLKS="0")



6 Absolute Maximum Rating

Items	Rating		
Temperature under bias	0°C	to	70°C
Storage temperature	-65°C	to	150°C
Input voltage	-0.3V	to	+6.0V
Output voltage	-0.3V	to	+6.0V
Operating Frequency (2clk)	DC	to	20MHz

7 Electrical Characteristics

7.1 DC Characteristic

Ta=25°C, VDD=5V±5%, VSS=0V

Symbol	Parameter	Condition	Min	Typ	Max	Unit
FXT	Crystal VDD to 1.8V	Two clocks	DC	–	4	MHz
	Crystal VDD to 3.3V		DC	–	16	
	Crystal VDD to 5V		DC	–	20	
IIL	Input Leakage Current	VIN = VDD, VSS	–	–	±1	μA
VIH1	Input High Voltage VDD=5V)	–	2.0	–	–	V
VIL1	Input Low Voltage (VDD=5V)	–	–	–	0.8	V
VIHX1	Clock Input High Voltage (VDD=5V)	OSCI	2.5	–	–	V
VILX1	Clock Input Low Voltage (VDD=5V)	OSCI	–	–	1.0	V
VIHT1	Input high threshold voltage (Schmitt trigger)	P70/RESET pin	2.0	–	–	V
VILT1	Input low threshold voltage (Schmitt trigger)	P70/RESET pin	–	–	0.8	V
VIH2	Input High Voltage (VDD=3V)	–	1.5	–	–	V
VIL2	Input Low Voltage (VDD=3V)	–	–	–	0.4	V
VIHX2	Clock Input High Voltage (VDD=3V)	OSCI	1.5	–	–	V
VILX2	Clock Input Low Voltage (VDD=3V)	OSCI	–	–	0.6	V
VOH1	Output High Voltage (Ports 5, 6, 8, P74~P77, P90~P92, P95~P97,)	IOH = -12.0mA	2.4	–	–	V
VOH2	Output High Voltage (P70~P72)	S7=1 (IOCD Register Bit 7), IOH = -9.0mA	2	2.4	–	V
		S7=0 (IOCD Register Bit 7), IOH = -12.0mA	2.4	–	–	
VOH3	Output High Voltage (P93/SDO, P94/SCK)	IOH = -12.0mA	2.4	–	–	V

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VOL1	Output Low Voltage (Ports 5, 6, 8, P74~P77, P90~P92, P95~P97)	IOL =12.0mA	–	–	0.4	V
VOL2	Output Low Voltage (P70~P72)	S7=1 (IOCD Register Bit 7), IOH = 9.0mA	–	0.4	0.8	V
		S7=0 (IOCD Register Bit 7), IOH = 12.0mA	–	–	0.4	
VOL3	Output Low Voltage (P93/SDO, P94/SCK)	IOL = 12.0mA	–	–	0.4	V
VOL4	Output Low Voltage (P74~P77)	IOL = 15.0mA	–	–	0.4	–
IPH	Pull-high current	Pull-high active, input pin at VSS	-50	-100	-240	μA
IPH2	Pull-high current (P74,P75)	Pull-high active, input pin at VSS	–	1	–	mA
IPH3	Pull high current (P70/RESET)	Pull-high active, input pin at VSS	-16	-22	-29	μA
ISB	Power down current	All input and I/O pin at VDD, output pin floating, WDT enabled	–	–	10	μA
ICC	Operating supply current	/RESET="High", Fosc=1.84324MHz (CK2="0"), output pin floating	–	–	3	mA

6.2 AC Characteristic

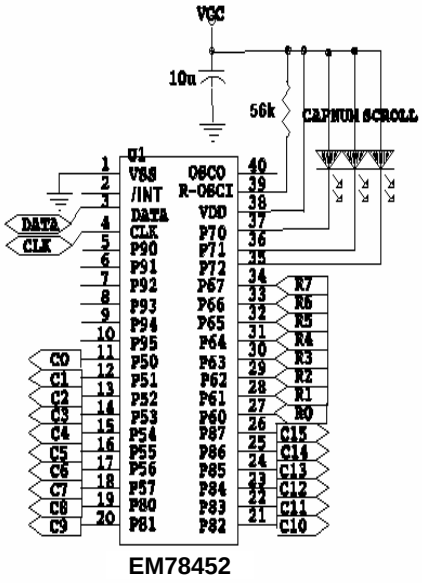
Ta=0°C~70°C, VDD=5V±5%, VSS=0V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Dclk	Input CLK duty cycle	–	45	50	55	%
Tins	Instruction cycle time (CK2="0")	RC Type	500	–	DC	ns
Ttcc	TCC input period	–	(Tins+20)/N*	–	–	ns
Twdt	Watchdog timer period	Ta=25°C	–	18	–	ms
Tdrh	Device reset hold period	Ta=25°C	–	18[3]	–	ms

*N= selected prescaler ratio.

[3] Vdd = 5V, set up time period = 16.2ms ± 30%
Vdd = 3V, set up time period = 18.0ms ± 30%

8 Application Circuit



EM78452

	R0	R1	R2	R3	R4	R5	R6	R7
C0			058				064	
C1		044					057	
C2	110	016	001	002	017	031	046	
C3	045	030	112	003	018	032	047	
C4	115	114	113	004	019	033	048	
C5	035	021	006	005	020	034	049	050
C6	036	022	007	008	023	037	052	051
C7		118	119	010	025	039	054	
C8	116	015	120	121		029	043	061
C9	117	028	013	009	024	038	053	
C10	041	027	012	011	026	040	042	055
C11		092	076	122	091	093	090	084
C12	099	097	075	123	096	098	095	089
C13	104	102	085	086	101	103	100	105
C14	083		080	081	106	108	126	079
C15	060			124	125			062

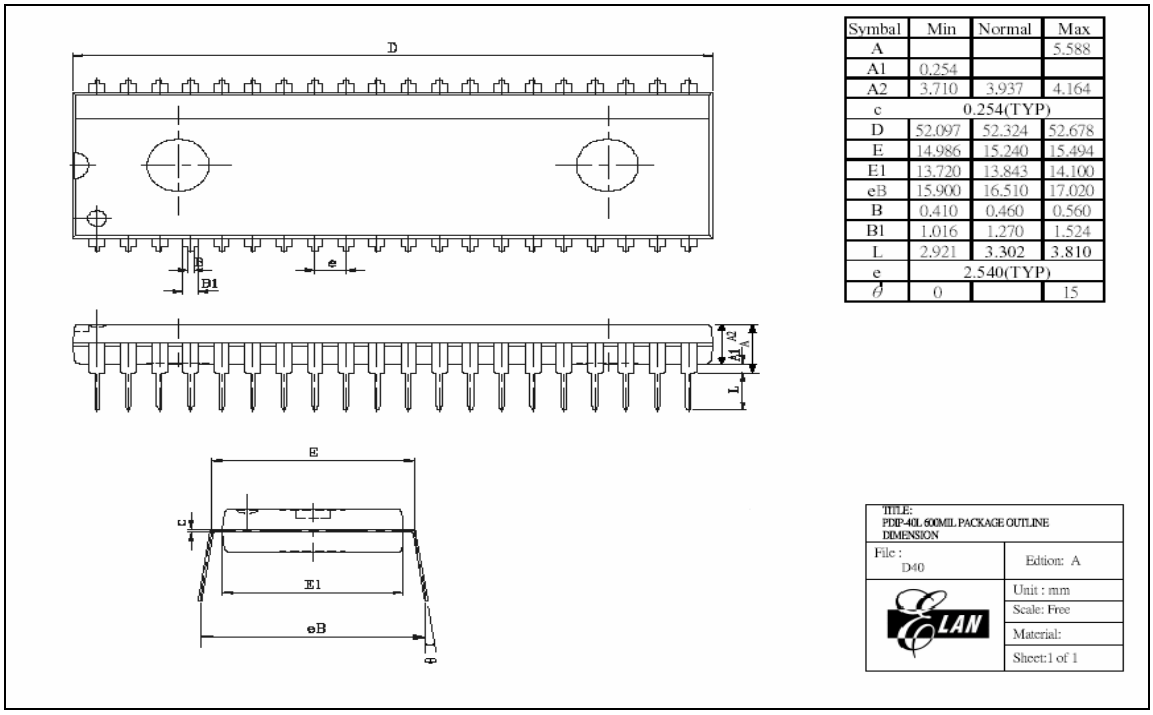
APPENDIX

A Package Type:

OTP MCU	Package Type	Pin Count	Package Size
EM78452P	DIP	40	600 mil
EM78452WM	SOP	40	450 mil
EM78452AQ	QFP	44	

B Package Information

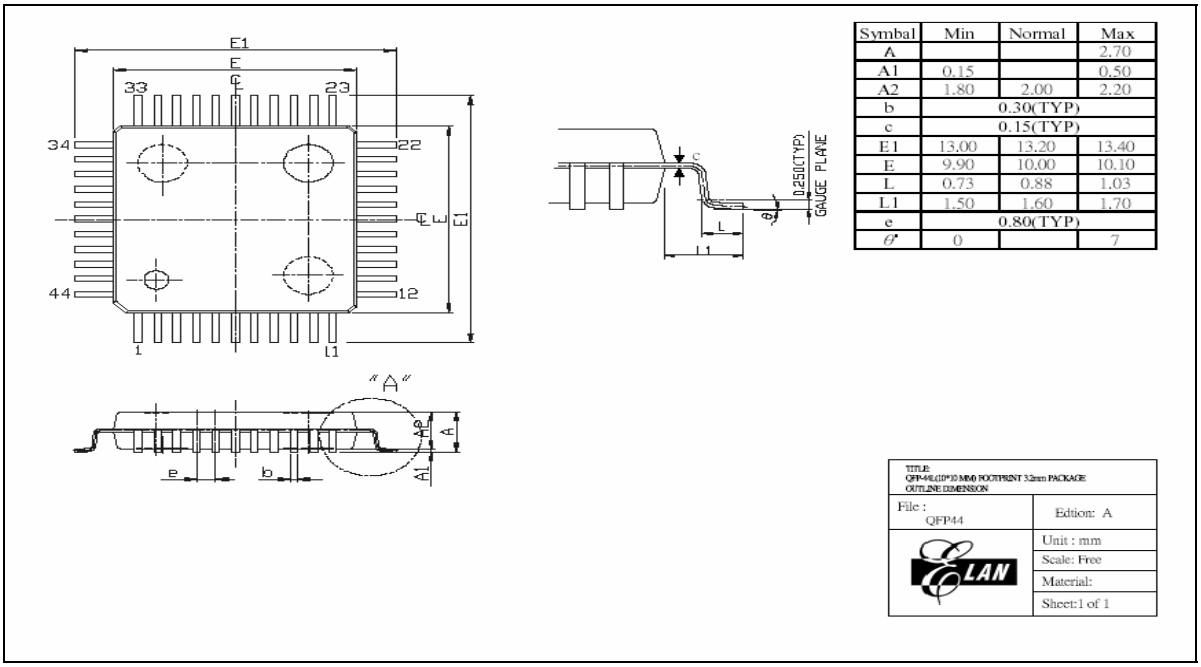
B.1 40-Lead Plastic Dual in line (PDIP) — 600 mil



Symbal	Min	Normal	Max
A			5.588
A1	0.254		
A2	3.710	3.937	4.164
c		0.254(TYP)	
D	52.097	52.324	52.678
E	14.986	15.240	15.494
E1	13.720	13.843	14.100
eB	15.900	16.510	17.020
B	0.410	0.460	0.560
B1	1.016	1.270	1.524
L	2.921	3.302	3.810
e		2.540(TYP)	
θ	0		15

TITLE: PDIP-40L 600MIL PACKAGE OUTLINE DIMENSION	
File : D40	Edtion: A
	Unit : mm
	Scale: Free
	Material:
	Sheet:1 of 1

B.2 44-Lead Quad Flat Package (QFP)



Symbal	Min	Normal	Max
A			2.70
A1	0.15		0.50
A2	1.80	2.00	2.20
b		0.30(TYP)	
c		0.15(TYP)	
E1	13.00	13.20	13.40
E	9.90	10.00	10.10
L	0.73	0.88	1.03
L1	1.50	1.60	1.70
e		0.80(TYP)	
θ°	0		7

TITLE: QFP-44L(10*10 MM) FOOTPRINT 3.2mm PACKAGE OUTLINE DIMENSION	
File : QFP44	Edtion: A
	Unit : mm
	Scale: Free
	Material:
	Sheet:1 of 1