EM78568

8-Bit Microcontroller for FRS

Product Specification

DOC. VERSION 3.6

ELAN MICROELECTRONICS CORP.

February 2005

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APPENDIX

Specification Revision History

Version	Revision Description	Date
1.0	Initial version	2002/01/04
1.1	Updated the description of errors	2002/01/07
1.2	Updated the description	2002/01/10
1.3	Revised the operating voltage for DAC and CTCSS	2002/01/11
1.4	Changed the package and pin configuration	2002/04/09
1.5	1. Removed the CTCSS VOX function 2. Added the Microphone Amp mute function 3. Changed the RE PAGE1 default value from 0x00 to 0xFF 4. Changed the CTCSS tone generation channel 19 setting	2002/04/12
1.6	1. Updated the description of the "program ROM" form 32kx13 ➔ 16kx13 2. Updated the "register configuration" table	2002/04/15
1.7	1. Added LCD waveform option bit in the code option. The new two option : select LCD waveform as Type0 or Type1.	2002/06/10
1.8	1. Changed P73 interrupt setting from INT2 to INT3 2. Updated the pin configuration and pin description 3. Updated the relative RF, IOCF register bit description 4. Changed the feature description for the interrupt numbers	2002/09/23
2.0	1. Added item 1 and 2 in the user application note (see user application note) 2. Clarified the "undefined bits" descriptions. Not allowed to use undefined bits. 3. Added LCD Type0 and Type1 waveforms	2002/10/04
2.1	1. Reduced the data RAM from 1k to 0.5k. Removed R7 PAGE1 bit1. 2. Relayout the chip to fit 100-pin compatible with EM78P568 3. Combined A/B version distinction	2002/10/29
2.2	1. Fixed the bug in the application note 2. Added extra notice in the application	2002/10/31
2.3	Revised the current consumption of the DC electrical characteristic	2002/11/06
2.4	Revised the test condition of electrical characteristic	2002/11/07
2.5	1. Updated the operating voltage of the Comparator, DAC and CTCSS block in the feature description 2. Added DC voltage characteristic for 2.5VREF 3. Revised the sleep current max value from 8μA to 5μA 4. Added description in the user application note	2002/11/22
2.6	1. Added DC characteristic under VDD=3V for 2.5VREF 2. Updated the description in the user application note	2002/11/26
2.7	1. Updated the DC characteristic 2. Fixed the code option 3. Removed /POVD function 4. Updated the user application note	2002/11/29
2.8	Revised the waveform of the LCD 1/4 duty for Type 1	2003/01/15

2.9	1. Removed the waveform of the LCD for Type0 2. Updated the DC characteristic for driver/sink current	2003/02/26
3.0	1. Revised the description in the operating current for analog circuit 2. Revised the dB to dBm on level for CTCSS tone to MTX	2003/10/24
3.5	Revised the current consumption of DC electrical characteristic	2004/07/28
3.6	Revised the test condition of the electrical characteristic	2005/02/02

1 General Description

The EM78568 is an 8-bit RISC type microprocessor with low power, high speed CMOS technology. This integrated single chip has an on-chip watchdog timer (WDT), program ROM, data RAM, LCD driver, programmable real time clock/counter, internal interrupt, power down mode, built-in 8-bit D/A converter, 5-bit Comparator, DAC tone generator, CTCSS analog circuit, programming dual tone generator and tri-state I/O.

2 Feature

2.1 CPU

- Operating voltage : 2.2V ~ 5.5V
- 16k x 13 program ROM
- 0.5k x 8 on chip data RAM
- Up to 36 bi-directional tri-state I/O ports
- 16 level stack for subroutine nesting
- 8-bit real time clock/counter (TCC)
- two 8-bit counters : COUNTER1 and COUNTER2
- On-chip watchdog timer (WDT)
- 99.9% single instruction cycle commands
- Four modes (Main clock can be programmed from 447.829k to 17.913MHz generated by internal PLL)

Mode	CPU Status	Main clock	32.768kHz Clock Status
Sleep mode	Turn off	Turn off	Turn off
Idle mode	Turn off	Turn off	Turn on
Green mode	Turn on	Turn off	Turn on
Normal mode	Turn on	Turn on	Turn on

- Input port interrupt function
- 8 interrupt source, 4 external , 4 internal
- Dual clock operation (Internal PLL main clock , External 32.768kHz)

2.2 PROGRAMMING TONE GENERATORS

- Operating voltage: 2.2V ~ 5.5V
- Programming Tone1 and Tone2 dual tone generators
- 11-bit Programming Tone1 generators
- 8-bit Programming Tone2 generator

2.3 COMPARATOR

- Operating voltage: 2.7V ~ 5.5V
- 3-channel input
- 5-bit comparison reference level setting
- Internal (2.5V or VDD) or external reference level

2.4 DAC

- Operating: 2.7V ~ 5.5V
- 8-bit R-2R D/A converter
- 8-bit programmable tone output
- Easy to direct access as programmable CTCSS tone output by DAC tone generator
- Internal (2.5V or VDD) or external reference level

2.5 CTCSS block

- Operating voltage : 2.7V ~ 5.5V
- Microphone amplifier (can be used as general OP Amp)
- Microphone mute function
- RX input OP
- Audio BPF (300Hz ~ 3400Hz)
- Sub-audio LPF (60Hz ~ 253Hz) for CTCSS tone detection
- Zero-crossing for detected CTCSS tone frequency output
- CTCSS Tx modulation summing Amp

2.6 POVD

- Power-on voltage detector reset
- Without external reset circuit while enabling

2.7 LCD

- Common driver pins: 4
- Segment driver pins: 20
- 1/3 bias
- 1/4 duty, 1/2 duty
- 16 Level LCD contrast control by software

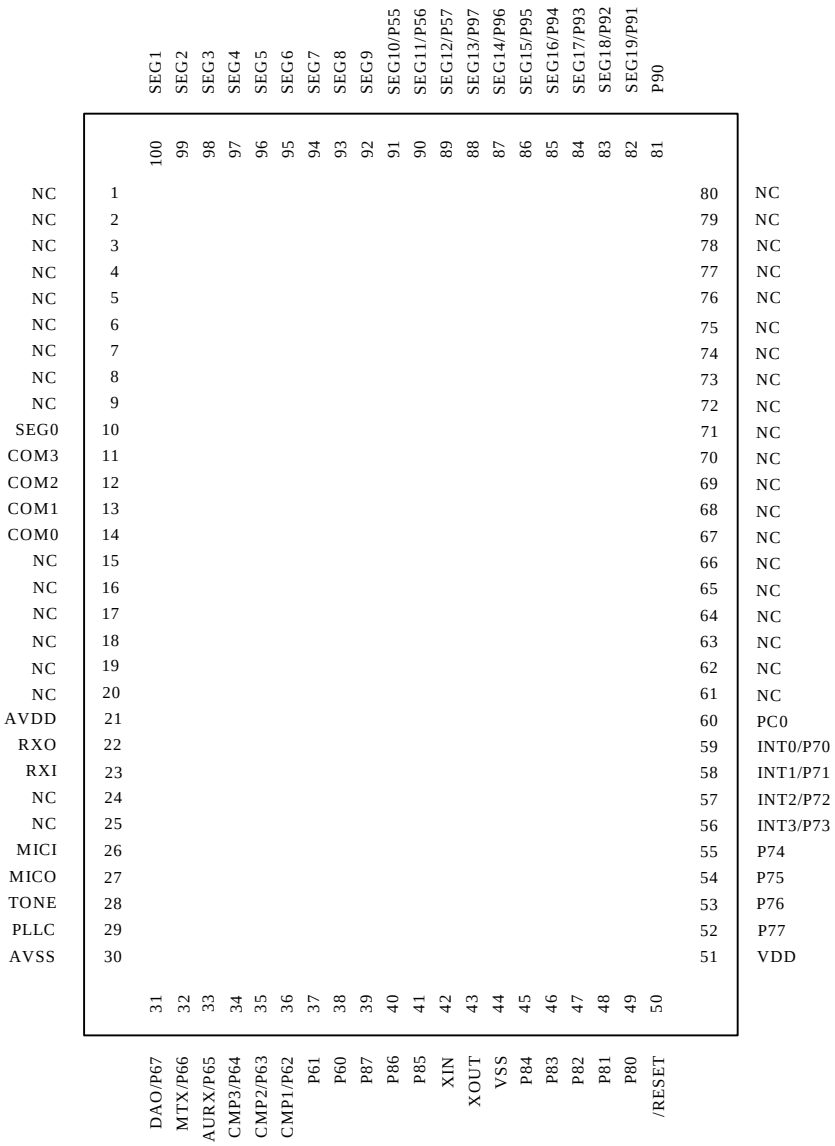
2.8 PACKAGE

- 100-pin QFP (EM78568Q)
- 63-pin die (EM78568H)

3 Application

FRS (Family Radio Systems) and other wireless portable products

4 Pin Configuration



100-pin QFP or 63-pin die
Fig.1b Pin Assignment

5 Functional Block Diagram

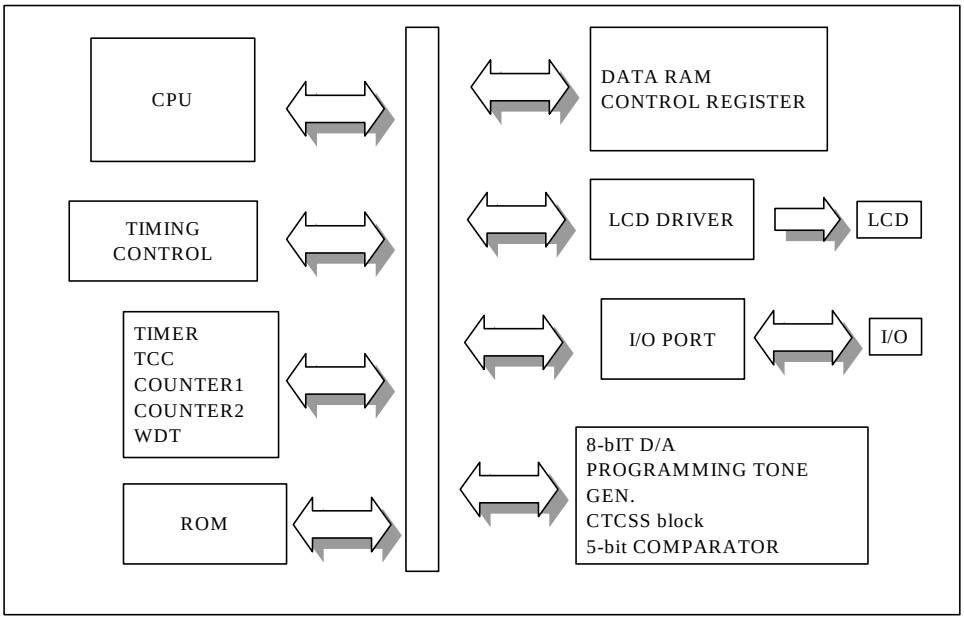


Fig.2a Block diagram

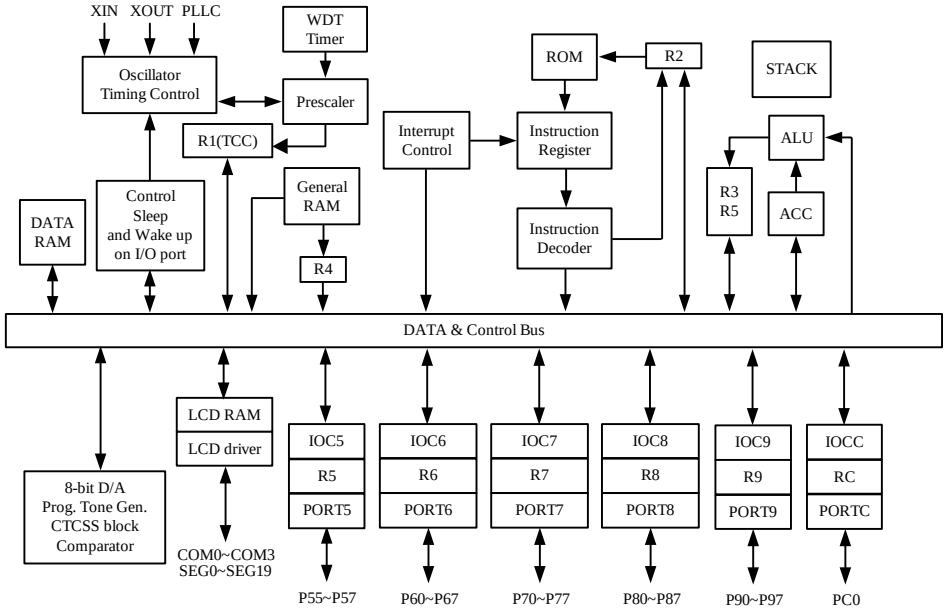


Fig.2b Block diagram

6 Pin Descriptions

PIN	I/O	DESCRIPTION
POWER		
VDD AVDD	POWER	Digital power Analog power
VSS AVSS	POWER	Digital ground Analog ground
CLOCK		
XIN	I	Input pin for 32.768 kHz oscillator
XOUT	O	Output pin for 32.768 kHz oscillator
PLLC	I	Phase loop lock capacitor, connect a capacitor 0.01µ to 0.047µ to the ground.
LCD		
COM0 ~ COM3	O	Common driver pins of LCD drivers
SEG0 ~ SEG9 SEG10 ~ SEG12 SEG13 ~ SEG19	O O (I/O : PORT5) O (I/O : PORT9)	Segment driver pins of LCD drivers SEG10 to SEG19 are shared with IO PORT.
Programming tone generators		
TONE	O	Programming single tone or dual tone output
Comparator		
CMP1 CMP2 CMP3	I (P62) I (P63) I (P64)	Comparator input pins, shared with PORT62, PORT63 and PORT64.
8-bit D/A		
DAO	O (P67)	D/A converter output pin Shared with PORT67
CTCSS		
MICO	O	Microphone amplifier output. Put a feedback resistor to adjust the gain
MICI	I	Microphone amplifier input
RXO	O	Receiver amplifier output. Put a feedback resistor to adjust the gain
RXI	I	Receiver amplifier input
AURX	O (P65)	Receiving audio output Share with PORT65
MTX	O (P66)	Modulation transmission output for CTCSS tone Shared with PORT66
IO		
P55~P57	I/O	Each bit on PORT5 can be INPUT or OUTPUT port PORT5 (7:5) are shared with LCD Segment signal
P60 ~P67	I/O	Each bit on PORT6 can be INPUT or OUTPUT

PIN	I/O	DESCRIPTION
P70 ~ P77	I/O	Each bit on PORT7 can be INPUT or OUTPUT Internal Pull high function PORT7 (0~3) has interrupt function
P80 ~ P87	I/O	Each bit on PORT8 can be INPUT or OUTPUT Internal pull high PORT8 (0~3) have wake-up functions (set by RE PAGE0)
P90 ~ P97	I/O	Each bit on PORT9 can be INPUT or OUTPUT port PORT9 (1~7) are shared with LCD Segment signal
PC0	I/O	Each bit on PORTC can be INPUT or OUTPUT port
INT0	(PORT70)	Interrupt sources. Once PORT70 has a falling edge or rising edge signal (controlled by CONT register), it will generate an interrupt.
INT1	(PORT71)	Interrupt sources which have the same interrupt flag. Any pin from PORT71 has a falling edge signal, which will generate an interrupt.
INT2	(PORT72)	Interrupt sources which have the same interrupt flag. Any pin from PORT72 has a falling edge signal, which will generate an interrupt.
INT3	(PORT73)	Interrupt sources which have the same interrupt flag. Any pin from PORT73 has a falling edge signal, which will generate an interrupt.
/RESET	I	Low reset

7 Functional Descriptions

7.1 Operational Registers

Register Configuration

	R PAGE Registers		IOC PAGE Registers	
Addr	**R PAGE0**	**R PAGE1**	**IOC PAGE0**	**IOC PAGE1**
00	Indirect addressing			
01	TCC			
02	PC			
03	Page, Status			
04	RAM bank, RSR			
05	Port 5 I/O data, Program ROM page	LCD RAM address	Port 5 I/O control, LCD bias control	Comparator control
06	Port 6 I/O data	LCD RAM data buffer	Port 6 I/O control	Port 6 switches
07	Port 7 I/O data	CTCSS detection output, Data RAM bank	Port 7 I/O control	Port 7 pull high
08	Port 8 I/O data	Data RAM address	Port 8 I/O control	Port 8 pull high
09	Port 9 I/O data	Data RAM data buffer	Port 9 I/O control	Port 9 switches
0A	PLL, Main clock, Comparator flag, WDTE	DAC input data buffer	TONE 2 control	DAC control, 2.5V ref control
0B				
0C	Port C I/O data	Counter1 data	PortC I/O control	Port 5 switch
0D	LCD control	Counter2 data	TONE1 control	Clock source (CN1, CN2) Prescaler (CN1, CN2)
0E	Wake-up control,	DAC tone selection	TONE1 extra control,	CTCSS control switches
0F	Interrupt flag		Interrupt mask	
10	16 bytes Common Registers			
:				
1F				
20	Bank 0~Bank 3 Common Registers (32x8 for each bank)			
:				
3F				

7.2 Operational Register Detail Description

7.2.1 R0 (Indirect Addressing Register)

R0 is not a physically implemented register. It is used as indirect addressing pointer. Any instruction using R0 as register actually accesses data pointed by the RAM Select Register (R4).

Example:

MovA, @0x20; store an address at R4 for indirect addressing

Mov0x04, A

MovA, @0xAA; write data 0xAA to R20 at bank0 through R0

Mov0x00, A

7.2.2 R1 (TCC)

TCC data buffer; Increased by 16.384kHz or by the instruction cycle clock (controlled by CONT register).

Written and read by the program as any other register.

7.2.3 R2 (Program Counter)

The structure is depicted in Fig. 5.

Generates 16k × 13 on-chip PROGRAM ROM addresses to the relative programming instruction codes.

"JMP" instruction allows the direct loading of the low 10 program counter bits.

"CALL" instruction loads the low 10 bits of the PC, PC+1, and then push into the stack.

"RET" ("RETL k", "RETI") instruction loads the program counter with the contents at the top of stack.

"MOV R2,A" allows the loading of an address from the A register to the PC, and the ninth and tenth bits are cleared to "0".

"ADD R2,A" allows a relative address be added to the current PC, and contents of the ninth and tenth bits are cleared to "0".

"TBL" allows a relative address added to the current PC, and contents of the ninth and tenth bits don't change. The most significant bit (A10~A13) will be loaded with the contents of bit PS0~PS3 in the status register (R5 PAGE0) upon the execution of a "JMP", "CALL", "ADD R2, A", or "MOV R2, A" instruction.

If an interrupt is triggered, PROGRAM ROM will jump to address 0x08 at page0. The CPU will store ACC, R3 status and R5 PAGE automatically, and they will be restored after instruction RETI.

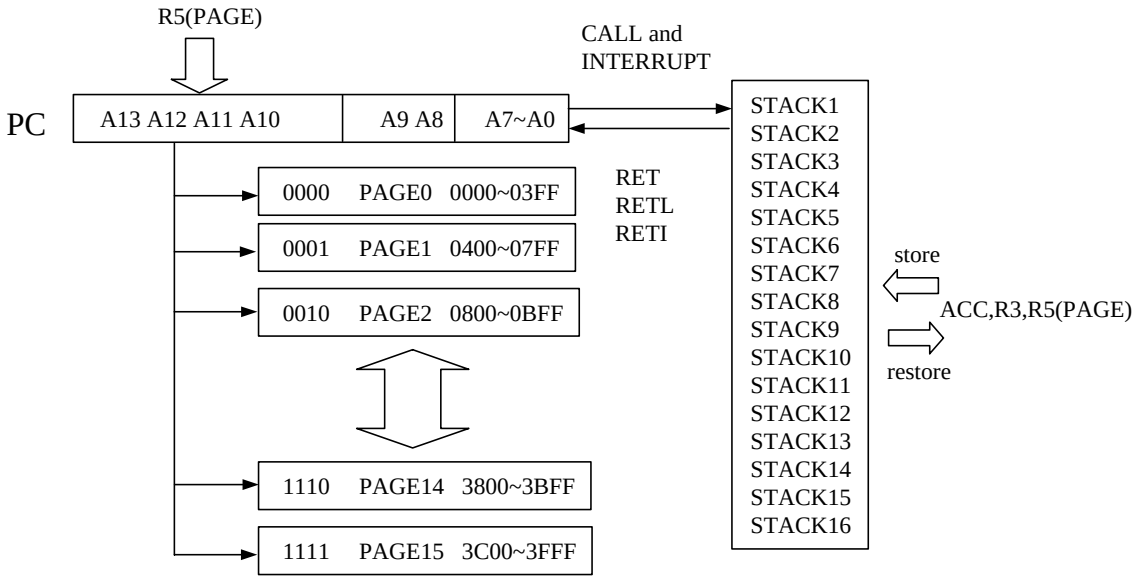


Fig.3 Program Counter Organization

7.2.4 R3 (Status, Page selection)

PAGE0 (Status flag, Page selection bits)

7	6	5	4	3	2	1	0
RPAGE2	RPAGE	IOCPAGE	T	P	Z	DC	C
R/W-0	R/W-0	R/W-0	R	R	R/W	R/W	R/W

Bit 0(C) : Carry flag

Bit 1(DC) : Auxiliary carry flag

Bit 2(Z) : Zero flag

Bit 3(P) : Power down bit

Set to 1 during power on or by a "WDTC" command and reset to 0 by a "SLEP" command.

Bit 4(T) : Time-out bit

Set to 1 by the "SLEP" and "WDTC" command, or during power up and reset to 0 by WDT timeout.

.EVENT	T	P	REMARK
WDT wake up from sleep mode	0	0	
WDT time out (not sleep mode)	0	1	

/RESET wake up from sleep	1	0	
Power up	1	1	
Low pulse on /RESET	x	x	x : don't care

Bit 5(IOCPAGE) : change IOC5 ~ IOCE to another page

Please refer to Fig.4 control register configuration for details.

0/1 ➔ page0 / page1

Bit 6(RPAGE) : change R5 ~ RE to another page

Refer to Fig.4 control register configuration for details.

0/1 ➔ page0 / page1

Bit 7(RPAGE2) : change R5 ~ RE to R page2 (keep this bit unchanged at "0")

0 ➔ The page for R5 ~ RE depends on Bit 6 (RPAGE)

1 ➔ change R5 ~ RE to page2

7.2.5 R4 (RAM selection for common registers R20 ~ R3F))

(RAM Selection Register)

7	6	5	4	3	2	1	0
RB1	RB0	RSR5	RSR4	RSR3	RSR2	RSR1	RSR0
R/W-0	R/W-0	R/W	R/W	R/W	R/W	R/W	R/W

Bit 0 ~ Bit 5 (RSR0 ~ RSR5) : Indirect addressing for common registers R20 ~ R3F

RSR bits are used to select up to 32 registers (R20 to R3F) in the indirect addressing mode.

Bit 6 ~ Bit 7 (RB0 ~ RB1) : Bank selection bits for common registers R20 ~ R3F

These selection bits are used to determine which bank is activated among the 4 banks of the 32 registers (R20 to R3F).

Refer to VII.1 Operational Registers for details.

7.2.6 R5 (PORT5 I/O data, Program page selection, LCD address)

7.2.6.1 PAGE0 (PORT5 I/O data register, Program page register)

7	6	5	4	3	2	1	0
P57	P56	P55	-	PS3	PS2	PS1	PS0
R/W	R/W	R/W		R/W-0	R/W-0	R/W-0	R/W-0

Bit 0 ~ Bit 3 (PS0 ~ PS3) : Program page selection bits

PS3	PS2	PS1	PS0	Program memory page (Address)
0	0	0	0	Page 0

0	0	0	1	Page 1
0	0	1	0	Page 2
0	0	1	1	Page 3
:	:	:	:	:
1	1	1	0	Page 14
1	1	1	1	Page 15

You can use PAGE instruction to change page to maintain program page by user. Otherwise, you can use far jump (FJMP) or far call (FCALL) instructions to program your code. And the program page is maintained by EMC's complier. It will change your program by inserting instructions within the program.

Bit 4 : (undefined) not allowed for use

Bit 5 ~ Bit 7 (P55 ~ P57) : 8-bit PORT5 (5~7) I/O data register

You can use the IOC register to define each bit as input or output.

7.2.6.2 PAGE1 (LCD address)

7	6	5	4	3	2	1	0
-	-	-	-	LCDA3	LCDA2	LCDA1	LCDA0
				R/W-0	R/W-0	R/W-0	R/W-0

Bit 0 ~ Bit 3 (LCDA0 ~ LCDA3) : LCD address for LCD RAM read or write

The address of the LCD RAM corresponds to the COMMON and SEGMENT signals as shown in the table.

COM3 ~ COM0	LCD Address (LCDA3 ~ LCDA0)
SEG1, SEG0	00H
SEG3, SEG2	01H
SEG5, SEG4	02H
SEG7, SEG6	03H
SEG9, SEG8	04H
SEG11, SEG10	05H
SEG13, SEG12	06H
SEG15, SEG14	07H
SEG17, SEG16	08H
SEG19, SEG18	09H

Bit 4 ~ Bit 7 : (undefined) not allowed for use

7.2.7 R6 (PORT6 I/O data, LCD data)

7.2.7.1 PAGE0 (PORT6 I/O data register)

7	6	5	4	3	2	1	0
P67	P66	P65	P64	P63	P62	P61	P60
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 0 ~ Bit 8 (P60 ~ P67) : 8-bit PORT6(0~7) I/O data register

You can use the IOC register to define each bit as input or output.

7.2.7.2 PAGE1 (LCD data)

7	6	5	4	3	2	1	0
LCDD7	LCDD6	LCDD5	LCDD4	LCDD3	LCDD2	LCDD1	LCDD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 0 ~ Bit 7 (LCDD0 ~ LCDD7) : LCD data buffer for LCD RAM read or write

LCD Data vs. COM-SEG		LCD Address
LCDD7 ~ LCDD4	LCDD3 ~ LCDD0	(LCDA3 ~ LCDA0)
COM3 ~ COM0	COM3 ~ COM0	
SEG1	SEG0	00H
SEG3	SEG2	01H
SEG5	SEG4	02H
SEG7	SEG6	03H
SEG9	SEG8	04H
SEG11	SEG10	05H
SEG13	SEG12	06H
SEG15	SEG14	07H
SEG17	SEG16	08H
SEG19	SEG18	09H

7.2.8 R7 (PORT7 I/O data, Data RAM bank)

7.2.8.1 PAGE0 (PORT7 I/O data register)

7	6	5	4	3	2	1	0
P77	P76	P75	P74	P73	P72	P71	P70
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 0 ~ Bit 7 (P70 ~ P77) : 8-bit PORT7 (0~7) I/O data register

You can use the IOC register to define each bit as input or output.

7.2.8.2 PAGE1 (VOX detection output, CTCSS detection output, Data RAM bank selection bit)

7	6	5	4	3	2	1	0
-	DETO	-	-	-	-	-	RAM_B0
	R						R/W-0

Bit 0 (RAM_B0) : Data RAM bank selection bit

Each bank has address 0 ~ address 255 which is total 256 (0.25k) bytes RAM size.

Data RAM bank selection : (Total RAM = 1.0K)

RAM_B1	RAM_B0	RAM bank
0	0	Bank0
0	1	Bank1
1	0	Bank2
1	1	Bank3

Bit 1 ~ Bit 5 : (undefined) not allowed to use

Bit 6(DETO) : CTCSS tone detection

The signal passing CTCSS sub audio LPF will be extracted CTCSS tone. Then this tone will go into the ZC(Zero-crossing detector) and output to DETO bit. This bit reflects the CTCSS tone frequency pulse waveform. The user can count the timing to get the CTCSS frequency. Also see IOCE PAGE1 for CTCSS block and switch control.

Bit 7 : (undefined) not allowed to use

7.2.9 R8 (PORT8 I/O data, Data RAM address)

7.2.9.1 PAGE0 (PORT8 I/O data register)

7	6	5	4	3	2	1	0
P87	P86	P85	P84	P83	P82	P81	P80
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 0 ~ Bit 7 (P80 ~ P87) : 8-bit PORT8(0~7) I/O data register

User can use IOC register to define input or output each bit.

7.2.9.2 PAGE1 (Data RAM address register)

7	6	5	4	3	2	1	0
RAM_A7	RAM_A6	RAM_A5	RAM_A4	RAM_A3	RAM_A2	RAM_A1	RAM_A0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0 ~ Bit 7 (RAM_A0 ~ RAM_A7) : data RAM address

The data RAM bank's selection is from R7 PAGE1 bit0 ~ bit 1 (RAM_B0 ~ RAM_B1).

7.2.10 R9 (PORT9 I/O data, Data RAM data buffer)

7.2.10.1PAGE0 (PORT9 I/O data register)

7	6	5	4	3	2	1	0
P97	P96	P95	P94	P93	P92	P91	P90
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 0 ~ Bit 7 (P90 ~ P97) : 8-bit PORT9(0~7) I/O data register

User can use IOC register to define input or output each bit.

7.2.10.2PAGE1 (Data RAM data register)

7	6	5	4	3	2	1	0
RAM_D7	RAM_D6	RAM_D5	RAM_D4	RAM_D3	RAM_D2	RAM_D1	RAM_D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 0 ~ Bit 7 (RAM_D0 ~ RAM_D7) : Data RAM's data

The address for data RAM is accessed from R8 PAGE1. The data RAM bank is selected by R7 PAGE1 Bit 0 ~ Bit 1 (RAM_B0 ~ RAM_B1).

7.2.11 RA (PLL, Main clock selection, Comparator flag, Watchdog timer, DAC input data buffer)

7.2.11.1PAGE0 (PLL enable bit, Main clock selection bits, Comparator control bits, Watchdog timer enable bit)

7	6	5	4	3	2	1	0
IDLE	PLLEN	CLK2	CLK1	CLK0	CMPFLAG	CMPREF	WDTEN
R/W-0	R/W-0	R/W-0	R/W-1	R/W-1	R	R/W-0	R/W-0

Bit 0(WDTEN) : Watch dog control bit

User can use WDTC instruction to clear watch dog counter. The counter 's clock source is 32768/2 Hz. If the prescaler assigns to TCC. Watch dog will time out by (1/32768)*2 * 256 = 15.616mS. If the prescaler assigns to WDT, the time of time out will be more times depending on the ratio of prescaler.

0/1 ➔ disable/enable

Bit 1(CMPREF) : Comparator's reference voltage source selection bit

0 ➔ Comparator's reference voltage is driven from internal bias resistor string. This reference voltage level can be set by RD PAGE0 bit 0 ~ bit 5 (CMP_B0 ~ CMP_B5).

1 ➔ Comparator's reference voltage is driven from external bias. This reference voltage input is CMP3/P65 pin. Also IOC6 PAGE1 bit 2(CMP63/P63) should be set to "1".

Bit 2(CMPFLAG) : Output of the comparator

0 ➔ Input voltage < reference voltage

1 ➔ input voltage > reference voltage

Bit 3 ~ Bit 5 (CLK0 ~ CLK2) : MAIN clock selection bits

User can choose different frequency of main clock by CLK1 and CLK2. All the clock selection is list below.

PLLEN	CLK2	CLK1	CLK0	Sub clock	MAIN clock	CPU clock
1	0	0	0	32.768kHz	447.829kHz	447.829kHz (Normal mode)
1	0	0	1	32.768kHz	895.658kHz	895.658kHz (Normal mode)
1	0	1	0	32.768kHz	1.791MHz	1.791MHz (Normal mode)
1	0	1	1	32.768kHz	3.582MHz	3.582MHz (Normal mode)
1	1	0	0	32.768kHz	7.165MHz	7.165MHz (Normal mode)
1	1	0	1	32.768kHz	10.747MHz	10.747MHz (Normal mode)
1	1	1	0	32.768kHz	14.331MHz	14.331MHz (Normal mode)
1	1	1	1	32.768kHz	17.913MHz	17.913MHz (Normal mode)
0	don't care		don't care	32.768kHz	don't care	32.768kHz (Green mode)

Bit 6(PLLEN) : PLL's power control bit which is CPU mode control register

0/1 ➔ disable PLL/enable PLL

If enable PLL, CPU will operate at normal mode (high frequency). Otherwise, it will run at green mode (low frequency, 32768 Hz).

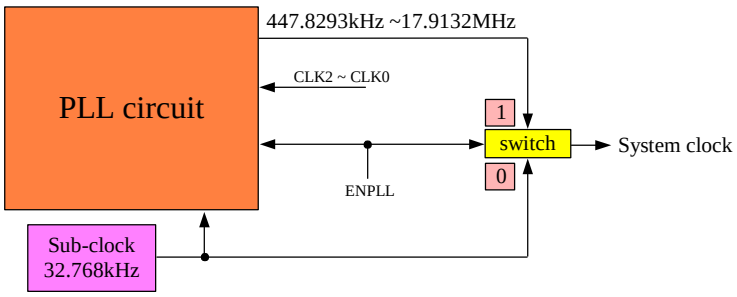


Fig.4 The relation between 32.768kHz and PLL

Bit 7(IDLE) : Sleep mode or IDLE mode control after using "SLEP" instruction.

0/1 ➔ SLEEP mode/IDLE mode.

This bit will decide SLEP instruction which mode to go.

The status after wake-up and the wake-up sources list as the table below.

Wakeup signal	SLEEP mode	IDLE mode
	RA(7,6)=(0,0) + SLEP	RA(7,6)=(1,0) + SLEP
TCC time out IOCF bit0=1	No function	(1) Wake-up (2) Jump to SLEP next instruction
COUNTER1 time out IOCF bit1=1	No function	(1) Wake-up (2) Jump to SLEP next instruction
COUNTER2 time out IOCF bit2=2	No function	(1) Wake-up (2) Jump to SLEP next instruction
WDT time out	Reset and jump to address 0	(1) Wake-up (2) Next instruction
PORT8(0~3) RE PAGE0 bit3 or bit4 or bit5 or bit6 = 1	Reset and Jump to address 0	(1) Wake-up (2) Jump to SLEP next instruction
PORT7(0~3) IOCF bit3 or bit4 or bit5 or bit7=1	Reset and Jump to address 0	(1) Wake-up (2) Jump to SLEP next instruction

Note

- PORT70 's wakeup function is controlled by IOCF bit 3. It's falling edge or rising edge trigger (controlled by CONT register bit7).
- PORT7(1~3) 's wakeup functions are controlled by IOCF bit (4,5,7). They are falling edge trigger.
- PORT80~PORT83's wakeup function are controlled by RE PAGE0 bit 0 ~ bit 3. They are falling edge trigger.

7.2.11.2PAGE1 (DAC input data register)

7	6	5	4	3	2	1	0
DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0
R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1

Bit 0 ~ Bit 7 (DA0 to DA7) : DA converter data buffer

7.2.12 RC (PORTC0 I/O data, Counter1 data)

7.2.12.1PAGE0 (PORT9 I/O data register)

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	PC0
							R/W

Bit 0 (PC0) : PORTC0 I/O data register

User can use IOC register to define input or output this bit.

Bit 1 ~ Bit 7 : (undefined) not allowed to use

7.2.12.2PAGE1 (Counter1 data register)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CN17	CN16	CN15	CN14	CN13	CN12	CN11	CN10
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0 ~ Bit 7 (CN10 ~ CN17) : Counter1's buffer that user can read and write.

Counter1 is a 8-bit up-counter with 8-bit prescaler that user can use RC PAGE1 to preset and read the counter.(write ➔ preset) After a interruption , it will reload the preset value.

Example for writing :

MOV 0x0C, A ; write the data at accumulator to counter1 (preset)

Example for reading :

MOV A, 0x0C ; read the data at counter1 to accumulator

7.2.13 RD (LCD control, Counter2 data)

7.2.13.1PAGE0 (LCD driver control bits)

7	6	5	4	3	2	1	0
DETOED	-	-	-	-	LCD_C1	LCD_C0	LCD_M
R/W-0					R/W-0	R/W-0	R/W-0

Bit 0 (LCD_M) : LCD operation method including duty and frame frequency

Bit 1 ~ Bit 2 (LCD_C0 ~ LCD_C1) : LCD display control

LCD_C1	LCD_C0	LCD_M	LCD Display Control	Duty	Bias
0	0	0	change duty	1/4	1/3
		1	Disable(turn off LCD)	1/2	1/3
0	1	:	Blanking	:	:
1	1	:	LCD display enable	:	:

Ps. To change the display duty must set the "LCD_C1 ,LCD_C0" to "00".

The controller can drive LCD directly. The LCD block is made up of common driver, segment driver, display LCD RAM, common output pins, segment output pins and LCD operating power supply. The basic structure contains a timing control. This timing control uses the basic frequency 32.768KHz to generate the proper timing for different duty and display access.

RD PAGE0 Bit 0 ~ Bit 2 are LCD control bits for LCD driver. These LCD control bits determine the duty, the number of common and the frame frequency. The LCD display (disable, enable, blanking) is controlled by Bit 1 and Bit 2. The driving duty is decided by Bit 0. The display data is stored in LCD RAM which address and data access controlled by registers R5 PAGE1 and R6 PAGE1.

You can regulate the contrast of the LCD display by IOC5 PAGE0 Bit 0 ~ Bit 3 (BIAS0 ~ BIAS3). Up to 16 levels contrast is convenient for better display.

Bit 3 ~ Bit 6 : (undefined) not allowed for use.

Bit 7 (DETOED) : the interrupt triggering edge control for CTCSS tone detection output

0/1 ➔ falling edge/falling and rising

7.2.13.2 PAGE1 (Counter2 data register)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CN27	CN26	CN25	CN24	CN23	CN22	CN21	CN20
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0 ~ Bit 7 (CN20 ~ CN27) : Counter2's buffer that you can read and write.

Counter2 is an 8-bit up-counter with 8-bit prescaler that you can use with RD PAGE1 to preset and read the counter.(write ➔ preset) After an interrupt, it will reload the preset value.

Example for writing:

```
MOV  0x0D, A  ; write the data at accumulator to counter2 (preset)
```

Example for reading:

```
MOV  A, 0x0D  ; read the data at counter2 to accumulator
```

7.2.14 RE (Wake-up control, DAC tone output frequency selection)

7.2.14.1PAGE0 (Interrupt flag, Wake-up control bits)

7	6	5	4	3	2	1	0
-	-	-	-	/WUP83	/WUP82	/WUP81	/WUP80
				R/W-0	R/W-0	R/W-0	R/W-0

Bit 0 (/WUP80) : PORT80 wake-up control, 0/1 ➔ disable/enable P80 pin wake-up function

Bit 1 (/WUP81) : PORT81 wake-up control, 0/1 ➔ disable/enable P81 pin wake-up function

Bit 2 (/WUP82) : PORT82 wake-up control, 0/1 ➔ disable/enable P82 pin wake-up function

Bit 3 (/WUP83) : PORT83 wake-up control, 0/1 ➔ disable/enable P83 pin wake-up function

Bit 4 ~ Bit 7 : (undefined) not allowed for use

7.2.14.2PAGE1 (Programmable D/A tone selection register)

7	6	5	4	3	2	1	0
DAT7	DAT6	DAT5	DAT4	DAT3	DAT2	DAT1	DAT0
R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1

Bit 0 ~ Bit 7 (DAT0 ~ DAT7) : D/A tone output frequency selection

The programmable D/A tone output frequency = 447829Hz / Mi / 32, where Mi = DAT7 ~ DAT0 = 1 ~ 255

When Mi = DAT7 ~ DAT0 = 0 or DAT/DAD (IOCA PAGE1 Bit 7) = 0, the D/A tone output generator circuit will be disabled. It is specially used for CTCSS tone generation. Also refer to DAC for details

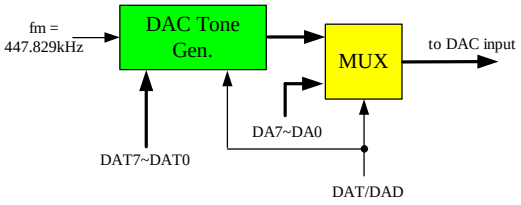


Fig.5 Programmable DAC tone generation

Example : CTCSS tone generation :

Channel	DAT7~DAT0	D/A tone generation	CTCSS tone	Mi	Act. Freq.
-	00000000	Disable	-	-	-
1	11010001	Enable	67.0	209	66.960
2	11001010		69.3	202	69.280
3	11000011		71.9	195	71.767
4	10111100		74.4	188	74.440
5	10110110		77.0	182	76.894
6	10110000		79.7	176	79.515
7	10101010		82.5	170	82.322
8	10100100		85.4	164	85.333
9	10011110		88.5	158	88.574
10	10011001		91.5	153	91.468
11	10010100		94.8	148	94.558
12	10010000		97.4	144	97.185
13	10001100		100.0	140	99.962

14	10000111		103.5	135	103.664
15	10000011		107.2	131	106.829
Channel	**DAT7~DAT0**	**D/A tone generation**	**CTCSS tone**	**Mi**	**Act. Freq.**
16	01111110		110.9	126	111.069
17	01111010		114.8	122	114.710
18	01110110		118.8	118	118.599
19	01110010		123.0	114	122.760
20	01101110		127.3	110	127.224
21	01101010		131.8	106	132.025
22	01100111		136.5	103	135.870
23	01100011		141.3	99	141.360
24	01100000		146.2	96	145.778
25	01011100		151.4	92	152.116
26	01011001		156.7	89	157.243
27	01011000		159.8	88	159.030
28	01010110		162.2	86	162.729
29	01010011		167.9	83	168.610
30	01010001		173.8	81	172.773
31	01001110		179.9	78	179.419
32	01001100		183.5	76	184.140
33	01001011		186.2	75	186.595
34	01001010		189.9	74	189.117
35	01001001		192.8	73	191.708
36	01000111		196.6	71	197.108
37	01000110		199.5	70	199.924
38	01000101		203.5	69	202.821
39	01000100		206.5	68	205.804
40	01000010		210.7	66	212.040
41	01000000		218.1	64	218.667
42	00111110		225.7	62	225.720
43	00111101		229.1	61	229.421
44	00111100		233.6	60	233.244
45	00111010		241.8	58	241.287
46	00111000		250.3	56	249.905
47	00110111		254.1	55	254.448

7.2.15 RF (Interrupt status)

(Interrupt status register)

7	6	5	4	3	2	1	0
INT3	DETO	INT2	INT1	INT0	CNT2	CNT1	TCIF
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

"1" means interrupt request, "0" means non-interrupt

Bit 0(TCIF) : TCC timer overflow interrupt flag

Set when the TCC timer overflows.

Bit 1(CNT1) : counter 1 timer overflow interrupt flag

Set when counter1 timer overflows.

Bit 2(CNT2) : Counter 2 timer overflow interrupt flag

Set when counter2 timer overflows.

Bit 3(INT0) : External INT0 pin interrupt flag

If PORT70 has a falling edge/rising edge (controlled by the CONT register) trigger signal, CPU will set this bit.

Bit 4(INT1) : External INT1 pin interrupt flag

If PORT71 has a falling edge trigger signal, CPU will set this bit.

Bit 5(INT2) : External INT2 pin interrupt flag

If PORT72 has a falling edge trigger signal, CPU will set this bit.

Bit 6(DETO) : CTCSS tone detection interrupt flag

If CTCSS detection output signal (R7 PAGE1 bit 6) has an edge signal (falling edge, falling and rising edge), CPU will set this bit.

Bit 7(INT3) : external INT3 pin interrupt flag

If PORT73 has a falling edge trigger signal, CPU will set this bit.

Note

IOCF is the interrupt mask register. User can read and clear.

Trigger edge as shown in the table

Signal	Trigger
TCC	Time out
COUNTER1	Time out
COUNTER2	Time out
INT0	Falling Rising edge
INT1	Falling edge
INT2	Falling edge
DETO	Falling edge Falling and rising edge

R10~R3F (General Purpose Register)

R10~R3F (Banks 0 ~ 3) : all are general purpose registers.

7.3 Special Purpose Registers

7.3.1 A (Accumulator)

Internal data transfer, or instruction operand holding

It is not an addressable register.

7.3.2 CONT (Control Register)

7	6	5	4	3	2	1	0
P70EG	INT	TS	RETBK	PAB	PSR2	PSR1	PSR0

Bit 0 ~ Bit 2 (PSR0 ~ PSR2) : TCC/WDT prescaler bits

PSR2	PSR1	PSR0	TCC Rate	WDT Rate
0	0	0	1:2	1:1
0	0	1	1:4	1:2
0	1	0	1:8	1:4
0	1	1	1:16	1:8
1	0	0	1:32	1:16
1	0	1	1:64	1:32
1	1	0	1:128	1:64
1	1	1	1:256	1:128

Bit 3(PAB) : Prescaler assignment bit

0/1 ➔ TCC/WDT

Bit 4(RETBK) : Return backup control value for the interrupt routine

0 ➔ disable/enable

When this bit is set to 1, the CPU will automatically store the ACC, R3 status and R5 PAGE after an interrupt is triggered. And it will be restored after instruction RETI. When this bit is set to 0, you need to store ACC, R3 and R5 PAGE in your program.

Bit 5(TS) : TCC signal source

0 ➔ internal instruction clock cycle

1 ➔ 16.384kHz

Bit 6 (INT) : INT enable flag

0 ➔ interrupt masked by DISI or hardware interrupt

1 ➔ interrupt enabled by ENI/RETI instructions

Bit 7(P70EG) : interrupt edge type of P70

0 ➔ P70 's interruption source is a rising edge signal.

1 ➔ P70 's interruption source is a falling edge signal.

CONT register is readable (CONTR) and writable (CONTW).

TCC and WDT :

There is an 8-bit counter available as prescaler for the TCC or WDT. The prescaler is available for TCC only or WDT only at the same time.

An 8 bit counter is available for TCC or WDT as determined by the status of the bit 3 (PAB) of the CONT register.

See the prescaler ratio in CONT register.

Fig.17 depicts the circuit diagram of TCC/WDT.

Both TCC and prescaler will be cleared by instructions which write to TCC each time.

The prescaler will be cleared by the WDTC and SLEP instructions, when assigned to WDT mode.

The prescaler will not be cleared by SLEP instructions, when assigned to TCC mode.

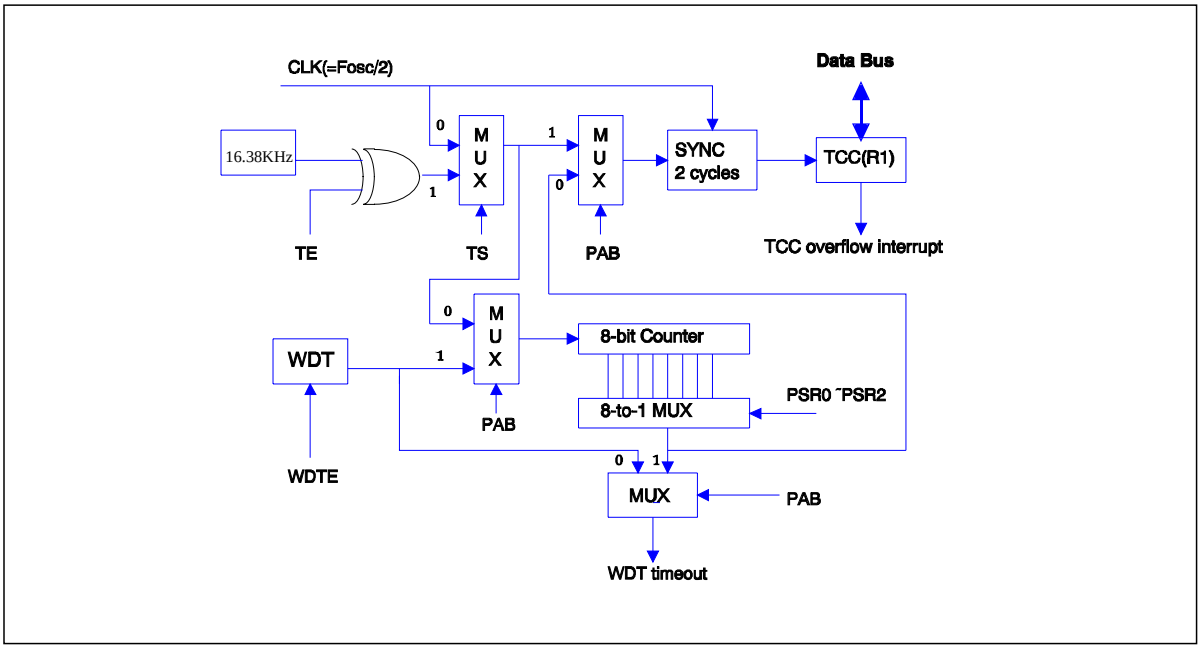


Fig.6 Block Diagram of TCC and WDT

7.3.3 IOC5 (PORT5 I/O control, LCD bias control, Comparator control)

7.3.3.1 PAGE0 (LCD bias control bits)

7	6	5	4	3	2	1	0
IOC57	IOC56	IOC55	-	BIAS3	BIAS2	BIAS1	BIAS0
R/W-1	R/W-1	R/W-1		R/W-0	R/W-0	R/W-0	R/W-0

Bit 0 ~ Bit 3 (BIAS0 ~ BIAS3) : LCD operation voltage selection. Vop = VDD * (1 - n/60), where n = 0 ~ 15

BIAS3	BIAS2	BIAS1	BIAS0	Vop (=VDD-VLCD)	Example (VDD = 3V)
0	0	0	0	VDD * (1-0/60)	3V
0	0	0	1	VDD * (1-1/60)	2.95V
0	0	1	0	VDD * (1-2/60)	2.90V
0	0	1	1	VDD * (1-3/60)	2.85V
0	1	0	0	VDD * (1-4/60)	2.80V
:	:	:	:	:	:
1	1	0	1	VDD * (1-13/60)	2.35V
1	1	1	0	VDD * (1-14/60)	2.30V
1	1	1	1	VDD * (1-15/60)	2.25V

Bit 4 : (undefined) not allowed for use

Bit 5 ~ Bit 7 (IOC55 ~ IOC57) : PORT5 (5~7) I/O direction control register

0 ➔ put the relative I/O pin as output

1 ➔ put the relative I/O pin into high impedance

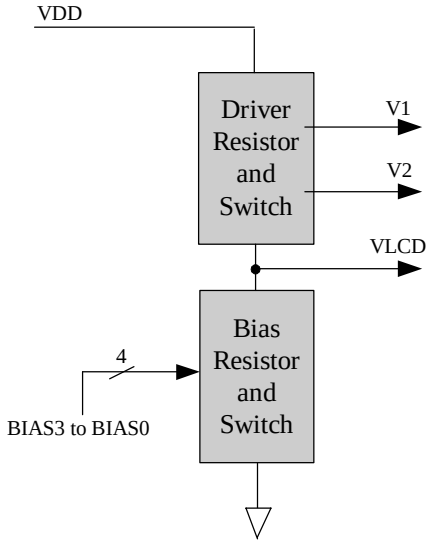


Fig.7 LCD Driver Bias Circuit

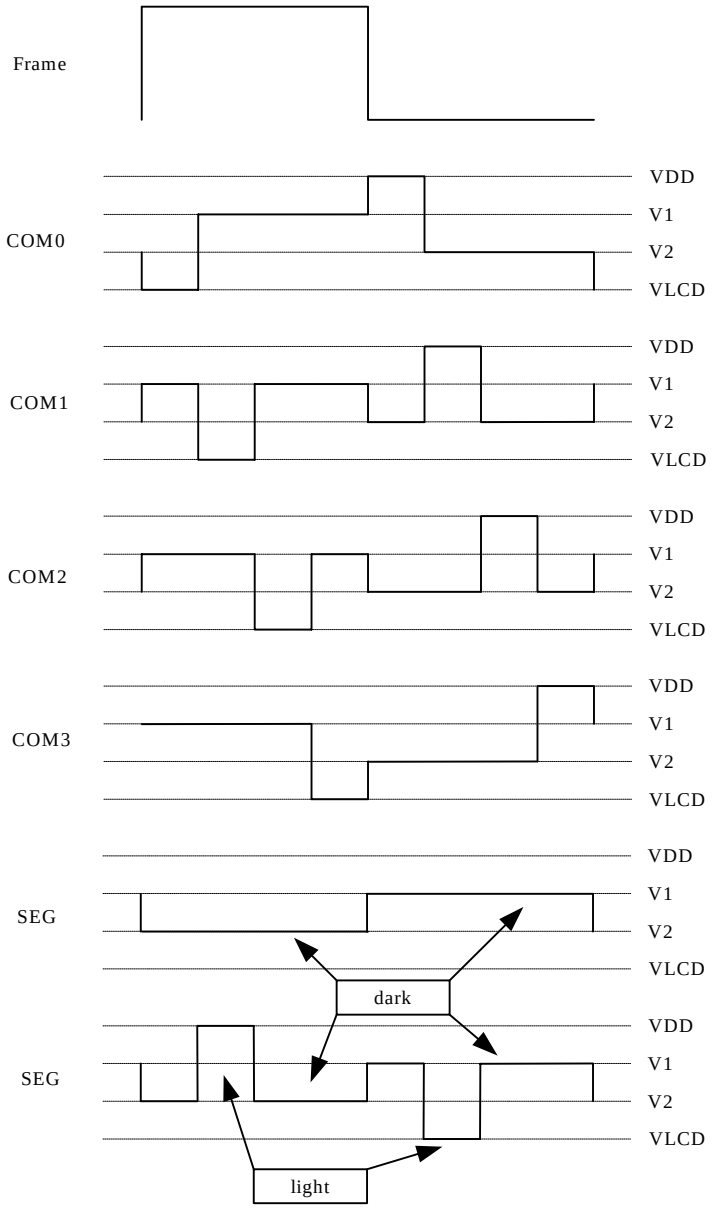


Fig.8 Type1's LCD Waveform for 1/3 bias, 1/4 duty

(Type 0 is no longer available in this mask version)

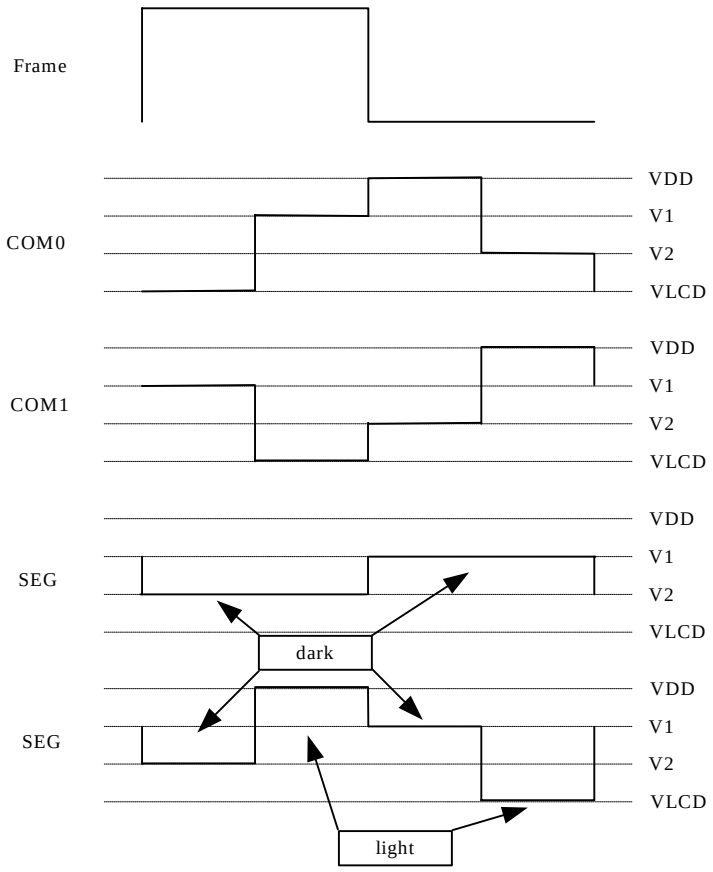


Fig.9 Type1's LCD Waveform for 1/3 bias, 1/2 duty

(Type0 is no longer available in this mask version)

7.3.3.2 PAGE1 (Comparator Control Register)

7	6	5	4	3	2	1	0
CMPEN	CMPS1	CMPS0	CMP_B4	CMP_B3	CMP_B2	CMP_B1	CMP_B0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

If you define CMP1/P63 pin, CMP2/P64 pin or CMP3/P65 pin (by CMPIN1, CMPIN2, CMPIN3 at IOCE page1) as CMP1, CMP2 pin or CMP3 pin (comparator's input pins), you can use this register to control the comparator's function.

Bit 0 ~ Bit 4 (CMP_B0 ~ CMP_B4) : Reference voltage selection of internal bias resistor string

Voltage = VR x (n + 0.5)/ 32 , n=0 to 31. Set RB bit 6 (VREF) to select VR = VREG or 2.0V

Bit 5 ~ Bit 6 (CMPS0 ~ CMPS1) : Comparator's channel selection bits from CMP1 to CMP3

Bit 7(CMPEN) : Enable bit of the comparator circuit

0/1 ➔ disable/enable the comparator circuit

CMPS1	CMPS0	Input
0	0	CMP1
0	1	CMP2
1	0	CMP3
1	1	Reserved

The relation between these registers is shown in Fig.10.

Ps. VRSEL bit is in IOCA PAGE1 bit 4.

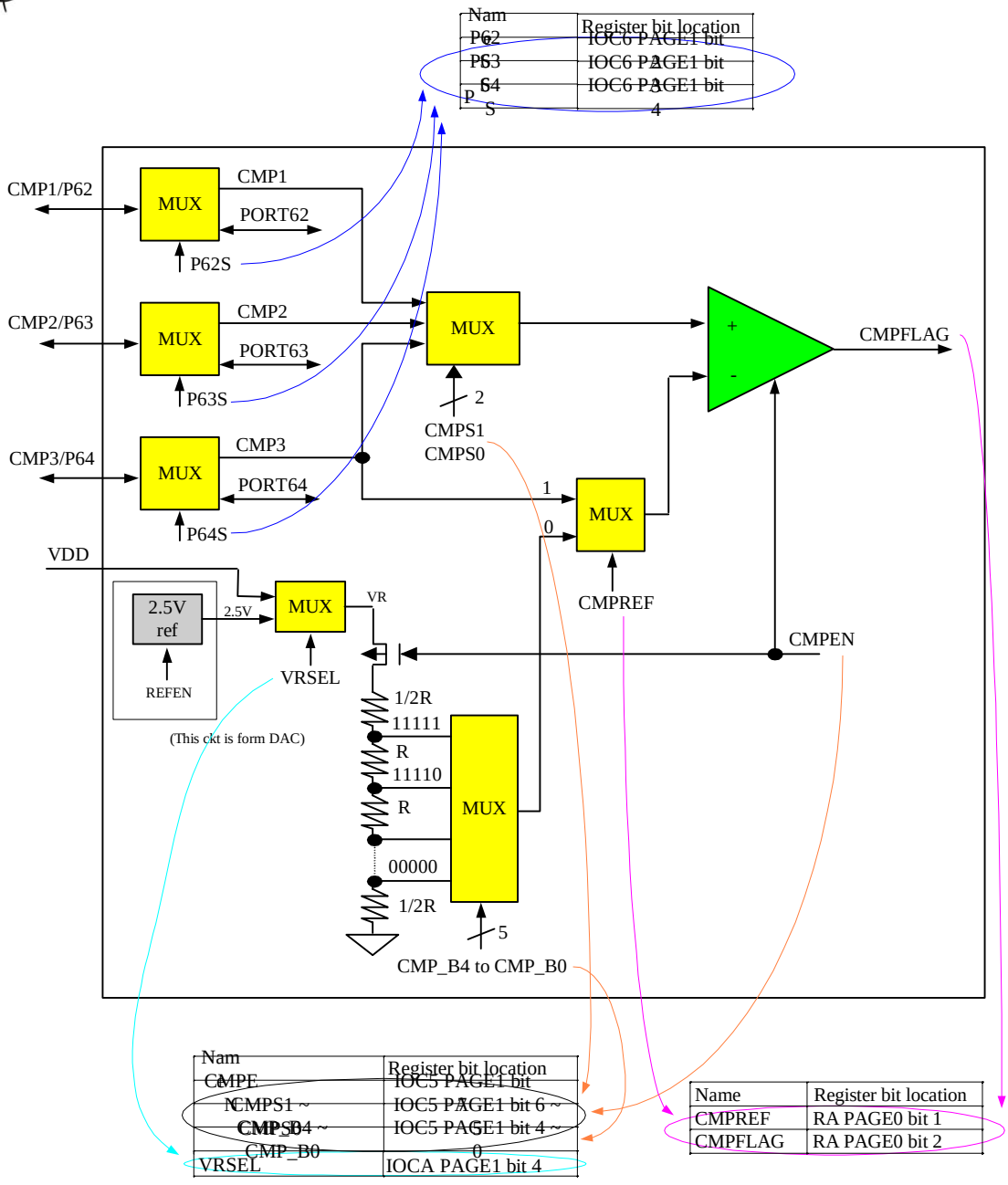


Fig.10 The Comparator Circuit

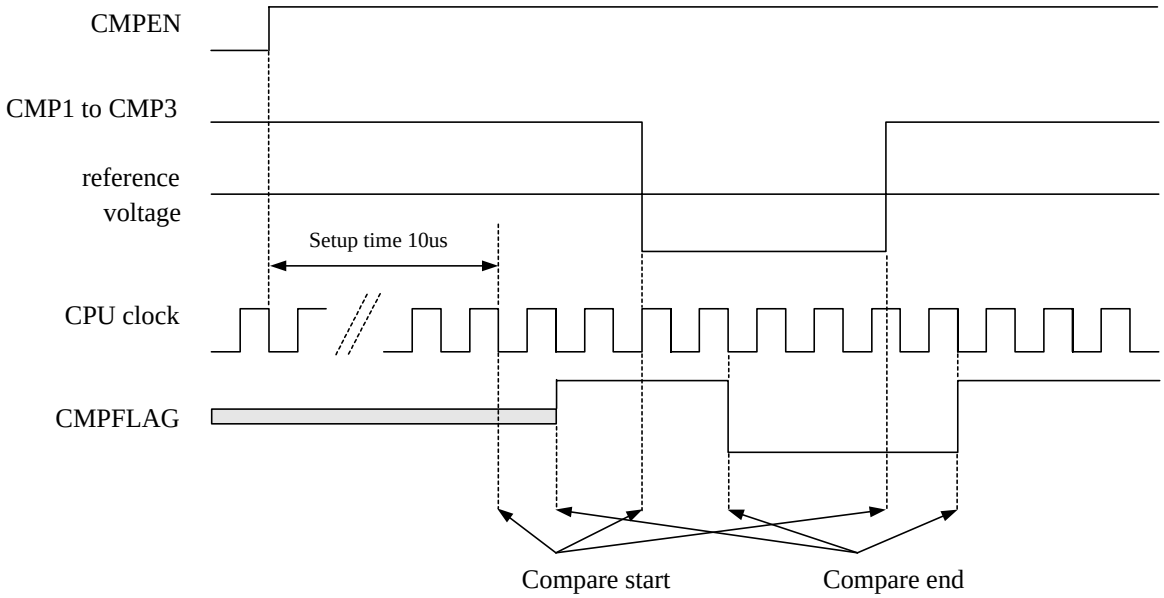


Fig.11 The Comparator Timing

7.3.4 IOC6 (PORT6 I/O control, P6 pins switch control)*

7.3.4.1 PAGE0 (PORT6 I/O control register)

7	6	5	4	3	2	1	0
IOC67	IOC66	IOC65	IOC64	IOC63	IOC62	IOC61	IOC60
R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1

Bit 0 ~ Bit 7 (IOC60 ~ IOC67) : PORT6(0~7) I/O direction control register

0 ➔ put the relative I/O pin as output

1 ➔ put the relative I/O pin into high impedance

7.3.4.2 PAGE1 (P6* pins switch control register)

7	6	5	4	3	2	1	0
AMUTE	P66S	P65S	P64S	P63S	P62S	-	-
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		

Bit 0 ~ Bit 1 : (undefined) not allowed F use

Bit 2(P62S) : Select channel 1 input pin of comparator or I/O PORT62 pin

0 ➔ P62 (I/O PORT62) pin is selected

1 ➔ CMP1 (Channel 1 input of comparator) pin is selected

Bit 3(P63S) : Select channel 2 input pin of comparator or I/O PORT63 pin

0 ➔ P63 (I/O PORT63) pin is selected

1 ➔ CMP2 (Channel 2 input of comparator) pin is selected

Bit 4(P64S) : Select channel 3 input pin of comparator or I/O PORT64 pin

0 ➔ P64 (I/O PORT64) pin is selected

1 ➔ CMP3 (Channel 3 input of comparator) pin is selected

Bit 5(P65S) : Select receiving audio output pin of CTCSS or I/O PORT65 pin

0 ➔ P65 (I/O PORT65) pin is selected

1 ➔ AURX (Receiving audio output pin of CTCSS) pin is selected

Bit 6(P66S) : Select modulation transmitting output pin of CTCSS or I/O PORT66 pin

0 ➔ P66 (I/O PORT66) pin is selected

1 ➔ MTX (Modulation transmitting output of CTCSS) pin is selected

Bit 7(AMUTE) : Audio mute for MIC AMP of CTCSS block

0 ➔ Voice transmitting path from MIC AMP output

1 ➔ Audio mute from MIC AMP output

Refer to Fig.14 CTCSS block for details.

7.3.5 IOC7 (PORT7 I/O control, PORT7 pull high control)

7.3.5.1 PAGE0 (PORT7 I/O control register)

7	6	5	4	3	2	1	0
IOC77	IOC76	IOC75	IOC74	IOC73	IOC72	IOC71	IOC70
R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1

Bit 0 ~ Bit 7 (IOC70 ~ IOC77) : PORT7(0~7) I/O direction control register

0 ➔ put the relative I/O pin as output

1 ➔ put the relative I/O pin into high impedance

7.3.5.2 PAGE1 (PORT7 pull high control register)

7	6	5	4	3	2	1	0
PH77	PH76	PH75	PH74	PH73	PH72	PH71	PH70
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0 ~ Bit 7 (PH70 ~ PH77) : PORT7 bit0~bit7 pull high control register

0 ➔ disable pull high function

1 ➔ enable pull high function

7.3.6 IOC8 (PORT8 I/O control, PORT8 pull high control)

7.3.6.1 PAGE0 (PORT8 I/O control register)

7	6	5	4	3	2	1	0
IOC87	IOC86	IOC85	IOC84	IOC83	IOC82	IOC81	IOC80
R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1

Bit 0 ~ Bit 7 (IOC80 ~ IOC87) : PORT8(0~7) I/O direction control register

0 ➔ put the relative I/O pin as output

1 ➔ put the relative I/O pin into high impedance

7.3.6.2 PAGE1 (PORT8 pull high control register)

7	6	5	4	3	2	1	0
PH87	PH86	PH85	PH84	PH83	PH82	PH81	PH80
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0 ~ Bit 7 (PH80 ~ PH87) : PORT8 bit0~bit7 pull high control register

0 ➔ disable pull high function

1 ➔ enable pull high function

7.3.7 IOC9 (PORT9 I/O control, PORT9 switches)

7.3.7.1 PAGE0 (PORT9 I/O control register)

7	6	5	4	3	2	1	0
IOC97	IOC96	IOC95	IOC94	IOC93	IOC92	IOC91	IOC90
R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1

Bit 0 ~ Bit 7 (IOC90 ~ IOC97) : PORT9(0~7) I/O direction control register

0 ➔ put the relative I/O pin as output

1 ➔ put the relative I/O pin into high impedance

7.3.7.2 PAGE1 (PORT9 switches)

P97S	P96S	P95S	P94S	P93S	P92S	P91S	-
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	

Bit 0 : (undefined) not allowed for use

Bit 1(P91S) : Switch I/O PORT91 or LCD segment signal

0 ➔ (P91 pin is selected) : normal PORT91

1 ➔ (SEG19 pin) : SEGMENT output

Bit 2(P92S) : Switch I/O PORT92 or LCD segment signal

0 ➔ (P92 pin is selected) : normal PORT92

1 ➔ (SEG18 pin) : SEGMENT output

Bit 3(P93S) : Switch I/O PORT93 or LCD segment signal

0 ➔ (P93 pin is selected) : normal PORT93

1 ➔ (SEG17 pin) : SEGMENT output

Bit 4(P94S) : Switch I/O PORT94 or LCD segment signal

0 ➔ (P94 pin is selected) : normal PORT94

1 ➔ (SEG16 pin) : SEGMENT output

Bit 5(P95S) : Switch I/O PORT95 or LCD segment signal

0 ➔ (P95 pin is selected) : normal PORT95

1 ➔ (SEG15 pin) : SEGMENT output

Bit 6(P96S) : Switch I/O PORT96 or LCD segment signal

0 ➔ (P96 pin is selected) : normal PORT96

1 ➔ (SEG14 pin) : SEGMENT output

Bit 7(P97S) : Switch I/O PORT97 or LCD segment signal

0 ➔ (P97 pin is selected) : normal PORT97

1 ➔ (SEG13 pin) : SEGMENT output

7.3.8 IOCA (TONE2 control, Control bits for DAC, DAC tone, Reference, VOX and P67 switch)

7.3.8.1 PAGE0 (TONE2 control register)

T27	T26	T25	T24	T23	T22	T21	T20
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0 ~ Bit 7(T20 ~ T27) : Tone generator 2 ‘s frequency divider and power control

Run in Normal mode.

Clock source = 111957Hz

T27~T20 = ‘11111111’ => Tone generator2 has 438Hz SIN wave output.

T27~T20 = '00000010' => Tone generator2 has 55921Hz SIN wave output.

T27~T20 = '00000001' => DC bias voltage output

T27~T20 = '00000000' => Power off

Built-in tone generators can generate dialing tone signals for telephone of dialing tone type or just a single tone. In DTMF application, there are two kinds of tones. One is the group with row frequency (TONE1), the other is the group with column frequency (TONE2), each group has 4 kinds of frequency, you can get a total of 16 kinds of DTMF frequency. The tone generator contains a row frequency sine wave generator for generating the DTMF signal which is selected by IOCD PAGE0, IOCE PAGE0 and a column frequency sine wave generator for generating the DTMF signal which is selected by IOCA PAGE0. This block can generate single tone by filling one of these two registers.

If all the values are low, the power of the tone generators will be turned off .

TONE1(IOCD, IOCE PAGE0) Low group freq.	699.7Hz (0x0A0)	1	2	3	A
	772.1Hz (0x091)	4	5	6	B
	854.6Hz (0x083)	7	8	9	C
	940.8Hz (0x077)	*	0	#	D

7.3.8.2 PAGE1 (Control bits for DAC, DAC tone, Reference, VOX and P67 switch)

DAT/DAD	VREF	DATEN	VRSEL	DAST/P67	-	-	-
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			

Bit 0 ~ Bit 2 : (undefined) not allowed for use

Bit 3(DAST/P67) : DAC enable control or P67 switch

0 ➔ switch DAO/P67 pin as normal I/O P67

1 ➔ enable DAC, enable DAC output buffer B1 and DAC output to DAO/P67 pin

When this bit is set by software, the DA converter will start converting and output to DAO/P67 pin. If you clean this bit, the DA converter will stop and the DAO/P67 pin will be become a normal I/O P67.

Refer also to bit 5 (DATEN) for DAC power control.

Bit 4(VRSEL) : Reference voltage selection bit for Comparator circuit

0/1 ➔ VDD/2.5V from DAC

See also Fig.13 in the next page.

Bit 5(DATEN) : DAC enable control

0/1 ➔ disable/enable DAC and its tone output buffer B2

When this bit is set by software, the DA converter will start converting and output to internal CTCSS VTX3 end. If you clean this bit, the DA converter will stop and the DAO tone output buffer B2 is disabled.

Refer also to bit 3 (DAST/P67) for DAC power control.

Bit 6(VREF) : Reference voltage selection bit for the DA converter circuit

DAC reference setting is shown as follows. Also see Fig.12 and Fig.13 in the next page.

ASW3	VREF	DATEN	DAST/P67	Function
1	x	1	x	Select 2.5V ref, enable 2.5V ref, enable DAC,
0	1	1	x	Enable buffer B2, buffer B2 output to CTCSS LPF
0	0	1	x	Select VDD, disable 2.5V, enable DAC, enable buffer B2
x	1	0	1	Select 2.5V ref, enable 2.5V ref, enable DAC, enable buffer B1, buffer B1 output to DAO/P67 pin
x	0	0	1	Select VDD, disable 2.5V, enable DAC, enable buffer B1, buffer B1 output to DAO/P67 pin

Ps. IOCE PAGE1 bit 2 (ASW3), IOCA PAGE1 bit 6 (VREF), IOCA PAGE1 bit 5 (DATEN),

IOCA PAGE1 bit 3 (DAST/P67)

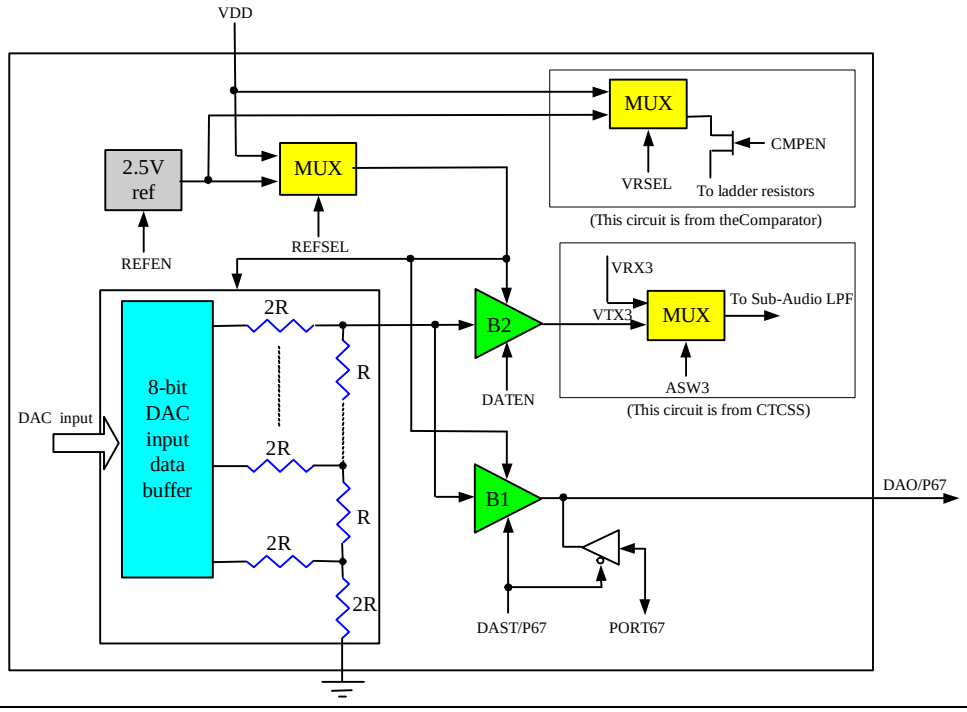


Fig.12 D/A converter (DAC)

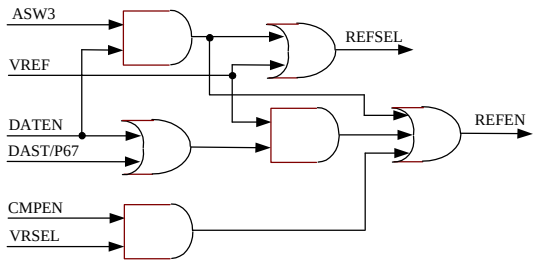


Fig.13 DAC reference voltage control logic

Bit 7(DAT/DAD) : Programmable D/A tone generation or D/A input data enable control

0 ➔ Enable D/A input data and disable D/A tone generation (also stop to D/A tone generation)

1 ➔ Enable Programmable D/A tone generation and disable D/A input data

7.3.9 IOCC (PORTC I/O control, PORT switch)

7.3.9.1 PAGE0 (PORTC I/O control register)

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	IOCC0
							R/W-1

Bit 0 (IOCC0) : PORTC0 I/O direction control register

Bit 1 ~ Bit 7 : (undefined) not allowed to use

7.3.9.2 PAGE1 (PORT switch)

7	6	5	4	3	2	1	0
-	-	-	-	-	P5SH	-	-
					R/W-0		

Bit 0 ~ Bit 1 : (undefined) not allowed to use

Bit 2(P5SH) : Switch I/O PORT5 high nibble(5~7) or LCD segment signal

0 ➔ (P55 ~ P57 pins are selected) : normal PORT5 high nibble(5~7)

1 ➔ (SEG10 ~ SEG12 pins are selected) : SEGMENT output

Bit 3 ~ Bit 7 : (undefined) not allowed to use

7.3.10 IOCD (TONE1 control, Clock source, Prescaler of CN1 and CN2)

7.3.10.1PAGE0 (TONE1 control)

7	6	5	4	3	2	1	0
T17	T16	T15	T14	T13	T12	T11	T10
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0 ~ Bit 7 (T10 ~ T17) : Tone generator 1‘s frequency divider and power control

Please Run in Normal mode.

Clock source = 111957Hz and Freq. = 111957Hz / N, where N is divider value for T1A ~ T10 (T1A ~ T18 are in the IOCE PAGE0 Bit 2 ~ Bit 0.

If T20 ~ T18 are all “0”, then

T17 ~ T10 = ‘11111111’ => Tone generator1 will has 439Hz SIN wave output.

:

T17~T10 = ‘00000010’ => Tone generator1 will has 55978Hz SIN wave output.

T17~T10 = ‘00000001’ => DC bias voltage output

T17~T10 = ‘00000000’ => Power off

7.3.10.2PAGE1 (Clock source and prescaler for COUNTER1 and COUNTER2)

7	6	5	4	3	2	1	0
CNT2S	C2_PSC2	C2_PSC1	C2_PSC0	CNT1S	C1_PSC2	C1_PSC1	C1_PSC0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0 ~ Bit 2 (C1_PSC0 ~ C1_PSC2) : COUNTER1 prescaler ratio

C1_PSC2	C1_PSC1	C1_PSC0	COUNTER1
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

Bit 3(CNT1S) : COUNTER1 clock source

0/1 ➔ 16.384kHz/system clock

Bit 4 ~ Bit 6 (C2_PSC0 ~ C2_PSC2) : COUNTER2 prescaler ratio

C2_PSC2	C2_PSC1	C2_PSC0	COUNTER2
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

Bit 7(CNT2S) : COUNTER2 clock source

0/1 ➔ 16.384kHz/system clock

7.3.11 IOCE (TONE1 extra control bits, CTCSS control switches)

7.3.11.1PAGE0 (Interrupt mask, TONE1 extra three control bits)

7	6	5	4	3	2	1	0
-	-	-	-	-	T1A	T19	T18
					R/W-0	R/W-0	R/W-0

Bit 0 ~ Bit 2 (T18 ~ T1A) : Most significant 3 bits of Tone generator 1‘s frequency divider and power control

These 3 bits and other 8 bits (IOCA PAGE0 bit 7 ~ bit0) are assembled as 11-bit frequency divider for Tone generator 1

Bit 3 ~ Bit 7 = 0 : (undefined) not allowed to use

7.3.11.2PAGE1 (CTCSS control switches)

7	6	5	4	3	2	1	0
TXPWR	RXPWR	BPFPWR	LPFPWR	ASW4	ASW3	ASW2	ASW1
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0(ASW1) : Analog switch-1 control for multi-plexer in the CTCSS block

0 ➔ Select VRX1 input

1 ➔ Select VTX1 input

Bit 1(ASW2) : Analog switch-2 control for multi-plexer in the CTCSS block

0 ➔ Select VRX2 output

1 ➔ Select VTX2 output

Bit 2(ASW3) : Analog switch-3 control for multi-plexer in the CTCSS block

0 ➔ Select VRX3 input

1 ➔ Select VTX3 input

Bit 3(ASW4) : Analog switch-4 control for multi-plexer in the CTCSS block

0 ➔ Select VRX4 input

1 ➔ Select VTX4 input

Bit 4(LPFPWR) : Power control for sub-audio LPF in the CTCSS block. 0/1 ➔ disable/enable

Bit 5(BPFPWR) : Power control for audio BPF in the CTCSS block. 0/1 ➔ disable/enable

Bit 6(RXPWR) : RX power control for the CTCSS block 0/1 ➔ disable/enable

Bit 7(TXPWR) : TX power control for the CTCSS block 0/1 ➔ disable/enable

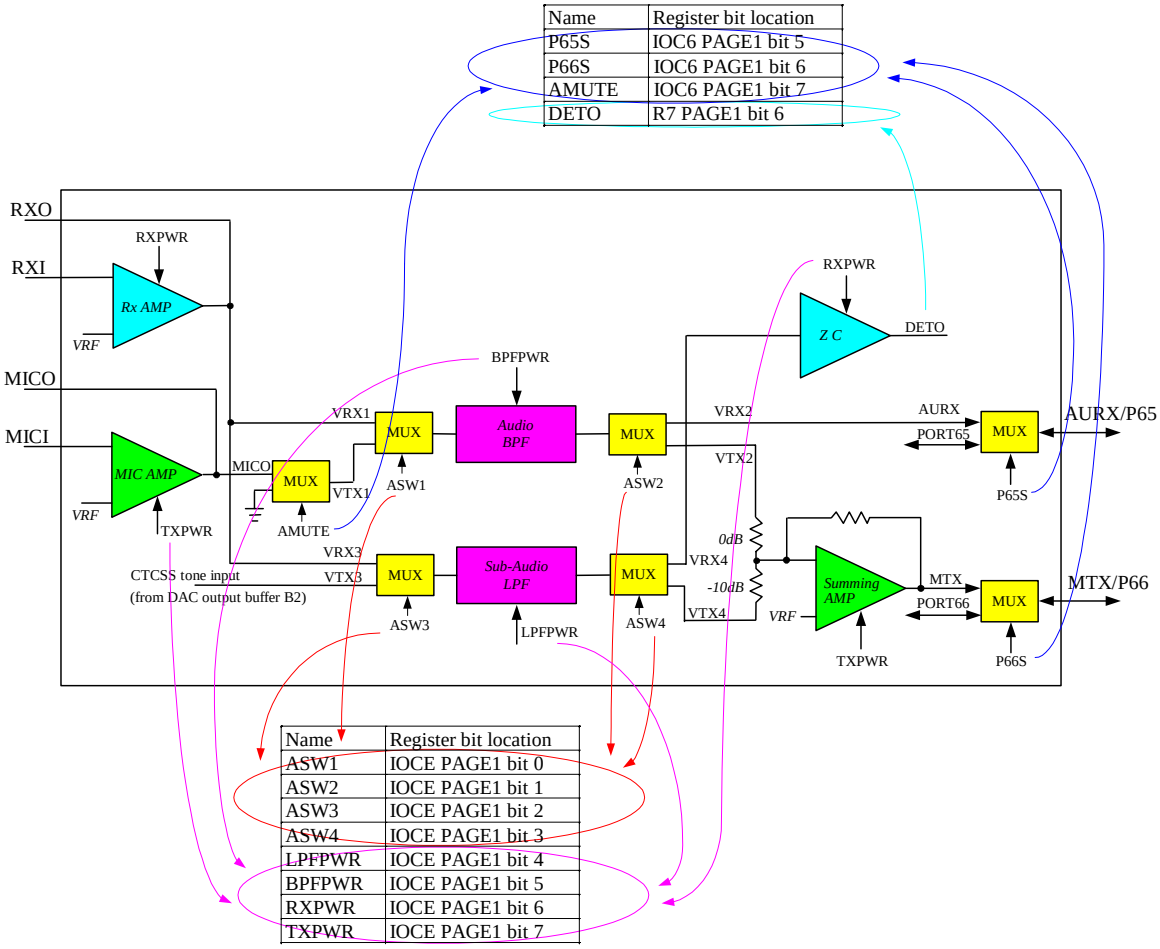


Fig.14 CTCSS block

7.3.12 IOCF (Interrupt mask)

(Interrupt mask register)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
INT3	DETO	INT2	INT1	INT0	CNT2	CNT1	TCIF
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0 ~ 7 : interrupt enable bit

0 ➔ disable interrupt

1 ➔ enable interrupt

The status after interrupt and the interrupt sources list as the table below.

Interrupt signal	IDLE mode	GREEN mode	NORMAL mode
	RA(7,6)=(1,0) + SLEP	RA(7,6)=(x,0) no SLEP	RA(7,6)=(x,1) no SLEP
TCC time out IOCF bit0=1 And "ENI"	(1) Wake-up (2) Interrupt (jump to address 8 at page0) (3) after RETI instruction, jump to SLEP Next instruction	Interrupt (jump to address 8 at page0)	Interrupt (jump to address 8 at page0)
COUNTER1 time out IOCF bit1=1 And "ENI"	(1) Wake-up (2)Interrupt (jump to address 8 at page0) (3) after RETI instruction, jump to SLEP Next instruction	Interrupt (jump to address 8 at page0)	Interrupt (jump to address 8 at page0)
COUNTER2 time out IOCF bit2=2 And "ENI"	(1) Wake-up (2) Interrupt (jump to address 8 at page0) (3) after RETI instruction, jump to SLEP Next instruction	Interrupt (jump to address 8 at page0)	Interrupt (jump to address 8 at page0)
PORT7(0~3) IOCF bit3 or bit4 or bit5 or bit7=1 And "ENI"	(1) Wake-up (2) Interrupt (jump to address 8 at page0) (3) after RETI instruction, jump to SLEP Next instruction	Interrupt (jump to address 8 at page0)	Interrupt (jump to address 8 at page0)
DETO IOCF bit6 = 1 And “ENI”	No function	No function	Interrupt (jump to address 8 at page0)

Note

- PORT70 's interrupt function is controlled by IOCF bit 3. It's falling edge or rising edge trigger (controlled by CONT register bit7).
- PORT7(1~3) 's wakeup functions are controlled by IOCF bit (4,5,7). They are falling edge trigger.
- DETO’s interrupt function is controlled by IOCF bit 6. It’s falling edge trigger, falling and rising edge trigger (set by RD PAGE0 bit 7).

7.4 I/O Port

The I/O registers are bi-directional tri-state I/O ports. The I/O ports can be defined as "input" or "output" pins by the I/O control registers under program control. The I/O data

registers and I/O control registers are both readable and writable. The I/O interface circuit is shown in Fig.17.

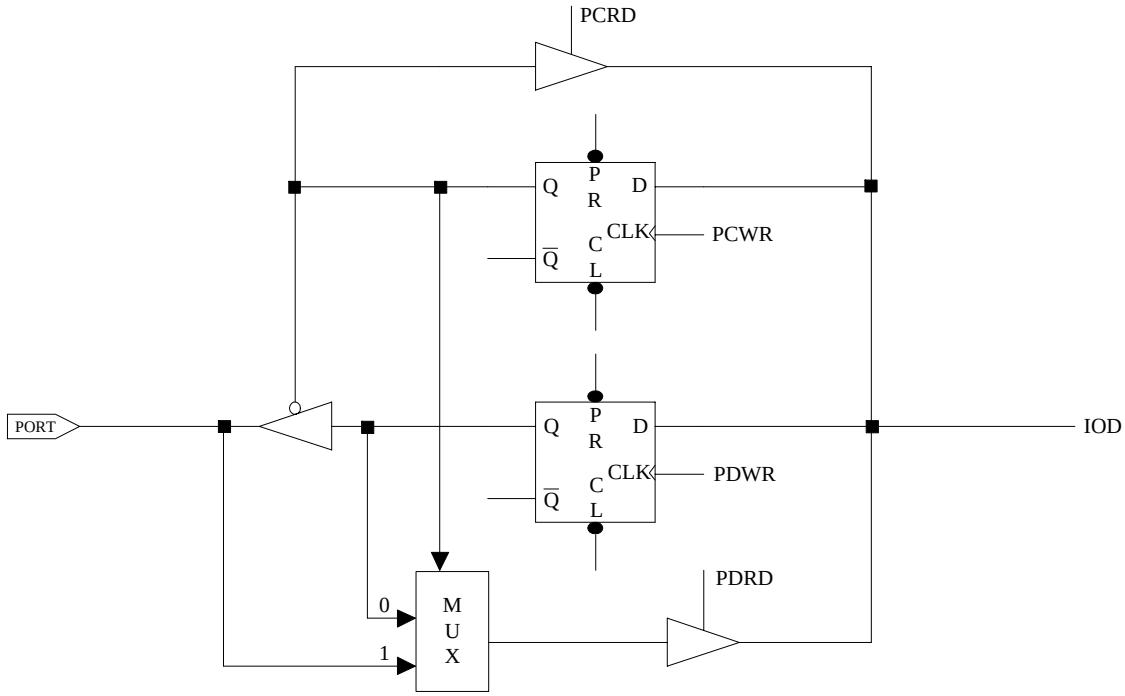


Fig.15 The circuit of I/O port and I/O control register

7.5 RESET

The RESET can be caused by

(1) Power on voltage detector reset (/POVD) and power on reset

(2) WDT timeout. (if enabled and in GREEN or NORMAL mode)

(3) /RESET pin pull low

Note

At case (1), /POVD is controlled by CODE OPTION. If you enable /POVD, CPU will reset at under 1.8V and CPU will consume more current about 5uA. It is used for low voltage reset/ And the power-on reset is a circuit which is always enabled and only works on initially power-on reset. It will reset CPU at about 1.4V and consume about 0.5uA.

Once a RESET occurs, the following functions are performed.

- The oscillator is running, or will be started.
- The Program Counter (R2) is set to all "0".

- When power is on, the upper 3 bits of R3 and the upper 2 bits of R4 are cleared.
- The Watchdog timer and prescaler counter are cleared.
- The Watchdog timer is disabled.
- The CONT register is set to all "1"
- The other register (bit 7 ~ bit 0) default values are as follows.

Operation registers :

Address	R register PAGE0	R register PAGE1	IOC register PAGE0	IOC register PAGE1
0x4	00xxxxxx			
0x5	xx0x0000	xxxx0000	111x0000	00000000
0x6	xxxxxxxx	xxxxxxxx	11111111	000000xx
0x7	xxxxxxxx	xxxxxx00	11111111	00000000
0x8	xxxxxxxx	00000000	11111111	00000000
0x9	xxxxxxxx	xxxxxxxx	11111111	0000000x
0xA	00011x00	11111111	00000000	00000xxx
0xB				
0xC	xxxxxxxx	00000000	xxxxxxxx	xxxxx0xx
0xD	0xxxx000	00000000	00000000	00000000
0xE	xxxx0000	11111111	xxxxx000	00000000
0xF	00000000		00000000	

7.6 Wake-up

The controller has two types of sleep mode for power saving:

7.6.1 SLEEP mode, RA(7) = 0 + "SLEP" instruction

The controller will turn off all the CPU and crystal. Other circuit with power control like key tone control or PLL control (which has an enable register), you have to turn it off by software.

7.6.2 IDLE mode, RA(7) = 1 + "SLEP" instruction.

The controller will turn the CPU off, but not the crystal.

Wake-up from SLEEP mode

WDT time out

External interrupt

7.6.3 /RESET pull low

All these cases will reset the controller, and run the program at address zero. The status is just like the power on reset. Be sure to enable the circuit in case (1) or (2).

Wake-up from IDLE mode

(1) WDT time out

(2) External interrupt

(3) Internal interrupt like counters

For all these cases, you have to enable the circuit before entering IDLE mode. After wake-up, all the registers will keep the values just like with "SLEP" instruction before.

In case (2) or (3), the controller will wake up and jump to address 0x08 for interrupt sub-routine. After finishing a sub-routine ("RETI" instruction), the program will jump to the next instruction from "SLEP" instruction.

7.7 Interrupt

RF is an interrupt status register which records the interrupt request in flag bit. IOCF is an interrupt mask register. Global interrupt is enabled by ENI instruction and is disabled by DISI instruction. When one of the interrupts (when enabled) is generated, it will allow the next instruction to be fetched from address 008H. Once in the interrupt service routine, the source of the interrupt can be determined by polling the flag bits in the RF register.

The interrupt flag bit must be cleared by software before leaving the interrupt service routine and enabling interrupts to avoid recursive interrupts.

7.8 Instruction Set

Instruction set has the following features:

(1) Every bit of any register can be set, cleared, or tested directly.

(2) The I/O register can be regarded as a general register. That is, the same instruction can operate on the I/O register.

The symbol "R" represents a register designator which specifies which one of the 64 registers (including operational registers and general purpose registers) is to be utilized by the instruction. Bits 6 and 7 in R4 determine the selected register bank. "b" represents a bit field designator which selects the number of the bit, located in the register "R", affected by the operation. "k" represents an 8 or 10-bit constant or literal value.

INSTRUCTION BINARY	HEX	MNEMONIC	OPERATION	STATUS AFFECTED	Instruction Cycle
0 0000 0000 0000	0000	NOP	No Operation	None	1
0 0000 0000 0001	0001	DAA	Decimal Adjust A	C	1
0 0000 0000 0010	0002	CONTW	A → CONT	None	1
0 0000 0000 0011	0003	SLEP	0 → WDT, Stop oscillator	T,P	1
0 0000 0000 0100	0004	WDTC	0 → WDT	T,P	1
0 0000 0000 rrrr	000r	IOW R	A → IOCR	None	1
0 0000 0001 0000	0010	ENI	Enable Interrupt	None	1
0 0000 0001 0001	0011	DISI	Disable Interrupt	None	1
0 0000 0001 0010	0012	RET	[Top of Stack] → PC	None	2
0 0000 0001 0011	0013	RETI	[Top of Stack] → PC Enable Interrupt	None	2
0 0000 0001 0100	0014	CONTR	CONT → A	None	1
0 0000 0001 rrrr	001r	IOR R	IOCR → A	None	1
0 0000 0010 0000	0020	TBL	R2+A → R2 bits 9,10 do not clear	Z,C,DC	2
0 0000 01rr rrrr	00rr	MOV R,A	A → R	None	1
0 0000 1000 0000	0080	CLRA	0 → A	Z	1
0 0000 11rr rrrr	00rr	CLR R	0 → R	Z	1
0 0001 00rr rrrr	01rr	SUB A,R	R-A → A	Z,C,DC	1
0 0001 01rr rrrr	01rr	SUB R,A	R-A → R	Z,C,DC	1
0 0001 10rr rrrr	01rr	DECA R	R-1 → A	Z	1
0 0001 11rr rrrr	01rr	DEC R	R-1 → R	Z	1
0 0010 00rr rrrr	02rr	OR A,R	A ∨ VR → A	Z	1
0 0010 01rr rrrr	02rr	OR R,A	A ∨ VR → R	Z	1
0 0010 10rr rrrr	02rr	AND A,R	A & R → A	Z	1
0 0010 11rr rrrr	02rr	AND R,A	A & R → R	Z	1
0 0011 00rr rrrr	03rr	XOR A,R	A ⊕ R → A	Z	1
0 0011 01rr rrrr	03rr	XOR R,A	A ⊕ R → R	Z	1
0 0011 10rr rrrr	03rr	ADD A,R	A + R → A	Z,C,DC	1
0 0011 11rr rrrr	03rr	ADD R,A	A + R → R	Z,C,DC	1
0 0100 00rr rrrr	04rr	MOV A,R	R → A	Z	1
0 0100 01rr rrrr	04rr	MOV R,R	R → R	Z	1
0 0100 10rr rrrr	04rr	COMA R	/R → A	Z	1
0 0100 11rr rrrr	04rr	COM R	/R → R	Z	1
0 0101 00rr rrrr	05rr	INCA R	R+1 → A	Z	1
0 0101 01rr rrrr	05rr	INC R	R+1 → R	Z	1
0 0101 10rr rrrr	05rr	DJZA R	R-1 → A, skip if zero	None	2 if skip

INSTRUCTION BINARY	HEX	MNEMONIC	OPERATION	STATUS AFFECTED	Instruction Cycle
0 0101 11rr rrrr	05rr	DJZ R	R-1 → R, skip if zero	None	2 if skip
0 0110 00rr rrrr	06rr	RRCA R	R(n) → A(n-1) R(0) → C, C → A(7)	C	1
0 0110 01rr rrrr	06rr	RRC R	R(n) → R(n-1) R(0) → C, C → R(7)	C	1
0 0110 10rr rrrr	06rr	RLCA R	R(n) → A(n+1) R(7) → C, C → A(0)	C	1
0 0110 11rr rrrr	06rr	RLC R	R(n) → R(n+1) R(7) → C, C → R(0)	C	1
0 0111 00rr rrrr	07rr	SWAPA R	R(0-3) → A(4-7) R(4-7) → A(0-3)	None	1
0 0111 01rr rrrr	07rr	SWAP R	R(0-3) ↔ R(4-7)	None	1
0 0111 10rr rrrr	07rr	JZA R	R+1 → A, skip if zero	None	2 if skip
0 0111 11rr rrrr	07rr	JZ R	R+1 → R, skip if zero	None	2 if skip
0 100b bbrr rrrr	0xxx	BC R,b	0 → R(b)	None	1
0 101b bbrr rrrr	0xxx	BS R,b	1 → R(b)	None	1
0 110b bbrr rrrr	0xxx	JBC R,b	if R(b)=0, skip	None	2 if skip
0 111b bbrr rrrr	0xxx	JBS R,b	if R(b)=1, skip	None	2 if skip
1 00kk kkkk kkkk	1kkk	CALL k	PC+1 → [SP] (Page, k) → PC	None	2
1 01kk kkkk kkkk	1kkk	JMP k	(Page, k) → PC	None	2
1 1000 kkkk kkkk	18kk	MOV A,k	k → A	None	1
1 1001 kkkk kkkk	19kk	OR A,k	A ∨ k → A	Z	1
1 1010 kkkk kkkk	1Akk	AND A,k	A & k → A	Z	1
1 1011 kkkk kkkk	1Bkk	XOR A,k	A ⊕ k → A	Z	1
1 1100 kkkk kkkk	1Ckk	RETL k	k → A, [Top of Stack] → PC	None	2
1 1101 kkkk kkkk	1Dkk	SUB A,k	k-A → A	Z,C,DC	1
1 1110 0000 0001	1E01	INT	PC+1 → [SP] 001H → PC	None	1
1 1110 1000 kkkk	1E8k	PAGE k	K->R5(3:0)	None	1
1 1111 kkkk kkkk	1Fkk	ADD A,k	k+A → A	Z,C,DC	1

7.9 CODE Option Register

The controller has one 13-bit CODE option register which is not part of the normal program memory. The option bits cannot be accessed during normal program execution.

Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
-	-	-	-	-	-	-	-	-	-	LCDOPT	ROMSEL	/POVD

Bit 0(/POVD) : Power on voltage detector, 0/1 ➔ enable/disable

This bit is fixed to 1 for disable.

Bit 1(ROMSEL) : 16k ROM/8k ROM option, 0/1 ➔ 16k/8k ROM selection

This bit is fixed to 0 for 16K ROM.

Bit 2 (LCDOPT) : LCD output waveform option

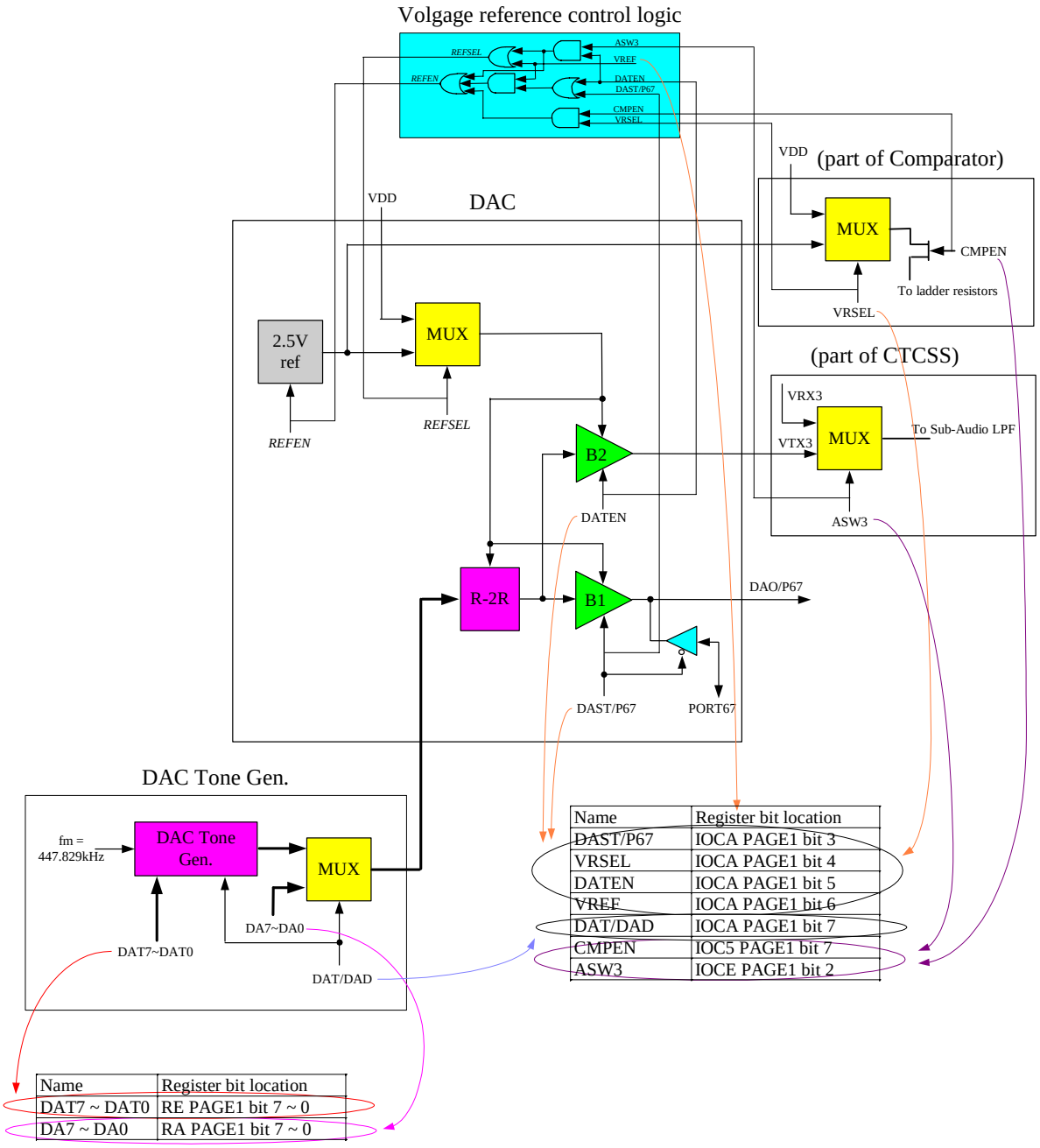
0 ➔ default LCD waveform for Type0 LCD waveform

1 ➔ switch over LCD bias V1 and V2 of segment for Type1 LCD waveform

This bit is fixed to 1 for Type1 LCD waveform

Bit 3 ~ Bit 12 : unused

7.10 Signal and control paths for DAC, DAC tone gen., CTCSS and Comparator



Name	Register bit location
DAST/P67	IOCA PAGE1 bit 3
VRSEL	IOCA PAGE1 bit 4
DATEN	IOCA PAGE1 bit 5
VREF	IOCA PAGE1 bit 6
DAT/DAD	IOCA PAGE1 bit 7
CMPEN	IOC5 PAGE1 bit 7
ASW3	IOCE PAGE1 bit 2

Name	Register bit location
DAT7 ~ DAT0	RE PAGE1 bit 7 ~ 0
DA7 ~ DA0	RA PAGE1 bit 7 ~ 0

Fig.16 Signal and control paths for analog circuit

ps. REFEN, REFSEL are not register bits.

The Fig.16 above try to explain how to use built-in 8-bit R-2R DAC. This DAC can be used as general DAC; here is call “DAC general mode”. Also it can be used as FRS CTCSS tone generation; here is called DAC tone generator mode. When you use DAC general mode, you have to software program DAC input data DA7 ~ DA0 bits with different points of value for tone generation. When you use DAC tone generator mode, you just need to set DAT7 ~ DAT0 bits and then the hardware “DAC Tone Gen.” will auto-program DAC to generate corresponding frequency signal output. Using this feature, it is easy and software free to generate accurate CTCSS tone.

7.10.1 DAC program mode：

The below item “1” is for DAC general mode. The below item “2,3” are for DAC tone generator mode.

(1) DAT/DAD = 0 ➔ DAC general mode, software-program DAC from DA7 ~ DA0 register bits , disable DAC tone generator。

(2) DAT/DAD = 1 ➔ DAC tone generator mode, hardware-program DAC by setting DAT7 ~ DAT0 register bits, enable DAC tone generator。

(3) DAT7 ~ DAT0 = 0 ➔ Disable DAC tone generator。

7.10.2 DAC output paths：

DAST/P67 is used to enable DAC output buffer B1. DATEN is used to enable DAC output buffer B2.

(1) External：DAC output from its output buffer B1 to DAO/P67 pin。

DAST/P67 = 1 ➔ power on DAC, enable DAC output buffer B1, output sent to DAO/P67 pin。

(2) Internal：DAC output from its output buffer B2 to CTCSS Sub-audio LPF。

DATEN = 1 ➔ power on DAC, enable DAC output buffer B2, output sent to CTCSS VTX3。

7.10.3 Using 2.5V ref and DAC

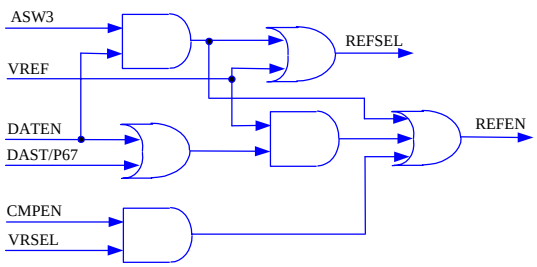


Fig.17 Voltage reference control logic

"2.5V ref." is the reference voltage used in DAC, Comparator or CTCSS. The voltage reference control logic process these combination use. For this reference used in Comparator, you just only take care of CMPEN and VRSEL bits. For this reference used in others, you need to set ASW3, VREF, DATEN and DAST/P67. The following table shows the least two bits setting to logic "1" (CMPEN=VRSEL=1 or ASW3=DATEN=1 or VREF=DATEN=1 or VREF=DAST/P67=1) will "select 2.5V and enable 2.5V ref".

When REFSEL = 1, the 2.5V ref is select not VDD. (select 2.5V ref)

When REFEN = 1, the 2.5V ref is power on. (2.5V ref enable)

ASW3	VREF	DATEN	DAST/P67	CMPEN	VRSEL	Function
x	x	x	x	1	1	select 2.5V ref, enable 2.5V ref, enable Comparator
1	x	1	x	x	x	select 2.5V ref, enable 2.5V ref, enable DAC,
0	1	1	x	x	x	enable buffer B2, buffer B2 output to CTCSS LPF
x	1	0	1	x	x	select 2.5V ref, enable 2.5V ref, enable DAC, enable buffer B1, buffer B1 output to DAO/P67 pin

7.10.4 Select DAO/P67 pin as normal I/O P67

Set DAST/P67 = 0 to select normal I/O P67.

7.10.5 Using DAC general mode

DAT/DAD = 0 ➔ select DAC general mode。

Program DA7 ~ DA0。

Enable DAC, enable DAC output buffer, select DAC reference source。

7.10.6 Using DAC tone generator mode

(1) DAT/DAD = 1 ➔ select DAC tone generator mode。

(2) Program DAT7 ~ DAT0 = 1 to 255. (If DAT7 ~ DAT0 = 0, DAC tone gen. is disabled.)。

(3) Enable DAC, enable DAC output buffer, select DAC reference source。

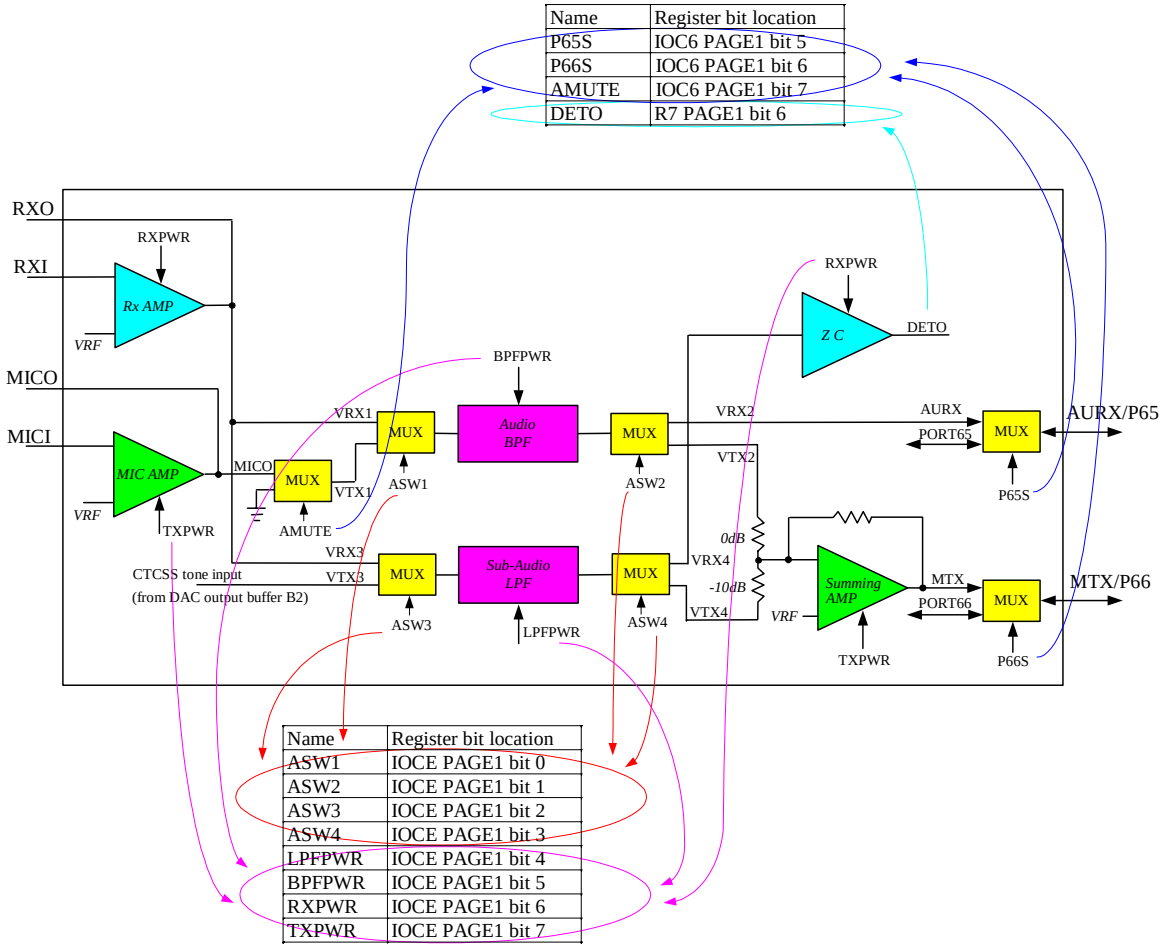
Ps. When DAC tone output is set to CTCSS Sub-audio LPF(ASW3=DATEN=1 or VREF=DATEN=1), it will be forced to select 2.5V ref by voltage reference control logic.

When its output is set to DAO/P67 pin, reference voltage can be selected as VDD or 2.5V.

Ref to Page 18,19 for CTCSS tone generation table.

7.11 CTCSS block

7.11.1 Block control and signal flow description



CTCSS block on page 36 Fig.14 is the key feature for FRS baseband signal processing. For receiving path, it receives the RF demodulator output signal and extract the audio output signal to AURX pin. Also it decodes CTCSS tone and its decoding data is shown in the DETO. For transmitting path, it combines audio signal from Mic Amp and CTCSS signal from DAC tone generator(as description in VII.9 section) thru MTX output to RF modulator input end. CTCSS block consists of amplifiers, analog switch, filters and zero-crossing detector which descriptions are shown below.

RX AMP : (Receiving amplifier) It accepts RF demodulator output signals which combine demodulated audio and CTCSS tone. Its bias voltage is VDD/2.

MIC AMP : (Microphone amplifier) It is the audio input amplifier. Its bias voltage is VDD/s.

MUX : (Analog multiplexer switch) It is used for analog signal path switching.

Audio BPF : (Audio band pass filter) This audio BPF has pass band 300Hz ~ 3.4kHz. It is used to let audio signal pass through and filter out CTCSS tones. It plays an important role in extracting audio signal. Also it cut out unwanted signal while audio signal transmitting.

Sub-Audio LPF : (Sub-audio low pass filter) This sub-audio LPF has pass band 253Hz. It is used to let CTCSS tone pass through and filters out audio signal. It plays an important in extracting CTCSS tone. Also it cut out unwanted signal while CTCSS tone transmitting.

Summing AMP : (Summing amplifier) It is an analog signal mixer for audio signal and CTCSS tone transmitting. CTCSS tone will be attenuated about 10dB before signal mixing.

ZC : (Zero-crossing detector) This detector transforms CTCSS tone signal from analog form to digital form. It will be the CTCSS tone detection.

Description for register control bits

ASW1 ~ ASW4 for analog input/output signal path switching

RXPWR for power control of receiving RX AMP and ZC

TXPWR for power control of transmitting MIC AMP and Summing AMP

AMUTE for MIC AMP output signal muting

P65S for receiving audio output pin AURX or port P65 pin switching

P66S for transmitting output pin MTX or port P66 pin switching

The following is the above CTCSS block signal flow and it is easy to use these figures to explain how CTCSS works. (‘blue’ highlight means signal flow and switch setting)

(1) RX : receiving CTCSS tone

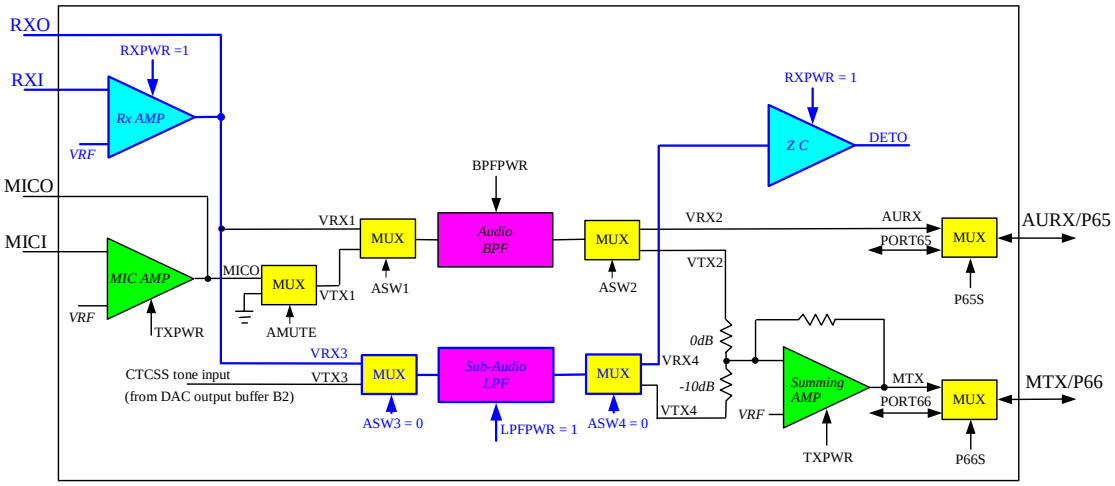


Fig.18

(2) RX : receiving audio

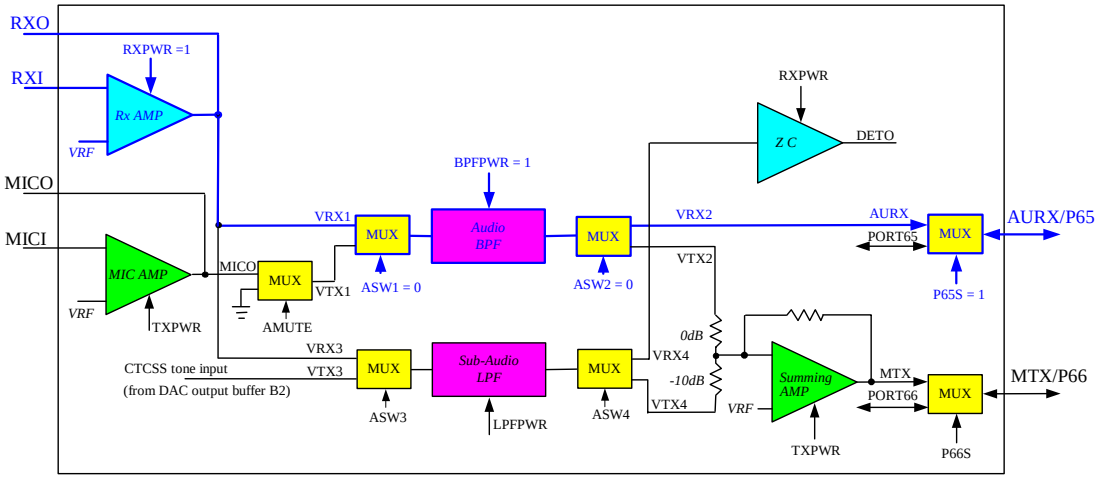


Fig.19

(3) TX : transmitting audio

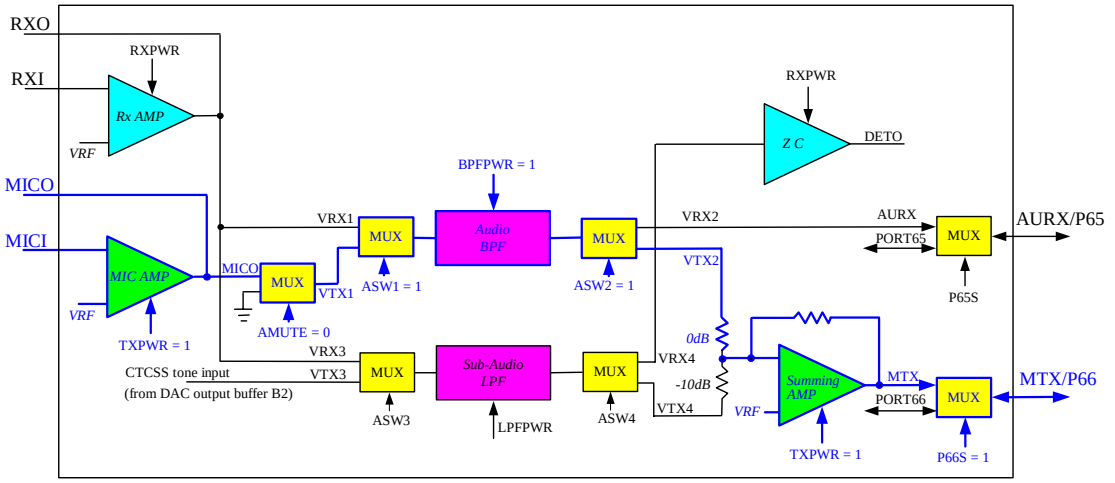


Fig.20

(4) TX : transmitting CTCSS tone

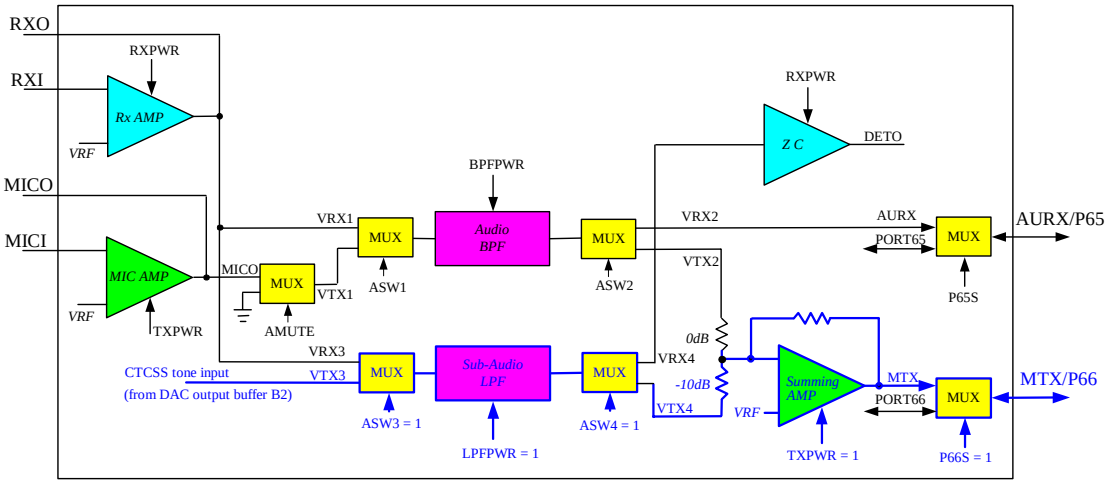


Fig.21

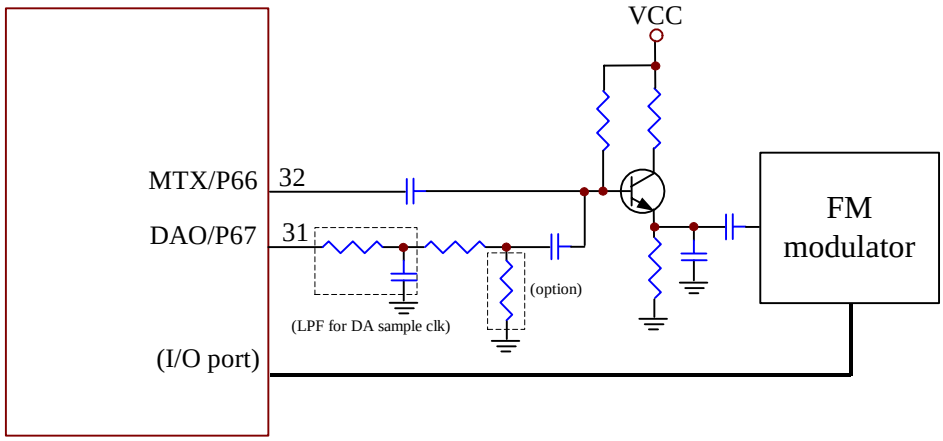
7.11.2 Special application on Audio/CTCSS tone mixing output

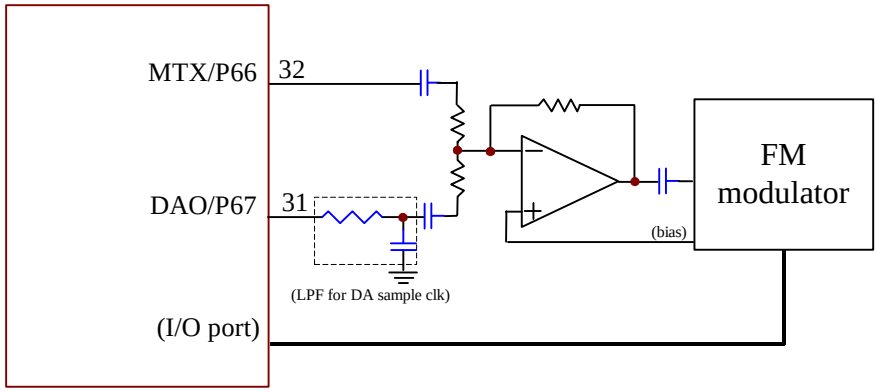
Generally speaking, users can use a built-in DAC tone generator (described in VII.9) to generate CTCSS tone accompanied with audio on MTX/P66 pin output without any problem. For some customers, due to modulation index criteria of their FM modulator cannot accept built-in CTCSS tone because this level is too large for them to use.

In this case, there are two ways to solve this problem :

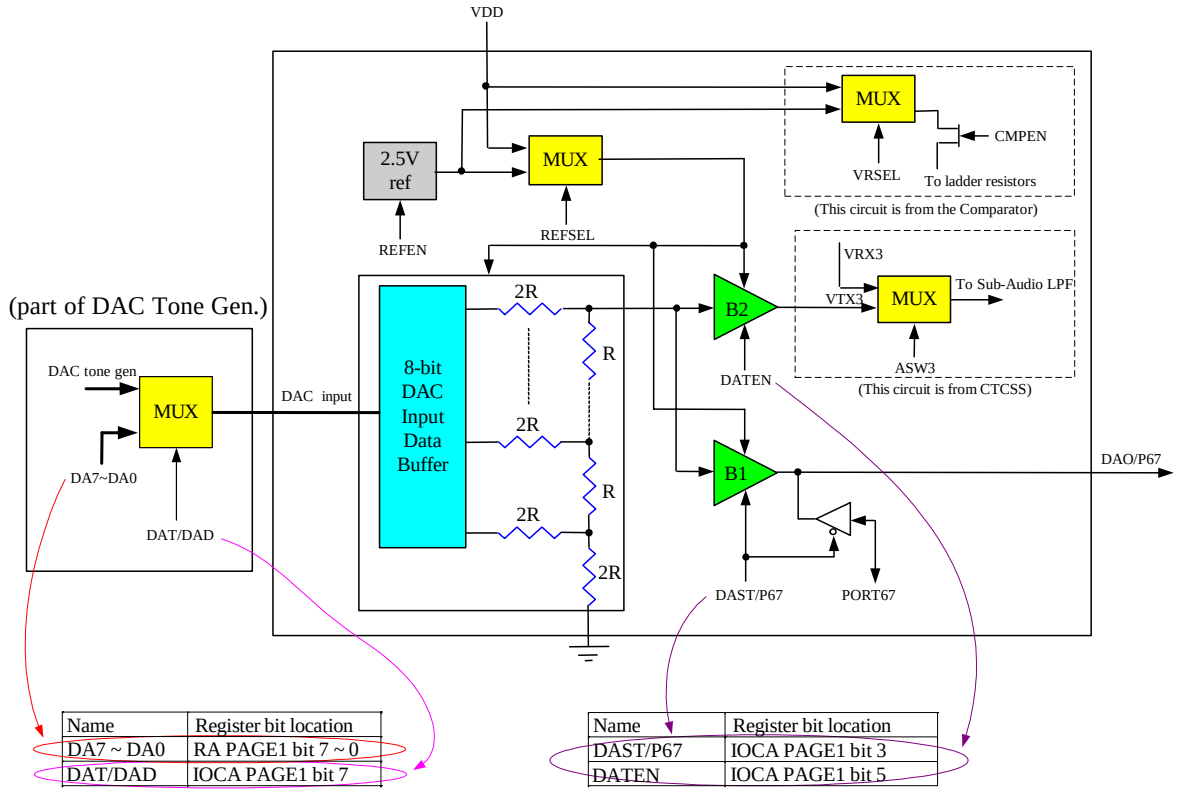
(1) One way is not to use built-in DAC tone generator but need to program the built-in DAC to generate CTCSS tone by user software algorithm. User software algorithm can normalize the final CTCSS tone level to their requirement without adding any external elements.

(2) The other way is still to use a built-in DAC tone generator but needs some external components to attenuate the CTCSS tone on the DAO/P67 pin. Program some control bits to output CTCSS tone on the DAO/P67 pin, refer to VII.9 (3) description. Since DAO/P67 output is a stair-case waveform, we need to put simple RC LPF circuit to smooth the output waveform before going to the CTCSS attenuation circuit. RC LPF also has some attenuation effect. It depends on its cut-off frequency of LPF. You can design it on your own. There are two circuits suggested for your reference.


VCC
MTX/P66
32
DAO/P67
31
(LPF for DA sample clk)
(option)
FM
modulator
(I/O port)


MTX/P66
32
DAO/P67
31
(LPF for DA sample clk)
(bias)
FM
modulator
(I/O port)

7.128-bit R-2R DAC



Name	Register bit location
DA7 ~ DA0	RA PAGE1 bit 7 ~ 0
DAT/DAD	IOCA PAGE1 bit 7

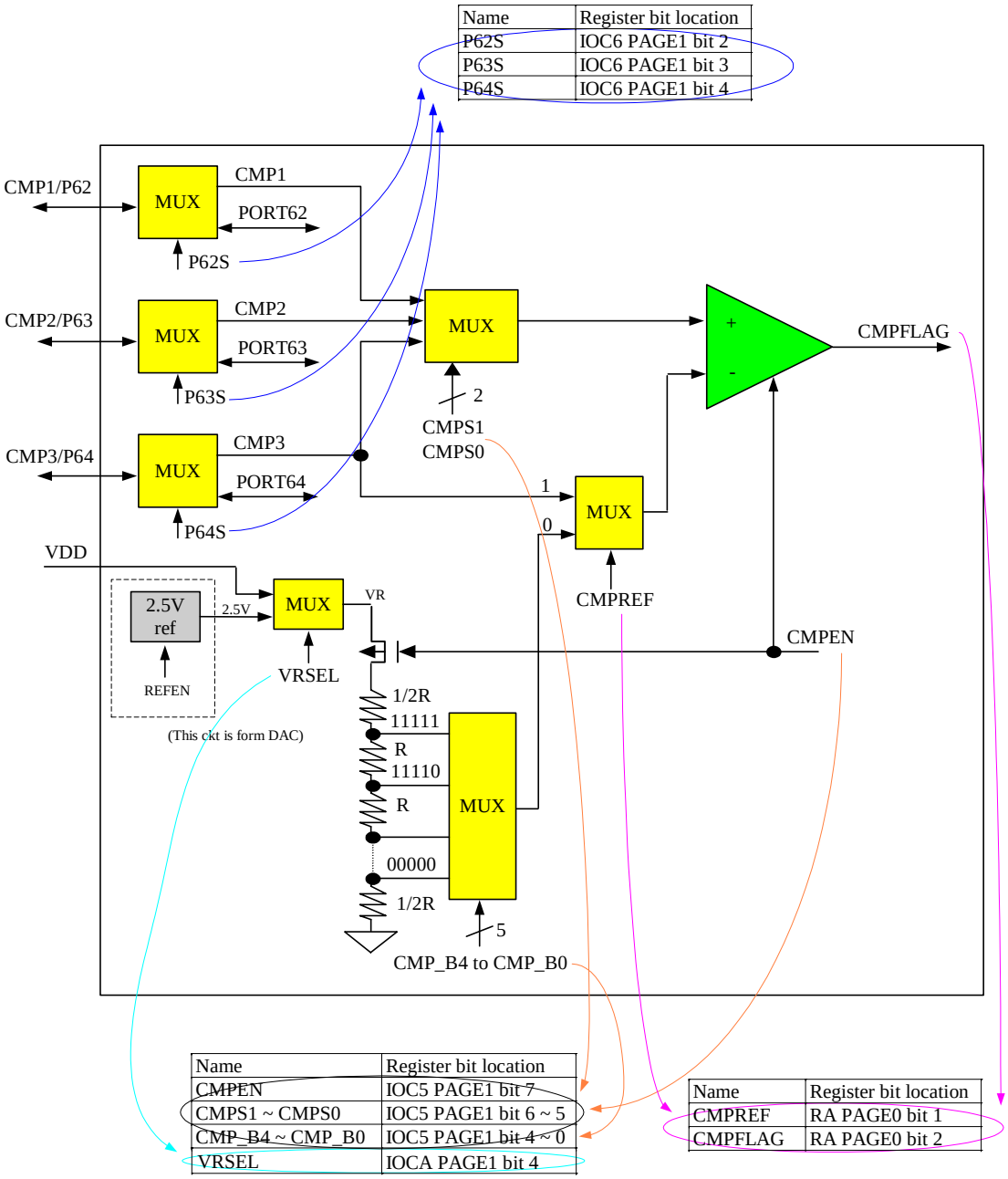
Name	Register bit location
DAST/P67	IOCA PAGE1 bit 3
DATEN	IOCA PAGE1 bit 5

Fig.22 DAC block

Refer to “Voltage reference control logic” to set the DAC reference.

In DAC tone generator mode, you can retrieve the CTCSS tone output. In other case, DAC is useful in general tone generation such as key tone, alert tone, music and so on. In DAC general mode, only VREF and DAST/P67 bits are relative to DAC reference voltage. DAC reference voltage comes from VDD or 2.5V ref. Setting VREF bit (IOCE PAGE1 bit 6) = 0/1 to select VDD/2.5V as reference. Set the DAST/P67 bit=1 to power on the DAC and also enable the output buffer B1. After that, the DAC output signal will be sent to DAO/P67 pin.

7.13 4-bit Comparator



This comparator is not only a single comparator. It consists of 16-R resistor string, 3-channel input and optional external comparison reference source input. The 16-R resistor string acts as a 16-level voltage divider of which top voltage reference can be selected from VDD or 2.5V ref. Use the above register bits to set the whole job. This comparator is used in some applications such as voltage detection, RSSI level, sensor output level and other slow signal level transition detection and so on. This comparator can be called a simple 4-bit low speed ADC but the sampling time is determine by

software. For AC frequency detection, it is limited by its output comparator structure. AC frequency below 1kHz is recommended.

7.14 Programming Tone Generators

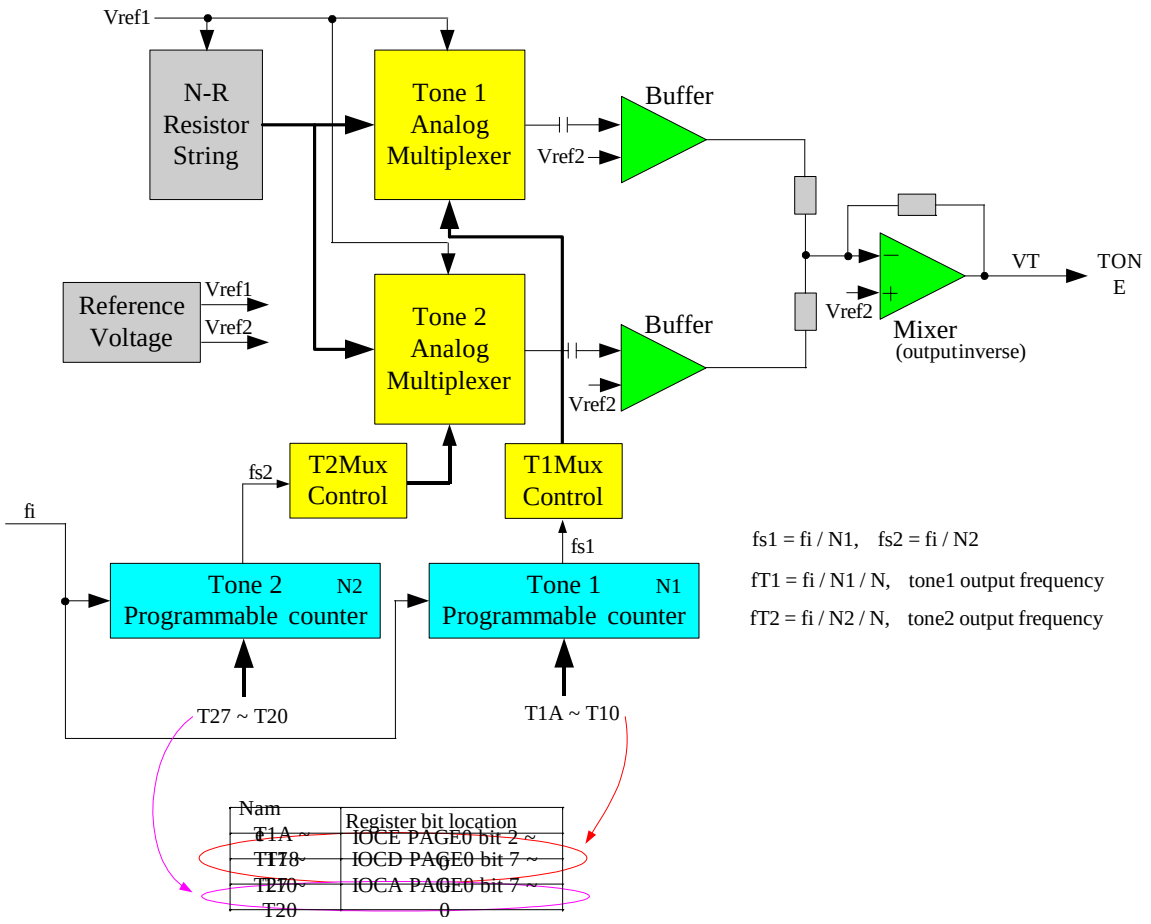


Fig.23 Programming Tone Generator

Programming tone generators are universal dual tone generators. It includes Tone 1 and Tone 2 generators which can be combined as dual tone output or either one tone output. The clock source fi comes from PLL and is divided to the required ratio. Tone 1 and Tone 2 are sinewave output. The programming tone generators consist of Tone 1/2 programmable counters, analog multiplexer, N-R resistor string, output buffers, mixer amplifier and reference voltage. N-R resistor is a voltage divider which has different output levels. By programmable counters and analog multiplexer, the hardware will automatically generate individual divider output with circular order back and forth. The output frequency is 119957/N1 for Tone 1 and 11.957/N2 for Tone 2, where N1 is 11-bit T1A ~ T10 and N2 is 8-bit T17 ~ T10.

8 Absolute Maximum Ratings

RATING	SYMBOL	VALUE	UNIT
DC Supply Voltage	VDD	-0.3 To 6	V
Input Voltage	V_{IN}	-0.5 to VDD +0.5	V
Operating Temperature Range	Ta	-30 to 70	℃

9 DC Electrical Characteristic

(Ta = 0°C ~ 70°C, AVDD=VDD=5V±5%, VSS=0V)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input leakage current for input pins	IIL1	VIN = VDD, VSS			±1	μA
Input leakage current for bi-directional pins	IIL2	VIN = VDD, VSS			±1	μA
Input high voltage	VIH		2.5			V
Input low voltage	VIL				0.8	V
Input high threshold voltage	VIHT	/RESET, TCC	2.0			V
Input low threshold voltage	VILT	/RESET, TCC			0.8	V
Clock input high voltage	VIHX	OSCI	3.5			V
Clock input low voltage	VILX	OSCI			1.5	V
Output high voltage for PORT 5, 6, 7, 8	VOH1	IOH = -5mA	2.4			V
Output high voltage for PORT 9, C	VOH2	IOH = -8 mA	2.4			V
Output low voltage for PORT 5, 6, 7,8	VOL1	IOH = 5mA			0.4	V
Output low voltage for PORT 9, C	VOL2	IOH = 8 mA			0.4	V
LCD drive reference voltage	VLCD	VDD=5V, Contrast adjust		4 ~ 5		V
Pull-high current	IPH	Pull-high active input pin at VSS		-10	-15	μA
Power down current (SLEEP mode)	ISB1	All input and I/O pin at VDD, Output pin floating, WDT disabled		1	5	μA
Low clock current (GREEN mode)	ISB2	CLK=32.768kHz, All analog circuits disabled, All input and I/O pin at VDD, output		35	50	μA
Low clock current (IDLE mode)	ISB3	CLK=32.768kHz, All analog circuits disabled, All input and I/O pin at VDD, output		30	45	μA

Operating supply current (Normal mode)	ICC1	/RESET=High, CLK=3.582MHz, All analog circuits disabled, Output pin floating		1	2	mA
Tone generator reference voltage	Vref2	VREG is regulator output	0.5		0.7	VREG
Tone1 signal strength	V1rms	Root mean square voltage	130	155	180	mV
Tone2 signal strength	V2rms	Root mean square voltage	1.259V1rms			mV

2.5Vref for Comparator or DAC

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Internal 2.5V ref. voltage.	2.5VREF	VDD=5V, 25 deg	2.32	2.46	2.58	V
		VDD=3V, 25 deg	2.22	2.36	2.48	V
Reference voltage linearity	△2.5VREF/△VDD	VDD=5.5V ~ 3.0V, 5 deg		5	8	%
		VDD=3.0V ~ 2.7V, 25 deg		8	15	%

Effective VDD reference for Comparator or DAC

Parameter	Symbol	Condition	Min	Typ	Max	Unit
VDD ref. voltage	VDDref	VDD=5V ~ 2.7V, - 20 ~ +50 deg	VDD-0.05	VDD-0.02	VDD	V

(Operating current consumption for analog circuit) (Ta = 0°C ~ 70°C, AVDD=VDD=5V±5%, VSS=0V)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Programming Tone Generators						
Operating current for Programming Tone Generators	I_TONE	TONE1 is power on TONE2 is power on		0.35	0.6	mA
Digital to Analog Converter						
Operating current for DAC	I_DA			0.65	0.9	mA
Comparator						
Operating current for Comparator	I_CMP			70	120	µA
CTCSS						
Operating current for RX power on	I_RX	RXPWR=1, TXPWR=0 LPFPWR=0, BPFPWR=0		0.7	1.0	mA
Operating current for TX power on	I_TX	RXPWR=0, TXPWR=1 LPFPWR=0, BPFPWR=0		0.12	0.2	mA
Operating current for LPF power on	I_LPF	RXPWR=0, TXPWR=0 LPFPWR=1, BPFPWR=0		0.3	0.5	mA
Operating current for BPF power on	I_BPF	RXPWR=0, TXPWR=0 LPFPWR=0, BPFPWR=1		0.3	0.5	mA

* The spec for the above table does not include the MCU current consumption

10 AC Electrical Characteristic

CPU instruction timing (Ta = -30°C ~ 70°C, AVDD=VDD=5V, VSS=0V)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input CLK duty cycle	Dclk		45	50	55	%
Instruction cycle time	Tins	32.768kHz 3.582MHz		60 550		μs ns
Device delay hold time	Tdrh			16		ms
TCC input period	Ttcc	Note 1	(Tins+20)/N			ns
Watchdog timer period	Twdt	Ta = 25°C		16		ms

Note 1
N= selected prescaler ratio.

OSC and reset timing characteristics (see Fig.25 in page 50 for details)

Description		Symbol	Min	Typ	Max	Unit
Oscillator timing characteristic						
OSC start up	32.768kHz	Toscs	400		1500	ms
	3.579MHz PLL			5	10	us
Reset timing characteristic						
The minimum width of reset low pulse		Trst	3			uS
The delay between reset and program start		Tdrs		18		mS

TONE generators for AC Characteristic (AVDD=VDD=5V,Ta=+25°C)

CHARACTERISTIC	Min	Typ	Max	Unit
Tone1/Tone2 signal strength (root mean square voltage)				
Tone1 signal strength V1rms (ps1) ~= -14dBm (600Ω)	130	155	180	mV
Tone2 signal strength V2rms (ps1) ~ = -12dBm (600Ω)	1.259V1rms			mV
Tone twist				
(Tone1 – Tone2) twist		-2		dB

(ps1) : V1rms and V2rms has 2 dB difference. It means 20log (V2rms/V1rms) = 20log1.259 = 2 (dB)

CTCSS block (AVDD=VDD=5V, Ta=+25°C)

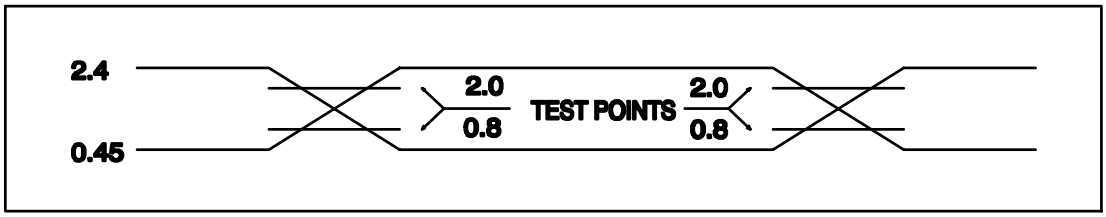
Parameter	Min.	Typ.	Max.	Unit
RX mode				
Zero crossing threshold (mVrms)		20		mV
Data Duty Ratio	30	50	70	%
TX mode				
CTCSS tone (form Tone 2) to VTX3, for 600Ω		-12		dBm
CTCSS tone to MTX, for 600Ω		-22		dBm
Filter				
BPF for Audio				
Pass-Band Frequency	300		3400	Hz
Pass-Band Ripple			1.0	dB
LPF for Sub-Audio				
Pass-Band Frequency	60		253	Hz
Pass-Band Ripple			1.0	dB
Output				
Driving capacity for AURX pin			30	µA
Driving capacity for MTX pin			30	µA
Output loading impedance for AURX pin (Ref. Voltage = 2.5V)	42			kΩ
Output loading impedance for MTX pin (Ref. Voltage = 2.5V)	42			kΩ

Note:

Test under Fig.26 application circuit. Zero crossing threshold means ZC's transition level in Fig.14 CTCSS block. This level is close but not equal to CTCSS receiving sensitivity. The CTCSS receiving sensitivity partially depends on your software judgment. Also CTCSS receiving sensitivity can be adjusted by changing the external resistors of RX AMP in Fig.26 application circuit.

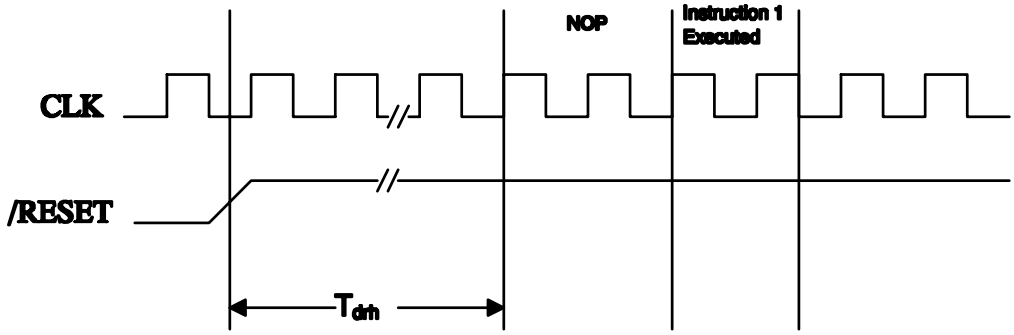
11 Timing Diagrams

AC Test Input/Output Waveform



AC Testing: Input are driven at 2.4V for logic "1", and 0.45V for logic "0". Timing measurements are made at 2.0V for logic "1", and 0.8V for logic "0".

RESET Timing



TCC Input Timing

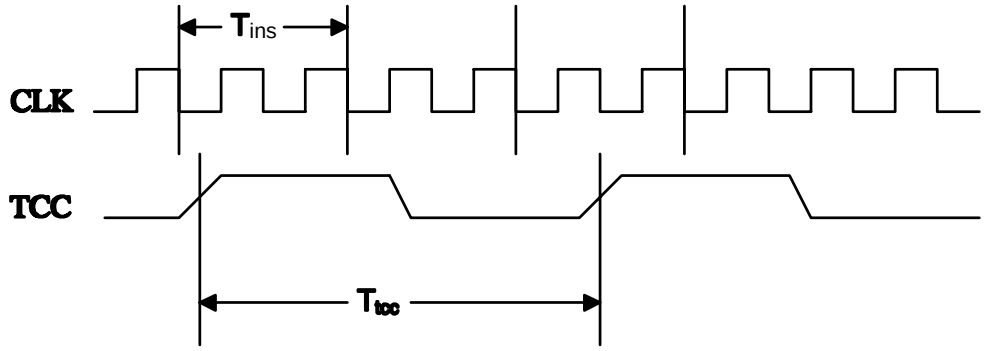


Fig.24 AC Timing

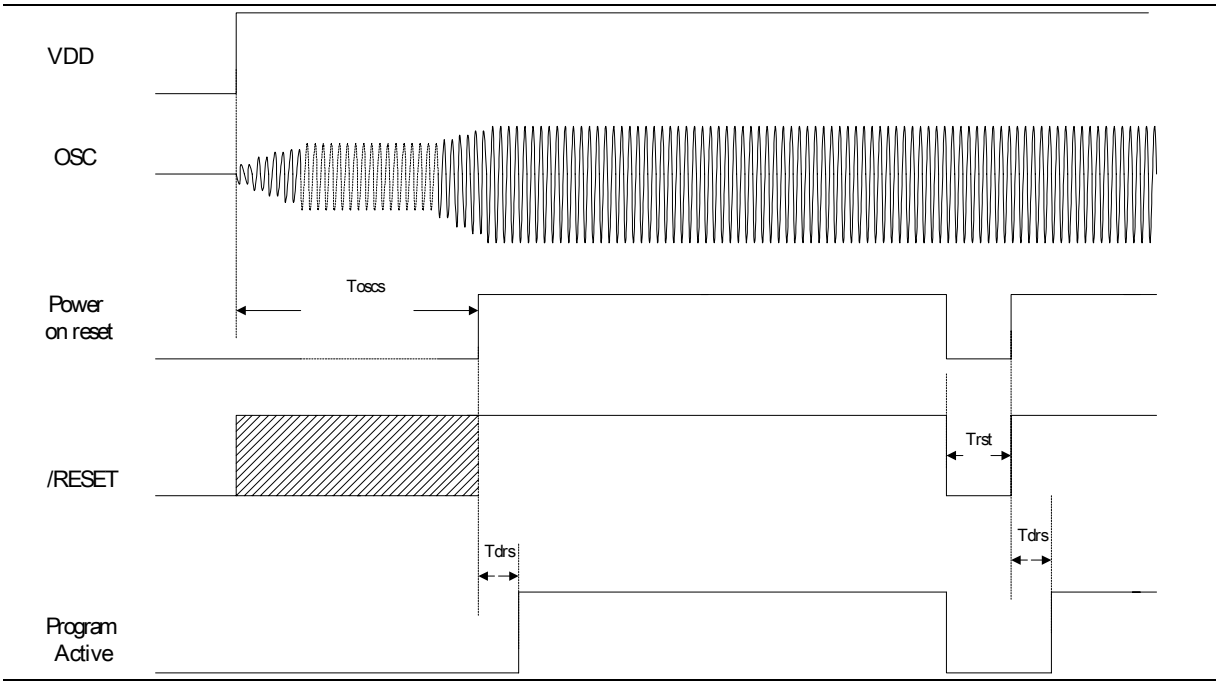


Fig.25 OSC and Reset Timing

12 Application Circuit

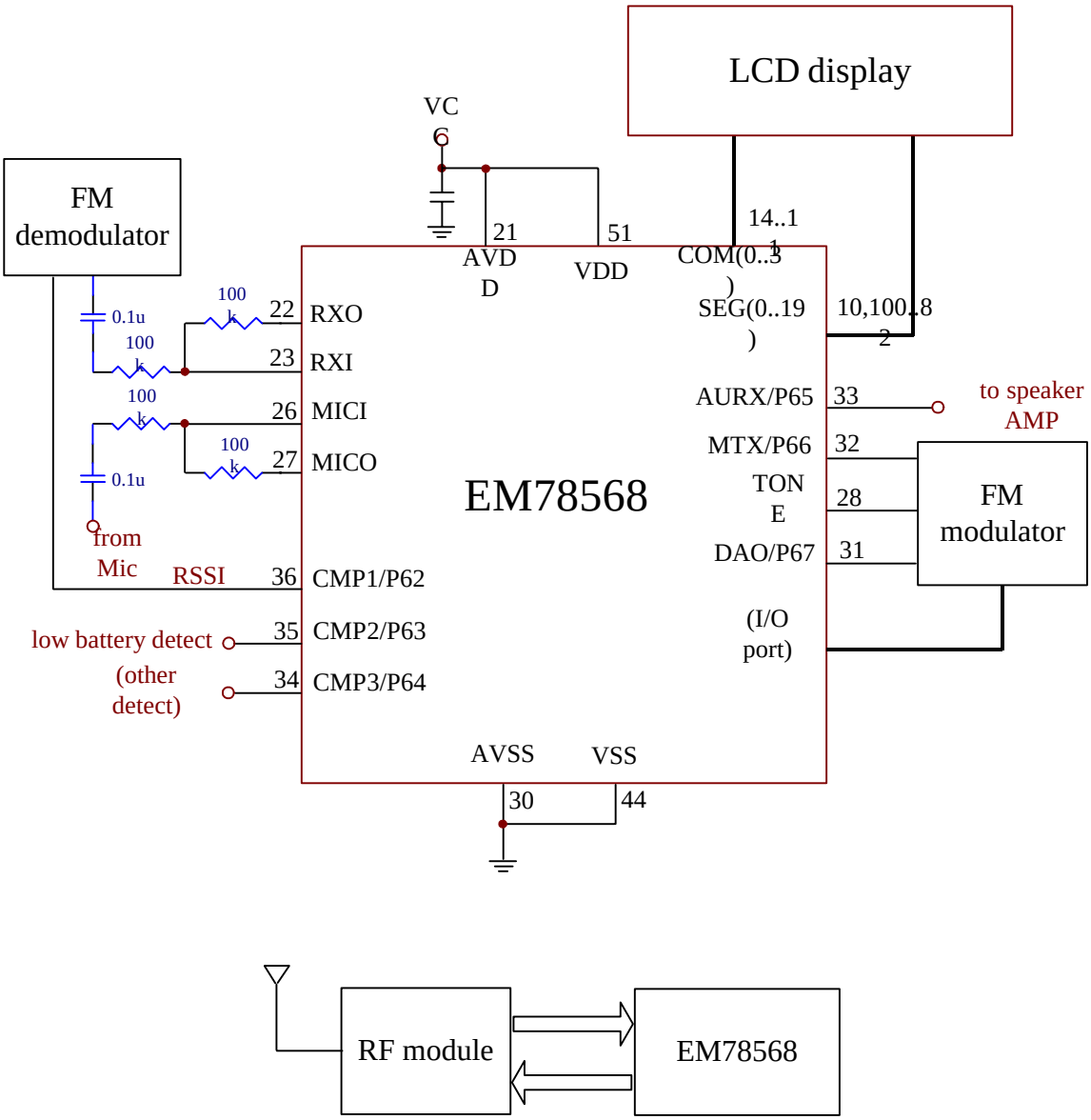


Fig.26 Application Circuit

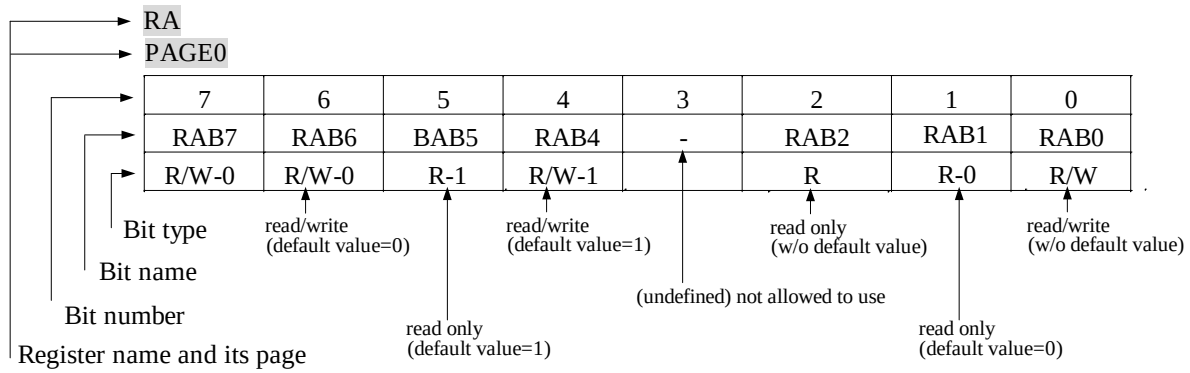
APPENDIX

A User Application Note

(Before using this chip, take a look at the following description note, it includes important messages.)

1. There are some undefined bits in the registers. The values in these bits are unpredictable. These bits are not allowed for use. We use the symbol "-" in the spec to recognize them.

2. You will see some names for the register bits definitions. Some name will appear very frequently in the whole spec. The following describes the meaning for the register's definitions such as bit type, bit name, bit number and so on.



3. While in the ICE programming, the you need to follow the rules :

Let "IOCE PAGE0 Bit 4 ~ Bit 7" retain these values to "0"otherwise it will generate unpredictable interrupts. Let "IOCC PAGE1 Bit 0" keep its value unchanged at "0", otherwise the Comparator and CTCSS function will fail.

4. The function differs between EM78568 and EM78P568.

Function

Item	EM78568	EM78P568
Data RAM	0.5K x 8	1K x 8
I/O	PC0	PC0 ~ PC7 PB0 ~ PB7
LCD driver	SEG0 ~ SEG19	SEG0 ~ SEG31
Package	100-pin QFP,63-pin die	100-Pin QPF, 78-pin die

DC Characteristics

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Internal 2.5V ref.. Voltage	2.5VREF	VDD=5V, 25 deg for EM78568	2.32	2.46	2.58	V
		VDD=5V, 25 deg for EM78P568	2.14	2.26	2.38	V
		VDD=3V, 25 deg for EM78568	2.22	2.36	2.48	V
		VDD=3V, 25 deg for EM78P568	2.04	2.18	2.3	V

5. In the features description, the CPU operating voltage is 2.2 ~ 5.5V, the minimum operating voltage 2.2V is under maximum main clock = 3.5826MHz.