EM78611E

Universal Serial Bus Series Microcontroller

Product Specification

DOC. VERSION 1.1

ELAN MICROELECTRONICS CORP.

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Specification Revision History

Version	Revision Description	Date
1.0	Initial released version	2007/12/27
1.1	1. Remove Pin Assignment. 2. Modified Application Circuit.	2011/11/30

1 General Description

The EM78611E is a series of 8-bit Universal Serial Bus RISC architecture microcontroller. It is specifically designed for USB low speed device application and to support standard devices such as PS/2 keyboard. The EM78611E also supports one device address and three endpoints. With no firmware involved, these series of microcontrollers can automatically identify and decode Standard USB Command to Endpoint Zero.

The EM78611E has eight-level stacks and six interrupt sources. It has a maximum of 12 General Input/Output pins. Each device has 144 bytes of general purpose SRAM, and 6K bytes of program ROM. These series of ICs have Dual Clock mode which allows the device to run on very low power saving frequency.

2 Features

- Operating voltage 4.4V ~ 5.5V
- Low-cost solution for low-speed USB devices, such as keyboard, joystick, and Gamepad.
- USB Specification Compliance
  - Universal Serial Bus Specification Version 1.1
  - USB Device Class Definition for Human Interface Device (HID), Firmware Specification Version 1.1
  - Support 1 device address and 3 endpoints
- USB Application
  - P75 (D-) has an internal pull-high resistor (1.5KΩ)
  - USB protocol handling
  - USB device state handling
  - Identifying and decoding of Standard USB commands to EndPoint Zero
- PS/2 Application Support
  - Built-in PS/2 port interface for keyboard and mouse
- Built-in 8-bit RISC MCU
  - 8-level stacks for subroutine and interrupt
  - 6 available interrupts
  - 8-bit real time clock/counter (TCC) with overflow interrupt
  - Built-in RC oscillator free running for Watchdog Timer and Dual clock mode
  - Two independent programmable prescalers for WDT and TCC

- Two methods of saving power:
  1. Power-down mode (Sleep mode)
  2. Dual clock mode
- Two clocks per instruction cycle
- Multi-time programmable

■ I/O Ports
- Up to 13 LED sink pins
- Each GPIO pin of Ports 5, 6, 8, and 9 have an internal programmable pull-high resistor (25KΩ)
- Each GPIO pin of Port 6, P74 ~ P77 and Port 9 can wakeup the MCU from sleep mode by input state change

■ Internal Memory
- Built-in 6K×13 bits Program ROM
- Built-in 144 bytes general purpose registers (SRAM)
- Built-in USB Application FIFOs

■ Operation Frequency
- Normal Mode: MCU runs at an external oscillator frequency; 6 MHz or 12 MHz
- Dual Clock Mode: MCU runs at a frequency of 256kHz (or 32kHz, 4kHz, 500Hz), emitted by the internal oscillator with the external ceramic resonator turned off to save power.

■ Built-in 3.3V Voltage Regulator
- Pull-up source for the external USB resistor on D-pin.

3 Application

■ USB Keyboard only

■ USB and PS/2 both compatible with Keyboard

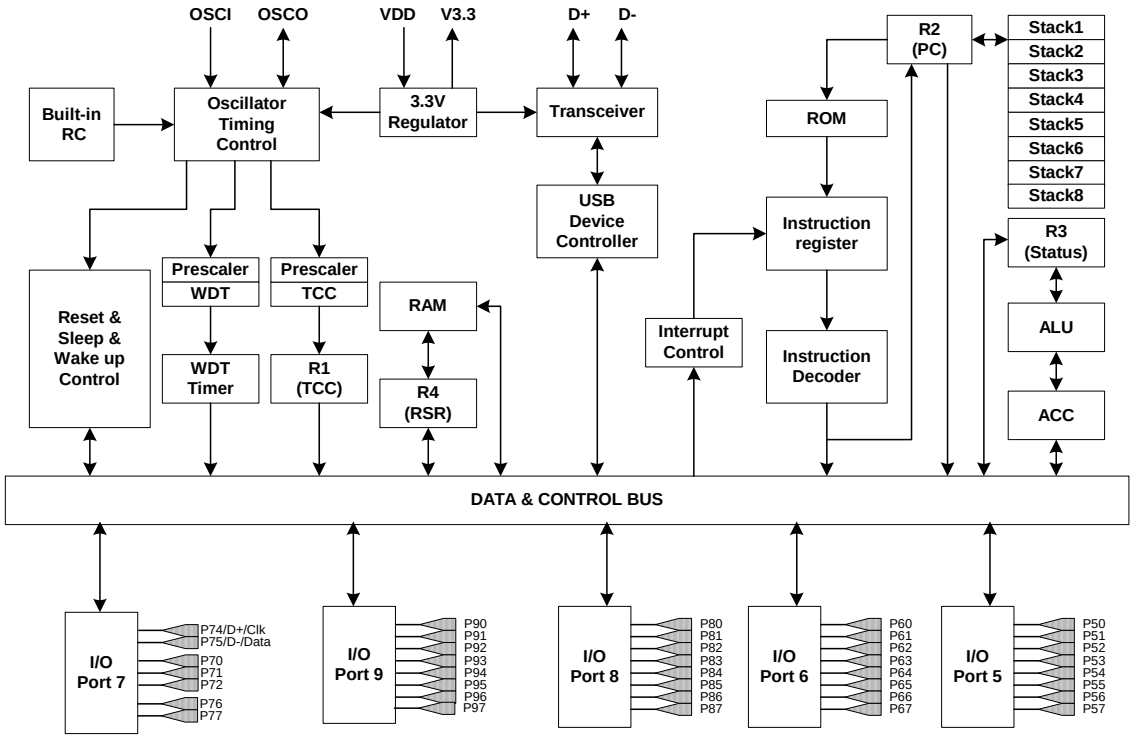
■ USB Keyboard with USB Mouse

■ USB Joystick

4 Pin Description

Pin Number	I/O	Function
P50 ~ P57 P60 ~ P67 P80 ~ P87	I/O	GPIO pins. These pins can be pulled-high internally through software control.
P90 ~ P97	I/O	GPIO pins. These pins can be pulled-high internally through software control or LED sink pins.
P70 ~ P72, P76, P77	I/O	LED sink pins. P76, P77 will have an internal pull-high resistor when the EM78611E is running in PS/2 mode.
D+ / CLK / P74	I/O	USB plus data line interface or CLK for PS/2 keyboard. When the EM78611E is running under PS/2 mode, this pin will have an internal pull-high resistor (2.2KΩ), with V_{DD}=5.0V.
D- / DATA / P75	I/O	USB minus data line interface or Data for PS/2 keyboard. When the EM78611E is running in PS/2 mode, this pin will have an internal pull-high resistor (2.2KΩ), with V_{DD}=5.0V. When the EM78611E is running in USB mode, this pin will have an internal pull-high resistor, 1.5KΩ, with $V_{3.3}$=3.3V.
OSCI	I	6MHz / 12MHz ceramic resonator input.
OSCO	O	Return path for 6-MHz / 12MHz ceramic resonator.
VDD	PWR	Power supply
GND	PWR	Ground
$V_{3.3}$	PWR	3.3V regulator output

5 Block Diagram



6 Function Description

The EM78611E memory is organized into three spaces, namely; User Program memory in 6K×13 bits ROM space, Data Memory in 144 bytes SRAM space, and USB Application FIFOs for EndPoint0, EndPoint1, and EndPoint2. Furthermore, several registers are used for special purposes.

6.1 Program Memory

The program space of the EM78611E is 6K words, and is divided into six pages. Each page is 1K words long. After a reset, the 13-bit Program Counter (PC) points to location zero of the program space.

The Interrupt Vector is at 0x0001 and accommodates TCC interrupt, P74~P77 State Changed interrupt, EndPoint 0 interrupt, USB Suspend interrupt, USB Reset interrupt, and USB Host Resume interrupt.

After an interrupt, the MCU will fetch the next instruction from the corresponding address as illustrated in the following diagram.

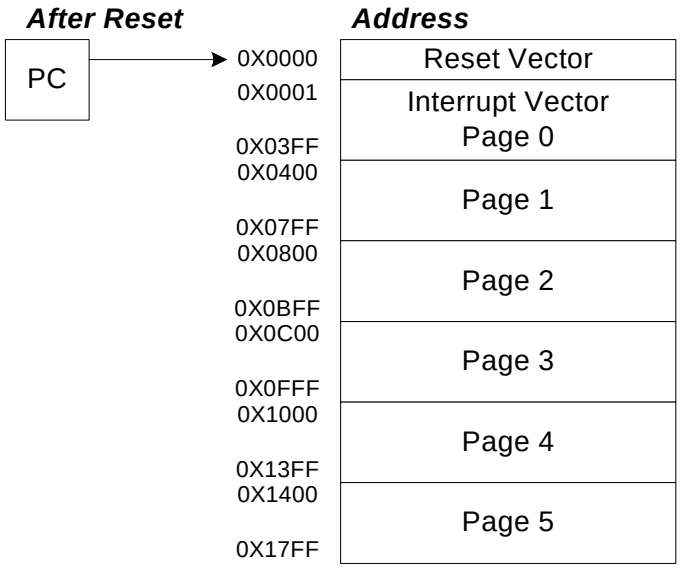


Figure 6-1 Program Memory Space

6.2 Data Memory

The Data Memory has 144 bytes SRAM space. It also has a built-in USB Application FIFO space for USB Application. Figure 7-2 shows the organization of the Data Memory Space.

6.2.1 Special Purpose Register

When the microcontroller executes instruction, specific registers are invoked for assistance, such as; Status Register which records the calculation status, Port I/O Control Registers which control the I/O pins' direction, etc. The EM78611E provides a lot of other special purpose registers for various functions.

Note that Special Control Registers can only be read or written by two instructions: IOR and IOW.

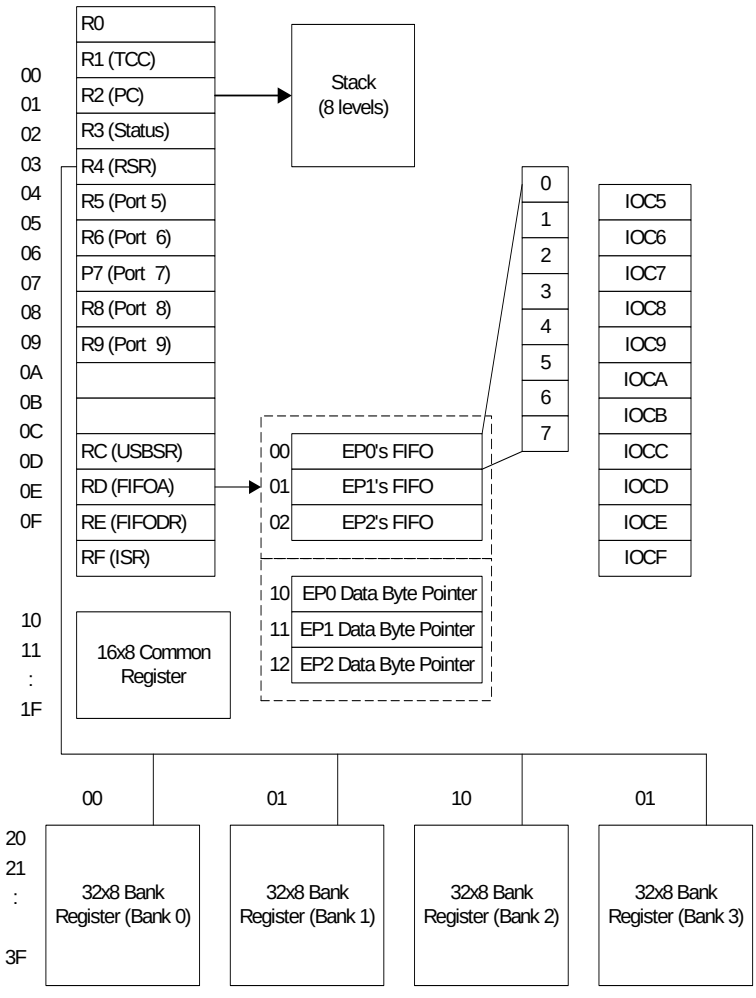


Figure 6-2 Data RAM Organization of EM78611E

6.2.2 Operation Registers

The following sections will introduce each of the Operation Registers of the Special Purpose Registers. The Operation Registers are arranged according to the order of registers' address. Note that some registers are read only, while others are both readable and writable.

6.2.2.1 R0 (Indirect Addressing Register) *Default Value: (0B_0000_0000)*

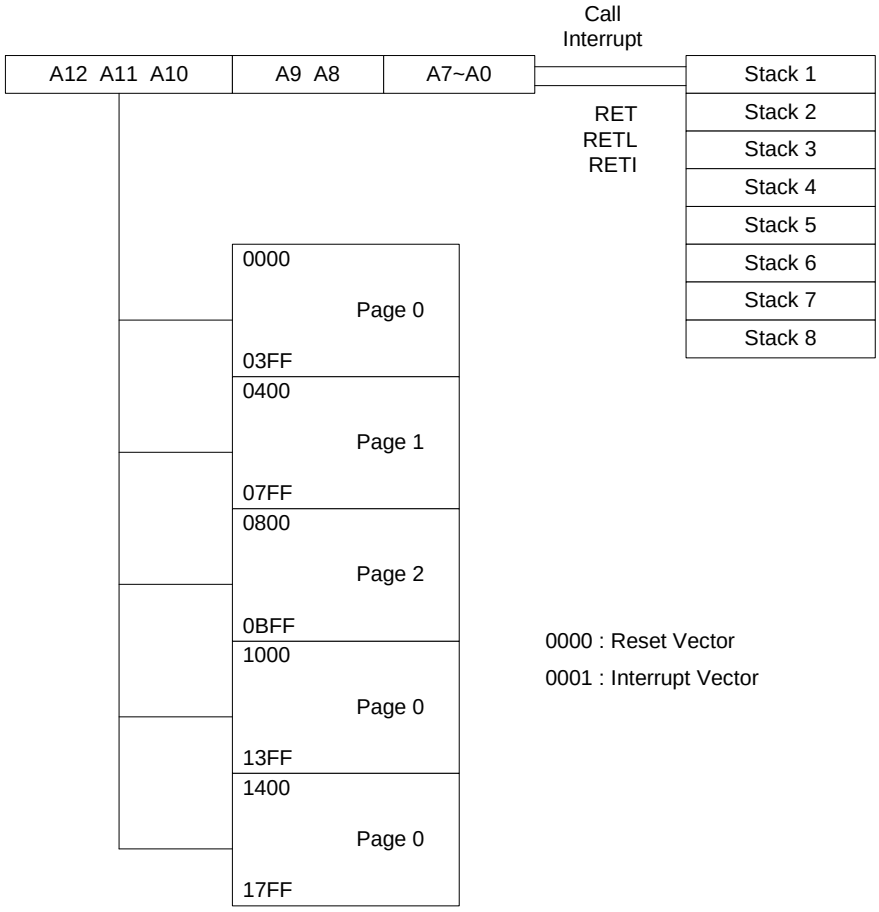
R0 is not a physically implemented register. Its major function is as an indirect addressing pointer. Any instruction using R0 as a pointer actually accesses the data pointed by the RAM Select Register (R4).

6.2.2.2 R1 (Timer / Clock Counter) *Default Value: (0B_0000_0000)*

This register TCC, is an 8-bit timer or counter. It is readable and writable as any other register. The Timer module will increment every instruction cycle. User can work around this by writing an adjusted value. The Timer interrupt is generated when the R1 register overflows from FFh to 00h. This overflow sets bit TCIF (RF[0]). The interrupt can be masked by clearing bit TCIE (IOCF[0]). After a Power-on reset and Watchdog reset, the initial value of this register is 0x00.

6.2.2.3 R2 (Program Counter & Stack) *Default Value: (0B_0000_0000)*

The EM78611E Program Counter is a 13-bit long register that allows accessing of the 6k words of Program Memory with 8-level stacks. The eight LSB bits, A0~A7, are located at R2, while the three MSB bits, A12~A10, are located at R3. The Program Counter is cleared after a Power-on reset or Watchdog reset. The first instruction that is executed after a reset is located at Address 00h.



6.2.2.4 R3 (Status Register) *Default Value:(0B_0001_1XXX)*

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PS2	PS1	PS0	T	P	Z	DC	C

R3 [0] Carry/Borrow flag

0: No carry-out from the Most Significant bit of the result occurred

1: A carry-out from the Most Significant bit of the result occurred

NOTE

For Borrow, the polarity is reversed. For rotate (RRC, RLC) instructions, this bit is loaded with either the high or low-order bit of the source register.

R3 [1] Auxiliary carry/borrow flag. For ADD, SUB Instructions

0: No carry-out from the 4th low-order bit of the result

1: A carry-out from the 4th low-order bit of the result occurred

NOTE

For Borrow, the polarity is reversed.

R3 [2] Zero flag. It will be set to 1 when the result of an arithmetic or logic operation is zero.

R3 [3] Power down flag. It will be set to 1 during Power-on phase or by "WDTC" command and cleared when the MCU enters into Power down mode. It remains in its previous state after a Watchdog Reset.

0: Power down

1: Power-on

R3 [4] Time-out flag. It will be set to 1 during Power-on phase or by "WDTC" command. It is reset to 0 by a WDT time-out.

0: Watchdog timer overflow

1: Watchdog timer no overflow

The various states of Power down flag and Time-out flag at different conditions are shown below:

T	P	Condition
1	1	Power-on reset
1	1	WDTC instruction
0	*P	WDT time-out
1	0	Power down mode
1	0	Wake-up caused by port change during Power down mode

* P: Previous status before WDT reset

R3 [5-7] Page selection bits. These three bits are used to select the program memory page.

PS2	PS1	PS0	Program Memory Page [Address]
0	0	0	Page 0 [0000-03FF]
0	0	1	Page 1 [0400-07FF]
0	1	0	Page 2 [0800-0BFF]
0	1	1	Page 3 [0C00-0FFF]
1	0	0	Page 4 [1000-13FF]
1	0	1	Page 5 [1400-17FF]

6.2.2.5 R4 (RAM Select Register) *Default Value: (0B_00XX_XXXX)*

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BK1	BK0	Ad5	Ad4	Ad3	Ad2	Ad1	Ad0

R4 (RAM select register) contains the address of the registers.

R4 [0~5]are used to select registers in 0x00h~0x3Fh. Address 0x00~0x1F is common space. After 0x1Fh, SRAM is divided into four banks, hence, use Bank Select Register.

R4 [6, 7]to select the register bank (refer to the table below). The following are two examples:

(1) R4=00001100 and R4=10001100 point to the same Register 0x0Ch. Since 0x0Ch is in the common space, Bit 6 and Bit 7 are meaningless.

(2) R4=10111100 points to Register 0x3C in Bank 2.

R4[7]Bk1	R4[6]Bk0	RAM Bank #
0	0	Bank 0
0	1	Bank 1
1	0	Bank 2
1	1	Bank 3

6.2.2.6 R5 (Port 5 I/O Register) *Default Value: (0B_0000_0000)*

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P57	P56	P55	P54	P53	P52	P51	P50

6.2.2.7 R6 (Port 6 I/O Register) *Default Value: (0B_0000_0000)*

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P67	P66	P65	P64	P63	P62	P61	P60

6.2.2.8 R7 (Port7 I/O Register) *Default Value: (0B_0000_X000)*

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P77	P76	D- / P75 / DATA	D+ / P74 / CLK	-	P72	P71	P70

6.2.2.9 R8 (Port 8 I/O Register) *Default Value: (0B_0000_0000)*

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P87	P86	P85	P84	P83	P82	P81	P80

6.2.2.10 R9 (Port 9 I/O Register) *Default Value: (0B_0000_0000)*

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P97	P96	P95	P94	P93	P92	P91	P90

6.2.2.11 RC (USB Application Status Register) *Default Value: (0B_0000_0000)*

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EP0_W	EP0_R	EP1_R	EP2_R	EP2_W	Host_Suspend	EP0_Busy	Stall

RC [0] Stall flag. While the MCU receives an unsupported command or invalid parameters from host, this bit will be set to 1 by the firmware to notify the UDC to return a STALL handshake. When a successful Setup transaction is received, this bit is cleared automatically. This bit is readable and writable.

RC [1] EP0_Busy flag. When this bit is equal to "1," it indicates that the UDC is writing data into the EP0'FIFO or reading data from it. During this time, the firmware will avoid accessing the FIFO until the UDC finishes writing or reading. This bit is readable only.

RC [2] Host Suspend flag. If this bit is equal to 1, it indicates that the USB bus has no traffic for a specified period of 3.0 ms. This bit will also be automatically cleared when there is bus activity. This bit is readable only.

RC [3] EP2_W flag. This bit is set when the UDC receives a successful data from the USB Host to EP2. Upon detecting that this bit is equal to 1, the firmware will execute a read sequence to the EP2's FIFO, then clear this bit. Otherwise, the subsequent data from USB Host won't be accepted by the UDC.

RC [4, 5, 6] EP0_R / EP1_R / EP2_R flag. These three bits inform the UDC to read the data from the FIFO. Then the UDC will automatically send the data to the Host. After the UDC finishes reading the data from the FIFO, this bit will be cleared automatically.

Therefore, before writing data into FIFO's, the firmware will first check this bit to avoid overwriting the data. These three bits can only be set by the firmware and cleared by hardware.

RC [7] EP0_W flag. After the UDC completes writing data to the FIFO, this bit will be set automatically. The firmware will clear it as soon as it gets the data from EP0's FIFO. Only when this bit is cleared that the UDC will be able to write a new data into the FIFO.

Therefore, before the firmware can write data into the FIFO, this bit must first be set by the firmware to prevent the UDC from writing data at the same time. This bit is both readable and writable.

6.2.2.12 RD (USB Application FIFO Address Register) *Default Value: (0B_0000_0000)*

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	UAD4	UAD3	UAD2	UAD1	UAD0

RD [0~4] USB Application FIFO address registers. These five bits are the address pointer of USB Application FIFO.

RD [5~7] Undefined registers. The default value is zero.

6.2.2.13 RE (USB Application FIFO Data Register) *Default Value: (0B_0000_0000)*

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
UD7	UD6	UD5	UD4	UD3	UD2	UD1	UD0

RE (USB Application FIFO data register) contains the data in the register of which address is pointed by RD.

NOTE

For example, if we want to read the fourth byte of the EndPoint Zero, we will use the address of EP0 (0x00) and Data Byte Pointer of EP0 (0x10) to access it.

```
// Read the 4th byte of the EP0 FIFO
// First, assign the data byte pointer of EP0 register (0X10) with 0X03.
   MOVA, @0X10
   MOVRD, a       // Move data in A to RD register
   MOVA, @0X03
   MOVRE , A      // Move data in A to RE register

// Then read the content from EP0 FIFO (0x00) 4th byte
   MOVA, @0X00
   MOVRD, A      // Assign address point to EP0 FIFO
   MOVA, RE      // Read the fourth byte data (Byte 3) of the EP0 FIFO
   MOV A, 0X0E// Read the fifth byte data (Byte 4) of the EP0 FIFO
```

6.2.2.14 RF (Interrupt Status Register) *Default Value: (0B_0XX0_0000)*

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
USB Host Resume_IF	_	_	Port7 state change_1F	USB Reset_IF	USB Suspend_IF	EP0_IF	TCC_IF

RF [0] TCC Overflow interrupt flag. It will be set while TCC overflows, and is cleared by firmware.

RF [1] EndPoint Zero interrupt flag. It will be set when the EM78611E receives Vendor /Customer Command to EndPoint Zero. This bit is cleared by firmware.

RF [2] USB Suspend interrupt flag. It will be set when the EM78611E finds the USB Suspend Signal on USB bus. This bit is cleared by firmware.

RF [3] USB Reset interrupt flag. It will be set when the host issues the USB Reset signal.

RF [4] P74/P75/P76/P77 port state change interrupt flag.

In PS2 Mode, only pins configured as inputs can cause this interrupt to occur. These pins (P74, P75, P76 and P77) are compared with the value latched on the last read of Port 7.

In USB Mode, only P76 and P77 have the interrupt function.

NOTE

RF[4]: Port State Change Interrupt Flag,
USB Mode – Only P76 and P77 have the interrupt function.
PS2 Mode – P74/P75/P76/P77 have the interrupt function.

RF [5, 6] Reserved bits

NOTE

RF[5] , RF[6]: Reserved bits, but do not modify them anyway.

RF [7] USB Host Resume interrupt flag. It will be set only in Dual clock mode when the USB suspend signal becomes low.

6.2.3 Control Registers

Some special purpose registers are available for special control purposes. Except for the Accumulator (ACC), these registers must be read and written to by special instructions. One of these registers, CONT, can only be read by the instruction "CONTR" and written by "CONTW" instruction. The other special control registers can be read by the instruction "IOR" and written to by the instruction "IOW."

The following paragraphs describe the general functions of the control registers.

6.2.3.1 A (Accumulator Register)

The accumulator is an 8-bit register that holds operands and results of arithmetic calculations. It is not addressable.

6.2.3.2 CONT (Control Register) *Default Value: (0B_0011_1111)*

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LED	/INT	TSR2	TSR1	TSR0	PSR2	PSR1	PSR0

Except for Bit-6 (Interrupt enable control bit), the CONT register can be read by the instruction "CONTR" and written by the instruction “CONTW."

CONT [0~2] Watchdog Timer prescaler bits. These three bits are used as the prescaler of the Watchdog Timer.

CONT [3~5] TCC Timer prescaler bits.

The relationship between the prescaler value and these bits are shown below:

PSR2/TSR2	PSR1/TSR1	PSR0/TSR0	TCC Rate	WDT Rate (8ms)
0	0	0	1: 2	1: 1
0	0	1	1: 4	1: 2
0	1	0	1: 8	1: 4
0	1	1	1: 16	1: 8
1	0	0	1: 32	1: 16
1	0	1	1: 64	1: 32
1	1	0	1: 128	1: 64
1	1	1	1: 256	1: 128

NOTE

*The WDT Timing base is fixed at **8ms**. Do not care for the code option selection.*

Ex. For WDT timeout computing: Set the prescaler = 1:128.

WDT overflow time is: 8mS × 2^7 = 1024 mS

CONT [6] Interrupt enable control bit. This bit toggles Interrupt function between enable and disable. It is set to 1 by the interrupt disable instruction "DISI" and reset by the interrupt enable instructions "ENI" or "RETI."

0: Enable the Interrupt function

1: Disable the Interrupt function

CONT [7] LED bit. This bit is used to enable the LED sink capacity of P76 and P77.

0: Disable the LED sink capacity of P76, P77

1: Enable the LED sink capacity of P76, P77

6.2.3.3 IOC5 ~IOC9 I/O Port Direction Control Registers *Default Value: (0B_1111_1111)*

These are I/O port (Port 5 ~ Port 7) direction control registers. Each bit controls the I/O direction of three I/O ports respectively. When these bits are set to 1, the relative I/O pins become input pins. Similarly, the I/O pins become outputs when the relative control bits are cleared.

0: Output direction

1: Input direction

6.2.3.4 IOCA (Operation Mode Control Register) *Default Value: (0B_1110_0000)*

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Dual_Frq.1	Dual_Frq.0	/P76,/P77 Pull high	Remote_Wake up	-	-	PS/2	USB

IOCA [0, 1] These two bits are used to select the operation mode. .

IOCA[1]	IOCA[0]	Operation Mode
0	0	Detect Mode
0	1	USB Mode
1	0	PS/2 Mode
1	1	USB Test Mode

IOCA[4] Indicate whether the device is currently requested to support remote wake up or not. The Remote Wake up field can be modified by SetFeature() and ClearFeature() requests.

0: Do not support remote wake up

1: Supports remote wake up

IOCA[5] Pull-high resistor of P77 and P76. USB mode only.

0: Pull-high is enabled

1: Pull-high is disabled

IOCA [6, 7] Selects the operation frequency in Dual Clock Mode. Four frequencies are available and can be chosen as Dual Clock Mode for running the MCU program.

Dual_Frq.1	Dual_Frq.0	Frequency
0	0	500Hz
0	1	4kHz
1	0	32kHz
1	1	256kHz

6.2.3.5 IOCB (Port 9 Wake-up Pin Select Register) *Default Value: (0B_1111_1111)*

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/P97	/P96	/P95	/P94	/P93	/P92	/P91	/P90

IOCB [0~7] These bits are used to select which of the Port 9 pins is to be assigned to wake up the MCU while in Power down mode.

0: Enable the function

1: Disable the function

6.2.3.6 IOCC (Port 9 LED Sink Capacity Control Register) *Default Value: (0B_0000_0000)*

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P97	P96	P95	P94	P93	P92	P91	P90

IOCC [0~7] LED sink control bit. These bits are used to enable the LED sink capacity of P90 ~ P97

0: Disable the LED sink capacity of the respective pins

1: Enable the LED sink capacity of the respective pins

6.2.3.7 IOCD (Port 9 Pull High Control Register) *Default Value: (0B_1111_1111)*

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/PH97	/PH96	/PH95	/PH94	/PH93	/PH92	/PH91	/PH90

IOCD [0~7] These bits control the 25KΩ pull-high resistor of individual pins in Port 9.

0: Enable the pull-high function

1: Disable the pull-high function

6.2.3.8 IOCE (Special Function Control Register) *Default Value: (0B_1101_01111)*

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/Dual clock	/WUE	WTE	RUN	Device_Resume	/PU8	/PU6	/PU5

IOCE [0, 1, 2] Port 5, Port 6, and Port 8 pull-high control bits.

0: Enable

1: Disable

IOCE [3] Setting this bit will allow the UDC to execute resume signaling. This bit is set by firmware to generate a signal to wake up the USB host and is cleared as soon as the USB Suspend signal becomes low. It can only be used in Dual clock mode when the USB suspend signal becomes low.

IOCE [4] Run bit. This bit can be cleared by the firmware and set during power-on, or by the hardware at the falling edge of wake-up signal. When this bit is cleared, the clock system is disabled and the MCU enters into Power down mode. At the transition of wake-up signal from high to low, this bit is set to enable the clock system.

0: Sleep mode. The EM78611E is in power down mode.

1: Run mode. The EM78611E is working normally

IOCE [5] Watchdog Timer enable bit. The bit disables/enables the Watchdog Timer.

0: Disable WDT

1: Enable WDT

IOCE [6] Enable the wake-up function as triggered by port-changed state. This bit is set by UDC.

0: Enable the wake-up function

1: Disable the wake-up function

IOCE [7] Dual clock Control bit. This bit is used to select the frequency of system clock. When this bit is cleared, the MCU will run on very low frequency for power saving and the UDC will stop working.

0: Selects to run on slow frequency

1: Selects EM78611E to run on normal frequency

6.2.3.9 IOCF (Interrupt Mask Register) *Default Value：(0B_0XX0_0000)*

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
USB Host Resume_IE	-	-	Port7 state change_1E	USB Reset_IE	USB Suspend_IE	EP0_IE	TCC_IE

IOCF [0~4, 7] TCC / EP0 / USB Suspend / USB Reset / Port 7 State Change / USB Host Resume interrupt enable bits. These eight bits control the TCC interrupt function, EP0 interrupt, USB Suspend interrupt, USB Reset interrupt, Port 7 State Change interrupt and USB Host Resume interrupt respectively. Individual interrupt is enabled by setting its associated control bit in the IOCF to "1."

0: Disable Interrupt

1: Enable Interrupt

Only when the global interrupt is enabled by the ENI instruction that the individual interrupt will work. After DISI instruction, any interrupt will not work even if the respective control bits of IOCF are set to 1.

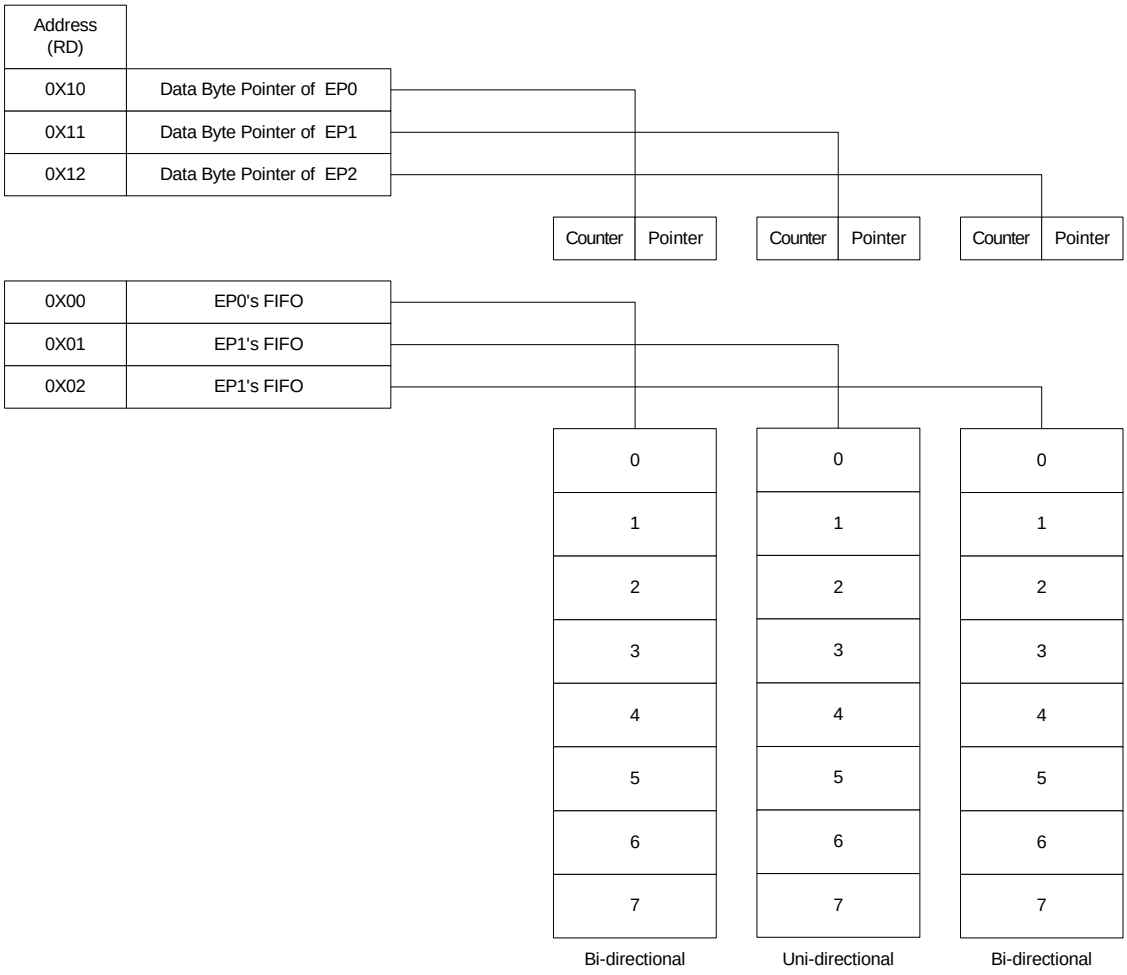
The USB Host Resume Interrupt works only in Dual clock mode. This is because when the MCU is in sleep mode, it will be automatically wakened up by the UDC Resume signal.

NOTE

IOCF[5], IOCF[6]: Reserved bits, but do not modify them anyway.

6.3 USB Application FIFOs

For USB Application, the EM78611E provides an 8-byte First-In-First-Out (FIFO) buffer for each endpoint. The buffer cannot be accessed directly. However, a corresponding Data Byte Pointer register for each endpoint is made available to address the individual byte of the FIFO buffer. The contents of the individual byte will map to a special register.



6.4 USB Application

The EM78611E is designed specially for USB device application and has many powerful functions that help the firmware to free itself from complex situation in various aspects of USB application.

6.4.1 USB Device Controller

The built-in USB Device Controller (UDC) in the EM78611E can interpret the USB Standard Command and respond automatically without involving the firmware. The embedded Series Interface Engine (SIE) handles the serialization and de-serialization of actual USB transmission. Thus, a developer can concentrate his efforts more in perfecting the device actual functions and spend less energy in dealing with USB transaction.

The UDC handles and decodes most Standard USB commands defined in the USB Specification Rev1.1. I f the UDC receives an unsupported command, it will set a flag to notify the MCU of the receipt of such command. The Standard Commands that the EM78611E supports include; **Clear Feature, Get Configuration, Get Interface, Get Status, Set Address, Set Configuration, Set Feature, and Set Interface**.

Each time the UDC receives a USB command, it writes the command into EP0's FIFO. Only when it receives unsupported command that the UDC will notify the MCU through an interrupt.

Therefore, the EM78611E is very flexible under USB application because the developer can freely choose the method of decoding the USB command as dictated by different situation.

6.4.2 Device Address and Endpoints

The EM78611E supports one device address and three endpoints, EP0 for control endpoint, EP1 and EP2 for interrupt endpoint. Sending data to USB host for the EM78611E is very easy. Just write data into EP's FIFO, then set the flag, and the UDC will handle the rest. It will then confirm that the USB host has received the correct data from the EM78611E.

6.5 Reset

The EM78611E provides three types of reset:

(1) Power-on Reset

(2) Watchdog Reset

(3) USB Reset

6.5.1 Power-on Reset

Power-on Reset occurs when the device is attached to power and a reset signal is initiated. The signal will last until the MCU becomes stable. After a Power-on Reset,

the MCU enters into the following pre-determined states (see below), and then, it is ready to execute the program.

a. The program counter is cleared.

b. The TCC timer and Watchdog timer are cleared.

c. Special registers and Special Control registers are all set to their initial values.

6.5.2 Watchdog Reset

When the Watchdog timer overflows, it causes the Watchdog to reset. After it resets, the program is executed from the beginning and some registers will be reset. The UDC however, remains unaffected.

6.5.3 USB Reset

When the UDC detects a USB Reset signal on the USB Bus, it interrupts the MCU, then proceed to perform the specified process that follows. After a USB device is attached to the USB port, it cannot respond to any bus transactions until it receives a USB Reset signal from the bus.

6.6 Power Saving Mode

The EM78611E provides two options for power-saving modes for energy conservation, i.e., Power Down mode and Dual clock mode.

6.6.1 Power Down Mode

The EM78611E enters into Power Down mode by clearing the RUN register (IOCE[4]). During this mode, the oscillator is turned off and the MCU goes to sleep. It will wake up when signal from the USB host is resumed, or when the Watchdog resets or the input port state changes.

If the MCU wakes up when I/O port status changes, the direction of I/O port should be set at input direction, and then read the state of port. For example:

```
:
// Set the Port 6 to input port
MOV      A, @0xFF
IOW       PORT6
// Read the state of Port 6
MOV      PORT6, PORT6
// Clear the RUN bit
IOR       0xE
AND      A, 0B11101111
IOW      0xE
:
```

:

6.6.2 Dual Clock Mode

The EM78611E has one internal oscillator for power saving application. Clearing the Bit IOCE [7] will enable the low frequency oscillator. At the same time, the external oscillator will be turned off. Then the MCU will run under very low frequency to conserve power. Four types of frequency are available for selection in setting bits IOCA [6, 7].

The USB Host Resume Interrupt can only be used in this mode. If this interrupt is enabled, the MCU will be interrupted when the USB Host Resume signal is detected on USB Bus.

6.7 Interrupt

The EM78611E has one interrupt vector in 0x0001. When an interrupt occurs during the MCU running program, it will jump to the interrupt vector (0x0001) and execute the instructions sequentially from the interrupt vector. RF is the interrupt status register, which records the interrupt status in the relative flags/bits.

The interrupt condition could be one of the following:

- TCC Overflow: When the Timer Clock / Counter Register (R1) overflows, the status flag RF[0] will be set to 1. Its interrupt Vector is 0X0001.
- Port 7 State Change: When the input signals in Port 7 changes, the status flag RF[4] will be set to 1. Its interrupt Vector is 0X0001.
- EP0 interrupt: When the UDC successfully accepts a setup transaction from host to EndPoint0, the status flag RF[1] is set to 1. Its interrupt Vector is 0X0001.
- USB suspend: When the UDC detects a USB Suspend signal on the USB bus, the status flag RF[2] is set to 1. Its interrupt Vector is 0X0001.
- USB Reset: When the UDC detects a USB Reset signal on the USB bus, the status flag R[3] is set to 1. Its interrupt Vector is 0X0001.
- USB Host Resume: When UDC detects that the USB bus is no longer in Suspend condition and without Device Resume signal, the status flag R[7] is set to 1. Its interrupt Vector is 0X0001.

IOCF is an interrupt mask register which can be set bit by bit. While their respective bit is written to 0, the hardware interrupt will inhibit, that is, the EM78611E will not jump to the interrupt vector to execute instructions. But the interrupt status flags still records the conditions no matter whether the interrupt is masked or not. The interrupt status flags must be cleared by firmware before leaving the interrupt service routine and enabling other interrupt.

The global interrupt is enabled by the ENI (RETI) instruction and is disabled by the DISI instruction.

7 Absolute Maximum Ratings

Symbol	Min	Max	Unit
Temperature under bias	0	70	ºC
Storage temperature	-65	150	ºC
Input voltage	-0.5	6.0	V
Output voltage	-0.5	6.0	V

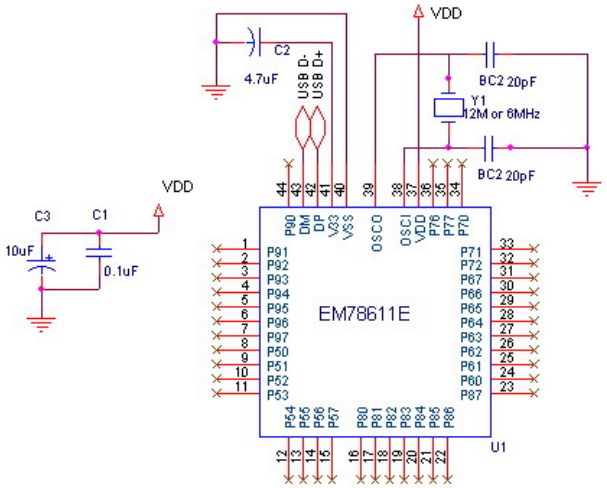
8 DC Electrical Characteristic

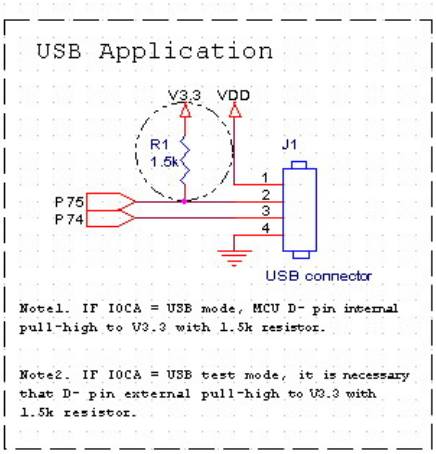
T = 25ºC, VDD=5V, VSS=0V)

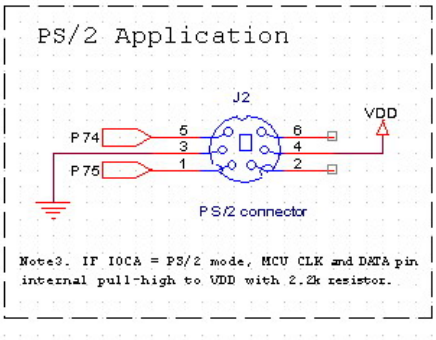
Symbol	Parameter	Condition	Min	Type	Max	Unit
3.3V Regulator						
V_{Rag}	Output voltage of 3.3v Regulator	V_{DD} = 5V	3.0	3.3	3.6	V
V_{ResetL}	Low Power Reset detecting low Voltage	–	–	–	2.2	V
V_{ResetH}	Low Power Reset detecting high Voltage	–	3.0	–	–	V
Ireg	3.3V Regulator driving capacity	V3.3 = 3.3V	–	–	100	mA
MCU operating						
I_{IL}	Input Leakage Current for input pins	VIN=VDD,VSS	–	–	±1	µA
V_{IHX}	Clock Input High Voltage	OSCI	2.5	–	-	V
V_{ILX}	Clock Input Low Voltage	OSCI	–	–	1.0	V
I_{CC1}	VDD operating supply current – Normal frequency operation mode	Freq. = 6MHz	–	–	10	mA
I_{CC2}	VDD operating supply current – Normal frequency operation mode	Freq. = 12MHz	–	–	20	mA
I_{CC3}	VDD operating supply current – Dual clock mode	Freq. = 256kHz	–	–	250	µA
I_{SB1}	Operating supply current 1 – Power down mode	WDT disabled	–	–	120	µA
GPIO Pins						
V_{IH}	Input High Voltage	Port 5 ~ Port 9	2.0	–	-	V
V_{IL}	Input Low Voltage	Port 5 ~ Port 9	–	–	0.8	V
I_{OH1}	Output High Voltage (P70~P73, P76 and P77)	I_{Sink} = 10.0mA V_{DD} = 5V	–	10.00	–	mA
I_{OH2}	Output High Voltage (P74, P75)	I_{Sink} = 5.0mA V_{DD} = 5V	–	5.00	–	mA
I_{OH3}	Output High Voltage (Port 5, Port 6, Port 8 and P90~P97)	I_{Sink} = 10.0mA V_{REG} = 5V	–	10.00	–	mA
I_{OL1}	Output Low Voltage (P76 and P77 normal mode)	I_{Sink} = 10.0mA V_{DD} = 5V	–	10.00	–	mA

Symbol	Parameter	Condition	Min	Type	Max	Unit
I_{OL2}	Output Low Voltage (P74, P75)	I_{Sink} = 10.0mA V_{DD} = 5V	–	10.00	–	mA
I_{OL3}	Output Low Voltage (P70~P73, P76 and P77 sink LED)	I_{Sink} = 10.0mA V_{DD} = 5V	–	10.00	–	mA
I_{OL4}	Output Low Voltage (P90 ~ P97 normal mode)	I_{Sink} = 10.0mA V_{REG} = 5V	–	10.00	–	mA
I_{OL5}	Output Low Voltage (P90 ~ P97 sink LED)	I_{Sink} = 10.0mA V_{REG} = 5V	–	10.00	–	mA
R_{PH1}	Pull-high resistor (Ports 5, 6, 8, 9)	Input pin with pull-high resistor, V_{REG} = 5V	–	25.00	–	KΩ
R_{PH2}	Pull-high resistor(P.74 ~ P.77), (P74/P75) PS2 mode	Input pin with pull-high resistor, V_{DD} = 5V	–	2.20	–	KΩ
USB Interface						
V_{OH}	Static Output High	USB operation Mode	2.8	–	3.6	V
V_{OL}	Static Output Low		–	–	0.3	V
V_{DI}	Differential Input Sensitivity		0.2	–	–	V
V_{CM}	Differential Input Command Mode Range		0.8	–	2.5	V
V_{SE}	Single Ended Receiver Threshold		0.8	–	2.0	V
C_{IN}	Transceiver Capacitance		–	–	20	pF
V_{RG}	Output Voltage of Internal Regulator		3.0	–	3.6	V
R_{PH3}	Pull-high resistor (P.75 / D-)		–	1.5	-	KΩ

9 Application Circuit







NOTE

A. BC1 BC2: Load Capacitor.

B. C1 (bypass capacitor): placed adjacent to VDD pin, to minimize noise.

C. C2, C3 (power capacitor): placed adjacent to Power source, will improve transient response and ripple rejection.

APPENDIX

A Special Register Map

Operation Registers

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default Value
0x00	R0	Indirect Addressing Register								0B_0000_0000
0x01	R1 (TCC)	Timer / Clock Counter								0B_0000_0000
0x02	R2 (PC)	Program Counter								0B_0000_0000
0x03	R3 (STATUS)	PS2	PS1	PS0	T	P	Z	DC	C	0B_0001_1xxx
0x04	R4 (RSR)	BK1	BK0	Select the Register (Address: 00~3F) in Indirect Addressing Mode						0B_00xx_xxxx
0x05	R5 (Port 5)	P57	P56	P55	P54	P53	P52	P51	P50	0B_0000_0000
0x06	R6 (Port 6)	P67	P66	P65	P64	P63	P62	P61	P60	0B_0000_0000
0x07	R 7(Port 7)	P77	P76	P75/D-/DATA	P74/D+/CLK	-	P72	P71	P70	0B_0000_u000
0x08	R8 (Port 8)	P87	P86	P85	P84	P83	P82	P81	P80	0B_0000_0000
0x09	R9 (Port 9)	P97	P96	P95	P94	P93	P92	P91	P90	0B_u00u_0000
0x0C	RC	EP0_W	EP0_R	EP1_R	EP2_R	EP2_W	UDC _SUSPEND	UDC _Writing	STALL	0B_0000_0000
0x0D	RD	USB Application FIFO Address Register								0B_0000_0000
0x0E	RE	USB Application FIFO Data Register								0B_0000_0000
0x0F	RF	USB Host Resume_IF	–	–	Port7 state change_1F	USB Reset_IF	USB Suspend_IF	EP0_IF	TCC_IF	0B_0000_0000

Control Registers

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default value
	CONT	S7	INT	TSR2	SR1	TSR0	PSR2	PSR1	PSR0	0B_0011_1111
0x05	IOC5	Port 5 Direction Control Register								0B_1111_1111
0x06	IOC6	Port 6 Direction Control Register								0B_1111_1111
0x07	IOC7	Port 7 Direction Control Register								0B_1111_1111
0x08	IOC8	Port 8 Direction Control Register								0B_1111_1111
0x09	IOC9	Port 9 Direction Control Register								0B_1111_1111
0x0A	IOCA	Dual_Frq.1	Dual_Frq.0	/P76,/P77 Pull high	Remote_ Wake up	–	–	PS/2	USB	0B_1110_0000
0x0B	IOCB	/P97	/P96	/P95	/P94	/P93	/P92	/P91	/P90	0B_1111_1111
0x0C	IOCC	P97	P96	P95	P94	P93	P92	P91	P90	0B_0000_0000
0x0D	IOCD	/P97	/P96	/P95	/94	/P93	/P92	/P91	/P90	0B_0000_0000
0x0E	IOCE	/Dual clock	/WUE	WTE	RUN	Device_ Resume	/PU8	/PU6	/PU5	0B_1101_0111
0x0F	IOCF	USB Host Resume_IE	–	–	Port 7 state change_1F	USB Reset_IE	USB Suspend_ IE	EP0_IE	TCC_IE	0B_0000_0000

B Instruction Set

Each instruction in the instruction set is a 13-bit word divided into an OP code and one or more operands. All instructions are executed within one single instruction cycle (consisting of 2 oscillator periods), unless the program counter is changed by-

(a) Executing the instruction "MOV R2, A", "ADD R2,A", "TBL", or any other instructions that write to R2 (e.g. "SUB R2,A", "BS R2,6", "CLR R2", ····).

(b) Execute CALL, RET, RETI, RETL, JMP, Conditional skip (JBS, JBC, JZ, JZA, DJZ, DJZA) which were tested to be true.

Under these cases, the execution takes two instruction cycles.

In addition, the instruction set has the following features:

(1). Every bit of any register can be set, cleared, or tested directly.

(2). The I/O register can be regarded as general register. That is, the same instruction can operate on I/O register.

Legend:

R = Register designator that specifies which one of the registers (including operation and general purpose registers) is to be utilized by the instruction.

Bits 6 and 7 in R4 determine the selected register bank.

b = Bit field designator that selects the value for the bit located in the register R and which affects the operation.

k = 8 or 10-bit constant or literal value

Binary Instruction	Hex	Mnemonic	Operation	Status Affected
0 0000 0000 0000	0000	NOP	No Operation	None
0 0000 0000 0001	0001	DAA	Decimal Adjust A	C
0 0000 0000 0010	0002	CONTW	A → CONT	None
0 0000 0000 0011	0003	SLEP	0 → WDT, Stop oscillator	T, P
0 0000 0000 0100	0004	WDTC	0 → WDT	T, P
0 0000 0000 rrrr	000r	IOW R	A → IOCR	None [1]
0 0000 0001 0000	0010	ENI	Enable Interrupt	None
0 0000 0001 0001	0011	DISI	Disable Interrupt	None
0 0000 0001 0010	0012	RET	[Top of Stack] → PC	None
0 0000 0001 0011	0013	RETI	[Top of Stack] → PC, Enable Interrupt	None
0 0000 0001 0100	0014	CONTR	CONT → A	None
0 0000 0001 rrrr	001r	IOR R	IOCR → A	None [1]
0 0000 0010 0000	0020	TBL	R2+A → R2, Bits 8~9 of R2 unchanged	Z, C, DC

Binary Instruction	Hex	Mnemonic	Operation	Status Affected
0 0000 01rr rrrr	00rr	MOV R,A	A → R	None
0 0000 1000 0000	0080	CLRA	0 → A	Z
0 0000 11rr rrrr	00rr	CLR R	0 → R	Z
0 0001 00rr rrrr	01rr	SUB A,R	R-A → A	Z, C, DC
0 0001 01rr rrrr	01rr	SUB R,A	R-A → R	Z, C, DC
0 0001 10rr rrrr	01rr	DECA R	R-1 → A	Z
0 0001 11rr rrrr	01rr	DEC R	R-1 → R	Z
0 0010 00rr rrrr	02rr	OR A,R	A ∨ VR → A	Z
0 0010 01rr rrrr	02rr	OR R,A	A ∨ VR → R	Z
0 0010 10rr rrrr	02rr	AND A,R	A & R → A	Z
0 0010 11rr rrrr	02rr	AND R,A	A & R → R	Z
0 0011 00rr rrrr	03rr	XOR A,R	A ⊕ R → A	Z
0 0011 01rr rrrr	03rr	XOR R,A	A ⊕ R → R	Z
0 0011 10rr rrrr	03rr	ADD A,R	A + R → A	Z, C, DC
0 0011 11rr rrrr	03rr	ADD R,A	A + R → R	Z, C, DC
0 0100 00rr rrrr	04rr	MOV A,R	R → A	Z
0 0100 01rr rrrr	04rr	MOV R,R	R → R	Z
0 0100 10rr rrrr	04rr	COMA R	/R → A	Z
0 0100 11rr rrrr	04rr	COM R	/R → R	Z
0 0101 00rr rrrr	05rr	INCA R	R+1 → A	Z
0 0101 01rr rrrr	05rr	INC R	R+1 → R	Z
0 0101 10rr rrrr	05rr	DJZA R	R-1 → A, skip if zero	None
0 0101 11rr rrrr	05rr	DJZ R	R-1 → R, skip if zero	None
0 0110 00rr rrrr	06rr	RRCA R	R(n) → A(n-1), R(0) → C, C → A(7)	C
0 0110 01rr rrrr	06rr	RRC R	R(n) → R(n-1), R(0) → C, C → R(7)	C
0 0110 10rr rrrr	06rr	RLCA R	R(n) → A(n+1), R(7) → C, C → A(0)	C
0 0110 11rr rrrr	06rr	RLC R	R(n) → R(n+1), R(7) → C, C → R(0)	C
0 0111 00rr rrrr	07rr	SWAPA R	R(0-3) → A(4-7), R(4-7) → A(0-3)	None
0 0111 01rr rrrr	07rr	SWAP R	R(0-3) ↔ R(4-7)	None
0 0111 10rr rrrr	07rr	JZA R	R+1 → A, skip if zero	None
0 0111 11rr rrrr	07rr	JZ R	R+1 → R, skip if zero	None

Binary Instruction	Hex	Mnemonic	Operation	Status Affected
0 100b bbrr rrrr	0xxx	BC R,b	0 → R(b)	None [2]
0 101b bbrr rrrr	0xxx	BS R,b	1 → R(b)	None
0 110b bbrr rrrr	0xxx	JBC R,b	if R(b)=0, skip	None
0 111b bbrr rrrr	0xxx	JBS R,b	if R(b)=1, skip	None
1 00kk kkkk kkkk	1kkk	CALL k	PC+1 → [SP], (Page, k) → PC	None
1 01kk kkkk kkkk	1kkk	JMP k	(Page, k) → PC	None
1 1000 kkkk kkkk	18kk	MOV A,k	k → A	None
1 1001 kkkk kkkk	19kk	OR A,k	A ∨ k → A	Z
1 1010 kkkk kkkk	1Akk	AND A,k	A & k → A	Z
1 1011 kkkk kkkk	1Bkk	XOR A,k	A ⊕ k → A	Z
1 1100 kkkk kkkk	1Ckk	RETL k	k → A, [Top of Stack] → PC	None
1 1101 kkkk kkkk	1Dkk	SUB A,k	k-A → A	Z, C, DC
1 1111 kkkk kkkk	1Fkk	ADD A,k	k+A → A	Z, C, DC

Note:

[1] This instruction is applicable for IOCx only.

[2] This instruction is not recommended for RE, and RF operations.

C Code Option Register

The EM78611E has two Code option registers, which are not part of the normal program memory. The option bits cannot be accessed during normal program execution.

Address 000:

Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/R.S.	Package _1	Package _0	OST_1	OST_0	Frequency

Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6
_	_	EP2_ Maxsize_2	EP2_ Maxsize_1	EP2_ Maxsize_0	EP2_ DIR	EP2_ Enable

Bit 0 (Frequency): Frequency Selection.

0: The MCU run on 12 MHz

1: The MCU run on 6 MHz

Bits 2~1 (OST_1 ~ OST_0): Oscillator start-up time.

00: 500 µs

01: 2 ms

10: 8 ms

11: 16 ms

Bits 4~3 (Package_1 ~ Package_0): Package type selection.

00: Not defined

01: 40 pins

10: No define

11: 44 pins

Bit 5 (/R.S.): D- Pull-up Resistance

0: Connect Resistor Switch

1: Disconnect Resistor Switch

Bit 6 (EP2_Enable): Endpoint2 Enable.

0: Disable

1: Enable

Bit 7 (EP2_Dir): Endpoint 2 Direction.

0: OUT

1: IN

Bits 10~8 (EP2_Maxsize_2~0): Endpoint 2 maximum size.

000: 1 Byte

001: 2 Bytes

010: 3 Bytes

011: 4 Bytes

100: 5 Bytes

101: 6 Bytes

110: 7 Bytes

111: 8 Bytes

Bits 12~11: The values are fixed.