EM78F568N/F668N

8-Bit Microcontroller

Product Specification

DOC. VERSION 1.4

ELAN MICROELECTRONICS CORP.

November 2012

Trademark Acknowledgments:
IBM is a registered trademark and PS/2 is a trademark of IBM.
Windows is a trademark of Microsoft Corporation.
ELAN and ELAN logo are trademarks of ELAN Microelectronics Corporation.

The contents of this specification are subject to change without further notice. ELAN Microelectronics assumes no responsibility concerning the accuracy, adequacy, or completeness of this specification. ELAN Microelectronics makes no commitment to update, or to keep current the information and material contained in this specification. Such information and material may change to conform to each confirmed order.

In no event shall ELAN Microelectronics be made responsible for any claims attributed to errors, omissions, or other inaccuracies in the information or material contained in this specification. ELAN Microelectronics shall not be liable for direct, indirect, special incidental, or consequential damages arising from the use of such information or material.

The software (if any) described in this specification is furnished under a license or nondisclosure agreement, and may be used or copied only in accordance with the terms of such agreement.

ELAN Microelectronics products are not intended for use in life support appliances, devices, or systems. Use of ELAN Microelectronics product in such applications is not supported and is prohibited.
NO PART OF THIS SPECIFICATION MAY BE REPRODUCED OR TRANSMITTED IN ANY FORM OR BY ANY MEANS WITHOUT THE EXPRESSED WRITTEN PERMISSION OF ELAN MICROELECTRONICS.

ELAN MICROELECTRONICS CORPORATION

Headquarters:

No. 12, Innovation 1st Road
Hsinchu Science Park
Hsinchu, TAIWAN 30076
Tel: +886 3 563-9977
Fax: +886 3 563-9966
webmaster@emc.com.tw
http://www.emc.com.tw

Hong Kong:

Elan (HK) Microelectronics Corporation, Ltd.
Flat A, 19F., World Tech Centre 95
How Ming Street, Kwun Tong
Kowloon, HONG KONG
Tel: +852 2723-3376
Fax: +852 2723-7780

USA:

Elan Information Technology Group (U.S.A.)
PO Box 601
Cupertino, CA 95015
U.S.A.
Tel: +1 408 366-8225
Fax: +1 408 366-8225

Korea:

Elan Korea Electronics Company, Ltd.
301 Dong-A Building
632 Kojan-Dong, Namdong-ku
Incheon City, KOREA
Tel: +82 32 814-7730
Fax: +82 32 813-7730

Shenzhen:

Elan Microelectronics Shenzhen, Ltd.
8A Floor, Microprofit Building
Gaoxin South Road 6
Shenzhen Hi-tech Industrial Park
South Area, Shenzhen
CHINA 518057
Tel: +86 755 2601-0565
Fax: +86 755 2601-0500
elan-sz@elanic.com.cn

Shanghai:

Elan Microelectronics Shanghai, Ltd.
6F, Ke Yuan Building
No. 5, Bibo Road
Zhangjiang Hi-Tech Park
Shanghai, CHINA 201203
Tel: +86 21 5080-3866
Fax: +86 21 5080-4600
elan-sh@elanic.com.cn

Contents

APPENDIX

Specification Revision History

Doc. Version	Revision Description	Date
1.0	Initial version	2010/05/11
1.1	Added new package QFN32	2010/10/15
1.2	Modified the EEPROM Endurance cycle from 100K to 1000K. Modified the DC Electrical Characteristics.	2010/11/01
1.3	1. Added Program Flash Memory Electrical Characteristics. 2. Added LVR release level. 3. Modified RCM1:RCM0 at DC Electrical Characteristics table. 4. Added ADC Characteristics table. 5. Added Comparator Charateristics table.	2010/11/11
1.4	1. Modified the description of PWM Enable Control Register. 2. Modified the description of Bank 0 R11 Bit 5. 3. Added Device Characteristics Curve. 4. Added Ordering and Production Information.	2012/11/28

1 General Description

EM78F568N/EM78F668N are 8-bit microprocessor designed and developed with low-power, high-speed CMOS technology. They are equipped with 8K×15 bits Electrical Flash Memory, 256×8 bits in-system programmable EEPROM (for EM78F668N only), two comparators, three 8-bit timers, one 16-bit timer, two 10-bit PWM, 8 channels AD with 12-bit resolution, SPI, UART and I^2C.

With enhanced Flash-ROM features, the EM78F568N/EM78F668N series provide a convenient way of developing and verifying user's programs. Moreover, this Flash-ROM device offers the advantages of easy and effective program updates, using development and programming tools. Users can avail of the ELAN Writer to easily program their development code.

2 Features

- CPU configuration
  - **Supports 8K×15** bits program ROM
  - **304×8** bits on chip registers (SRAM)
  - **256** bytes in-system programmable EEPROM (for EM78F668N only)
    *Endurance: 1000,000 write/erase cycles
  - More than 10 years data retention
  - 8-level stacks for subroutine nesting
  - Less than 2 mA at 5V/4MHz
  - Typically 20 μA, at 3V/32kHz
  - Typically 2 μA, during sleep mode
  - Four operation mode

Mode	CPU	Main Clock	WDT Clock
Sleep mode	Turn off	Turn off	Turn off
Idle Mode	Turn off	Turn off	Turn on
Green mode	Turn on	Turn off	Turn on
Normal mode	Turn on	Turn on	Turn on

- I/O port configuration
  - 5 bidirectional I/O ports: P5, P6, P7, P8, P9
  - Pin change wake-up port : P6
  - **40** Programmable pull-down I/O pins
  - **40** programmable pull-high I/O pins
  - **40** programmable open-drain I/O pins
  - **40** programmable high-sink/drive I/O pins
  - External interrupt : P60
- Operating voltage range:
  - 2.4V~ 5.5V at 0°C ~ 70°C (Commercial)
  - 2.6V~ 5.5V at -40°C ~ 85°C (Industrial)
- Operating frequency range (base on two clocks):
  - Crystal mode: DC ~ 20 MHz @ 5V ;
    DC ~ 8 MHz @ 3V ; DC ~ 4 MHz @ 2.4V
  - ERC mode: DC ~ 20 MHz @ 5V ;
    DC ~ 8 MHz @ 3V ; DC ~ 4 MHz @ 2.4V
  - IRC mode: DC ~ 16 MHz @ 4.5V~5.5V ;
    DC ~ 8 MHz @ 3V ;DC ~ 4 MHz @ 2.4V~5.5V
  - Internal RC Drift Rate (Ta=25°C, VDD = 5V± 5%, VSS=0V)

Internal RC Frequency	Drift Rate			
	Temperature (-40°C~85°C)	Voltage (2.4V~5.5V)	Process	Total
455kHz	± 5%	± 5%	± 4%	± 14%
4 MHz	± 5%	± 5%	± 4%	± 14%
8 MHz	± 5%	± 5%	± 4%	± 14%
16 MHz	± 5%	± 5%	± 4%	± 14%

- Peripheral configuration
  - 8-bit real time clock/counter (TCC) with selective signal sources, trigger edges, and overflow interrupt
  - Two Pulse Width Modulation (PWMA, PWMB) with 10-bit resolution shared with Timers A and B
  - Two 8-bit Timer/Counter
    TC1 : Timer/Counter/Capture mode selection
    TC3: Timer/Counter/PWM/PDO
  - One 16-bit Timer/Counter
    TC2 : Timer/Counter/Window mode selection
  - 4 programmable Level Voltage Detector (LVD)
    *Vdd power monitors and supports low voltage detector interrupt flag
  - 8 channels Analog-to-Digital Converter with 12-bit resolution in Vref mode
  - Two comparators
  - Serial transmitter/receiver interface (SPI): 3-wire synchronous communication
  - UART interface: 2-wire asynchronous communication
  - Power down (Sleep) mode
  - High EFT immunity (4 MHz, 4 clocks)
  - I^2C function with 7/10 bits address and 8 bits data transmit/receive mode
- 19 available interrupts: (4 external, 15 internal)
  - External interrupt: P60
  - TCC overflow interrupt
  - TC1, TC2, TC3 overflow interrupt
  - Input-port status changed interrupt (wake up from sleep mode)
  - ADC completion interrupt
  - PWMA, PWMB period match completion
  - Comparator high/low interrupt
  - I^2C transfer/receive/stop interrupt
  - UART TX, RX , RX error interrupt
  - SPI interrupt
  - LVD interrupt
- Single instruction cycle commands
- Four kinds of oscillation range in Crystal Mode

Crystal Range	Oscillator Mode
20 MHz ~ 6 MHz	HXT
6 MHz ~ 1 MHz	XT
1 MHz ~ 100kHz	LXT1
32.768kHz	LXT2

- Programmable free running watchdog timer
  - Watchdog Timer: 16.5ms ± 5% with Vdd =5V at 25°C, Temperature range ± 5% (-40°C ~+85°C)
  - Watchdog Timer: 18ms ± 5% with Vdd = 3V at 25°C
  - Temperature range ± 5% (-40°C~+85°C)
  - Two clocks per instruction cycle
- Package Type:
  - 44-pin QFP : EM78Fx68NQ44J/S
  - 40-pin DIP : EM78Fx68ND40J/S
  - 32-pin QFN : EM78F668NQN32J/S
  - 28-pin SKDIP : EM78Fx68NK28J/S
  - 28-pin SOP : EM78Fx68NSO28J/S

Note: *These are all Green products which do not contain hazardous substances.*

3 Pin Configuration

(1) 28-Pin SKDIP/SOP

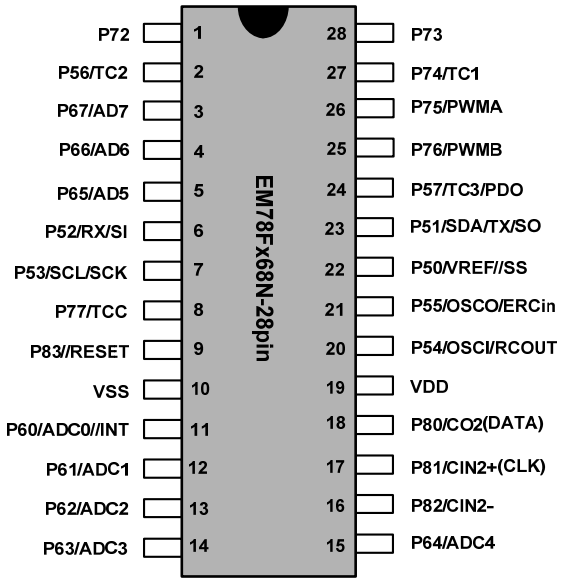


Figure 3-1 28-pin EM78Fx68N

(2) 40-Pin DIP

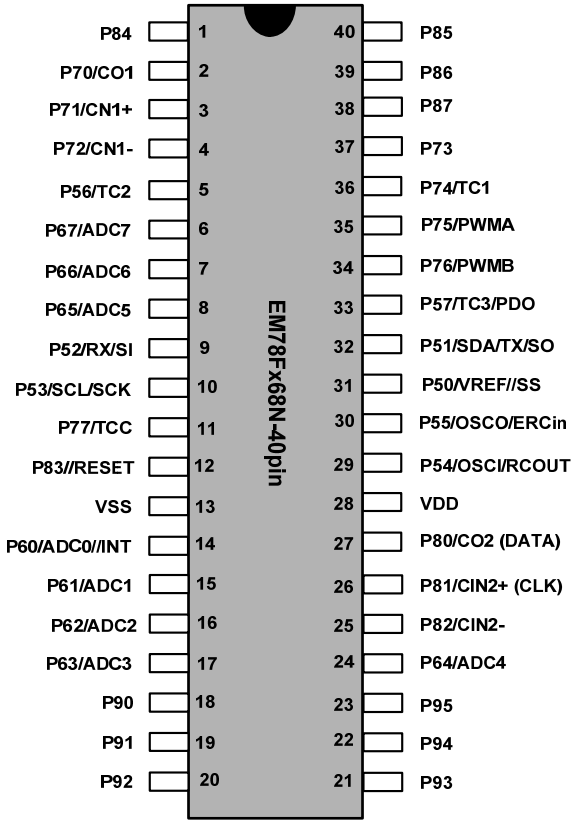


Figure 3-2 40-pin EM78Fx68N

(3) 32-Pin QFN

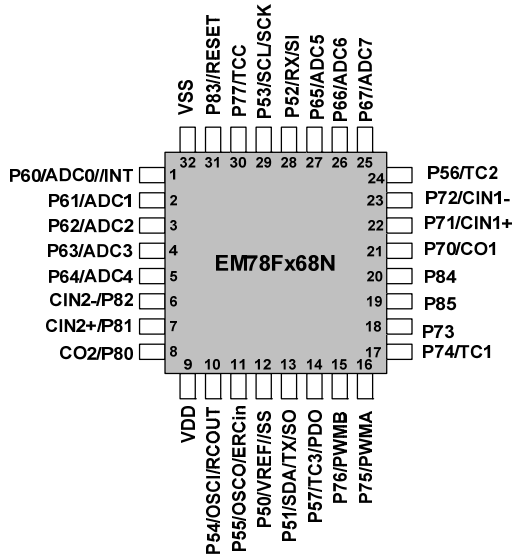


Figure 3-3 32-pin EM78Fx68N

(4) 44-Pin QFP

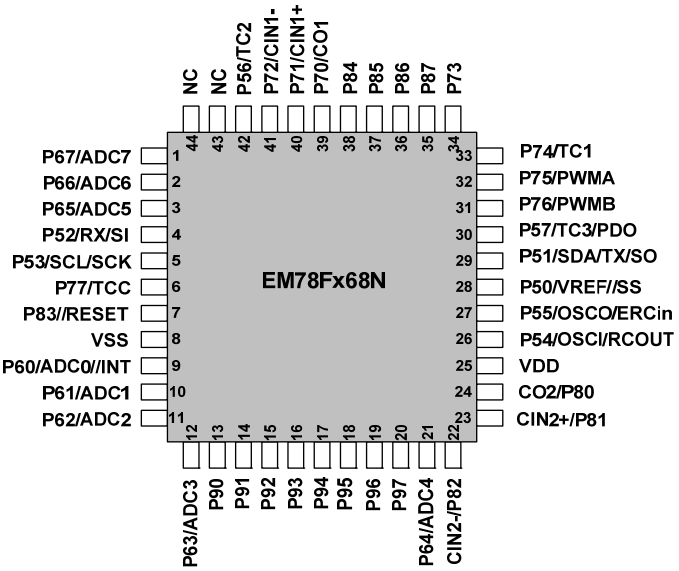


Figure 3-4 40-pin EM78Fx68N

4 Pin Description

4.1 EM78F568N/EM78F668N

Name	Function	Input Type	Output Type	Description
–	VDD	Power	–	Power
–	VSS	Power	–	Ground
P50/DAVREF//SS	P50	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	DAVREF	AN	–	Voltage reference for DAC
	/SS	ST	–	SPI slave select pin
P51/SDA/TX/SO	P51	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	SDA	ST	CMOS	I^2C serial data line. It is open-drain
	TX	–	CMOS	UART TX output
	SO	–	CMOS	SPI serial data output
P52/RX/SI	P52	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	RX	ST	–	UART RX input
	SI	ST	–	SPI serial data input
P53/SCL/SCK	P53	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	SCL	ST	CMOS	I^2C serial clock line. It is open-drain.
	SCK	ST	CMOS	SPI serial clock input/output
P54/OSCI/RCOUT	P54	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wakeup
	OSCI	XTAL	–	Clock input of crystal/ resonator oscillator
	RCOUT	–	CMOS	Clock output of internal RC oscillator Clock output of external RC oscillator (open-drain)
P55/OSCO/ERCin	P55	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	OSCO	–	XTAL	Clock output of crystal/resonator oscillator
	ERCin	AN	–	External RC input pin
P56/TC2	P56	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	TC2	ST	–	Timer 2 clock input
P57/TC3/PDO	P57	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	TC3	ST	–	Timer 3 clock input
	PDO	–	CMOS	Programmable divider output

Name	Function	Input Type	Output Type	Description
P60/ADC0//INT	P60	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	ADC0	AN	–	ADC Input 0
	/INT	ST	–	External interrupt pin
P61/ADC1	P61	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	ADC1	AN	–	ADC Input 1
P62/ADC2	P62	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	ADC2	AN	–	ADC Input 2
P63/ADC3	P63	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	ADC3	AN	–	ADC Input 3
P64/ADC4	P64	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	ADC4	AN	–	ADC Input 4
P65/ADC5	P65	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	ADC5	AN	–	ADC Input 5
P66/ADC6	P66	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	ADC6	AN	–	ADC Input 6
P67/ADC7	P67	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	ADC7	AN	–	ADC Input 7
P70/CO1	P70	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	CO1	–	CMOS	Output of Comparator 1
P71/CIN1+	P71	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	CIN1+	AN	–	Non-inverting end of Comparator 1
P72/CIN1-	P72	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	CIN1-	AN	–	Inverting end of Comparator 1
P73	P73	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
P74/TC1	P74	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	TC1	ST	–	Timer 1 clock input
P75/PWMA	P75	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	PWMA	–	CMOS	PWMA output

Name	Function	Input Type	Output Type	Description
P76/PWMB	P76	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	PWMB	–	CMOS	PWMB output
P77/TCC	P77	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	TCC	ST	–	Real Time Clock/Counter clock input
P80/CO2	P80	–	–	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain
	CO2	–	CMOS	Output of Comparator 2
P81/CIN2+	P81	–	–	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain
	CIN2+	AN	–	Non-inverting end of Comparator 2
P82/CIN2-	P82	–	–	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain
	CIN2-	AN	–	Inverting end of Comparator 2
P83//RESET	P83	–	–	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain
	/RESET	ST	–	Internal pull-high reset pin
P84	P84	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain
P85	P85	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain
P86	P86	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain
P87	P87	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain
P90	P90	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain
P91	P91	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain
P92	P92	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain
P93	P93	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain
P94	P94	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain
P95	P95	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain
P96	P96	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain
P97	P97	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain

5 Block Diagram

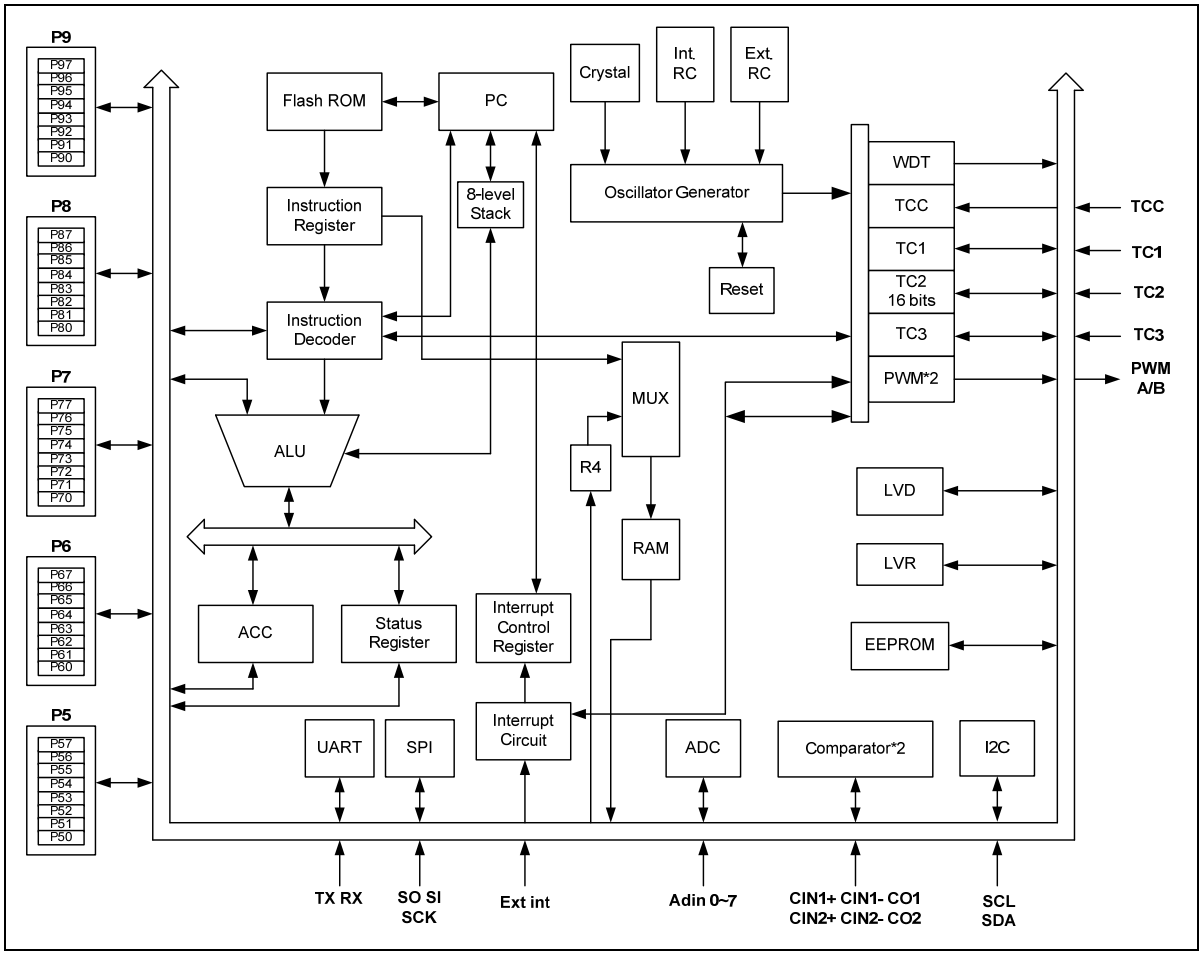


Figure 5-1 Functional Block Diagram

6 Functional Description

6.1 Operational Registers

6.1.1 R0: IAR (Indirect Addressing Register)

R0 is not a physically implemented register. Its major function is to perform as an indirect addressing pointer. Any instruction using R0 as a pointer actually accesses data pointed by the RAM Select Register (R4).

6.1.2 R1: BSR (Bank Select Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	SBS0	0	0	0	GBS0

Bits 7 ~ 5: not used bits, fixed to 0 all the time.

Bit 4 (SBS0): Special register bank select bit. It is used to select Bank 0/1 of the Special Registers R5~R4F.

0: Bank 0

1: Bank 1

Bits 3 ~ 1: not used bits, fixed to 0 all the time.

Bit 0 (GBS0): General register bank select bit. It is used to select Bank 0/1of the General Register R80~RFF.

0: Bank 0

1: Bank 1

6.1.3 R2: PC (Program Counter)

- Depending on the device type, R2 and hardware stack are 12-bit wide. The structure is depicted in Figure 6-1.
- Generates 8K×15 bits on-chip Flash ROM addresses to the relative programming instruction codes. One program page is 4096 words long.
- R2 is set as all "0"s when under Reset condition.
- "JMP" instruction allows direct loading of the lower 12 program counter bits. Thus, "JMP" allows the PC to go to any location within a page.

- "CALL" instruction loads the lower 12 bits of the PC, and the present PC value will be incremented by 1 and is pushed onto the stack. Thus, the subroutine entry address can be located anywhere within a page.
- "LJMP" instruction allows direct loading of the lower 13 program counter bits. Therefore, "LJMP" allows the PC to jump to any location within 8K (2^{13}).
- "LCALL" instruction loads the lower 13 bits of the PC and PC+1 will be pushed onto the stack. Thus, the subroutine entry address can be located anywhere within 8K (2^{13}).
- "RET" ("RETL k", "RETI") instruction loads the program counter with the contents of the top-level stack.
- "ADD R2, A" allows a relative address to be added to the current PC, and the ninth and above bits of the PC will increase progressively.
- "MOV R2, A" allows to load an address from the "A" register to the lower 8 bits of the PC, and the ninth and above bits of the PC to remain unchanged.
- Any instruction except “ADD R2,A” that is written to R2 (e.g. "MOV R2, A", "BC R2, 6",·etc.) will cause the ninth bit and the above bits (A8~A11) of the PC to remain unchanged.
- All instructions are single instruction cycle (fclk/2, fclk/4, fclk/8, fclk/16). The instruction that would change the contents of R2 will need one more instruction cycle.

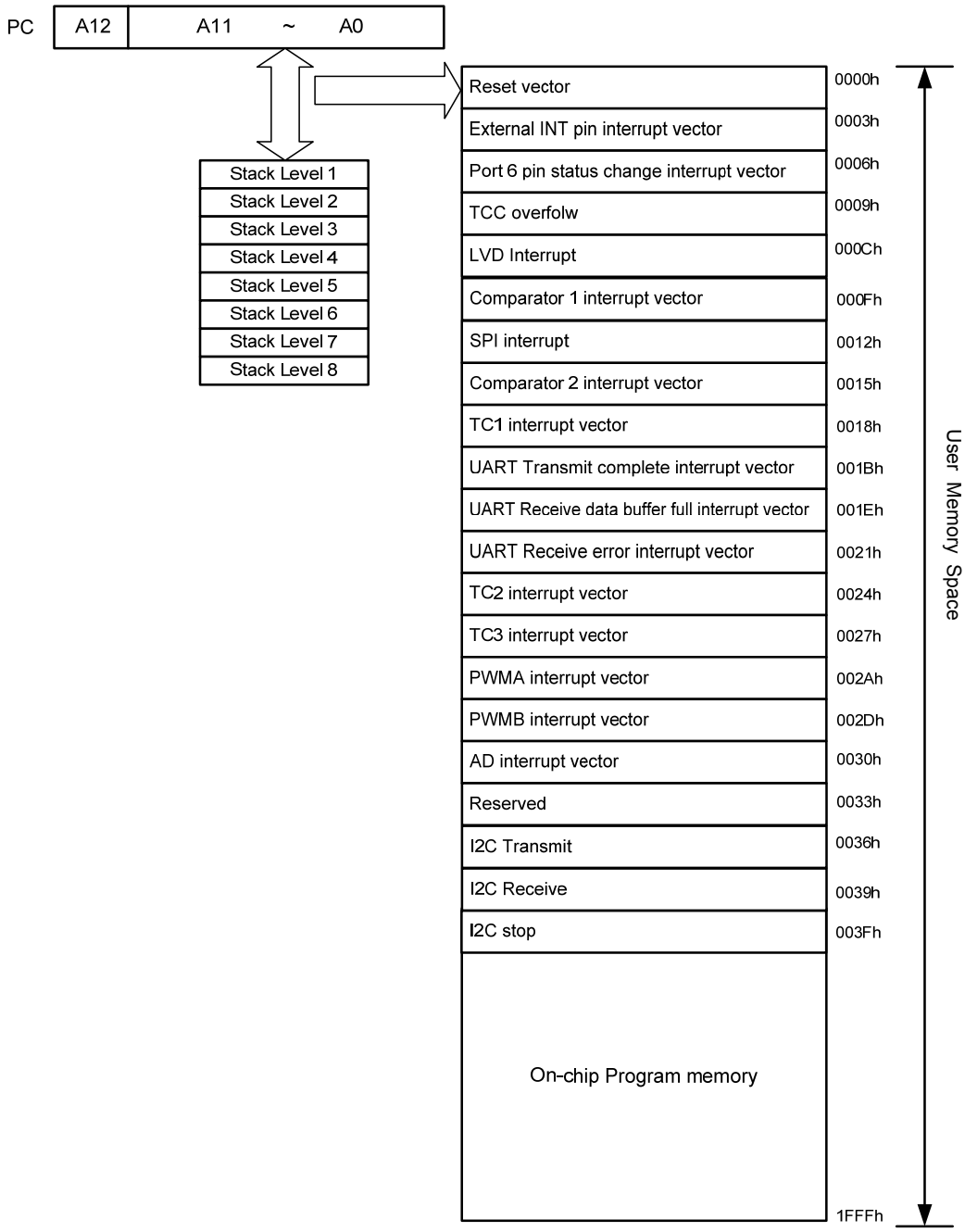


Figure 6-1 Program Counter Organization

Address	Bank 0	Bank 1
0×00	IAR (Indirect Addressing Register)	
0×01	BSR (Bank Selection Control Register)	
0×02	PC (Program Counter)	
0×03	SR (Status Register)	
0×04	RSR (RAM Select Register)	
0×05	Port 5	P5PHCR
0×06	Port 6	P6PHCR
0×07	Port 7	P7PHCR
0×08	Port 8	P8PHCR
0×09	Port 9	P9PHCR
0×0A	-	-
0×0B	OMCR (Operating Mode Control Register)	P5PLCR
0×0C	ISR1 (Interrupt Status Register 1)	P6PLCR
0×0D	ISR2 (Interrupt Status Register 2)	P7PLCR
0×0E	ISR3 (Interrupt Status Register 3)	P8PLCR
0×0F	-	P9PLCR
0×10	EIESCR	-
0×11	WDTCR	P5HD/SCR
0×12	LVDCR	P6HD/SCR
0×13	TCCCR	P7HD/SCR
0×14	TCCDATA	P8HD/SCR
0×15	IOCR5	P9HD/SCR
0×16	IOCR6	-
0×17	IOCR7	P5ODCR
0×18	IOCR8	P6ODCR
0×19	IOCR9	P7ODCR
0×1A	-	P8ODCR
0×1B	-	P9ODCR
0×1C	IMR1 (Interrupt Mask Register 1)	-
0×1D	IMR2 (Interrupt Mask Register 2)	IRCS
0×1E	IMR3 (Interrupt Mask Register 3)	-
0×1F	-	EEROM Control
0×20	P5WUCR	EEPROM ADDR
0×21	P5WUECR	EEPROM DATA
0×22	P7WUCR	-
0×23	P7WUECR	I^2CCR1 (I^2C Status and Control Register 1)
0×24	ADCR1 (ADC Control Register 1)	I^2CCR2 (I^2C Status and Control Register 2)
0×25	ADCR2 (ADC Control Register 2)	I^2CSA (I^2C Slave Address Register)

(Continuation)

Address	Bank 0	Bank 1
0×26	ADICL (ADC Input Select Low Byte Reg.)	I2CDA (I^2C device address register)
0×27	-	I^2CDB (I^2C data buffer)
0×28	-	I^2CA
0×29	ADDH (AD Data High 8-bit Register)	-
0×2A	ADDL (AD Data Low 4-bit Register)	PWMER (PWM Enable Control Register)
0×2B	SPICR (SPI Control Register)	TIMEN (Timer/PWM Enable Control Register)
0×2C	SPIS (SPI Status Register)	-
0×2D	SPIR (SPI Read Buffer)	-
0×2E	SPIW (SPI Write Buffer)	-
0×2F	WUCR1	PWMACR (PWM A Control Register)
0×30	-	PWMBCR (PWM B Control Register)
0×31	-	-
0×32	URCR1 (UART Control Register 1)	TACR (Timer A Control Register)
0×33	URCR2 (UART Control Register 2)	TBCR (Timer B Control Register)
0×34	URS (UART Status Register)	-
0×35	URRD (UART Receive Data Buffer Register)	TAPRD (Timer A Period buffer)
0×36	URTD (UART Transmit Data Buffer Register)	TBPRD (Timer B Period buffer)
0×37	TBPTL	-
0×38	TBPTH	TADT (Timer A Duty Buffer)
0×39	CMP1CR (Comparator 1 Control Register)	TBDT (Timer B Duty Buffer)
0×3A	-	-
0×3B	-	PRDxL
0×3C	CMP2CR	DTxL
0×3D	-	-
0×3E	-	-
0×3F	-	-
0×40	-	-
0×41	-	-
0×42	-	-
0×43	CPIRLCON	-
0×44	-	-
0×45	-	-
0×46	-	-
0×47	-	-
0×48	TC1CR	-

(Continuation)

Address	Bank 0	Bank 1
0×49	TCR1DA	-
0×4A	TCR1DB	-
0×4B	TC2CR	-
0×4C	TCR2DH	-
0×4D	TCR2DL	-
0×4E	TC3CR	-
0×4F	TCR3D	-
0×50	General Purpose Register	
0×51		
. .		
0×7F		
0×80	Bank 0	Bank 1
0×81		
. . .		
0×FE		
0×FF		

Figure 6-2 Data Memory Configuration

6.1.4 R3: SR (Status Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	T	P	Z	DC	C

Bits 7 ~ 5: not used bits, fixed to 0 all the time.

Bit 4 (T): Time-out bit

Set to 1 with the "SLEP" and "WDTC" commands, or during power-up and reset to 0 by WDT time-out.

Bit 3 (P): Power down bit.

Set to 1 during power-on or by a "WDTC" command and reset to 0 by a "SLEP" command.

Bit 2 (Z): Zero flag

Set to "1" if the result of an arithmetic or logic operation is zero.

Bit 1 (DC): Auxiliary carry flag

Bit 0 (C): Carry flag

6.1.5 R4: RSR (RAM Select Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RSR7	RSR6	RSR5	RSR4	RSR3	RSR2	RSR1	RSR0

Bits 7 ~ 0 (RSR7 ~ RSR0): these bits are used to select registers (Address: 00~FF) in indirect address mode. Users can see more details of the data memory configuration in Figure 6-2.

6.1.6 Bank 0 R5 ~ R9 (Port 5 ~ Port 9)

R5, R6, R7, R8 and R9 are I/O data registers.

6.1.7 Bank 0 RA (Unused)

6.1.8 Bank 0 RB OMCR (Operating Mode Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CPUS	IDLE	TC1SS	TC2SS	TC3SS	TASS	TBSS	0

Bit 7 (CPUS): CPU Oscillator Source Select

0: Fs: sub-oscillator for WDT internal RC time base

1: Fm: main-oscillator

When CPUS=0, the CPU oscillator selects the sub-oscillator and the main oscillator is stopped.

Bit 6 (IDLE): Idle Mode Enable Bit. This bit will determine as to which mode to proceed to after execution of the SLEP instruction.

0: "IDLE=0"+ SLEP instruction → sleep mode

1: "IDLE=1"+ SLEP instruction → idle mode

CPU Operation Mode

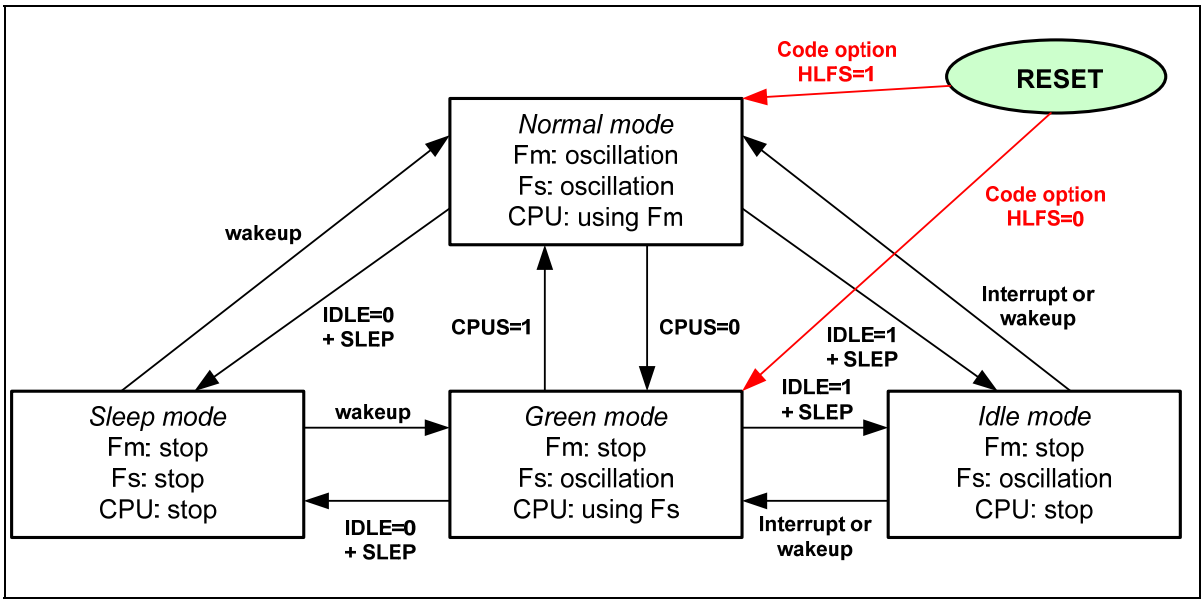


Figure 6-3 CPU Operation Mode

Bit 5 (TC1SS): TC1 clock source select bit

0: Fs is used as Fc

1: Fm is used as Fc

Bit 4 (TC2SS): TC2 clock source select bit

0: Fs is used as Fc

1: Fm is used as Fc

Bit 3 (TC3SS): TC3 clock source select bit

0: Fs is used as Fc

1: Fm is used as Fc

Bit 2 (TASS): Timer A clock source select bit

0: Fs is used as Fc

1: Fm is used as Fc

Bit 1 (TBSS): Timer B clock source select bit

0: Fs is used as Fc

1: Fm is used as Fc

Bit 0: not used, fixed to “0” all the time.

6.1.9 Bank 0 RC: ISR1 (Interrupt Status Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LVDIF	ADIF	SPIF	PWMBIF	PWMAIF	EXIF	ICIF	TCIF

"1" means there's interrupt request, and "0" means no interrupt occurs

Bit 7 (LVDIF): Low Voltage Detector Interrupt flag

When LVD1, LVD0 = "0, 0", Vdd > 2.3V, LVDIF is "0", Vdd ≤ 2.3V, set LVDIF to "1". LVDIF is reset to "0" by software.

When LVD1, LVD0 = "0, 1", Vdd > 3.3V, LVDIF is "0", Vdd ≤ 3.3V, set LVDIF to "1". LVDIF is reset to "0" by software.

When LVD1, LVD0 = "1, 0", Vdd > 4.0V, LVDIF is "0", Vdd ≤ 4.0V, set LVDIF to "1". LVDIF is reset to "0" by software.

When LVD1, LVD0 = "1, 1", Vdd > 4.5V, LVDIF is "0", Vdd ≤ 4.5V, set LVDIF to "1". LVDIF is reset to "0" by software.

Bit 6 (ADIF): Interrupt flag for analog-to-digital conversion. Set when AD conversion is completed, reset by software.

Bit 5 (SPIF): SPI mode interrupt flag. Flag is cleared by software.

Bit 4 (PWMBIF): PWMB (Pulse Width Modulation) interrupt flag. Set when a selected period is reached, reset by software.

Bit 3 (PWMAIF): PWMA (Pulse Width Modulation) interrupt flag. Set when a selected period is reached, reset by software.

Bit 2 (EXIF): External Interrupt Flag.

Bit 1 (ICIF): Port 6 Input Status Change Interrupt Flag. Set when Port 6 input changes, reset by software.

Bit 0 (TCIF): TCC Overflow Interrupt Flag. Set when TCC overflows, reset by software.

6.1.10 Bank 0 RD: ISR2 (Interrupt Status Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CMP2IF	CMP1IF	TC3IF	TC2IF	TC1IF	UERRIF	RBFF	TBEF

Bit 7 (CMP2IF): Comparator 2 Interrupt flag. Set when a change occurs in the output of Comparator 2, reset by software.

Bit 6 (CMP1IF): Comparator 1 Interrupt flag. Set when a change occurs in the output of Comparator 1, reset by software.

Bit 5 (TC3IF): 8-bit Timer/Counter 3 interrupt flag. Interrupt flag is cleared by software.

Bit 4 (TC2IF): 16-bit Timer/Counter 2 Interrupt Flag. Interrupt flag is cleared by software.

Bit 3 (TC1IF): 8-bit Timer/Counter 1 Interrupt Flag. Interrupt flag is cleared by software.

Bit 2 (UERRIF): UART Receiving Error Interrupt. Interrupt flag is cleared by software or UART disabled.

Bit 1 (RBFF): UART receive mode data buffer full interrupt flag. Flag is cleared by software.

Bit 0 (TBEF): UART transmit mode data buffer empty interrupt flag. Flag is cleared by software.

6.1.11 Bank 0 RE: ISR3 (Interrupt Status Register 3)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	I2CSTPIF	0	I2CRIF	I2CTIF

Bits 7 ~ 4: not used, fixed to "0" all the time.

Bit 3 (I2CSTPIF): I^2C slave received data stop interrupt flag.

Bit 2: not used bit, fixed to "0" all the time.

Bit 1 (I2CRIF): I^2C receive interrupt flag. Set when I^2C receives 1 byte data and responds ACK signal. Reset by firmware or I^2C disabled.

Bit 0 (I2CTIF): I^2C transmit interrupt flag. Set when I^2C transmits 1 byte data and receives handshake signal (ACK or NACK). Reset by firmware or I^2C disable**.**

6.1.12 Bank 0 RF (Unused)

6.1.13 Bank 0 R10: EIESCR (External Interrupt Edge Select Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	0	0	EIES

Bits 7 ~ 1: unused bit, set to 0 all the time.

Bit 0 (EIES): External Interrupt Edge Select Bit

0: falling edge interrupt

1: rising edge interrupt

6.1.14 Bank 0 R11: WDTCR

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WDTE	EIS	INT	0	PSWE	PSW2	PSW1	PSW0

Bit 7 (WDTE): Watchdog Timer Enable Bit. WDTE is both readable and writable.

0: Disable WDT

1: Enable WDT

Bit 6 (EIS): P60/ /INT switch control bit

0: P60

1: /INT, external interrupt pin. In this case, the I/O control bit of P60 must be set to "1". When EIS is "0", the path of /INT is masked. When EIS is "1", the status of /INT pin can also be read by way of reading Port 6 (R6).

EIS is both readable and writable.

Bits 5 (INT): interrupt enable flag.

0: interrupt masked by DISI or hardware interrupt

1: interrupt enabled by ENI/RETI instructions

Bit 4: not used bit, fixed to “0” all the time.

Bit 3 (PSWE): Prescaler Enable Bit for WDT

0: Prescaler disable, WDT rate is 1:1

1: Prescaler enable, WDT rate is set from Bits 2 ~ 0.

Bits 2 ~ 0 (PSW2~PSW0): WDT Prescale Bits

PSW2	PSW1	PSW0	WDT Rate
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

6.1.15 Bank 0 R12: LVDCR (Low Voltage Detector Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	LVDEN	/LVD	LVD1	LVD0

Bits 7 ~ 4: not used bits, fixed to 0 all the time.

Bit 3 (LVDEN): Low voltage detector enable bit

0: LVD disable

1: LVD enable

Bit 2 (/LVD): Low voltage detector. This is a read only bit. When the VDD pin voltage is lower than the LVD voltage, the interrupt level which set by LVD1 and LVD0, this bit will be cleared.

0: low voltage is detected

1: low voltage is not detected or LVD function is disabled

Bits 1 ~ 0 (LVD1 ~ LVD0): Low voltage detector level select bits

LVD1	LVD0	LVD Voltage Interrup Level
0	0	2.3
0	1	3.3
1	0	4.0
1	1	4.5

6.1.16 Bank 0 R13: TCCCR (TCC Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	TCCS	TS	TE	PSTE	PST2	PST1	PST0

Bit 7: unused bit, set to 0 all the time.

Bit 6 (TCCS): TCC Clock Source Select Bit

0: Fs (sub clock)

1: Fm (main clock)

Bit 5 (TS): TCC Signal Source

0: Internal oscillator cycle clock. If P77 is used as I/O pin, TS must be 0.

1: Transition on the TCC pin

Bit 4 (TE): TCC Signal Edge

0: Increment if the transition from low to high takes place on the TCC pin.

1: Increment if the transition from high to low takes place on the TCC pin.

Bit 3 (PSTE): Prescaler Enable Bit for TCC

0: prescaler disable, TCC rate is 1:1

1: prescaler enable, TCC rate is set from Bits 2~0.

Bits 2 ~ 0 (PST2 ~ PST0): TCC Prescaler Bits

PST2	PST1	PST0	TCC Rate
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

6.1.17 Bank 0 R14: TCCDATA (TCC Data Register)

Increase by an external signal edge through the TCC pin, or by the instruction cycle clock. External signal of TCC trigger pulse width must be greater than one instruction. The signals to increase the counter are determined by Bit 4 and Bit 5 of the TCCCR register. Writable and readable as any other registers.

6.1.18 Bank 0 R15 ~ R19 (IOCR5 ~ IOCR9)

These registers are used to control the I/O port direction. They are both readable and writable.

0: set the relative I/O pin as output

1: put the relative I/O pin into high impedance

6.1.19 Bank 0 R1A~R1B (Unused)

6.1.20 Bank 0 R1C: IMR1 (Interrupt Mask Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LVDIE	ADIE	SPIE	PWMBIE	PWMAIE	EXIE	ICIE	TCIE

Bit 7 (LVDIE): LVDIF interrupt enable bit.

0: Disable LVDIF interrupt

1: Enable LVDIF interrupt

Bit 6 (ADIE): ADIF interrupt enable bit.

0: Disable ADIF interrupt

1: Enable ADIF interrupt

When ADC Complete is used to enter an interrupt vector or enter the next instruction, the ADIE bit must be set to “Enable“.

Bit 5 (SPIE): Interrupt enable bit.

0: disable SPIF interrupt

1: enable SPIF interrupt

Bit 4 (PWMBIE): PWMBIF interrupt enable bit.

0: Disable PWMB interrupt

1: Enable PWMB interrupt

Bit 3 (PWMAIE): PWMAIF interrupt enable bit.

0: Disable PWMA interrupt

1: Enable PWMA interrupt

Bit 2 (EXIE): EXIF interrupt enable bit.

0: disable EXIF interrupt

1: enable EXIF interrupt

Bit 1 (ICIE): ICIF interrupt enable bit.

0: disable ICIF interrupt

1: enable ICIF interrupt

Bit 0 (TCIE): TCIF interrupt enable bit.

0: disable TCIF interrupt

1: enable TCIF interrupt

6.1.21 Bank 0 R1D: IMR2 (Interrupt Mask Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CMP2IE	CMP1IE	TC3IE	TC2IE	TC1IE	UERRIE	URIE	UTIE

Bit 7 (CMP2IE): CMP2IF interrupt enable bit.

0 : Disable CMP2IF interrupt

1 : Enable CMP2IF interrupt

When the Comparator output status changed is used to enter an interrupt vector or enter the next instruction, the CMP2IE bit must be set to “Enable“.

Bit 6 (CMP2IE): CMP1IF interrupt enable bit.

0 : Disable CMP1IF interrupt

1 : Enable CMP1IF interrupt

When the Comparator output status changed is used to enter an interrupt vector or enter the next instruction, the CMP1IE bit must be set to “Enable“.

Bit 5 (TC3IE): Interrupt enable bit.

0 : Disable TC3IF interrupt

1 : Enable TC3IF interrupt

Bit 4 (TC2IE): Interrupt enable bit.

0 : Disable TC2IF interrupt

1 : Enable TC2IF interrupt

Bit 3 (TC1IE): Interrupt enable bit.

0 : Disable TC1IF interrupt

1 : Enable TC1IF interrupt

Bit 2 (UERRIE): UART receive error interrupt enable bit.

0 : Disable UERRIF interrupt

1 : Enable UERRIF interrupt

Bit 1 (URIE): UART receive mode Interrupt enable bit.

0 : Disable RBFF interrupt

1 : Enable RBFF interrupt

Bit 0 (UTIE): UART transmit mode interrupt enable bit.

0 : Disable TBEF interrupt

1 : Enable TBEF interrupt

6.1.22 Bank 0 R1E: IMR3 (Interrupt Mask Register 3)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	I2CSTPIE	0	I2CRIE	I2CTIE

Bits 7 ~ 3: Unused, set to 0 all the time.

Bit 3 (I2CSTPIE): I2CSTPIF interrupt enable bit.

0: Disable I2CSTP interrupt

1: Enable I2CSTP interrupt

Bit 2: Unused, set to 0 all the time.

Bit 1 (I2CRIE): I2C Interface Rx interrupt enable bit

0: Disable interrupt

1: Enable interrupt

Bit 2 (I2CTIE): I2C Interface Tx interrupt enable bit

0: Disable interrupt

1: Enable interrupt

6.1.23 Bank 0 R1F (Unused)

6.1.24 Bank 0 R20: P5WUCR (Port 5 Wake-up Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WU_P57	WU_P56	WU_P55	WU_P54	WU_P53	WU_P52	WU_P51	WU_P50

Bits 7 ~ 0 (WU_P57 ~ WU_P50): Port 5 wake-up function control.

0: disable wake-up function

1: enable wake-up function

6.1.25 Bank 0 R21: P5WUECR (Port 5 Wake-up Edge Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WUE_P57	WUE_P56	WUE_P55	WUE_P54	WUE_P53	WUE_P52	WUE_P51	WUE_P50

Bits 7 ~ 0 (WUE_P57 ~ WUE_P50): Port 5 wake-up signal edge select.

0: falling edge trigger

1: rising edge trigger

6.1.26 Bank 0 R22: P7WUCR (Port 7 Wake-up Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WU_P77	WU_P76	WU_P75	WU_P74	WU_P73	WU_P72	WU_P71	WU_P70

Bits 7 ~ 0 (WU_P77 ~ WU_P70): Port 7 wake-up function control.

0: disable wake-up function

1: enable wake-up function

6.1.27 Bank 0 R23: P7WUECR (Port 7 Wake-up Edge Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WUE_P77	WUE_P76	WUE_P75	WUE_P74	WUE_P73	WUE_P72	WUE_P71	WUE_P70

Bits 7 ~ 0 (WUE_P77 ~ WUE_P70): Port 7 wake-up signal edge select.

0: falling edge trigger

1: rising edge trigger

6.1.28 Bank 0 R24: ADCR1 (ADC Control Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
VREFS	ADRUN	ADPD	0	0	ADIS2	ADIS1	ADIS0

Bit 7 (VREFS): Input source of the VREF of the ADC.

0: The Vref of the ADC is connected to Vdd (default value), and the P50/VREF pin carries out the function of P50

1: The Vref of the ADC is connected to P50/VREF.

Note: the following shows the priority of P50/VREF pin

P50/VREF Pin Priority	
High	Low
VREF	P50

Bit 6 (ADRUN): ADC starts to run

0: Reset on completion of the conversion. This bit can not be reset by software.

1: A/D conversion starts. This bit can be set by software.

Bit 5 (ADPD): ADC Power-down mode

0: switch off the resistor reference to save power even while the CPU is operating.

1: ADC is operating

Bits 4 ~ 3: unused bits, set to 0 all the time

Bit 2 ~ 0 (ADIS2 ~ ADIS0): Analog Input Selection

ADIS2	ADIS1	ADIS0	Analog Input Pin
0	0	0	AD0/P60
0	0	1	AD1/P61
0	1	0	AD2/P62
0	1	1	AD3/P63
1	0	0	AD4/P64
1	0	1	AD5/P65
1	1	0	AD6/P66
1	1	1	AD7/P67

Note: *The AD channel can only be changed when the ADIF bit and the ADRUN bit are both low.*

6.1.29 Bank 0 R25: ADCR2 (ADC Control Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CALI	SIGN	VOF2	VOF1	VOF0	**CKR2**	**CKR1**	**CKR0**

Bit 7 (CALI): Calibration enable bit for A/D offset

0: Disable Calibration

1: Enable Calibration

Bit 6 (SIGN): Polarity bit of offset voltage

0: Negative voltage

1: Positive voltage

Bits 5 ~ 3 (VOF2 ~ VOF0): Offset voltage bits

VOF2	VOF1	VOF0	OFFSET
0	0	0	0 LSB
0	0	1	2 LSB
0	1	0	4 LSB
0	1	1	6 LSB
1	0	0	8 LSB
1	0	1	10 LSB
1	1	0	12 LSB
1	1	1	14 LSB

Bits 2 ~ 0 (CKR2 ~ CKR0): prescaler of ADC oscillator clock rate

CKR2 CKR1 CKR0	Operation Mode	Max. System Operation Frequency
000 (default)	Fosc/4	4 MHz
001	Fosc/1	1 MHz
010	Fosc/2	2 MHz
011	Fosc/8	8 MHz
100	Fosc/16	16 MHz
101	Fosc/32	32 MHz
110	Fosc/64	64 MHz
111	Internal RC	–

6.1.30 Bank 0 R26: ADICL (ADC Input Select Low Byte Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADE7	ADE6	ADE5	ADE4	ADE3	ADE2	ADE1	ADE0

Bit 7 (ADE7): AD converter enable bit of P67 pin.

0: Disable ADC7, P67 act as I/O pin.

1: Enable ADC7 to act as analog input pin.

Bit 6 (ADE6): AD converter enable bit of P66 pin.

0: Disable ADC6, P66 act as I/O pin

1: Enable ADC6 to act as analog input pin

Bit 5 (ADE5): AD converter enable bit of P65 pin.

0: Disable ADC5, P65 act as I/O pin

1: Enable ADC5 to act as analog input pin

Bit 4 (ADE4): AD converter enable bit of P64 pin.

0: Disable ADC4, P64 act as I/O pin

1: Enable ADC4 to act as analog input pin

Bit 3 (ADE3): AD converter enable bit of P63 pin.

0: Disable ADC3, P63 act as I/O pin

1: Enable ADC3 to act as analog input pin

Bit 2 (ADE2): AD converter enable bit of P62 pin.

0: Disable ADC2, P62 act as I/O pin

1: Enable ADC2 to act as analog input pin

Bit 1 (ADE1): AD converter enable bit of the P61 pin.

0 : Disable ADC1, P61 act as I/O pin

1 : Enable ADC1 to act as analog input pin

Bit 0 (ADE0): AD converter enable bit of the P60 pin.

0 : Disable ADC0, P60 act as I/O pin

1 : Enable ADC0 act as analog input pin

The following table shows the priority of P60/ADC0//INT pin.

P60/ADC0//INT Pin Priority		
High	Medium	Low
/INT	ADC0	P60

6.1.31 Bank 0 R27 ~ R28 (Unused)

6.1.32 Bank 0 R29: ADDH (AD Data High Bits Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AD11	AD10	AD9	AD8	AD7	AD6	AD5	AD4

Bits 7 ~ 0 (AD11 ~ AD4): AD high 8-bit data buffer. When A/D conversion is completed, the result of high 8 bits is stored into ADDH; the low 4 bits is stored into ADDL. Then the ADRUN bit is cleared and the ADIF is set.

6.1.33 Bank 0 R2A: ADDL (AD Data Low Bits Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	AD3	AD2	AD1	AD0

Bits 7 ~ 4: unused, set to 0 all the time.

Bits 3 ~ 0 (AD3 ~ AD0): AD low 4-bit data buffer.

6.1.34 Bank 0 R2B: SPICR (SPI Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CES	SPIE	SRO	SSE	SDOC	SBRS2	SBRS1	SBRS0

Bit 7 (CES): Clock Edge Select Bit

0 : Data shift out on a rising edge, and shifts in on a falling edge. Data is on hold during low-level.

1 : Data shift out on a falling edge, and shift in on a rising edge. Data is on hold during high-level.

Bit 6 (SPIE): SPI Enable Bit

0 : Disable SPI mode

1 : Enable SPI mode

Bit 5 (SRO): SPI Read Overflow Bit

0 : No overflow

1 : A new data is received while the previous data is still being held in the SPIR register. In this situation, the data in SPIS register will be destroyed. To avoid setting this bit, user is required to read the SPIR register although only transmission is implemented. This can only occur in slave mode.

Bit 4 (SSE): SPI Shift Enable Bit

0 : Reset as soon as the shift is completed, and the next byte is read to shift.

1 : Start to shift, and remain on "1" while the current byte is still being transmitted.

Bit 3 (SDOC): SDO Output Status Control Bit

0 : After the serial data output, SDO remain high.

1 : After the serial data output, SDO remain low.

Bits 2 ~ 0 (SBRS2 ~ SBRS0): SPI Baud Rate Select Bits

SBRS2	SBRS1	SBRS0	Mode	SPI Baud Rate
0	0	0	Master	Fosc/2
0	0	1	Master	Fosc/4
0	1	0	Master	Fosc/8
0	1	1	Master	Fosc/16
1	0	0	Master	Fosc/32
1	0	1	Master	Fosc/64
1	1	0	Slave	/SS enable
1	1	1	Slave	/SS disable

6.1.35 Bank 0 R2C: SPIS (SPI Status Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DORD	TD1	TD0	0	OD3	OD4	0	RBF

Bit 7 (DORD): Data Shift of Type Control Bit

0 : Shift left (MSB first)

1 : Shift right (LSB first)

Bits 6 ~ 5 (TD1 ~ TD0): SDO Status Output Delay Times Options. When the CPU oscillator source uses Fs, it is delayed by just 1 CLK time.

TD1	TD0	Delay Time
0	0	8 CLK
0	1	16 CLK
1	0	24 CLK
1	1	32 CLK

Bit 4: Not used, set to 0 all the time.

Bit 3 (OD3): Open drain control bit

0 : disable Open drain for SDO

1 : enable Open drain for SDO

Bit 2 (OD4): Open drain control bit

0 : disable Open drain for SCK

1 : enable Open drain for SCK

Bit 1: Unused, set to 0 all the time.

Bit 0 (RBF): Read Buffer Full Flag

0 : Receiving not completed, and SPIR has not fully exchanged.

1 : Receiving completed, and SPIR is fully exchanged.

6.1.36 Bank 0 R2D: SPIR (SPI Read Buffer Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SRB7	SRB6	SRB5	SRB4	SRB3	SRB2	SRB1	SRB0

Bits 7 ~ 0 (SRB7 ~ SRB0): SPI Read Data Buffer

6.1.37 Bank 0 R2E: SPIR (SPI Write Buffer Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SWB7	SWB6	SWB5	SWB4	SWB3	SWB2	SWB1	SWB0

Bits 7 ~ 0 (SWB7 ~ SWB0): SPI Write Data Buffer

6.1.38 Bank 0 R2F: WUCR1 (Wake-up Control Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	SPIWE	LVDWE	ICWE	ADWE	CMP2WE	CMP1WE	EXWE

Bit 7: Unused, set to 0 all the time.

Bit 6 (SPIWE): SPI wake-up enable bit. Acts when SPI works in slave mode.

0: Disable SPI wake up

1: Enable SPI wake up

Bit 5 (LVDWE): Low Voltage Detect Wake-up Enable Bit

0: Disable Low Voltage Detect wake-up

1: Enable Low Voltage Detect wake-up

When Low Voltage Detect is used to enter an interrupt vector or to wake-up the IC from sleep/idle with Low Voltage Detect running, the LVDWE bit must be set to “Enable“.

Bit 4 (ICWE): Port 6 Input Status Change Wake-up enable bit.

0: Disable Port 6 input status change wake-up

1: Enable Port 6 input status change wake-up

When Port 6 input status changed is used to enter an interrupt vector or to wake-up the IC from sleep/idle, the ICWE bit must be set to “Enable“.

Bit 3 (ADWE): A/D Converter Wake-up Function Enable Bit

0: Disable AD converter wake-up

1: Enable AD converter wake-up

When AD Complete status is used to enter an interrupt vector or to wake-up the IC from sleep/idle with AD conversion running, the ADWE bit must be set to “Enable“.

Bits 2 ~ 1 (CMP2WE ~ CMP1WE): Comparators 2 ~ 1 wake-up enable bits

0: Disable Comparator wake up

1: Enable Comparator wake up

When Comparators 2 ~ 1 output status change is used to enter an interrupt vector or to wake up the IC from sleep, the CMPWE bit must be set to “Enable“.

Bit 0 (EXWE): External Interrupt Wake-up Function Enable Bit

0: Disable external interrupt wake-up

1: Enable external interrupt wake-up

When the External Interrupt status changed is used to enter an interrupt vector or to wake up the IC from sleep, the EXWE bits must be set to "Enable".

6.1.39 Bank 0 R30~R31 (Unused)

6.1.40 Bank 0 R32: URCR1 (UART Control Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
URTD8	UMODE1	UMODE0	BRATE2	BRATE1	BRATE0	UTBE	TXE

Bit 7 (URTD8): Transmission Data Bit 8

Bits 6 ~ 5 (UMODE1 ~ UMODE0): UART mode select bits

UMODE1	UMODE0	UART Mode
0	0	Mode 1: 7-bit
0	1	Mode 1: 8-bit
1	0	Mode 1: 9-bit
1	1	Reserved

Bits 4 ~ 2 (BRATE2 ~ BRATE0): Transmit Baud rate selection

BRATE2	BRATE1	BRATE0	Baud Rate	8 MHz
0	0	0	Fc/13	38400
0	0	1	Fc/26	19200
0	1	0	Fc/52	9600
0	1	1	Fc/104	4800
1	0	0	Fc/208	2400
1	0	1	Fc/416	1200
1	1	0	TC3	–
1	1	1	Reserved	

Bit 1 (UTBE): UART transfer buffer empty flag. Set to 1 when transfer buffer is empty. Reset to 0 automatically when writing into the URTD register. The UTBE bit will be cleared by hardware when enabling transmission. The UTBE bit is read-only. Therefore, writing to the URTD register is necessary when it is desired to start transmit shifting.

Bit 0 (TXE): Enable transmission

0: Disable

1: Enable

6.1.41 Bank 0 R33: URCR2 (UART Control Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	SBIM1	SBIM0	UINVEN	0	0	0

Bits 7 ~ 6: Unused, set to 0 all the time.

Bits 5 ~ 4 (SBIM1 ~ SBIM0): Serial bus interface operating mode select

SBIM1	SBIM0	Operation Mode
0	0	I/O mode
0	1	SPI mode
1	0	UART mode
1	1	I^2C mode

Bit 3 (UINVEN): Enable UART TX and RX port inverse output.

0: Disable **TX** and **RX** port inverse output

1: Enable **TX** and **RX** port inverse output

Bits 2 ~ 0: Unused, set to 0 all the time.

6.1.42 Bank 0 R34: URS (UART Status Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
URRD8	EVEN	PRE	PRERR	OVERR	FMERR	URBF	RXE

Bit 7 (URRD8): Receiving Data Bit 8

Bit 6 (EVEN): Select Parity Check

0: Odd parity

1: Even parity

Bit 5 (PRE): enable parity addition

0: Disable

1: Enable

Bit 4 (PRERR): Parity error flag. Set to 1 when parity error occurs, clear to 0 by software.

Bit 3 (OVERR): Over running error flag. Set to 1 when overrun error occurs, clear to 0 by software.

Bit 2 (FMERR): Framing error flag. Set to 1 when framing error occurs, clear to 0 by software.

Bit 1 (URBF): UART read buffer full flag. Set to 1 when one character is received. Reset to 0 automatically when read from URS register. URBF will be cleared by hardware when enabling receiving. URBF bit is read-only. Therefore, reading the URS register is necessary to avoid overrun error.

Bit 0 (RXE): Enable receiving

0: Disable

1: Enable

6.1.43 Bank 0 R35: URRD (UART Receive Data Buffer Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
URRD7	URRD6	URRD5	URRD4	URRD3	URRD2	URRD1	URRD0

Bits 7 ~ 0 (URRD7 ~ URRD0): UART receive data buffer. Read only.

6.1.44 Bank 0 R36: URTD (UART Transmit Data Buffer Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
URTD7	URTD6	URTD5	URTD4	URTD3	URTD2	URTD1	URTD0

Bits 7 ~ 0 (URTD7 ~ URTD0): UART transmit data buffer. Write only.

6.1.45 Bank 0 R37: TBPTL (Table Point Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TB7	TB6	TB5	TB4	TB3	TB2	TB1	TB0

Bits 7 ~ 0 (TB7 ~ TB0): Table Point Address Bits 7~0.

For EM78F568N, this register is unused.

6.1.46 Bank 0 R38: TBPTH (Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
HLB	GP1	GP0	TB12	TB11	TB10	TB9	TB8

Bit 7 (HLB): take MLB or LSB at machine code.

Bits 6 ~ 5 (GP1 ~ GP0): general purpose read/write bits

Bits 4 ~ 0: Table Point Address Bits 12 ~ 8.

For EM78F568N, this register is unused.

6.1.47 Bank 0 R39: CMP1CR (Comparator 1 Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
C1RS	CP1OUT	CMP1COS1	CMP1COS0	CP1NS	CP1PS	CP1NRE	CP1NRDT

Bit 7 (C1RS): Comparator input reference source select bit

0 : Cin1+ external source

1 : Cin1+ internal source

Bit 6 (CP1OUT): Result of comparator output

Bits 5 ~ 4 (CMP1COS1 ~ CMP1COS0): Comparator 1/OP1 select bits

CMP1COS1	CMP1COS0	Function Description
		Comparator 1 is not used. P70, P71, P72 act as normal I/O pin
		P71, P72, act as Comparator 1 input pin and P70 acts as normal I/O pin
		P71, P72 act as Comparator 1 input pin and P70 acts as Comparator 1 output pin (CO1).
		Reserved

Bit 3 (CP1NS): negative end of Comparator 1 is connected to ground.

0: disable, P72/CIN1- as CIN1-

1: enable, P72/CIN1- as P72

Bit 2 (CP1PS): positive end of Comparator 1 is connected to ground.

0: disable, P71/CIN1+ as CIN1+.

1: enable, P71/CIN1+ as P71

Bit 1 (CP1NRE): Noise Rejection Enable Bit for Comparator 1

0: Disable noise rejection

1: Enable noise rejection (default). **But in Low Crystal 2 Oscillator (LXT2) mode, Green mode and Idle mode, the noise rejection circuits are always disabled.**

Bit 0 (CP1NRDT): Comparator 1 Noise Rejection Delay Time. In Low XTAL1 oscillator (LXT1) mode the noise rejection high/low pulse is always 4/Fm.

0: Comparator 1 output H/L pulses equal to 4/Fm (0.5 μs at 8 MHz) is regarded as signal.

1: Comparator 1 output H/L pulses equal to 8/Fm (1 μs at 8 MHz) is regarded as signal.

6.1.48 Bank 0 R3A~R3B: Unused

6.1.49 Bank 0 R3C: CMP2CR (Comparator 2 Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
C2RS	CP2OUT	CMP2COS1	CMP2COS0	CP2NS	CP2PS	CP2NRE	CP2NRDT

Bit 7 (C2RS): Comparator 2 input reference source select bit

0: Cin2+ external source

1: Cin2+ internal source

Bit 6 (CP2OUT): Result of Comparator 2 output

Bits 5 ~ 4 (CMP2COS1 ~ CMP2COS0): Comparator 2 / OP2 select bits

CMP2COS1	CMP2COS0	Function Description
0	0	Comparator 2 is not used. P80, P81, P82 act as normal I/O pin.
0	1	P81, P82, act as Comparator 2 input pin and P80 acts as normal I/O pin.
1	0	P81, P82 act as Comparator 2 input pin and P80 acts as Comparator 2 output pin (CO2).
1	1	Reserved

Bit 3 (CP2NS): Negative end of Comparator 2 is connected to ground.

0: disable, P82/CIN2- as CIN2-

1: enable, P82/CIN2- as P82

Bit 2 (CP2PS): Positive end of Comparator 2 is connected to ground.

0: disable, P81/CIN2+ as CIN2+

1: enable, P81/CIN2+ as P81

Bit 1 (CP2NRE): Noise Rejection Enable Bit for Comparator 2

0: Disable noise rejection

1: Enable noise rejection (default). But in Low Crystal 2 Oscillator (LXT2) mode, Green mode and Idle mode, the noise rejection circuits are always disabled.

Bit 0 (CP2NRDT): Comparator 2 Noise Rejection Delay Time. In Low XTAL1 oscillator (LXT1) mode the noise rejection high/low pulse is always 4/Fm.

0: Comparator 1 output H/L pulses equal to 4/Fm (0.5 μs at 8 MHz) is regarded as signal.

1: Comparator 1 output H/L pulses equal to 8/Fm (1 μs at 8 MHz) is regarded as signal.

6.1.50 Bank 0 R3D: Unused

6.1.51 Bank 0 R3E ~ R42: Unused

6.1.52 Bank 0 R43: CPIRLCON (Comparator Internal Reference Level Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BG2OUT	C2IRL2	C2IRL1	C2IRL0	BG1OUT	C1IRL2	C1IRL1	C1IRL0

Bit 7 (BG2OUT): when this bit is set to 1, P83 pin will output band gap reference voltage

Bits 6 ~ 4 (C2IRL2 ~ C2IRL0): Comparator 2 internal reference level

Bit 3 (BG1OUT): when this bit set to 1, P73 pin will output band gap reference voltage

Bits 2 ~ 0 (C1IRL2 ~ C1IRL0): Comparator 1 internal reference level

CxIRL2	CxIRL1	CxIRL0	Voltage Level (V)
0	0	0	0.5
0	0	1	0.8
0	1	0	1.0
0	1	1	1.5
1	0	0	2.0
1	0	1	2.2
1	1	0	2.5
1	1	1	3.0

6.1.53 Bank 0 R44 ~ R47: Unused

6.1.54 Bank 0 R48: TC1CR (Timer 1 Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TC1CAP	TC1S	TC1CK1	TC1CK0	TC1M	TC1ES	0	0

Bit 7 (TC1CAP): Software capture control

0: Software capture control disabled

1: Software capture control enabled

Bit 6 (TC1S): Timer/Counter 1 start control

0: Stop and clear counter

1: Start

Bits 5 ~ 4 (TC1CK1 ~ TC1CK0): Timer/Counter 1 clock source select bits

TC1CK1	TC1CK0	Clock Source	Resolution 8 MHz	Max. Time 8 MHz	Resolution 16kHz	Max. Time 16kHz
		Normal	Fc= 8M	Fc=8M	Fc=16K	Fc=16K
0	0	$Fc/2^{12}$	512 µs	131072 µs	256 ms	65536 ms
0	1	$Fc/2^{10}$	128 µs	32768 µs	64 ms	16384 ms
1	0	$Fc/2^{7}$	16 µs	4096 µs	8 ms	2048 ms
1	1	External clock (TC1 pin)	-	-	-	-

Bit 3 (TC1M): Timer/Counter 1 mode select

0: Timer/Counter 1 mode

1: Capture mode

Bit 2 (TC1ES): Timer/Counter 1 signal edge

0: increment if the transition from low to high (rising edge) takes place on the TC1 pin.

1: increment if the transition from high to low (falling edge) takes place on the TC1 pin.

Bits 1 ~ 0: not used, set to 0 all the time.

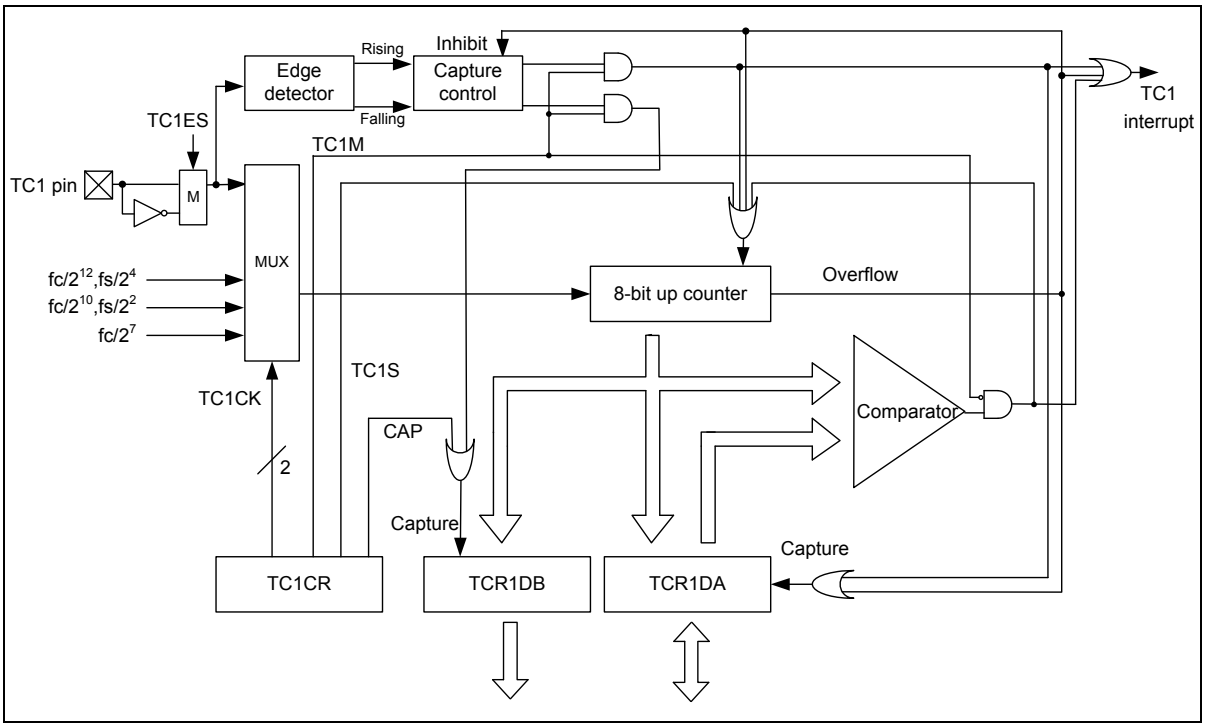


Figure 6-4 Configuration of Timer/Counter 1

In **Timer mode**, counting up is performed using the internal clock. When the contents of the up-counter matched with TCR1DA, then interrupt is generated and the counter is cleared. Counting up resumes after the counter is cleared. The current contents of the up-counter are loaded into TCR1DB by setting TC1CAP to “1” and TC1CAP is automatically cleared to “0” after capture.

In **Counter mode**, counting up is performed using the external clock input pin (TC1 pin) and either rising or falling edge can be selected by TC1ES but **both edges cannot be used**. When the contents of the up-counter matched with TCR1DA, then interrupt is generated and the counter is cleared. Counting up resumes after the counter is cleared. The current contents of the up-counter are loaded into TCR1DB by setting TC1CAP to “1” and TC1CAP is automatically cleared to “0” after capture.

In **Capture mode**, the pulse width, period and duty of the TC1 input pin are measured in this mode, which can be used to decode the remote control signal. The counter is free running by the internal clock. On a rising (falling) edge of TC1 pin input, the contents of the counter is loaded into TCR1DA, then the counter is cleared and interrupt is generated. On a falling (rising) edge of TC1 pin input, the contents of the counter are loaded into TCR1DB. The counter is still counting, on the next rising edge of TC1 pin input, the contents of the counter are loaded into TCR1DA, the counter is cleared and interrupt is generated again. If an overflow occurs before the edge is detected, FFH is loaded into TCR1DA and an overflow interrupt is generated. During interrupt processing, it can be determined whether or not there is an overflow by checking whether or not the TCR1DA value is FFH. After an interrupt (capture to TCR1DA or overflow detection) is generated, capture and overflow detection are halted until TCR1DA is read out.

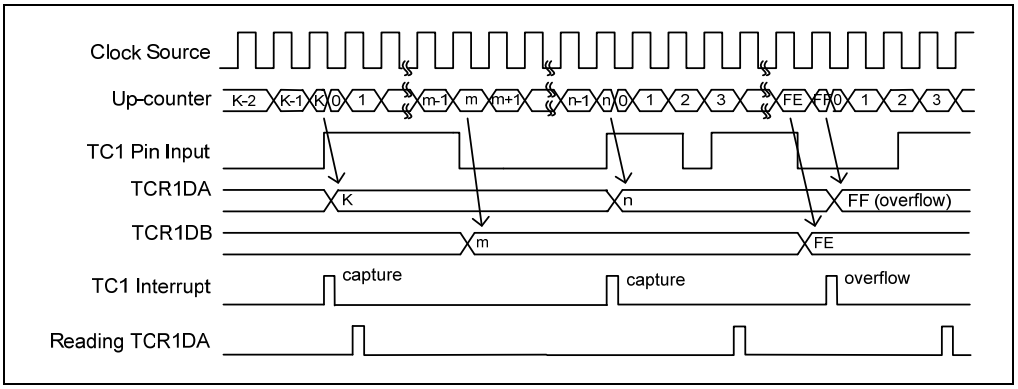


Figure 6-5 Capture Mode Timing Diagram

6.1.55 Bank 0 R49: TCR1DA (Timer 1 Data Buffer A)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TCR1DA7	TCR1DA6	TCR1DA5	TCR1DA4	TCR1DA3	TCR1DA2	TCR1DA1	TCR1DA0

Bits 7 ~ 0 (TCR1DA7 ~ TCR1DA0): Data buffer of 8-bit Timer/Counter 1

6.1.56 Bank 0 R4A: TCR1DB (Timer 1 Data Buffer B)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TCR1DB7	TCR1DB6	TCR1DB5	TCR1DB4	TCR1DB3	TCR1DB2	TCR1DB1	TCR1DB0

Bits 7 ~ 0 (TCR1DB7 ~ TCR1DB0): Data buffer of 8-bit Timer/Counter 1

6.1.57 Bank 0 R4B: TC2CR (Timer 2 Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	TC2ES	TC2M	TC2S	TC2CK2	TC2CK1	TC2CK0

Bits 7 ~ 6: Unused, set to 0 all the time.

Bit 5 (TC2ES): TC2 signal edge

0 : Increment if the transition from low to high (rising edge) takes place on the TC2 pin

1: Increment if the transition from high to low (falling edge) takes place on the TC2 pin

Bit 4 (TC2M): Timer/Counter 2 mode select

0: Timer/Counter 2 mode

1: Window mode

Bit 3 (TC2S): Timer/Counter 2 start control

0: Stop and clear counter

1: start

Bits 2 ~ 0 (TC2CK2 ~ TC2CK0): Timer/Counter 2 clock source select

TC2CK2	TC2CK1	TC1CK0	Clock Source Normal	Resolution 8 MHz F_C=8M	Max. Time 8 MHz F_C=8M	Resolution 16kHz F_C=16K	Max. Time 16kHz F_C=16K
0	0	0	$F_C/2^{23}$	1.05s	19.1hr	145hr	9544hr
0	0	1	$F_C/2^{13}$	1.024ms	67.11s	512ms	33554.432 s
0	1	0	$F_C/2^8$	32μs	2.097s	16ms	1048.576s
0	1	1	$F_C/2^3$	1μs	65.536ms	0.5ms	32768ms
1	0	0	F_C	125ns	8.192ms	0.0625ms	4096ms
1	0	1	-	-	-	-	-
1	1	0	-	-	-	-	-
1	1	1	External clock (TC2 pin)	-	-	-	-

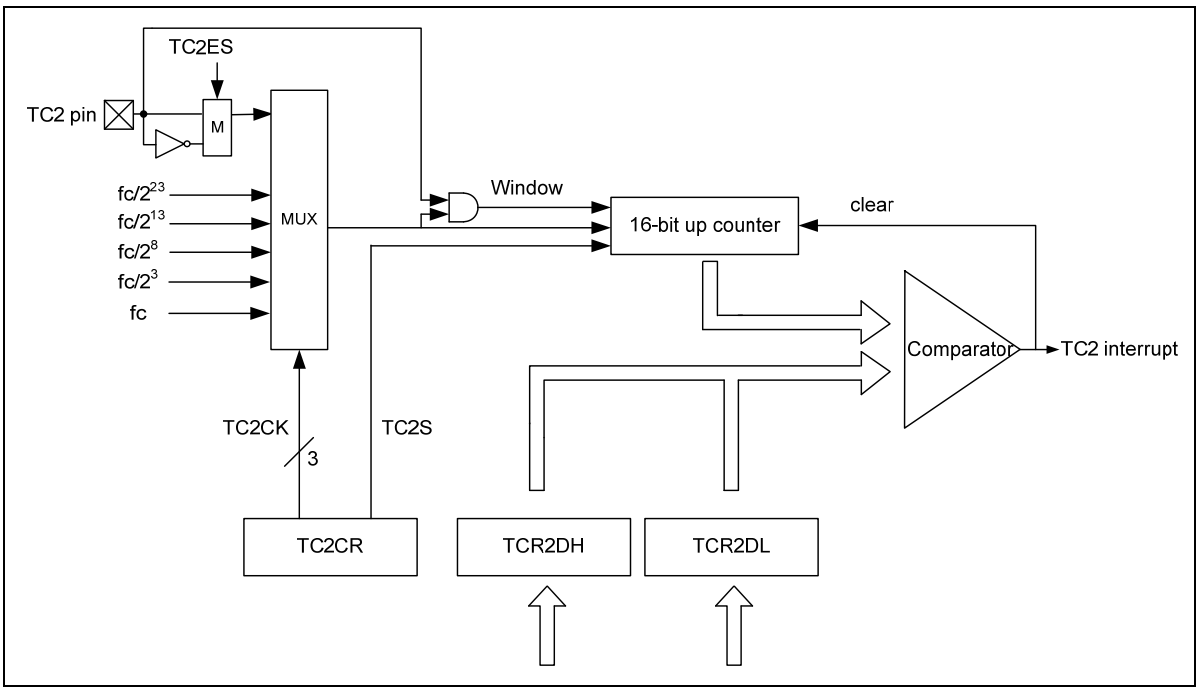


Figure 6-6 Configuration of Timer/Counter 2

In **Timer mode**, counting up is performed using the internal clock. When the contents of the up-counter matched with the TCR2 (TCR2H+TCR2L), then interrupt is generated and the counter is cleared. Counting up resumes after the counter is cleared.

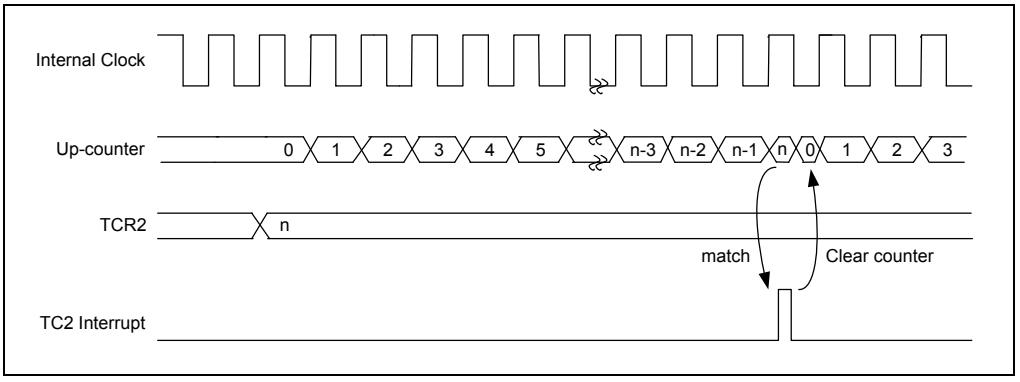


Figure 6-7 Timer Mode Timing Diagram

In **Counter mode**, counting up is performed using an external clock input pin (TC2 pin) and either rising or falling can be selected by setting TC2ES. When the contents of the up-counter matched with the TCR2 (TCR2H+TCR2L), then interrupt is generated and the counter is cleared. Counting up resumes after the counter is cleared.

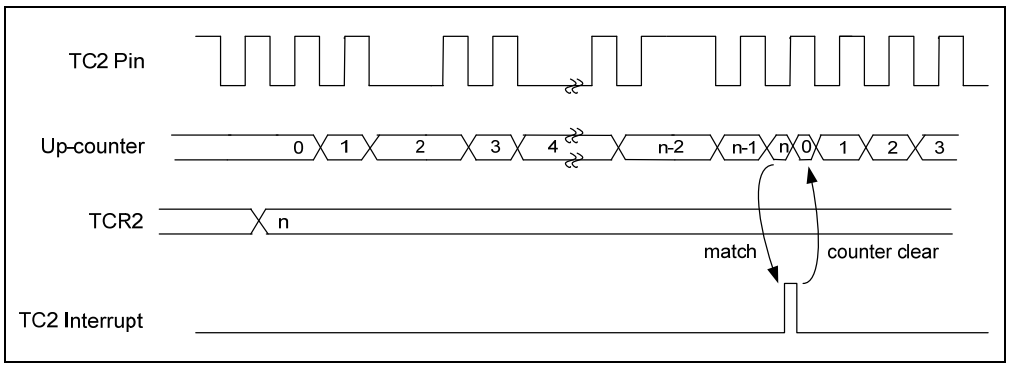


Figure 6-8 Counter Mode Timing Diagram (INT2ES = 1)

In **Window mode**, counting up is performed on a rising edge of the pulse that is logical AND of an internal clock and the TC2 pin (window pulse). When the contents of the up-counter matched with the TCR2 (TCR2H+TCR2L), then interrupt is generated and the counter is cleared. **The frequency (window pulse) must be slower than the selected internal clock.**

Writing to the TCR2L, comparison is inhibited until TCR2H is written.

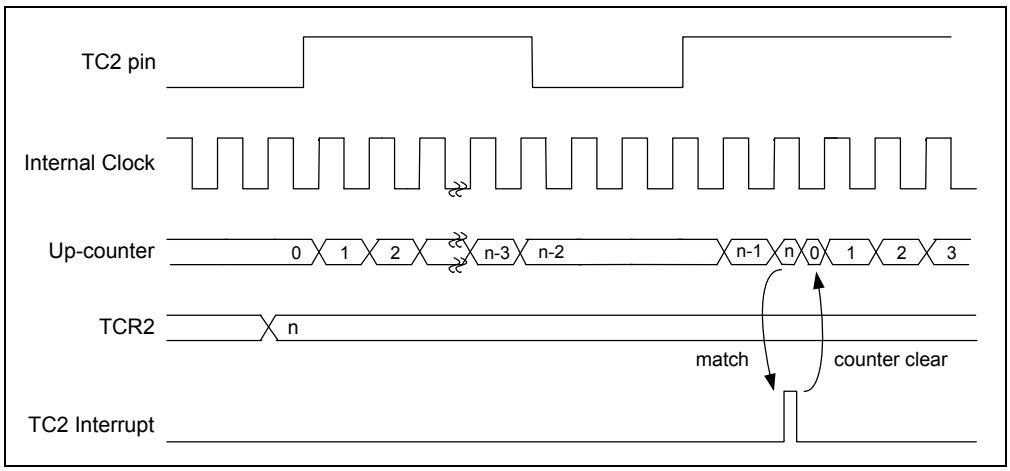


Figure 6-9 Window Mode Timing Diagram

6.1.58 Bank 0 R4C: TCR2DH (Timer 2 High Byte Data Buffer Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TCR2D15	TCR2D14	TCR2D13	TCR2D12	TCR2D11	TCR2D10	TCR2D9	TCR2D8

Bits 7 ~ 0 (TCR2D15 ~ TCR2D8): High byte data buffer of 16-bit Timer/Counter 2

6.1.59 Bank 0 R4D: TCR2DL (Timer 2 Low Byte Data Buffer Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TCR2D7	TCR2D6	TCR2D5	TCR2D4	TCR2D3	TCR2D2	TCR2D1	TCR2D0

Bits 7 ~ 0 (TCR2D7 ~ TCR2D0): Low byte data buffer of 16-bit Timer/Counter 2

6.1.60 Bank 0 R4E: TC3CR (Timer 3 Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TC3FF1	TC3FF0	TC3S	TC3CK2	TC3CK1	TC3CK0	TC3M1	TC3M0

Bits 7 ~ 6 (TC3FF1 ~ TC3FF0): Timer/Counter 3 flip-flop control

TC3FF1	TC3FF0	Operating Mode
0	0	Clear
0	1	Toggle
1	0	Set
1	1	Reserved

Bit 5 (TC3S): Timer/Counter 3 start control

0: Stop and clear counter

1: Start

Bits 4 ~ 2 (TC3CK2 ~ TC3CK0): Timer/Counter 3 clock source select

TC3CK2	TC3CK1	TC3CK0	Clock Source Normal	Resolution 8 MHz F_C=8M	Max Time 8 MHz F_C=8M	Resolution 16kHz F_C=16K	Max Time 16kHz F_C=16K
0	0	0	$F_C/2^{11}$	256μs	65536μs	128ms	32768ms
0	0	1	$F_C/2^7$	16μs	4096μs	8ms	2048ms
0	1	0	$F_C/2^5$	4μs	1024μs	2ms	512ms
0	1	1	$F_C/2^3$	1μs	256μs	500μs	128ms
1	0	0	$F_C/2^2$	500ns	128μs	250μs	64ms
1	0	1	$F_C/2$	250ns	64μs	125μs	32ms
1	1	0	F_C	125ns	32μs	62.5μs	16ms
1	1	1	External clock (TC3 pin)	-	-	-	-

Bits 1 ~ 0 (TC3M1 ~ TC3M0): Timer/Counter 3 operation mode select.

TC3M1	TC3M0	Operating mode
0	0	Timer/Counter
0	1	Reserved
1	0	Programmable Divider output
1	1	Pulse Width Modulation output

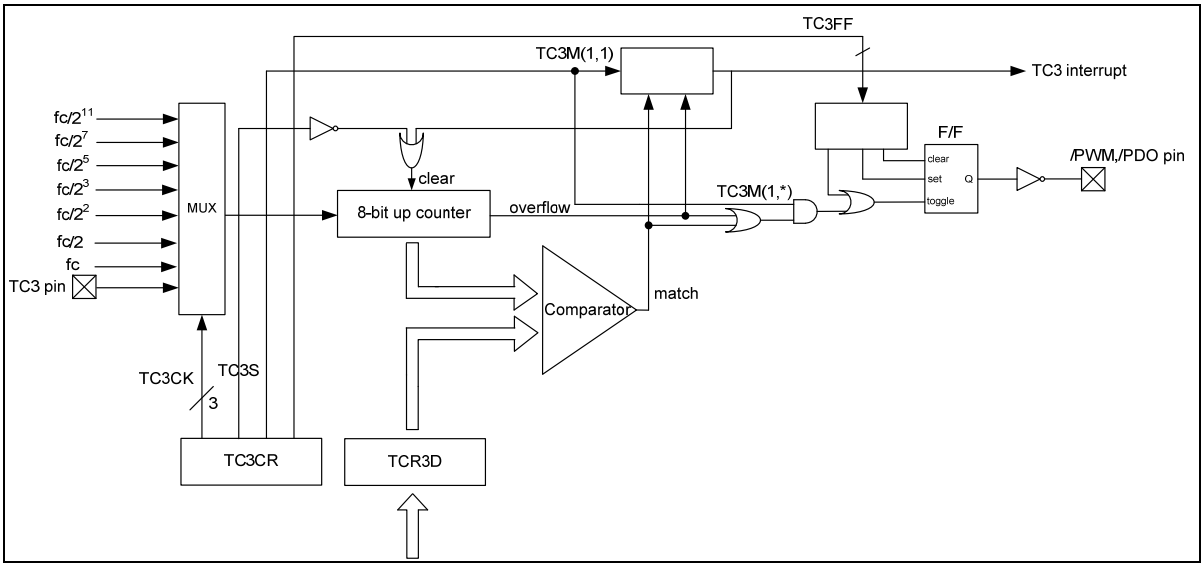


Figure 6-10 Timer/Counter 3 Configuration

In **Timer mode**, counting up is performed using the internal clock (rising edge trigger). When the contents of the up-counter matched with the contents of TCR3D, then interrupt is generated and the counter is cleared. Counting up resumes after the counter is cleared.

In **Counter mode**, counting up is performed using the external clock input pin (TC3 pin). When the contents of up-counter matched with the contents of TCR3D, then interrupt is generated and the counter is cleared. Counting up resumes after the counter is cleared.

In **Programmable Divider Output** (PDO) mode, counting up is performed using the internal clock. The contents of TCR3D are compared with the contents of the up-counter. The F/F output is toggled and the counter is cleared each time a match is found. The F/F output is inverted and output to /PDO pin. This mode can generate 50% duty pulse output. **The F/F can be initialized by program and it is initialized to "0" during reset**. A TC3 interrupt is generated each time the /PDO output is toggled.

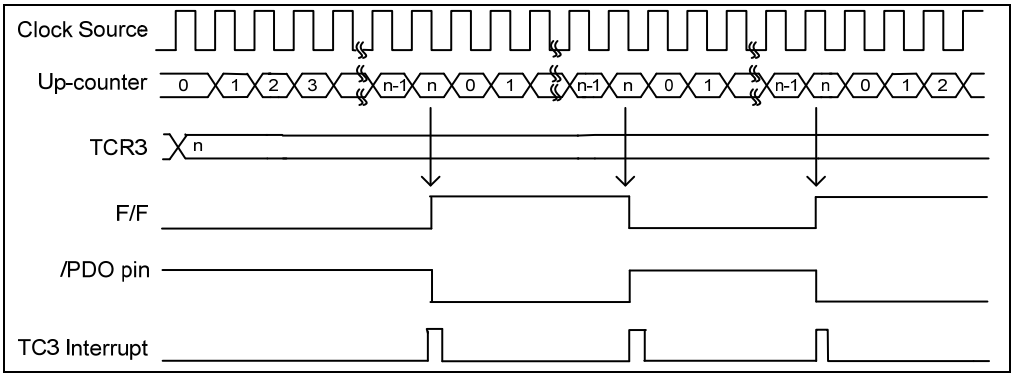


Figure 6-11 Timing Diagram for PDO Mode

In **Pulse Width Modulation** (PWM) Output mode, counting up is performed using the internal clock. The contents of TCR3 are compared with the contents of the up-counter. The F/F is toggled when match is found. The counter is still counting, F/F is toggled again when the counter overflows, and the counter is cleared. The F/F output is inverted and output to /PWM pin. A TC3 interrupt is generated each time an overflow occurs. **TCR3 is configured as a 2-stage shift register and, during output, will not switch until one output cycle is completed even if TCR3 is overwritten.** Therefore, the output can be changed continuously. Also, the first time, TRC3 is shifted by setting TC3S to "1" after data is loaded to TCR3.

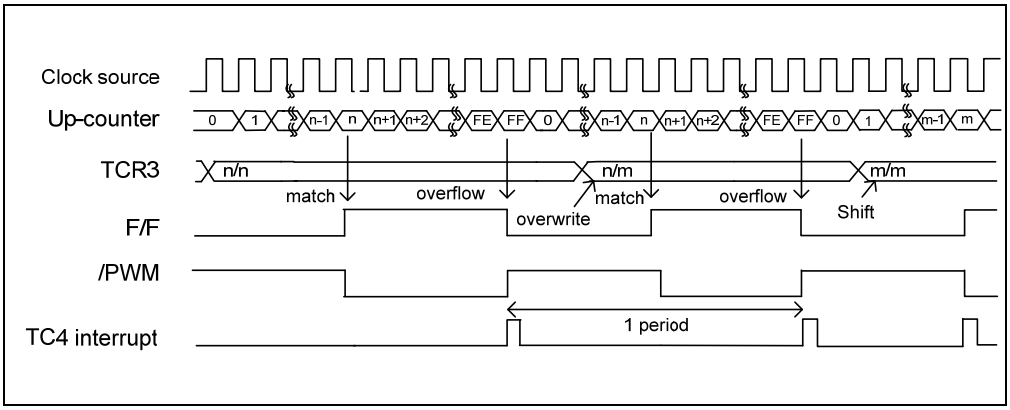


Figure 6-12 Timing Diagram for PWM Mode

6.1.61 Bank 0 R4F: TCR3D (Timer 3 Duty Buffer Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TCR3D7	TCR3D6	TCR3D5	TCR3D4	TCR3D3	TCR3D2	TCR3D1	TCR3D0

Bits 7 ~ 0 (TCR3DB7 ~ TCR3D0): Data buffer of 8 bit Timer/Counter 3

6.1.62 Bank 1 R5: P5PHCR (Port 5 Pull-high Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/PH57	/PH56	/PH55	/PH54	/PH53	/PH52	/PH51	/PH50

Bit 7 (/PH57): Control bit used to enable pull-high of the P57 pin

0: enable internal pull-high

1: disable internal pull-high

Bit 6 (/PH56): Control bit used to enable pull-high of the P56 pin.

Bit 5 (/PH55): Control bit used to enable pull-high of the P55 pin.

Bit 4 (/PH54): Control bit used to enable pull-high of the P54 pin.

Bit 3 (/PH53): Control bit used to enable pull-high of the P53 pin.

Bit 2 (/PH52): Control bit used to enable pull-high of the P52 pin.

Bit 1 (/PH51): Control bit used to enable pull-high of the P51 pin.

Bit 0 (/PH50): Control bit used to enable pull-high of the P50 pin.

6.1.63 Bank 1 R6: P6PHCR (Port 6 Pull-high Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/PH67	/PH66	/PH65	/PH64	/PH63	/PH62	/PH61	/PH60

Bit 7 (/PH67): Control bit used to enable pull-high of the P67 pin.

Bit 6 (/PH66): Control bit used to enable pull-high of the P66 pin.

Bit 5 (/PH65): Control bit used to enable pull-high of the P65 pin.

Bit 4 (/PH64): Control bit used to enable pull-high of the P64 pin.

Bit 3 (/PH63): Control bit used to enable pull-high of the P63 pin.

Bit 2 (/PH62): Control bit used to enable pull-high of the P62 pin.

Bit 1 (/PH61): Control bit used to enable pull-high of the P61 pin.

Bit 0 (/PH60): Control bit used to enable pull-high of the P60 pin

6.1.64 Bank 1 R7: P7PHCR (Port 7 Pull-high Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/PH77	/PH76	/PH75	/PH74	/PH73	/PH72	/PH71	/PH70

Bit 7 (/PH77): Control bit used to enable pull-high of the P77 pin.

Bit 6 (/PH76): Control bit used to enable pull-high of the P76 pin.

Bit 5 (/PH75): Control bit used to enable pull-high of the P75 pin.

Bit 4 (/PH74): Control bit used to enable pull-high of the P74 pin.

Bit 3 (/PH73): Control bit used to enable pull-high of the P73 pin.

Bit 2 (/PH72): Control bit used to enable pull-high of the P72 pin.

Bit 1 (/PH71): Control bit used to enable pull-high of the P71 pin.

Bit 0 (/PH70): Control bit used to enable pull-high of the P70 pin.

6.1.65 Bank 1 R8: P8PHCR (Port 8 Pull-high Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/PH87	/PH86	/PH85	/PH84	/PH83	/PH82	/PH81	/PH80

Bit 7(/PH87): Control bit used to enable pull-high of the P87 pin.

Bit 6(/PH86): Control bit used to enable pull-high of the P86 pin.

Bit 5(/PH85): Control bit used to enable pull-high of the P85 pin.

Bit 4(/PH84): Control bit used to enable pull-high of the P84 pin.

Bit 3(/PH83): Control bit used to enable pull-high of the P83 pin.

Bit 2(/PH82): Control bit used to enable pull-high of the P82 pin.

Bit 1(/PH81): Control bit used to enable pull-high of the P81 pin.

Bit 0(/PH80): Control bit used to enable pull-high of the P80 pin.

6.1.66 Bank 1 R9: P9PHCR (Port 9 Pull-high Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/PH97	/PH96	/PH95	/PH94	/PH93	/PH92	/PH91	/PH90

Bit 7 (/PH97): Control bit used to enable pull-high of the P97 pin.

Bit 6 (/PH96): Control bit used to enable pull-high of the P96 pin.

Bit 5 (/PH95): Control bit used to enable pull-high of the P95 pin.

Bit 4 (/PH94): Control bit used to enable pull-high of the P94 pin.

Bit 3 (/PH93): Control bit used to enable pull-high of the P93 pin.

Bit 2 (/PH92): Control bit used to enable pull-high of the P92 pin.

Bit 1 (/PH91): Control bit used to enable pull-high of the P91 pin.

Bit 0 (/PH90): Control bit used to enable pull-high of the P90 pin.

6.1.67 Bank 1 RA (Unused)

6.1.68 Bank 1 RB: P5PLCR (Port 5 Pull Low Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/PL57	/PL56	/PL55	/PL54	/PL53	/PL52	/PL51	/PL50

Bit 7(/PL57): Control bit used to enable pull low of the P57 pin.

0: enable internal pull-low

1: disable internal pull-low

Bit 6 (/PL56): Control bit used to enable pull low of the P56 pin.

Bit 5 (/PL55): Control bit used to enable pull low of the P55 pin.

Bit 4 (/PL54): Control bit used to enable pull low of the P54 pin.

Bit 3 (/PL53): Control bit used to enable pull low of the P53 pin.

Bit 2 (/PL52): Control bit used to enable pull low of the P52 pin.

Bit 1 (/PL51): Control bit used to enable pull low of the P51 pin.

Bit 0 (/PL50): Control bit used to enable pull low of the P50 pin.

6.1.69 Bank1 RC: P6PLCR (Port 6 Pull Low Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/PL67	/PL66	/PL65	/PL64	/PL63	/PL62	/PL61	/PL60

Bit 7 (/PL67): Control bit used to enable pull low of the P67 pin.

Bit 6 (/PL66): Control bit used to enable pull low of the P66 pin.

Bit 5 (/PL65): Control bit used to enable pull low of the P65 pin.

Bit 4 (/PL64): Control bit used to enable pull low of the P64 pin.

Bit 3 (/PL63): Control bit used to enable pull low of the P63 pin.

Bit 2 (/PL62): Control bit used to enable pull low of the P62 pin.

Bit 1 (/PL61): Control bit used to enable pull low of the P61 pin.

Bit 0 (/PL60): Control bit used to enable pull low of the P60 pin.

6.1.70 Bank 1 RD: P7PLCR (Port 7 Pull Low Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/PL77	/PL76	/PL75	/PL74	/PL73	/PL72	/PL71	/PL70

Bit 7 (/PL77): Control bit used to enable pull low of the P77 pin.

Bit 6 (/PL76): Control bit used to enable pull low of the P76 pin.

Bit 5 (/PL75): Control bit used to enable pull low of the P75 pin.

Bit 4 (/PL74): Control bit used to enable pull low of the P74 pin.

Bit 3 (/PL73): Control bit used to enable pull low of the P73 pin.

Bit 2 (/PL72): Control bit used to enable pull low of the P72 pin.

Bit 1 (/PL71): Control bit used to enable pull low of the P71 pin.

Bit 0 (/PL70): Control bit used to enable pull low of the P70 pin.

6.1.71 Bank 1 RE: P8PLCR (Port 8 Pull Low Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/PL87	/PL86	/PL85	/PL84	/PL83	/PL82	/PL81	/PL80

Bit 7(/PL87): Control bit used to enable pull low of the P87 pin.

Bit 6(/PL86): Control bit used to enable pull low of the P86 pin.

Bit 5(/PL85): Control bit used to enable pull low of the P85 pin.

Bit 4(/PL84): Control bit used to enable pull low of the P84 pin.

Bit 3(/PL83): Control bit used to enable pull low of the P83 pin.

Bit 2(/PL82): Control bit used to enable pull low of the P82 pin.

Bit 1(/PL81): Control bit used to enable the pull low of P81 pin.

Bit 0(/PL80): Control bit used to enable the pull low of P80 pin.

6.1.72 Bank 1 RF: P9PLCR (Port 9 Pull Low Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/PL97	/PL96	/PL95	/PL94	/PL93	/PL92	/PL91	/PL90

Bit 7 (/PL97): Control bit used to enable pull low of the P97 pin.

Bit 6 (/PL96): Control bit used to enable pull low of the P96 pin.

Bit 5 (/PL95): Control bit used to enable pull low of the P95 pin.

Bit 4 (/PL94): Control bit used to enable pull low of the P94 pin.

Bit 3 (/PL93): Control bit used to enable pull low of the P93 pin.

Bit 2 (/PL92): Control bit used to enable pull low of the P92 pin.

Bit 1 (/PL91): Control bit used to enable pull low of the P91 pin.

Bit 0 (/PL90): Control bit used to enable pull low of the P90 pin.

6.1.73 Bank 1 R10 (Unused)

6.1.74 Bank 1 R11: P5HD/SCR (Port 5 High Drive/Sink Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/H57	/H56	/H55	/H54	/H53	/H52	/H51	/H50

Bits 7 ~ 0 (H57 ~ H50): P57~P50 high drive/sink current control bits

0: enable high drive/sink

1: disable high drive/sink

6.1.75 Bank 1 R12: P6HD/SCR (Port 6 High Drive/Sink Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/H67	/H66	/H65	/H64	/H63	/H62	/H61	/H60

Bits 7 ~ 0 (H67 ~ H60): P67~P60 high drive/sink current control bits

0: enable high drive/sink

1: disable high drive/sink

6.1.76 Bank 1 R13: P7HD/SCR (Port 7 High Drive/Sink Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/H77	/H76	/H75	/H74	/H73	/H72	/H71	/H70

Bits 7 ~ 0 (H77 ~ H70): P77 ~ P70 high drive/sink current control bits

0: enable high drive/sink

1: disable high drive/sink

6.1.77 Bank 1 R14: P8HD/SCR (Port 8 High Drive/Sink Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/H87	/H86	/H85	/H84	/H83	/H82	/H81	/H80

Bits 7 ~ 0 (H87 ~ H80): P87~P80 high drive/sink current control bits

0: enable high drive/sink

1: disable high drive/sink

6.1.78 Bank 1 R15: P9HD/SCR (Port 9 High Drive/Sink Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/H97	/H96	/H95	/H94	/H93	/H92	/H91	/H90

Bits 7 ~ 0 (H97 ~ H90): P97~P90 high drive/sink current control bits

0: enable high drive/sink

1: disable high drive/sink

6.1.79 Bank 1 R16 (Unused)

6.1.80 Bank 1 R17: P5ODCR (Port 5 Open Drain Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OD57	OD56	OD55	OD54	OD53	OD52	OD51	OD50

Bits 7 ~ 0 (OD57 ~ OD50): Open-Drain control bits

0: disable open-drain function

1: enable open-drain function

6.1.81 Bank 1 R18: P6ODCR (Port 6 Open Drain Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OD67	OD66	OD65	OD64	OD63	OD62	OD61	OD60

Bits 7 ~ 0 (OD67 ~ OD60): Open-Drain control bits

0: disable open-drain function

1: enable open-drain function

6.1.82 Bank1 R19: P7ODCR (Port 7 Open Drain Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OD77	OD76	OD75	OD74	OD73	OD72	OD71	OD70

Bits 7 ~ 0 (OD77 ~ OD70): Open-Drain control bits

0: disable open-drain function

1: enable open-drain function

6.1.83 Bank 1 R1A: P8ODCR (Port 8 Open Drain Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OD87	OD86	OD85	OD84	OD83	OD82	OD81	OD80

Bits 7 ~ 0 (OD87 ~ OD80): Open-Drain control bits

0: disable open-drain function

1: enable open-drain function

6.1.84 Bank 1 R1B: P9ODCR (Port 9 Open Drain Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OD97	OD96	OD95	OD94	OD93	OD92	OD91	OD90

Bits 7 ~ 0 (OD97 ~ OD90): Open-Drain control bits

0: disable open-drain function

1: enable open-drain function

6.1.85 Bank 1 R1C (Unused)

6.1.86 Bank 1 R1D: IRCS (IRC Frequency Selection Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	RCM1	RCM0	0	0	0	0

Bits 7 ~ 6: Unused, set to 0 all the time.

Bits 5 ~ 4 (RCM1 ~ RCM0): IRC Mode Frequency Selection Bits

RCM 1	RCM 0	Frequency (MHz)
0	0	4
0	1	16
1	0	8
1	1	455kHz

Word 1 COBS0=0 :

R1D<5, 4> of the initialized values will be kept the same as Word 1<6, 5>.

R1D<5, 4> cannot be changed.

Word 1 COBS0=1 :

R1D<5, 4> of the initialized values will be kept the same as Word1<6, 5>.

R1D<5, 4> can be changed, when user wants to work on the other IRC frequency.

ex. 4M → 16M

Bits 3 ~ 0: Unused, set to 0 all the time.

6.1.87 Bank 1 R1E (Unused)

6.1.88 Bank 1 R1F: EEPROM Control

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RD	WR	EEWE	EEDF	EEPC	0	0	0

Bit 7 (RD): Read control bit

0: do not execute EEPROM read

1: read EEPROM content (RD can be set by software. When read instruction is completed, RD will be cleared by hardware).

Bit 6 (WR): Write control bit

0: write cycle to the EEPROM is completed.

1: initiate a write cycle (WR can be set by software. When write cycle is completed, WR will be cleared by hardware).

Bit 5 (EEWE): EEPROM write enable bit

0: Prohibit write to the EEPROM

1: allow EEPROM write cycles

Bit 4 (EEDF): EEPROM detective flag

0: write cycle is completed

1: write cycle is unfinished

Bit 3 (EEPC): EEPROM power down control bit

0: switch of EEPROM

1: EEPROM is operating

Bits 2 ~ 1: unused bits, set to 0 all the time

Bit 0: unused

6.1.89 Bank 1 R20: EEPROM ADDR

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EERA7	EERA6	EERA5	EERA4	EERA3	EERA2	EERA1	EERA0

Bits 7 ~ 0 (EERA7 ~ EERA0): EEPROM address register

6.1.90 Bank 1 R21: EEPROM Data

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EERD7	EERD6	EERD5	EERD4	EERD3	EERD2	EERD1	EERD0

Bits 7 ~ 0 (EERD7 ~ EERD0): EEPROM data register. Read only.

6.1.91 Bank 1 R22 (Unused)

6.1.92 Bank 1 R23: I^2CCR1 (I^2C Status and Control Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Strobe/Pend	IMS	ISS	STOP	SAR_EMPTY	ACK	FULL	EMPTY

Bit 7 (Strobe/Pend): In master mode, it is used as strobe signal to control the I^2C circuit to send SCL clock. Reset automatically after receiving or transmitting handshake signal (ACK or NACK). In slave mode, it is used as pending signal, user should clear it after filling data into the Tx buffer or getting data from Rx buffer to inform slave I^2C circuit to release SCL signal.

Bit 6 (IMS): I^2C Master/Slave mode select bit.

0: Slave

1: Master

Bit 5 (ISS): I^2C Fast/Standard mode select bit. (If Fm is 4 MHz and I2CTS1~0<0, 0>)

0: Standard mode (100Kbit/s)

1: Fast mode (400Kbit/s)

Bit 4 (STOP): In Master mode, if STOP=1 and R/nW=1 then the EM78F568N / EM78F668N must return a nACK signal to a slave device before sending a STOP signal. If STOP=1 and R/nW=0, then the EM78F568N / EM78F668N sends a STOP signal after receiving an ACK signal. Reset when the EM78F568N/EM78F668N sends a STOP signal to the Slave device. In slave mode, if STOP=1 and R/nW=0 then the EM78F568N/EM78F668N must return a nACK signal to the master device.

Bit 3 (SAR_EMPTY): Set when the EM78F568N/EM78F668N transmits a 1-byte data from the I^2C Slave Address Register and receives an ACK (or nACK) signal. Reset when the MCU writes a 1-byte data to the I^2C Slave Address Register.

Bit 2 (ACK): The ACK condition bit is set to 1 by the hardware when the device responds acknowledge (ACK). Reset when the device responds with a not-acknowledge (nACK) signal.

Bit 1 (FULL): Set by the hardware when I^2C receives “buffer register is full”. Reset by the hardware when the MCU reads data from the I^2C receive buffer register.

Bit 0 (EMPTY): Set by the hardware when I^2C transmits a “buffer register is empty” and receives an ACK (or nACK) signal. This is reset by the hardware when the MCU writes new data to the I^2C transmit buffer register.

6.1.93 Bank 1 R24: I2CCR2 (I2C Status and Control Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
I2CBF	GCEN	0	0	I2CTS1	I2CTS0	0	I2CEN

Bit 7 (I2CBF): I^2C Busy Flag Bit

0: clear to "0", in Slave mode, if the device receives a STOP signal or the I^2C slave address does not match.

1: set when I^2C communicates with master device in slave mode.

Bit 6 (GCEN): I^2C General Call Function Enable Bit

0: Disable General Call Function

1: Enable General Call Function

Bits 5 ~ 4: Not used, set to 0 all the time.

Bits 3 ~ 2 (I2CTS1 ~ I2CTS0): I^2C Transmit Clock Source Select Bits (When I2CCS=0). When operating different Fm, these bits must be set with the correct value to let the SCL clock match with standard/fast mode.

I2CCR1 Bit 5=1, fast mode

I2CTS1	I2CTS0	SCL CLK	Operating Fm (MHz)
0	0	Fm/10	4
0	1	Fm/20	8
1	0	Fm/30	12
1	1	Fm/40	16

I2CCR1 Bit 5=0, standard mode

I2CTS1	I2CTS0	SCL CLK	Operating Fm (MHz)
0	0	Fm/40	4
0	1	Fm/80	8
1	0	Fm/120	12
1	1	Fm/160	16

Bit 1: Not used bit, set to 0 all the time.

Bit 0 (I2CEN): I^2C Enable Bit

0: Disable I^2C mode

1: Enable I^2C mode

6.1.94 Bank 1 R25: I2CSA (I2C Slave Address Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SA6	SA5	SA4	SA3	SA2	SA1	SA0	IRW

Bits 7 ~ 1 (SA6 ~ SA0): The EM78F568N/EM78F668N is used as a master device for I^2C application. This is the slave device address register.

Bit 0 (IRW): The EM78F568N/EM78F668N is used as a master device for I^2C application. This bit is Read/Write transaction control bit.

0: Write

1: Read

6.1.95 Bank 1 R26: I2CDA (I2C Device Address Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0

Bits 7 ~ 0 (DA7 ~ DA0): The EM78F568N/EM78F668N is used as a slave device for I^2C application. This register stores the address of EM78F568N/EM78F668N. It is used to identify the data on the I^2C bus to extract the message delivered to the EM78F568N/EM78F668N.

6.1.96 Bank 1 R27: I2CDB (I2C Data Buffer Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

Bits 7 ~ 0 (DB7~DB0): I^2C Receive/Transmit Data Buffer.

6.1.97 Bank 1 R28: I2CA (I2C Data Buffer Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	0	DA9	DA8

Bits 7 ~ 2: unused

Bits 1 ~ 0 (DA9 ~ DA8): high bits of device address.

6.1.98 Bank 1 R29 (Unused)

6.1.99 Bank 1 R2A: PWMER (PWM Enable Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	0	PWMBE	PWMAE

Bits 7 ~ 2: Unused, set to 0 all the time.

Bit 1 (PWMBE): PWM B Enable bit

0: PWM B is off (default value), and its related pin carries out the I/O pin function.

1: PWM B is on, and its related pin is automatically set to output.

Bit 0 (PWMAE): PWM A Enable bit

0: PWM A is off (default value), and its related pin carries out the I/O pin function

1: PWM A is on, and its related pin is automatically set to output

6.1.100 Bank 1 R2B: TIMEN (Timer/PWM Enable Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	0	TBEN	TAEN

Bits 7 ~ 2: Unused, set to 0 all the time.

Bit 1 (TBEN): Timer B enable bit

0: Timer B is off (Default)

1: Timer B is on

Bit 0 (TAEN): Timer A enable bit

0: Timer A is off (Default)

1: Timer A is on

6.1.101 Bank 1 R2C~R2E: Unused

6.1.102 Bank 1 R2F: PWMACR (PWM A Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	TRCBA	0	0	0

Bits 7 ~ 4: Unused, set 0 all the time

Bit 3 (TRCBA): Timer A Read Control Bit

0: When this bit is set to 0, the values of PRDA[9]~PRDA[0] in PRDAL and PRDxH are PWMA period data.

1: When this bit set to 1, Read values from PRDA[9]~PRDA[0] in PRDAL and PRDxH are PWMA timer data.

Bits 2 ~ 0: unused bits, set 0 all the time

6.1.103 Bank 1 R30: PWMBCR (PWM B Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	TRCBB	0	0	0

Bits 7 ~ 4: unused bits, set 0 all the time

Bit 3 (TRCBB): Timer B Read Control Bit

0: When this bit is set to 0, the values of PRDB[9]~PRDB[0] in PRDBL and PRDxH are PWMB period data

1: When this bit set to 1, the values of PRDB[9]~PRDB[0] in PRDBL and PRDxH are PWMB timer data

Bits 2 ~ 0: Unused, set 0 all the time

6.1.104 Bank 1 R31: Unused

6.1.105 Bank 1 R32: TACR (Timer A Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	TAP2	TAP1	TAP0

Bits 7 ~ 3: Unused, set 0 all the time.

TAP2	TAP1	T1AP0	Prescaler
0	0	0	1:2 (Default)
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1 : 64
1	1	0	1 : 128
1	1	1	1 : 256

6.1.106 Bank 1 R33: TBCR (Timer B Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	TBP2	TBP1	TBP0

Bits 7 ~ 3: Unused, set 0 all the time.

Bits 2 ~ 0 (TBP2 ~ TBP0): Timer B Prescaler Bits

TBP2	TBP1	TBP0	Prescaler
0	0	0	1:2 (Default)
0	0	1	1 : 4
0	1	0	1 : 8
0	1	1	1 : 16
1	0	0	1 : 32
1	0	1	1 : 64
1	1	0	1 : 128
1	1	1	1 : 256

6.1.107 Bank 1 R34: Unused

6.1.108 Bank 1 R35: TAPRDH (Timer A Period Buffer Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PRDA[9]	PRDA[8]	PRDB[7]	PRDB[6]	PRDB[5]	PRDB[4]	PRDB[3]	PRDB[2]

Bits 7 ~ 0 (PRDA[9] ~ PRDA[2]): The contents of this register is a period of Timer A.

6.1.109 Bank 1 R36: TBPRDH (Timer B Period Buffer Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PRDB[9]	PRDB[8]	PRDB[7]	PRDB[6]	PRDB[5]	PRDB[4]	PRDB[3]	PRDB[2]

Bits 7 ~ 0 (PRDB[9] ~ PRDB[2]): The contents of this register is a period of Timer B.

6.1.110 Bank 1 R37: Unused

6.1.111 Bank 1 R38: TADTH (Timer A Duty Buffer Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DTA[9]	DTA[8]	DTA[7]	DTA[6]	DTA[5]	DTA[4]	DTA[3]	DTA[2]

Bits 7 ~ 0 (DTA[9]~ DTA[2]): The contents of this register is a duty of Timer A.

6.1.112 Bank 1 R39: TBDTH (Timer B Duty Buffer Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DTB[9]	DTB[8]	DTB[7]	DTB[6]	DTB[5]	DTB[4]	DTB[3]	DTB[2]

Bits 7 ~ 0 (DTB[7]~DTB[0]): The contents of this register is a duty of Timer B.

6.1.113 Bank 1 R3A: Unused

6.1.114 Bank 1 R3B: PRDxL (PWM A/B/C Period Buffer Low Bits Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	PRDB[1]	PRDB[0]	PRDA[1]	PRDA[0]

Bits 7 ~ 4: Unused, set to 0 all the time.

Bits 3 ~ 2 (PRDB[1] ~ PRDB[0]): PWM B period buffer low bits

Bits 1 ~ 0 (PRDA[1] ~ PRDA[0]): PWM A period buffer low bits

6.1.115 Bank 1 R3C: DTxL (PWM1/2 Duty Buffer Low Bits Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	DTB[1]	DTB[0]	DTA[1]	DTA[0]

Bits 7 ~ 4: Unused, set to 0 all the time.

Bits 3 ~ 2 (DTB[1]~DTB[0]): PWM B duty buffer high bits

Bits 1 ~ 0 (DTA[1]~DTA[0]): PWM A duty buffer high bits

6.1.116 Bank 1 R3D~R4F (Unused)

6.1.117 Bank 0 R50~R7F, Banks 0~1 R80~RFF

All of these are 8-bit general-purpose registers.

6.2 TCC/WDT and Prescaler

There are two 8-bit counters available as prescalers for the TCC and WDT respectively. The PST0~PST2 bits of the TCCCR register (Bank 0 R13) are used to determine the ratio of the TCC prescaler. Likewise, the PSW0~PSW2 bits of the WDTCR register (Bank 0 R11) are used to determine the WDT prescaler. The prescaler counter will be cleared by the instructions each time they are written into TCC. The WDT and prescaler will be cleared by the "WDTC" and "SLEP" instructions. Figure 6-13 depicts the circuit diagram of TCC/WDT.

Bank 0 R14 (TCCDATA) is an 8-bit timer/counter. The TCC clock source can be an internal clock or an external signal input (edge selectable from the TCC pin). If TCC signal source is from an internal clock, TCC will be incremented by 1 at every instruction cycle (without prescaler). As illustrated in Figure 6-13, if the TCC signal source is from an external clock input, TCC will be incremented by 1 at every falling edge or rising edge of the TCC pin. The TCC pin input time length (keep in high or low level) must be greater than 1CLK. **The TCC will stop running when sleep mode occurs.**

The watchdog timer is a free running on-chip RC oscillator. The WDT will keep on running even after the oscillator driver has been turned off (i.e. in sleep mode). During normal operation or sleep mode, a WDT time-out (if enabled) will cause the device to reset. The WDT can be enabled or disabled at any time during normal mode by software programming. Refer to the WDTE bit of the IOCE0 register. With no prescaler, the WDT time-out period is approximately 18 ms[1] (one oscillator start-up timer period).

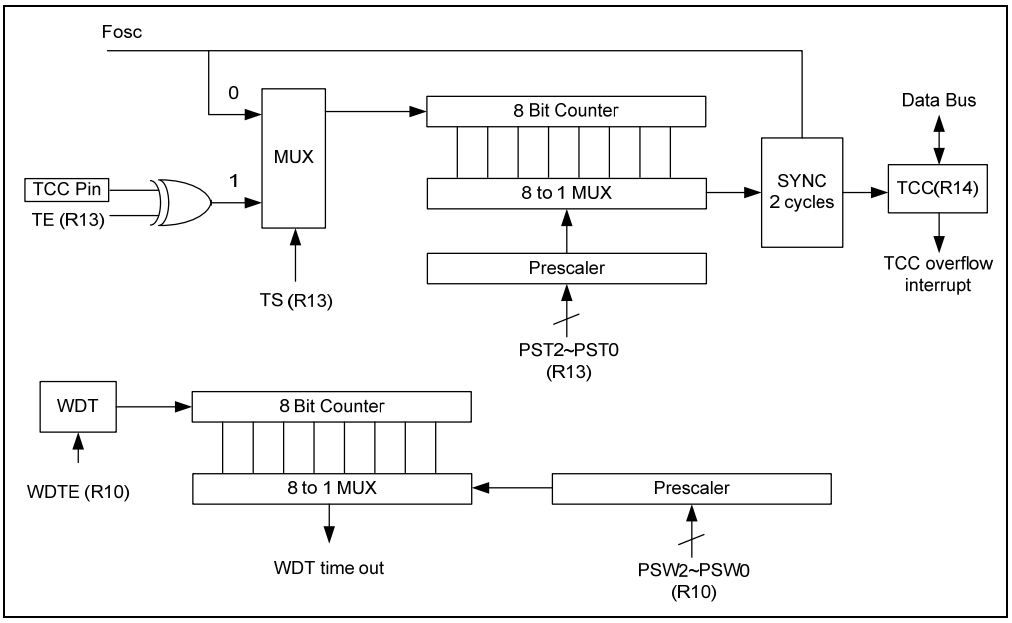


Figure 6-13 Block Diagram of TCC and WDT

[1] **Note:** VDD=5V, WDT time-out period = 16.5ms ± 8%.
VDD=3V, WDT time-out period = 18ms ± 8%.

6.3 I/O Ports

The I/O registers, Port 5 ~ Port 9 are bidirectional tri-state I/O ports. All have high sink/drive setting by software. Port 5, Port 6 and Port 7 also have wake-up function. Further, Port 6 has input status change interrupt function. Each I/O pin can be defined as "input" or "output" pin by the I/O control registers (IOC5 ~ IOC9).

The I/O registers and I/O control registers are both readable and writable.

Table 3 Usage of Port 6 Input Change Wake-up/Interrupt Function

Usage of Port 6 Input Status Changed Wake-up/Interrupt	
(I) Wake-up from Port 6 Input Status Change	(II) Port 6 Input Status Change Interrupt
(a) Before Sleep	1. Read I/O Port 6 (MOV R6,R6)
1. Disable WDT2 (use this very carefully)	2. Execute "ENI"
2. Read I/O Port 6 (MOV R6,R6)	3. Enable interrupt
3.a Enable interrupt after wake-up, if “ENI”, switch to interrupt Vector (006H), if “DISI”, execute the next instruction.	4. If Port 6 change (interrupt) → Interrupt Vector (006H)
3.b Disable interrupt, always execute next instruction	
4. Enable wake-up enable bit	
5. Execute "SLEP" instruction	
(b) After Wake-up	
1. IF "ENI" → Interrupt vector (006H)	
2. IF "DISI" → Next instruction	

6.4 UART (Universal Asynchronous Receiver/Transmitter)

Registers for UART Circuit

R_Bank	Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bank 0	0×32	URCR1	URTD8	UMODE1	UMODE0	BRATE2	BRATE1	BRATE0	UTBE	TXE
			R/W	R/W	R/W	R/W	R/W	R/W	R	R/W
Bank 0	0×33	URCR2	0	0	SBIM1	SBIM0	UINVEN	0	0	0
					R/W	R/W	R/W			
Bank 0	0×34	URS	URRD8	EVEN	PRE	PRERR	OVERR	FMERR	URBF	RXE
			R	R/W	R/W	R	R	R	R	R/W
Bank 0	0×35	URRD	URRD7	URRD6	URRD5	URRD4	URRD3	URRD2	URRD1	URRD0
			R	R	R	R	R	R	R	R
Bank 0	0×36	URTD	URTD7	URTD6	URTD5	URTD4	URTD3	URTD2	URTD1	URTD0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 0	0×0D	ISR2	CMP2IF	CMP1IF	TC3IF	TC2IF	TC1IF	UERRIF	RBFF	TBEF
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 0	0×1D	IMR2	CMP2IE	CMP1IE	TC3IE	TC2IE	TC1IE	UERRIE	URIE	UTIE
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

[2] **Note:** The Software disables the WDT (Watchdog Timer) but the hardware must be enabled before applying Port 6 Change Wake-up function. (Set Code Option Register and Bit 11 (ENWDTB-) to “1”).

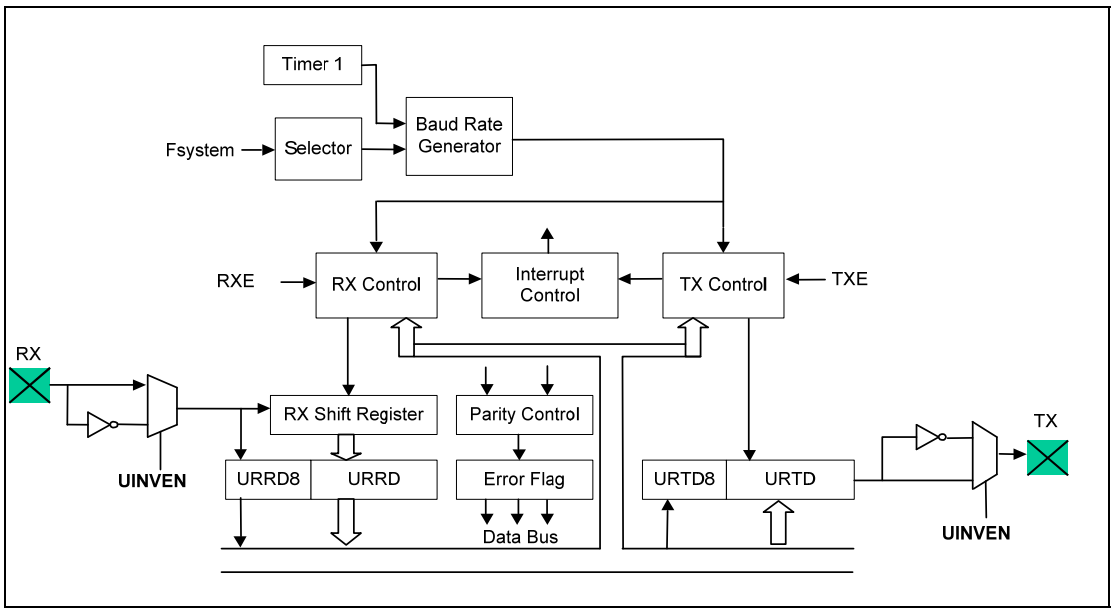


Figure 6-14 Functional Block Diagram

In Universal Asynchronous Receiver Transmitter (UART), each transmitted or received character is individually synchronized by framing it with a start bit and stop bit.

Full duplex data transfer is possible since the UART has independent transmit and receive sections. Double buffering for both sections allows the UART to be programmed for continuous data transfer.

The figure below shows the general format of one character sent or received. The communication channel is normally held in the marked state (high). Character transmission or reception starts with a transition to the space state (low).

The first bit transmitted or received is the start bit (low). It is followed by the data bits, in which the least significant bit (LSB) comes first. The data bits are followed by the parity bit. If present, then the stop bit or bits (high) confirm the end of the frame.

In receiving, the UART synchronizes on the falling edge of the start bit. When two or three “0” are detected during three samples, it is recognized as normal start bit and receiving operation is started.

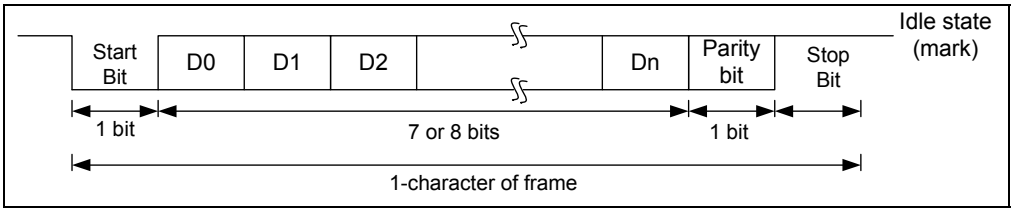


Figure 6-15 Data Format in UART

6.4.1 UART Mode

There are three UART modes. Mode 1 (7 bits data) and Mode 2 (8 bits data) allow the addition of a parity bit. The parity bit addition is not available in Mode 3. Figure 6-16 below shows the data format in each mode.

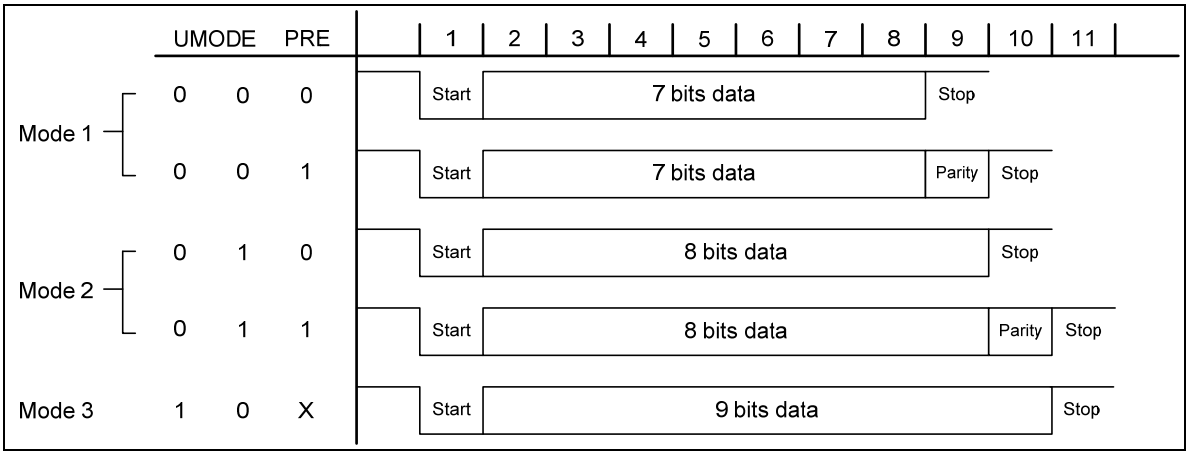


Figure 6-16 UART Model

6.4.2 Transmitting

In transmitting serial data, the UART operates as follows:

1. Set the TXE bit of the URCR1 register to enable the UART transmission function.
2. Write data into the URTD register and the UTBE bit of the URCR1 register will be set by hardware.
3. Then start transmitting.
4. Serially transmitted data are transmitted in the following order from the TX pin.
5. Start bit: one “0” bit is output.
6. Transmit data: 7, 8 or 9 bits data are output from the LSB to the MSB.
7. Parity bit: one parity bit (odd or even selectable) is output.
8. Stop bit: one “1” bit (stop bit) is output.

Mark state: output “1” continues until the start bit of the next transmitted data.
After transmitting the stop bit, the UART generates a TBEF interrupt (if enabled).

6.4.3 Receiving

In receiving, the UART operates as follows:

1. Set the RXE bit of the URS register to enable the UART receiving function. The UART monitors the RX pin and synchronizes internally when it detects a start bit.
2. Receive data is shifted into the URRD register in the order from LSB to MSB.
3. The parity bit and the stop bit are received. After one character is received, the URBF bit of the URS register will be set to 1. This means UART interrupt will occur.

4. The UART makes the following checks:

   (a) Parity check: The number of 1's of the received data must match the even or odd parity setting of the EVEN bit in the URS register.

   (b) Frame check: The start bit must be 0 and the stop bit must be 1.

   (c) Overrun check: The URBF bit of the URS register must be cleared (that means the URRD register should be read out) before the next received data is loaded into the URRD register.

   If any checks failed, the UERRIF interrupt will be generated (if enabled), and an error flag is indicated in PRERR, OVERR or FMERR bit. The error flag should be cleared by software otherwise, UERRIF interrupt will occur when the next byte is received.

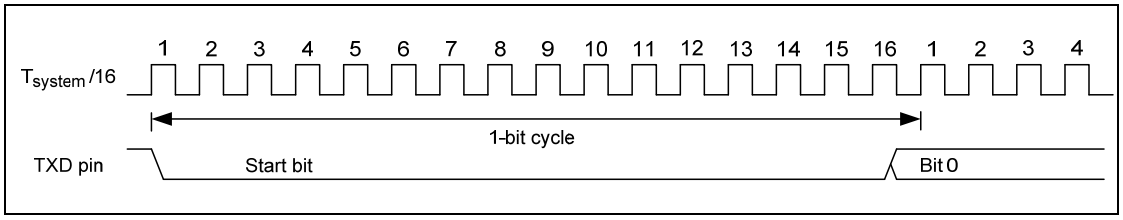
5. Read received data from URRD register. The URBF bit will be cleared by hardware.

6.4.4 Baud Rate Generator

The baud rate generator is comprised of a circuit that generates a clock pulse to determine the transfer speed for transmission/reception in the UART.
The BRATE2~BRATE0 bits of the URC register can determine the desired baud rate.

6.4.5 UART Timing

1. Transmission Counter Timing:



2. Receiving Counter Timing:

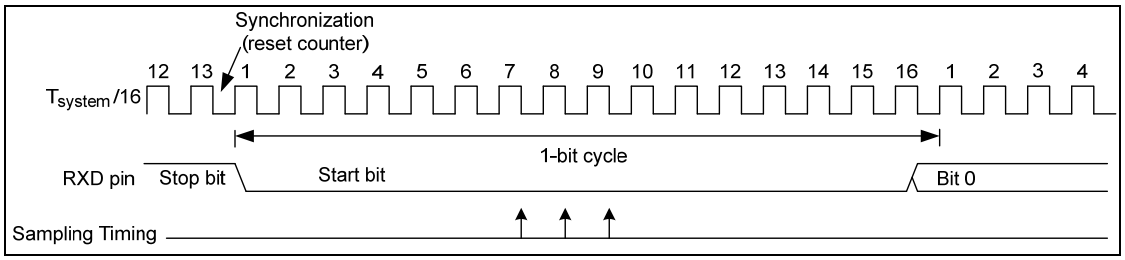


Figure 6-17 UART Timing

6.5 SPI Function

R_Bank	Addr.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bank 0	0×2B	SPICR	CES	SPIE	SRO	SSE	SDOC	SBRS2	SBRS1	SBRS0
			R/W	R/W	R	R/W	R/W	R/W	R/W	R/W
Bank 0	0×2C	SPIS	DORD	TD1	TD0	0	OD3	OD4	0	RBF
			R/W	R/W	R	R	R/W	R/W	R	R/W
Bank 0	0×2D	SPIR	SRB7	SRB6	SRB5	SRB4	SRB3	SRB2	SRB1	SRB0
			R	R	R	R	R	R	R	R
Bank 0	0×2E	SPIW	SWB7	SWB6	SWB5	SWB4	SWB3	SWB2	SWB1	SWB0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 0	0×0C	ISR1	LVDIF	ADIF	SPIF	PWMBIF	PWMAIF	EXIF	ICIF	TCIF
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 0	0×1C	IMR1	LVDIE	ADIE	SPIE	PWMBIE	PWMAIE	EXIE	ICIE	TCIE
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

6.5.1 Overview and Features

Overview:

Figures 6-18, 6-19, and 6-20 show how the EM78F568N/EM78F668N communicates with other devices through the SPI module. If the EM78F568N/EM78F668N is a master controller, it sends clock through the SCK pin. A couple of 8-bit data are transmitted and received at the same time. However, if the EM78F568N/EM78F668N is defined as a slave, its SCK pin could be programmed as an input pin. Data will continue to be shifted based on both the clock rate and the selected edge. The SPIS Bit 7 (DORD) can be set to determine the SPI transmission order, the SPICR Bit 3 (SDOC) can also be set to control the SDO pin after the serial data output status and the SPIS Bit 6 (TD1), Bit 5 (TD0) determines the SDO status output delay time.

Features:

- Operation in either Master mode or Slave mode
- Three-wire or four-wire full duplex synchronous communication
- Programmable baud rates of communication
- Programming clock polarity, (R2B Bit 7)
- Interrupt flag available for the read buffer full
- SPI transmission order
- After serial data output SDO status select
- SDO status output delay times
- SPI handshake pin
- Up to a maximum of 8 MHz bit frequency

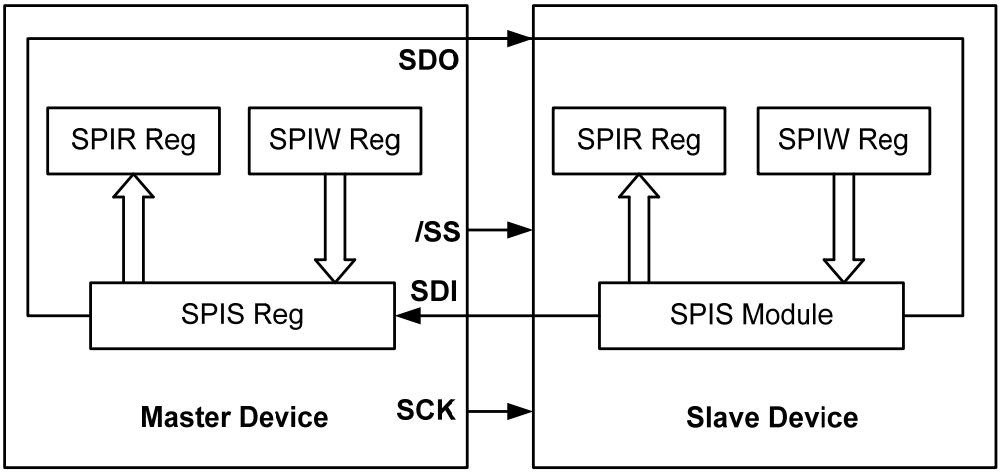


Figure 6-18 SPI Master/Slave Communication

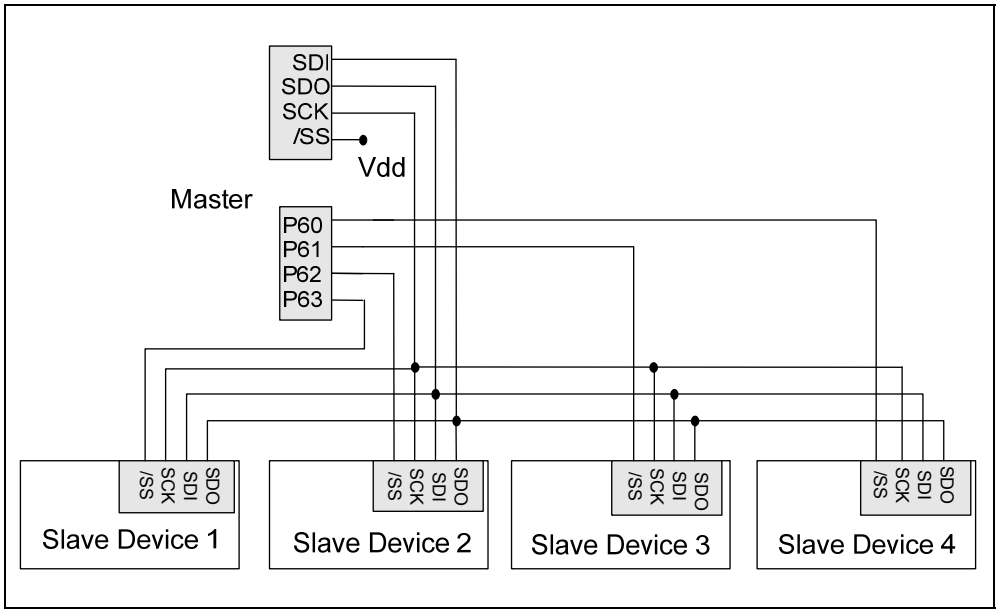


Figure 6-19 SPI Configuration of Single-Master and Multi-Slave

6.5.2 SPI Function Description

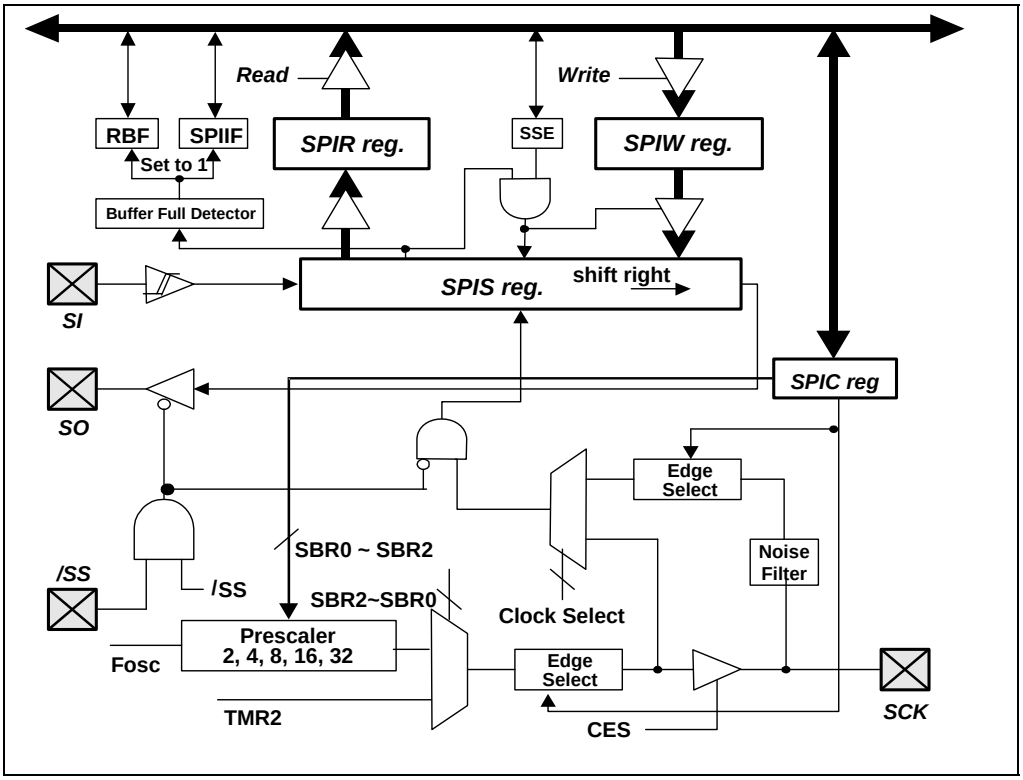


Figure 6-20 SPI Block Diagram

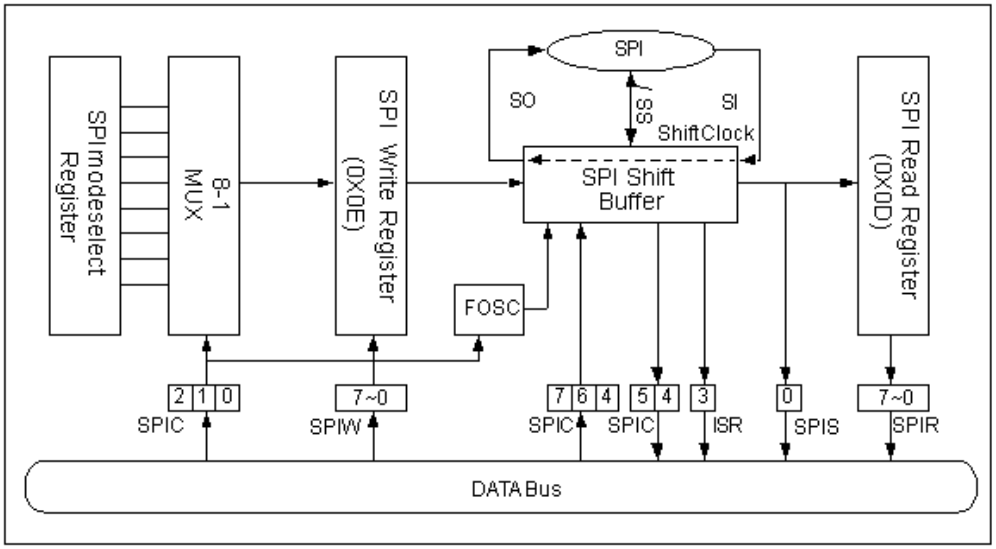


Figure 6-21 Functional Block Diagram of SPI Transmission

Below are the functions of each block and explanations on how to carry out the SPI communication with the signals depicted in Figures 6-20 and 6-21.

- P52/RX/SI: Serial Data In
- P51/SDA/TX/SO: Serial Data Out
- P53/SCL/SCK: Serial Clock
- P50/VREF//SS: /Slave Select (Option). This pin (/SS) may be required in slave mode
- RBF: Set by Buffer Full Detector
- Buffer Full Detector: Set to 1 when an 8-bit shifting is completed.
- SSE: Loads the data in SPIS register, and begin to shift
- SPIS reg.: Shifting byte in and out. The MSB is shifted first. Both the SPIR and the SPIW registers are shifted at the same time. Once data are written, SPIS starts transmission / reception. The data received will be moved to the SPIR register as the shifting of the 8-bit data is completed. The RBF (Read Buffer Full) flag and the SPIIF (SPI Interrupt) flag are then set.
- SPIR reg.: Read buffer. The buffer will be updated as the 8-bit shifting is completed. The data must be read before the next reception is completed. The RBF flag is cleared as the SPIR register reads.
- SPIW reg.: Write buffer. The buffer will deny any attempt to write until the 8-bit shifting is completed.

The SSE bit will be kept in “1“ if the communication is still undergoing. This flag must be cleared as the shifting is completed. Users can determine if the next write attempt is available.

- SBRS2~SBRS0: Programming the clock frequency/rates and sources.
- Clock Select: Select either the internal or the external clock as the shifting clock.
- Edge Select: Select the appropriate clock edges by programming the CES bit

6.5.3 SPI Signal and Pin Description

The detailed functions of the four pins, SI, SO, SCK, and /SS are as follows:

P52/RX/SI:

- Serial Data In
- Receive sequentially, the Most Significant Bit (MSB) first, Least Significant Bit (LSB) last,
- Defined as high-impedance, if not selected

- Program the same clock rate and clock edge to latch on both the master and slave devices
- The byte received will update the transmitted byte
- The RBF will be set as the SPI operation is completed
- Timing is shown in Figures 6-22 and 6-23

P51/SDA/TX/SO:

- Serial Data Out
- Transmit sequentially; the Most Significant Bit (MSB) first, Least Significant Bit (LSB) last
- Program the same clock rate and clock edge to latch on both the master and slave devices
- The received byte will update the transmitted byte
- The CES bit will be reset, as the SPI operation is completed
- Timing is shown in Figures 6-22 and 6-23

P53/SCL/SCK:

- Serial Clock
- Generated by a master device
- Synchronize the data communication on both the SI and SO pins
- The CES is used to select the edge to communicate.
- The SBR0~SBR2 is used to determine the baud rate of communication
- The CES, SBR0, SBR1, and SBR2 bits have no effect in slave mode
- Timing is shown in Figures 6-22 and 6-23

P50/VREF//SS:

- Slave Select; negative logic
- Generated by a master device to signify the slave(s) to receive data
- Goes low before the first cycle of SCK appears, and remains low until the last (8th) cycle is completed
- Ignores the data on the SI and SO pins while /SS is high, because the SO is no longer driven
- Timing is shown in Figures 6-22 and 6-23

6.5.4 SPI Mode Timing

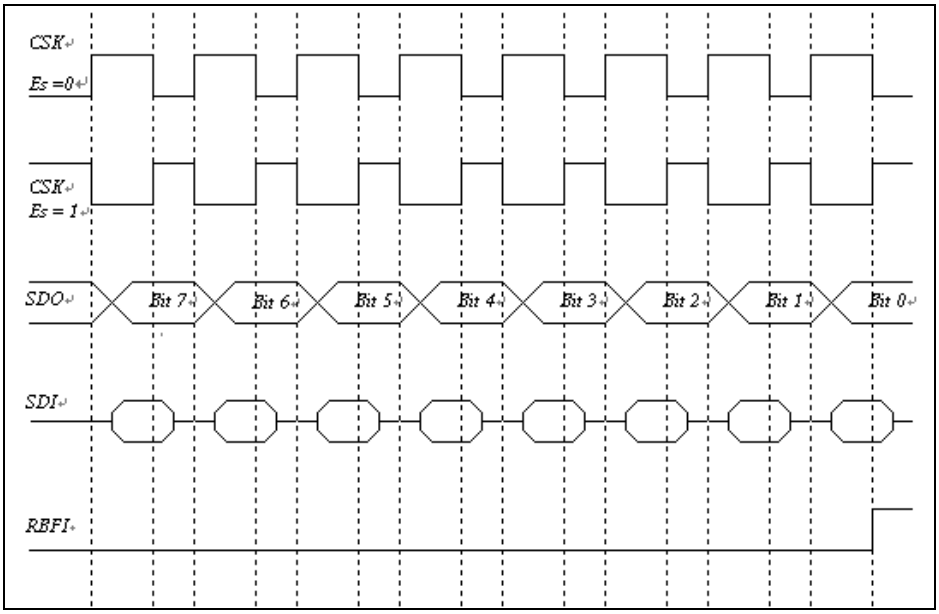


Figure 6-22 SPI Mode with /SS Disabled

The SCK edge is selected by programming bit CES. The waveform shown in Figure 6-22 is applicable regardless whether the EM78F568N/EM78F668N is in master or slave mode with /SS disabled. However, the waveform in Figure 6-23 can only be implemented in slave mode with /SS enabled.

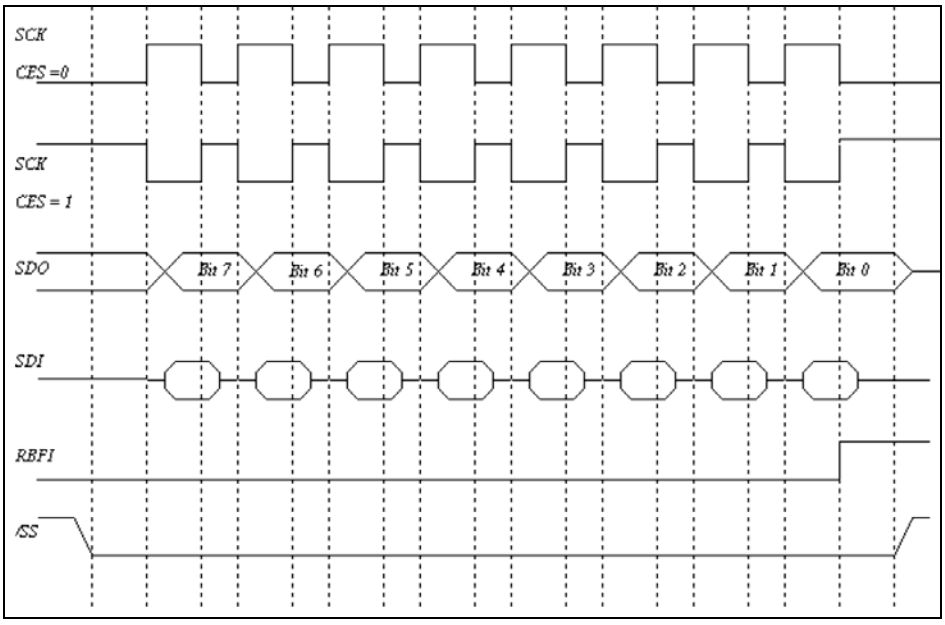


Figure 6-23 SPI Mode with /SS Enabled

6.6 I²C Function

Registers for I²C Circuit

R_BANK	Addr.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bank 1	0×23	I2CCR1	Strobe/Pend	IMS	ISS	STOP	SAR_EMPTY	ACK	FULL	EMPTY
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 1	0×24	I2CCR2	0	0	0	0	I2CTS1	I2CTS0	I2CCS	I2CEN
			R	R	R	R	R/W	R/W	R/W	R/W
Bank 1	0×25	I2CSA	SA6	SA5	SA4	SA3	SA2	SA1	SA0	IRW
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 1	0×26	I2CDA	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0
				R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 1	0×27	I2CDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 1	0×28	I2CA	0	0	0	0	0	0	DA9	DA8
				R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 0	0×0E	ISR3	0	0	0	0	0	PWMCIF	I2CRIF	I2CTIF
			R	R	R	R	R	R/W	R/W	R/W
Bank 0	0×1E	IMR3	0	0	0	0	0	PWMCIE	I2CRIE	I2CTIE
			R	R	R	R	R	R/W	R/W	R/W

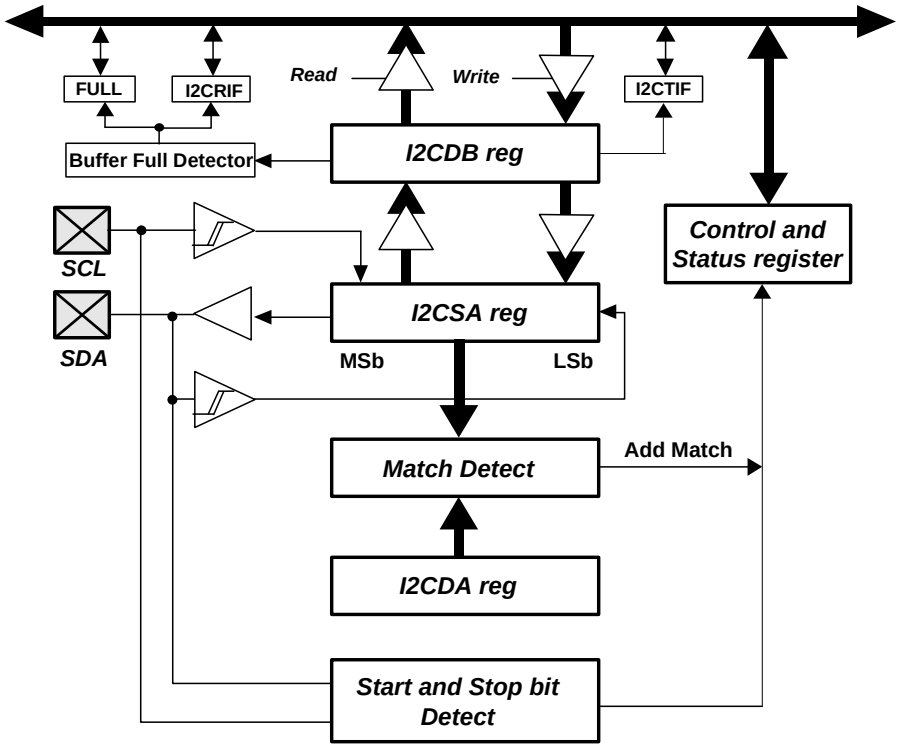


Figure 6-24 I²C Block Diagram

The EM78F568N/EM78F668N supports a bidirectional, 2-wire bus, 7-bit and 10-bit addressing and data transmission protocol. A device that sends data onto the bus is defined as transmitter, while a device receiving data is defined as a receiver. The bus has to be controlled by a master device which generates the Serial Clock (SCL), controls the bus access and generates the Start and Stop conditions. Both master and slave can operate as transmitter or receiver, but the master device determines which mode is activated.

Both SDA and SCL are bidirectional lines, connected to a positive supply voltage via a pull-up resistor. When the bus is free, both lines are high. The output stages of devices connected to the bus must have an open-drain or open-collector to perform the wired-AND function. Data on the I^2C-bus can be transferred at a rate of 100 kbit/s in Standard mode or up to 400 kbit/s in Fast mode.

The data on the SDA line must be stable during the High period of the clock. The High or Low state of the data line can only change when the clock signal on the SCL line is Low.

Within the procedure of the I^2C bus, unique situations arise which are defined as Start (S) and Stop (P) conditions.

A High to Low transition on the SDA line while SCL is High is one such unique case. This situation indicates a Start condition.

A Low to High transition on the SDA line while SCL is High defines a Stop condition.

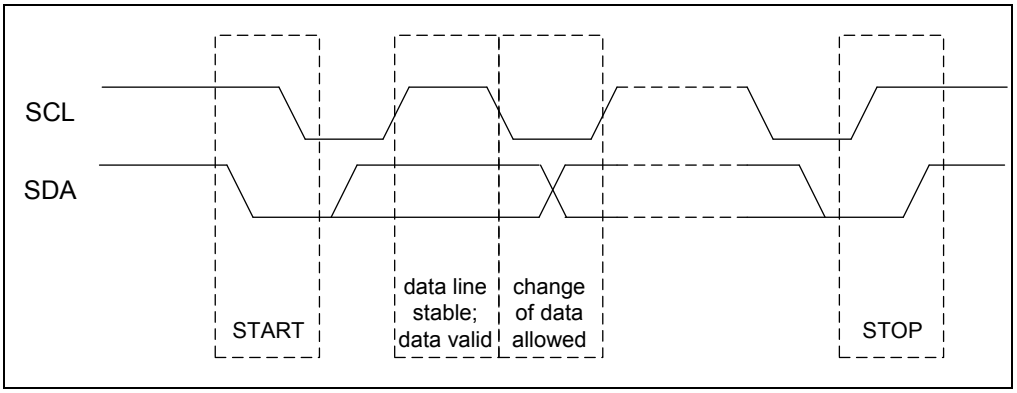


Figure 6-25 I^2C Transfer Condition

7-Bit Slave Address

Master-transmitter transmits to slave-receiver. The transfer direction is not changed.

The master reads the slave immediately after the first byte. At the moment of the first acknowledge, the master-transmitter becomes a master-receiver and the slave-receiver becomes a slave-transmitter. This first acknowledge is still generated by the slave. The Stop condition is generated by the master, which has previously sent a not-acknowledge (/A).

The difference between a master transmitter from a master receiver is only in R//W bit, if the R//W bit were “0”, the master device would be a transmitter, the other way, the master device would be a receiver. The master transmitter is described in the “Figure 6-26 *7-Bit Slave Address in Master-transmitter Transmits to Slave-receiver*”, and the master receiver is described in the “Figure 6-27 *7-Bit Slave Address in Master-Receiver read Slave-Transmitter*”.

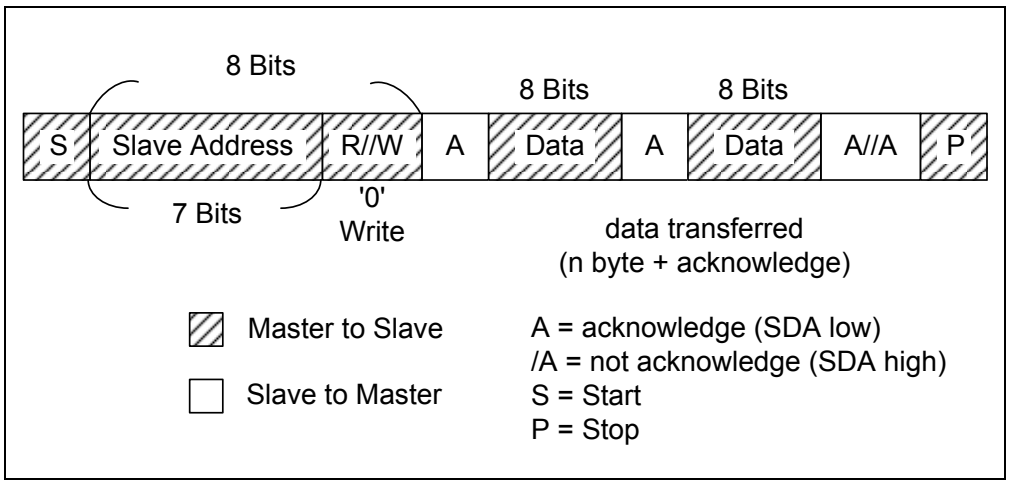


Figure 6-26 7-Bit Slave Address in Master-transmitter Transmits to Slave-receiver

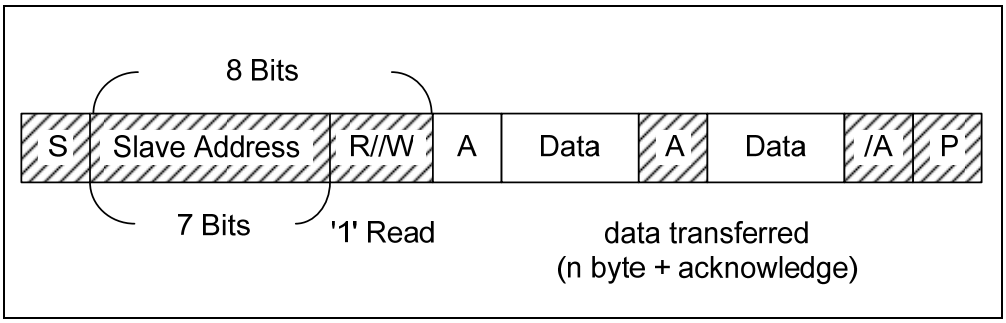


Figure 6-27 7-Bit Slave Address in Master Receiver Read Slave-transmitter

10-Bit Slave Address:

In 10-bit slave address mode, using 10-bit for addressing exploits the reserved combination 11110XX for the first 7 bits of the first byte following a START (S) or repeated START (Sr) condition. The first 7 bits of the first byte are the combination 11110XX of which the last 2 bits (XX) are the two most-significant bits of the 10-bit address. If the R//W bit were “0”, the second byte after acknowledge would be the 8 address bits of the10-bit slave address; on the other way, the second byte would just only be the next transmitted data from a slave to master device. The first bytes 11110XX would be transmitted by using the slave address register (I2CSA), and the second bytes XXXXXXXX would be transmitted by using the data buffer (I2CDB).

There are few kinds of different formats that would be explained in Fig 6-28 ~ Fig 6-32 in the 10-bit slave address mode. The possible data transfer formats are:

- **Master-Transmitter Transmits to Slave-Receiver with a 10-bit Slave Address**

When the slave has received the first byte after the START bit from the master, each slave device will compare the 7 bits of the first byte (11110XX) with their own address and the 8th bit, R//W, if the R//W bit is “0”, the slave would return the acknowledge (A1) and that would be possible for more than 1 slave device to return it. Then all slave devices will continue to compare the second address (XXXXXXXX), if the slave device has matched, that would be only 1 slave device to return acknowledge. The matching slave device will remain addressed by the master until it receives a STOP condition or a repeated START condition followed by the different slave address.

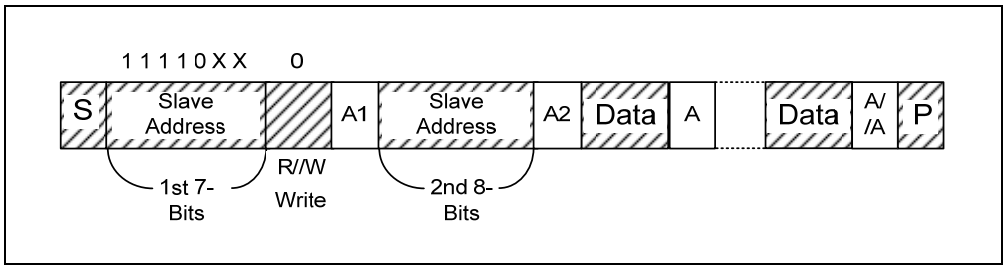


Figure 6-28 Master-transmitter Transmits to Slave-receiver with a 10-bit Slave Address

- **Master-Receiver Read Slave-Transmitter with a 10-bit Slave Address**

Up to and including Acknowledge Bit A2, the procedure is the same as that described for master-transmitter addressing a slave receiver. After the Acknowledge A2, a repeated START condition (Sr) followed by 7 bits slave address (11110XX) but the 8th bit R//W is “1”, the addressed slave device will return an Acknowledge A3. If the repeated START (Sr) condition and the 7 bits of the first byte (11110XX) are received by the slave device, all the slave device would compare with their own address and test the 8th R//W, but none of the slave devices return an acknowledge because R//W=1.

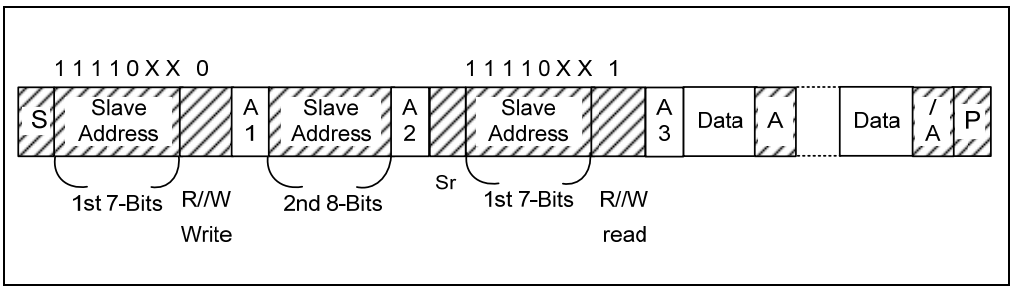


Figure 6 -29 Master-receiver Read slave-transmitter with a 10-bit Slave Address

- **Master Addresses a Slave with 10-Bit Addresses Transmits and Receives Data in the Same Slave Device.**

At first, the transmitter procedure is the same as the section of the “Master-transmitter transmits to slave-receiver with a 10-bit slave address”, then the master device can start to transmit the data to the slave device. If the slave device has received an Acknowledge or None Acknowledge which were followed by repeat START (Sr), repeat the procedure of the section of “Master-receiver read slave-transmitter with a 10-bit slave address”.

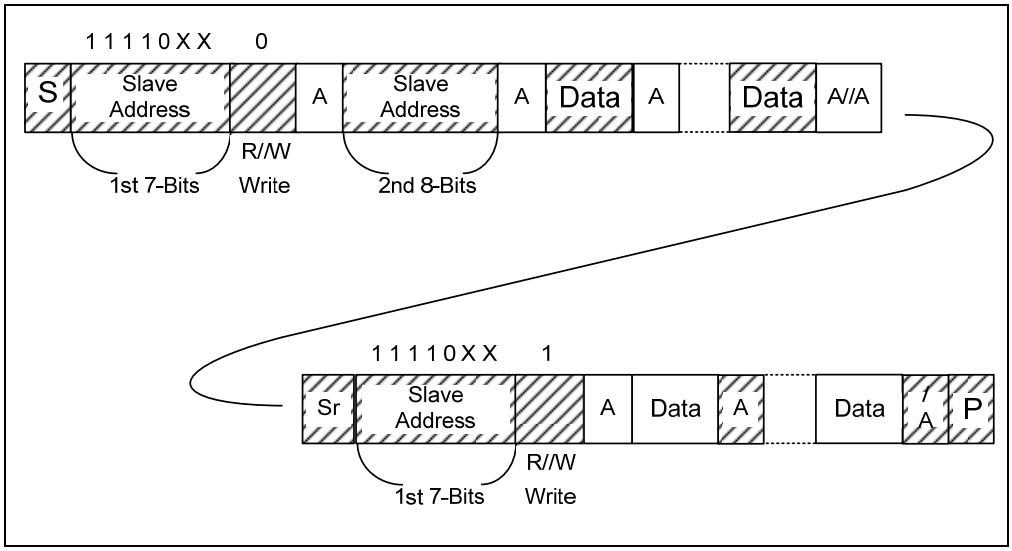


Figure 6-30 Master Addresses a Slave with 10-Bit addresses Transmits and Receives Data in the Same Slave Device.

■ Master Device Transmits Data to Two or More Than Two Slave Devices

The section of “Master-transmitter transmits to slave-receiver with a 10-bits slave address” describes the procedure on how to transmit the data to a slave device, if the master device has finished the transmittal, and wants to transmit the data to another device, the master would need to address the new slave device, the address procedure is described in the section of the “Master-transmitter transmits to slave-receiver with a 10-Bits slave address”. If the master device wants to transmit the data in 7-Bit slave address mode and transmit the data in 10-Bit slave address mode in the serial transfer, after the START or repeat START conditions, a 7-Bit and 10-Bit address could be transmitted. Figure 6-31 shows how to transmit the data in 7-Bit and 10-Bit address mode in serial transfer.

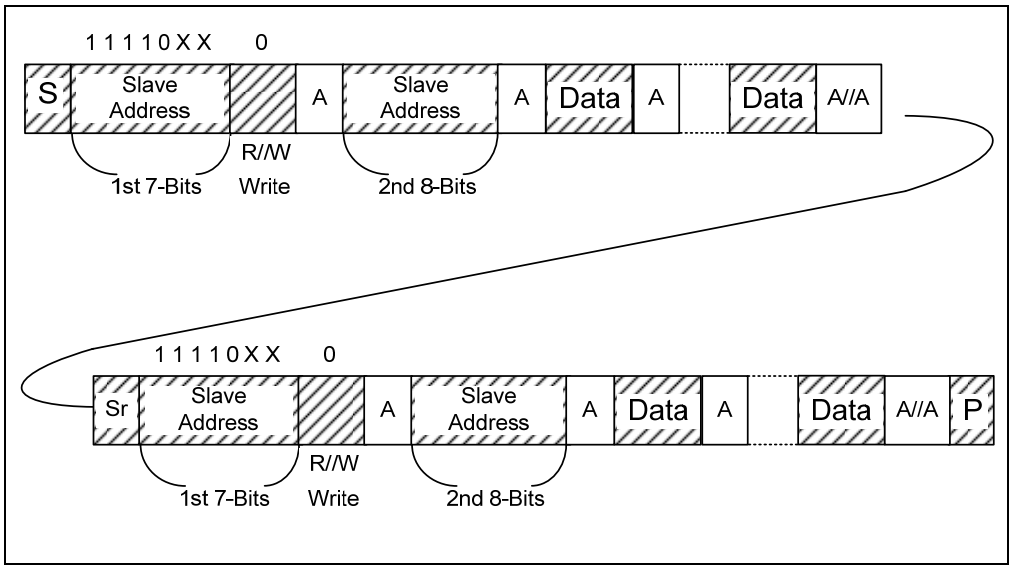


Figure 6-31 Transmit one more device with a 10-bit Slave Address

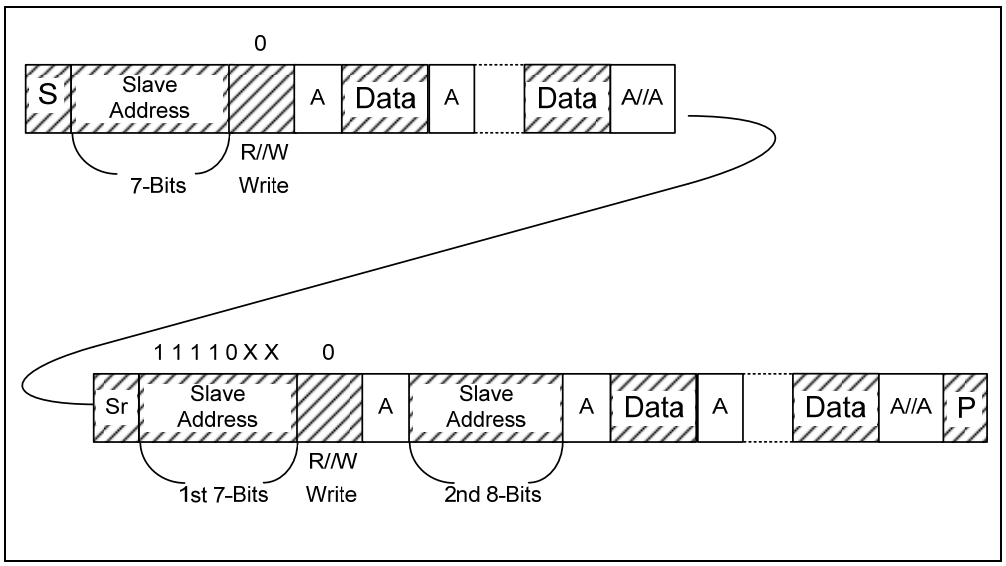


Figure 6-32 7-bit and 10-bit Slave Address Modes

6.6.1 Master Mode

In transmitting serial data, the I^2C operates as follows:

1. Set the I2CTS1~0, I2CCS and ISS bits to select the I^2C transmit clock source.
2. Set the I2CEN and IMS bits to enable the I^2C master function.
3. Write the slave address into the I^2CSA register and IRW bit to select read or write.
4. Setting the strobe bit will start the transmission and then check the SAR_EMPTY bit.
5. Write the 1st data into the I2CDB register, set the strobe bit and Check EMPTY bit.
6. Write the 2nd data into the I2CDB register, set the strobe bit, STOP bit and Check the EMPTY bit.

6.6.2 Slave Mode

In receiving, the I^2C operates as follows:

1. Set the I2CTS1~0, I2CCS and ISS bits to select the I^2C transmit clock source.
2. Set the I2CEN and IMS bits to enable the I^2C slave function.
3. Write the device address into the I2CDA register.
4. Check the FULL bit, read the I2CDB register (address) and then clear the Pend bit.
5. Check the FULL bit, read the I2CDB register (1st data) and then clear the Pend bit.
6. Check the FULL bit, read the I2CDB register (2nd data) and then clear the Pend bit.

6.7 A/D Converter

Registers for AD Converter Circuit

R_Bank	Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bank 0	0×24	ADCR1	VREFS	ADRUN	ADPD	0	0	ADIS2	ADIS1	ADIS0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 0	0×25	ADCR2	CALI	SIGN	VOF2	VOF1	VOF0	CKR2	CKR1	CKR0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 0	0×26	ADICL	ADE7	ADE6	ADE5	ADE4	ADE3	ADE2	ADE1	ADE0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 0	0×29	ADDH	ADD11	ADD10	ADD9	ADD8	ADD7	ADD6	ADD5	ADD4
			R	R	R	R	R	R	R	R
Bank 0	0×2A	ADDL	0	0	0	0	ADD3	ADD2	ADD1	ADD0
			-	-	-	-	R	R	R	R
Bank 0	0×1C	IMR1	LVDIE	ADIE	SPIE	PWMBIE	PWMAIE	EXIE	ICIE	TCIE
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 0	0×0C	ISR1	LVDIF	ADIF	SPIF	PWMBIF	PWMAIF	EXIF	ICIF	TCIF
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 0	0×2F	WUCR1	0	0	LVDWE	ICWE	ADWE	CMP2WE	CMP1WE	EXWE
			R	R	R/W	R/W	R/W	R/W	R/W	R/W

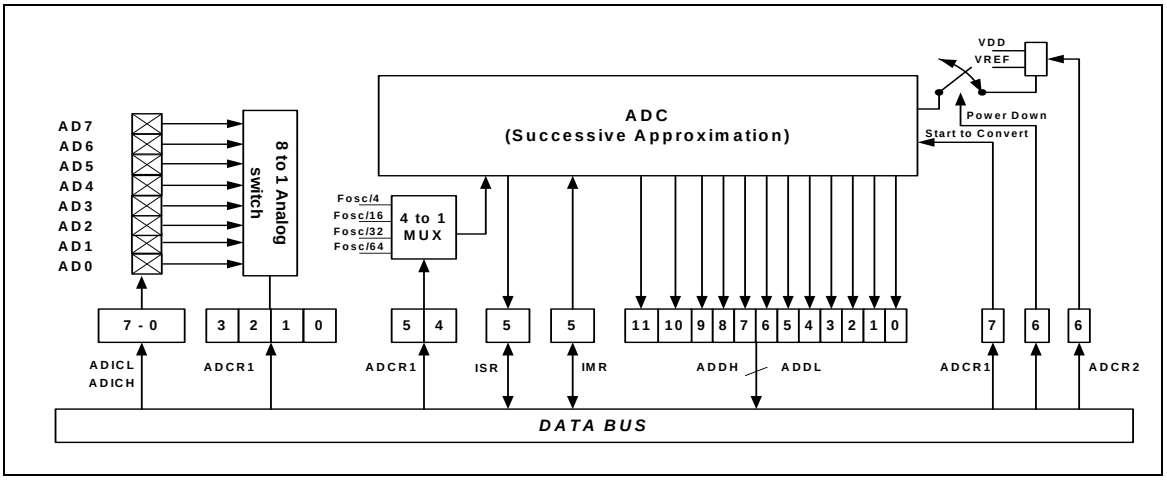


Figure 6-33 AD Converter

This is a 12-bit successive approximation type AD converter. The upper side of analog reference voltage can select either internal VDD or external input pin P50 (VREF) by setting the VREFS bit in ADCR1. Connecting to external VREF is more accurate than connecting to internal VDD.

6.7.1 ADC Data Register

When the A/D conversion is completed, the result is loaded to the ADDH (8-bit) and ADDL (4-bit). The START/END bit is cleared, and the ADIF is set.

6.7.2 A/D Sampling Time

The accuracy, linearity, and speed of the successive approximation of the A/D converter are dependent on the properties of the ADC. The source impedance and the internal sampling impedance directly affect the time required to charge the sample holding capacitor. The application program controls the length of the sample time to meet the specified accuracy. Generally speaking, the program should wait for 2 μs for each KΩ of the analog source impedance and at least 2 μs for the low-impedance source. The maximum recommended impedance for the analog source is 10KΩ at VDD =5V. After the analog input channel is selected, this acquisition time must be done before A/D conversion can be started.

6.7.3 A/D Conversion Time

ADCK0 and ADCK1 select the conversion time (Tct), in terms of instruction cycles. This allows the MCU to run at maximum frequency without sacrificing accuracy of the A/D conversion. Table 5 shows the relationship between Tct and the maximum operating frequencies.

Table 5

CKR2~CKR0	Operation Mode	Max. Frequency (Fc)	Max. Conversion Rate per Bit	Max. Conversion Rate
000	Fosc/4	4 MHz	1 MHz (1μs)	15μs (66.66kHz)
001	Fosc/1	1 MHz	1 MHz (1μs)	15μs (66.66kHz)
010	Fosc/2	2 MHz	1 MHz (1μs)	15μs (66.66kHz)
011	Fosc/8	8 MHz	1 MHz (1μs)	15μs (66.66kHz)
100	Fosc/16	16 MHz	1 MHz (1μs)	15μs (66.66kHz)
101	Fosc/32	32 MHz	1 MHz (1μs)	15μs (66.66kHz)
110	Fosc/64	64 MHz	1 MHz (1μs)	15μs (66.66kHz)
111	Internal RC	–	1 MHz (1μs)	15μs (66.66kHz)

6.8 PWM

6.8.1 Overview

In PWM mode, PWMA, PWMB pins produce up to 10-bit resolution PWM output (see Figure 6-34 for the functional block diagram). A PWM output has a period and a duty cycle, and it keeps the output high. The PWM baud rate is the inverse of the period. Figure 6-35 depicts the relationships between a period and a duty cycle.

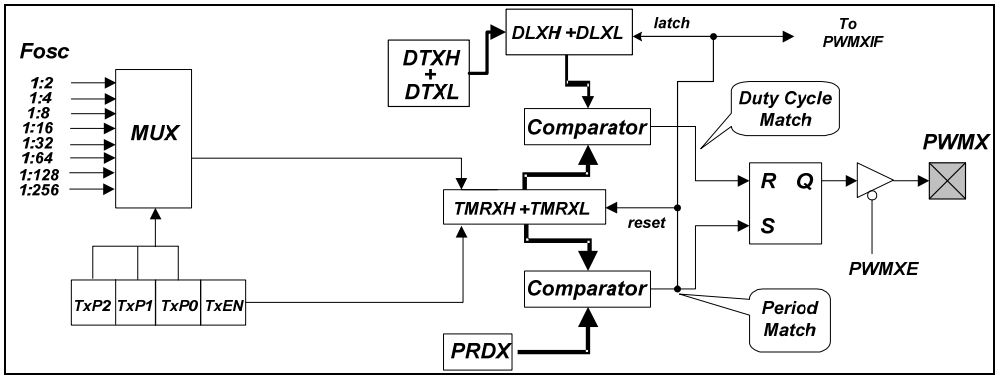


Figure 6-34 Functional Block Diagram of the three PWMs

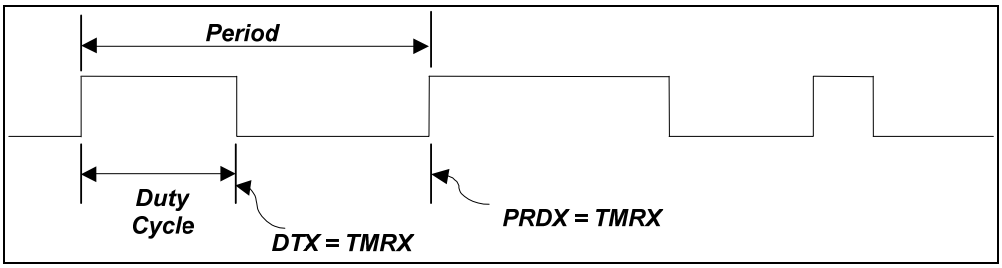


Figure 6-35 Output Timing of the PWM

6.8.2 Increment Timer Counter (TMRX: TMRAH/TWRAL or TMRBH/TWRBL)

TMRX are 10-bit clock counters with programmable prescalers. They are designed for the PWM module as baud rate clock generators. TMRX just can be read only. If employed, they can be turned down for power saving by setting TXEN bits to 0.

6.8.3 PWM Period (PRDX: PRDA, PRDB)

The PWM period is defined by writing to the PRDX register. When TMRX is equal to PRDX, the following events occur on the next increment cycle:

- TMRX is cleared.
- The PWMX pin is set to 1.
- The PWM duty cycle is latched from DTXL/DTXH to DLXL/DLXH.

  Note: The PWM output will not be set, if the duty cycle is 0.
- The PWMXIF pin is set to 1.

The following formula describes how to calculate the PWM Time Period**:**

$$Period = (PRDX + 1) \times \left(\frac{1}{Fosc}\right) \times (TMRX \ \ prescaler\ value)$$

Example:

PRDX = 49; Fosc = 4 MHz TMRX (0, 0, 0) = 1 : 2,

Then

$$Period = (49+1) \times \left(\frac{1}{4M}\right) \times 2 = 25\,\mu s$$

6.8.4 PWM Duty Cycle (DTX: DTXH/ DTXL; DLX: DLXH/DLXL)

The PWM duty cycle is defined by writing to the DTX register, and is latched from DTX to DLX while TMRX is cleared. When DLX is equal to TMRX, the PWMX pin is cleared. DTX can be loaded at any time. However, it cannot be latched into DLX until the current value of DLX is equal to TMRX.

The following formula describes how to calculate the PWM duty cycle**:**

$$Duty\ cycle = (DTX) \times \left(\frac{1}{F_{OSC}}\right) \times (TMRX \ \ prescale\ value)$$

Example:

DTX = 10; Fosc = 4 MHz; TMRX (0, 0, 0) = 1 : 2,

Then

$$Duty\ cycle = (10) \times \left(\frac{1}{4M}\right) \times 2 = 5\,\mu s$$

6.9 Comparator

R_Bank	Addr.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bank 0	0X39	CMP1CR	C1RS	CP1OUT	CMP1COS1	CMP1COS0	CP1NS	CP1PS	CP1NRE	CP1NRDT
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 0	0X3C	CMP2CR	C2RS	CP2OUT	CMP2COS1	CMP2COS0	CP2NS	CP2PS	CP2NRE	CP2NRDT
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 0	0X43	CPIRLCON	BG2OUT	C2IRL2	C2IRL1	C2IRL0	BG1OUT	C1IRL2	C1IRL1	C1IRL0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 0	0X0D	ISR2	CMP2IF	CMP1IF	TC3IF	TC2IF	TC1IF	UERRIF	RBFF	TBEF
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 0	0x1D	IMR2	CMP2IE	CMP1IE	TC3IE	TC2IE	TC1IE	UERRIE	URIE	UTIE
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The EM78F668N has two comparators, each of which has two analog inputs and one output. The comparators can be employed to wake up from sleep mode. The Figure shows the comparator circuit.

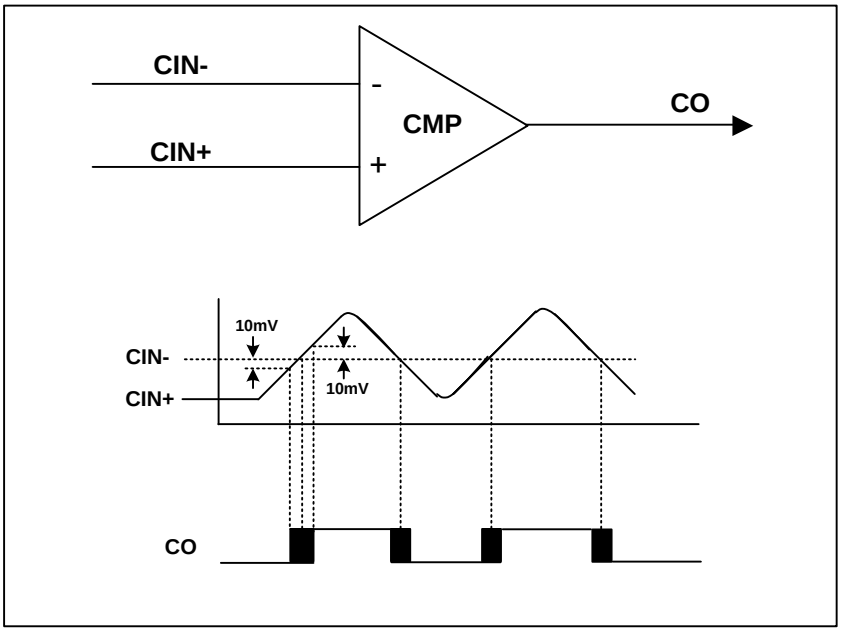


Figure 6-36 Comparator Operating Mode

6.9.1 External Reference Signal

The analog signal that is presented at CIN- is compared to the signal at CIN+, and the digital output (CO) of the comparator is adjusted accordingly.

- The reference signal must be between VSS and VDD.
- The reference voltage can be applied to either pin of the comparator.
- Threshold detector applications may be of the same reference.
- The comparator can operate from the same or different reference source.

6.9.2 Internal Reference Signal

The EM78F668N offers two internal voltage references which can be applied to CIN1+/ CIN2+. Users can use by setting C1RS of R39 Bank 0/C2RS of R3C Bank 0 and corresponding voltage level in R43 Bank 0.

6.9.3 Comparator Outputs

- The compared result is stored in CP1OUT of R39 Bit 6 of Bank 0 for Comparator 1; in CP2OUT of R3C Bit 6 of Bank 0 for Comparator 2.
- By programming Bit 5, Bit 4 <CMP1COS1, CMP1COS0> of Register R39 Bank 0 and Bit 5, Bit 4 <CMP2COS1, CMP2COS0> of Register R3C Bank 0, the compared results can output to CO1 and CO2 pins.
- Figure 6-37 shows the Comparator Output Block Diagram.

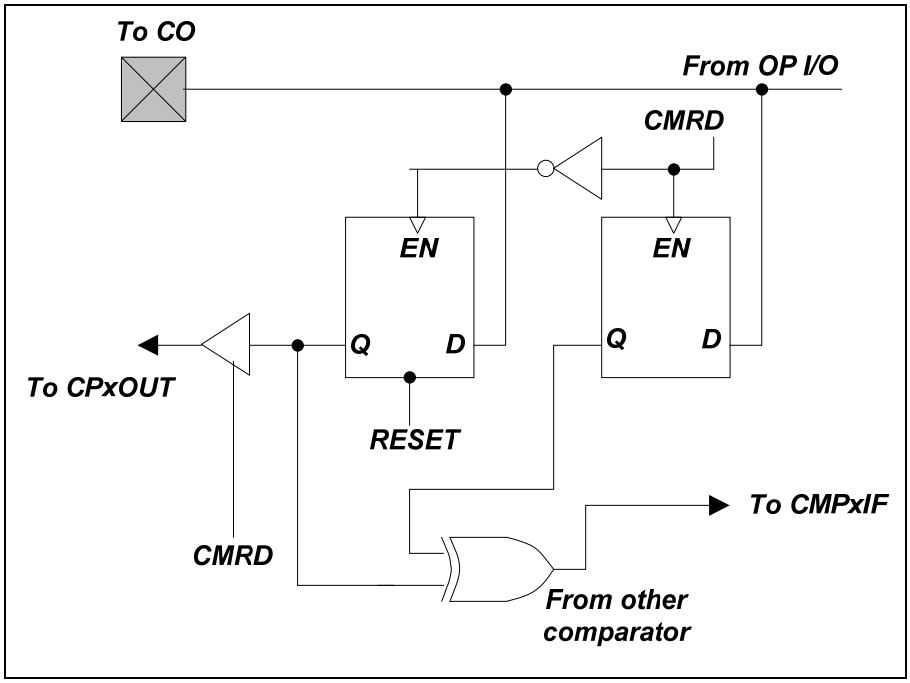


Figure 6-37 Comparator Output Block Diagram

6.9.4 Interrupt

- CMP1IE and CMP2IE (R1D.6 and 7 Bank 0) and the "ENI" instruction execution must be enabled.
- Interrupt occurs whenever a change occurs on the output pins of the comparators.
- The actual change on the pins can be determined by reading the bit CP1OUT of R39 Bit 6 of Bank 0 for Comparator 1 and the bit CP2OUT of R3C Bit 6 of Bank 0 for Comparator 2.
- CMP1IF and CMP2IF (RD.6 and 7 Bank 0), the comparator interrupt flags, can only be cleared by software.

6.9.5 Wake-up from Sleep Mode

- If enabled, the comparator remains active and the interrupt remains functional, even in Sleep mode.
- If a mismatch occurs, the interrupt will wake up the device from Sleep mode.
- The power consumption should be taken into consideration for the benefit of energy conservation.
- If the function is unemployed during Sleep mode, turn off the comparator before entering into sleep mode.

6.10 Reset and Wake-up

6.10.1. Reset

A reset is initiated by one of the following events-

(1) Power-on reset.

(2) /RESET pin input "low", or

(3) WDT time-out (if enabled).

The device is kept in a reset condition for a period of approximately 18ms[3] (one oscillator start-up timer period) after the reset is detected. If the /Reset pin goes “low” or the WDT time-out is active, a reset is generated, in RC mode the reset time is 34 clocks, High Crystal mode reset time is 2 ms and 32 clocks. In low Crystal mode, the reset time is 500 ms. Once a reset occurs, the following functions are performed.

- The oscillator is running, or will be started.
- The Program Counter (R2) is set to all "0".
- All I/O port pins are configured as input mode (high-impedance state).
- The Watchdog timer and prescaler are cleared.
- The bits of the control register are set at Table 4.

Sleep (power down) mode is asserted by executing the “SLEP” instruction. While entering sleep mode, WDT (if enabled) is cleared but keeps on running. After wake-up is generated, in RC mode the wake-up time is 34 clocks, High Crystal mode wake-up time is 2 ms and 32 clocks. In low Crystal mode, the wake-up time is 500 ms.

The controller can be awakened by:

1. External reset input on /RESET pin
2. WDT time-out (if enabled)
3. External (P60, /INT) pin change (if EXWE is enabled)
4. Port 6 Input Status change (if ICWE is enabled)
5. Comparator 1 or 2 output status change (if CMP1WE/CMP2WE is enabled)
6. A/D conversion completed (if ADWE is enabled)
7. SPI received data, when SPI acts as slave device (if SPIWE is enabled)
8. Port 5 / Port 7 input status change (if the corresponding control bits are enabled)

[3] **Note:** Vdd = 5V, set up time period = 16.8ms ± 8%
Vdd = 3V, set up time period = 18ms ± 8%

The first two cases will cause the EM78F568N/EM78F668N to reset. The T and P flags of R3 can be used to determine the source of the reset (wake-up). Cases 3, 4, 5, 6, 7 are considered the continuation of program execution and the global interrupt ("ENI" or "DISI" being executed) determines whether or not the controller branches to the interrupt vector following a wake-up. If ENI is executed before SLEP, the instruction will begin to execute from the Address 0×3, 0×6, 0×15, 0×30 after wake-up. If DISI is executed before SLEP, the execution will restart from the instruction right next to SLEP after wake-up. Case 8 has no interrupt. The wake-up time of all sleep mode is 150 μs, no matter what the oscillation mode is (except low Crystal mode). In low Crystal mode, the wake-up time is 500 ms.

Only one of Cases 2 to 6 can be enabled before entering into sleep mode. That is,

[a] If WDT is enabled before SLEP, the EM78F568N/EM78F668N can be waken-up only by Case 1 or 2. Refer to the section on Interrupt for further details.

[b] If External (P60,/INT) pin change is used to wake-up the EM78F568N/EM78F668N and the EXWE bit is enabled before SLEP, WDT must be disabled. Hence, the EM78F568N/EM78F668N can be waken-up only by Case 3.

[c] If Port 6 Input Status Change is used to wake-up the EM78F568N/EM78F668N and the corresponding wake-up setting is enabled before SLEP, WDT must be disabled. Hence, the EM78F568N/EM78F668N can be waken-up only by Case 4.

[d] If Comparator 1 or 2 output status change is used to wake-up the EM78F568N/EM78F668N and the CMP1WE/CMP2WE bit of Bank 0 R2F register is enabled before SLEP, WDT must be disabled by software. Hence, the EM78F568N/EM78F668N can be waken-up only by Case 5.

[e] If AD conversion completed is used to wake-up the EM78F568N/EM78F668N and the ADWE bit of Bank 0 R2F register is enabled before SLEP, WDT must be disabled by software. Hence, the EM78F568N/EM78F668N can be waken-up only by Case 6.

[f] When SPI act as slave device, after receiving data, it will wake-up the EM78F568N/EM78F668N and the SPIWE bit of Bank 0 R2F register is enabled before SLEP, WDT must be disabled by software. Hence, the EM78F568N/EM78F668N can be waken-up only by Case 7.

All kinds of wake-up mode and interrupt mode are shown below:

Wake-up Signal	Condition Signal	Sleep Mode		Idle Mode		Green Mode		Normal Mode	
		DISI	ENI	DISI	ENI	DISI	ENI	DISI	ENI
External INT	EXWE = 0, EXIE = 0	Wake-up is invalid		Wake-up is invalid		Interrupt is invalid		Interrupt is invalid	
	EXWE = 0, EXIE = 1	Wake-up is invalid		Wake-up is invalid		Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
	EXWE = 1, EXIE = 0	Wake up + Next Instruction		Wake up + Next Instruction		Interrupt is invalid		Interrupt is invalid	
	EXWE = 1, EXIE = 1	Wake up + Next Instruction	Wake up + Interrupt Vector	Wake up + Next Instruction	Wake up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
Port 6 Pin Change	ICWE = 0, ICIE = 0	Wake-up is invalid		Wake-up is invalid		Interrupt is invalid		Interrupt is invalid	
	ICWE = 0, ICIE = 1	Wake-up is invalid		Wake-up is invalid		Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
	ICWE = 1, ICIE = 0	Wake up + Next Instruction		Wake up + Next Instruction		Interrupt is invalid		Interrupt is invalid	
	ICWE = 1, ICIE = 1	Wake up + Next Instruction	Wake up + Interrupt Vector	Wake up + Next Instruction	Wake up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
TCC Overflow	TCIE = 0	Wake-up is invalid		Wake-up is invalid		Interrupt is invalid		Interrupt is invalid	
	TCIE = 1	Wake-up is invalid		Wake up + Next Instruction	Wake up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
SPI Interrupt	SPIWE = 0, SPIIE = 0	Wake-up is invalid		Wake-up is invalid		Interrupt is invalid		Interrupt is invalid	
	SPIWE = 0, SPIIE = 1	Wake-up is invalid		Wake-up is invalid		Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
	SPIWE = 1, SPIIE = 0	Wake up + Next Instruction (SPI must be in slave mode)		Wake up + Next Instruction (SPI must be in slave mode)		Interrupt is invalid		Interrupt is invalid	
	SPIWE = 1, SPIIE = 1	Wake up + Next Instruction (SPI must be in slave mode)	Wake up + Interrupt Vector (SPI must be in slave mode)	Wake up + Next Instruction (SPI must be in slave mode)	Wake up + Interrupt Vector (SPI must be in slave mode)	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector

Wake-up Signal	Condition Signal	Sleep Mode		Idle Mode		Green Mode		Normal Mode	
		DISI	ENI	DISI	ENI	DISI	ENI	DISI	ENI
Comparator x (Comparator Output Status Change) x=1,2	CMPxWE = 0, CMPxIE = 0	Wake-up is invalid		Wake-up is invalid		Interrupt is invalid		Interrupt is invalid	
	CMPxWE = 0, CMPxIE = 1	Wake-up is invalid		Wake-up is invalid		Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
	CMPxWE = 1, CMPxIE = 0	Wake up + Next Instruction		Wake up + Next Instruction		Interrupt is invalid		Interrupt is invalid	
	CMPxWE = 1, CMPxIE = 1	Wake up + Next Instruction	Wake up + Interrupt Vector	Wake up + Next Instruction	Wake up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
TC1 interrupt	TC1IE = 0	Wake-up is invalid		Wake-up is invalid.		Interrupt is invalid.		Interrupt is invalid	
	TC1IE = 1	Wake-up is invalid		Wake up + Next Instruction	Wake up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
UART Receive error interrupt	UTIE = 0	Wake-up is invalid		Wake-up is invalid		Interrupt is invalid		Interrupt is invalid	
	UTIE = 1	Wake-up is invalid		Wake-up is invalid		Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
TC2 interrupt	TC2IE = 0	Wake-up is invalid		Wake-up is invalid		Interrupt is invalid		Interrupt is invalid	
	TC2IE = 1	Wake-up is invalid		Wake up + Next Instruction	Wake up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
LVD	LVDWE = 0, CMPxIE = 0	Wake-up is invalid		Wake-up is invalid		Interrupt is invalid		Interrupt is invalid	
	LVDWE = 0, LVDIE = 1	Wake-up is invalid		Wake-up is invalid		Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
	LVDWE = 1, LVDIE = 0	Wake up + Next Instruction		Wake up + Next Instruction		Interrupt is invalid		Interrupt is invalid	
	LVDWE = 1, LVDIE = 1	Wake up + Next Instruction	Wake up + Interrupt Vector	Wake up + Next Instruction	Wake up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector

Wake-up Signal	Condition Signal	Sleep Mode		Idle Mode		Green Mode		Normal Mode	
		DISI	ENI	DISI	ENI	DISI	ENI	DISI	ENI
TC3 Interrupt	TC3IE = 0	Wake-up is invalid		Wake-up is invalid		Interrupt is invalid		Interrupt is invalid	
	TC3IE = 1	Wake-up is invalid		Wake up + Next Instruction	Wake up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
PWM A/B (When TimerA/B Match PRDA/B)	PWMxIE = 0 (x = A or B)	Wake-up is invalid		wake-up is invalid		Interrupt is invalid		Interrupt is invalid	
	PWMxIE = 1 (x = A or B)	Wake-up is invalid		Wake up + Next Instruction	Wake up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
I2C TX Interrupt	I2CTIE = 0	Wake-up is invalid		Wake-up is invalid		Interrupt is invalid		Interrupt is invalid	
	I2CTIE = 1	Wake-up is invalid		Wake-up is invalid		Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
I2C RX Interrupt	I2CRIE = 0	Wake-up if received correct address		Wake-up if received correct address		Interrupt is invalid		Interrupt is invalid	
	I2CRIE = 1	Wake-up if received correct address		Wake-up if received correct address		Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
I2C STOP Interrupt	I2CSTPIE = 0	Wake-up is invalid		Wake-up is invalid		Interrupt is invalid		Interrupt is invalid	
	I2CSTPIE = 1	Wake-up is invalid		Wake-up is invalid		Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector

After wake up:

1. If interrupt is enabled → interrupt+ next instruction
2. If interrupt is disabled → next instruction

Table 6-3 Summary of the Registers Initial Values

Addr.	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0×00	R0 (IAR)	Bit Name	-	-	-	-	-	-	-	-
		Power-on	U	U	U	U	U	U	U	U
		/RESET & WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×01	R1 (BSR)	Bit Name	0	0	0	SBS0	0	0	0	GBS0
		Power-on	0	0	0	U	0	0	0	U
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	0	0	0	P	0	0	0	P
0×02	R2 (PC)	Bit Name	-	-	-	-	-	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×03	R3 (SR)	Bit Name	0	0	0	T	P	Z	DC	C
		Power-on	0	0	0	1	1	U	U	U
		/RESET & WDT	0	0	0	t	t	P	P	P
		Wake-up from Pin Change	0	0	0	t	t	P	P	P
0×04	R4 (RSR)	Bit Name	RSR7	RSR6	RSR5	RSR4	RSR3	RSR2	RSR1	RSR0
		Power-on	U	U	U	U	U	U	U	U
		/RESET & WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×05	Bank 0, R5 (Port 5)	Bit Name	P57	P56	P55	P54	P53	P52	P51	P50
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×06	Bank 0, R6 (Port 6)	Bit Name	P67	P66	P65	P64	P63	P62	P61	P60
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×07	Bank 0, R7 (Port 7)	Bit Name	P77	P76	P75	P74	P73	P72	P71	P70
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×08	Bank 0, R8 (Port 8)	Bit Name	P87	P86	P85	P84	P83	P82	P81	P80
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×09	Bank 0, R9 (Port 9)	Bit Name	P97	P96	P95	P94	P93	P92	P91	P90
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P

Addr.	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0×0B	Bank 0, RB (OMCR)	Bit Name	CPUS	IDLE	TC1SS	TC2SS	TC3SS	TASS	TBSS	0
		Power-on	1	1	0	0	0	0	0	0
		/RESET & WDT	1	1	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	0
0×0C	Bank 0, RC (ISR1)	Bit Name	LVDIF	ADIF	SPIF	PWMBIF	PWMAIF	EXIF	ICIF	TCIF
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0D	Bank 0, RD (ISR2)	Bit Name	CMP2IF	CMP1IF	TC3IF	TC2IF	TC1IF	UERRIF	RBFF	TBEF
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0E	Bank 0, RE (ISR3)	Bit Name	0	0	0	0	I2CSTPIF	0	I2CRIF	I2CTIF
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	0	0	0	0	P	0	P	P
0×10	Bank 0, R10 EIESCR	Bit Name	0	0	0	0	0	0	0	EIES
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	0	0	0	0	0	0	0	P
0×11	Bank 0, R11 WDTCR	Bit Name	WDTE	EIS	INT	0	PSWE	PSW2	PSW1	PSW0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	0	P	P	P	P
0×12	Bank 0, R12 LVDCR	Bit Name	0	0	0	0	LVDEN	/LVD	LVD1	LVD0
		Power-on	0	0	0	0	0	R	0	0
		/RESET and WDT	0	0	0	0	0	R	0	0
		Wake-up from Pin Change	0	0	0	0	P	R	P	P
0×13	Bank 0, R13 TCCCR	Bit Name	0	TCCS	TS	TE	PSTE	PST2	PST1	PST0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	0	P	P	P	P	P	P	P

Addr.	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0×14	Bank 0, R14 TCCDATA	Bit Name	-	-	-	-	-	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×15	Bank 0, R15 IOCR5	Bit Name	IOC57	IOC56	IOC55	IOC54	IOC53	IOC52	IOC51	IOC50
		Power-on	1	1	1	1	1	1	1	1
		/RESET & WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×16	Bank 0, R16 IOCR6	Bit Name	IOC67	IOC66	IOC65	IOC64	IOC63	IOC62	IOC61	IOC60
		Power-on	1	1	1	1	1	1	1	1
		/RESET & WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×17	Bank 0, R17 IOCR7	Bit Name	IOC77	IOC76	IOC75	IOC74	IOC73	IOC72	IOC71	IOC70
		Power-on	1	1	1	1	1	1	1	1
		/RESET & WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×18	Bank 0, R18 IOCR8	Bit Name	IOC87	IOC86	IOC85	IOC84	IOC83	IOC82	IOC81	IOC80
		Power-on	1	1	1	1	1	1	1	1
		/RESET & WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×19	Bank 0, R19 IOCR9	Bit Name	IOC97	IOC96	IOC95	IOC94	IOC93	IOC92	IOC91	IOC90
		Power-on	1	1	1	1	1	1	1	1
		/RESET & WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×1C	Bank 0, R1C IMR1	Bit Name	LVDIE	ADIE	SPIE	PWMBIE	PWMAIE	EXIE	ICIE	TCIE
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×1D	Bank 0, R1D IMR2	Bit Name	CMP2IE	CMP1IE	TC3IE	TC2IE	TC1IE	UERRIE	URIE	UTIE
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×1E	Bank 0, R1E IMR3	Bit Name	0	0	0	0	I2CSTPIE	0	I2CRIE	I2CTIE
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P

Addr.	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0×20	Bank 0, R20 P5WUCR	Bit Name	WU_P57	WU_P56	WU_P55	WU_P54	WU_P53	WU_P52	WU_P51	WU_P50
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×21	Bank 0, R21 P5WUECR	Bit Name	WUE_P57	WUE_P56	WUE_P55	WUE_P54	WUE_P53	WUE_P52	WUE_P51	WUE_P50
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×22	Bank 0, R22 P7WUCR	Bit Name	WU_P77	WU_P76	WU_P75	WU_P74	WU_P73	WU_P72	WU_P71	WU_P70
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×23	Bank 0, R23 P7WUECR	Bit Name	WUE_P77	WUE_P76	WUE_P75	WUE_P74	WUE_P73	WUE_P72	WUE_P71	WUE_P70
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×24	BANK 0, R24 ADCR1	Bit Name	VREFS	ADRUN	ADPD	0	0	ADIS2	ADIS1	ADIS0
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	0	0	P	P	P
0×25	Bank 0, R25 ADCR2	Bit Name	CALI	SIGN	VOF2	VOF1	VOF0	CKR2	CKR1	CKR0
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×26	Bank 0, R26 ADICL	Bit Name	ADE7	ADE6	ADE5	ADE4	ADE3	ADE2	ADE1	ADE0
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×29	Bank 0, R29 ADDH	Bit Name	AD11	AD10	AD9	AD8	AD7	AD6	AD5	AD4
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×2A	Bank 0, R2A ADDL	Bit Name	0	0	0	0	AD3	AD2	AD1	AD0
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	0	0	0	0	P	P	P	P

Addr.	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0×2B	Bank 0, R2B SPICR	Bit Name	CES	SPIE	SRO	SSE	SDOC	SBRS2	SBRS1	SBRS0
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×2C	Bank 0, R2C SPIS	Bit Name	DORD	TD1	TD0	0	OD3	OD4	0	RBF
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	0	P	P	0	P
0×2D	Bank 0, R2D SPIR	Bit Name	SRB7	SRB6	SRB5	SRB4	SRB3	SRB2	SRB1	SRB0
		Power-on	U	U	U	U	U	U	U	U
		/RESET & WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×2E	Bank 0, R2E SPIW	Bit Name	SWB7	SWB6	SWB5	SWB4	SWB3	SWB2	SWB1	SWB0
		Power-on	U	U	U	U	U	U	U	U
		/RESET & WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×2F	Bank 0, R2F WUCR1	Bit Name	0	SPIWE	LVDWE	ICWE	ADWE	CMP2WE	CMP1WE	EXWE
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	0	P	P	P	P	P	P	P
0×32	Bank 0, R32 URCR1	Bit Name	URTD8	UMODE1	UMODE0	BRATE2	BRATE1	BRATE0	UTBE	TXE
		Power-on	U	0	0	0	0	0	1	0
		/RESET & WDT	P	0	0	0	0	0	1	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×33	Bank 0, R33 URCR2	Bit Name	0	0	SBIM1	SBIM0	UINVEN	0	0	0
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	0	0	P	P	P	0	0	0
0×34	Bank 0, R34 URS	Bit Name	URRD8	EVEN	PRE	PRERR	OVERR	FMERR	URBF	RXE
		Power-on	U	0	0	0	0	0	0	0
		/RESET & WDT	P	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×35	Bank 0, R35 URRD	Bit Name	URRD7	URRD6	URRD5	URRD4	URRD3	URRD2	URRD1	URRD0
		Power-on	U	U	U	U	U	U	U	U
		/RESET & WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×36	Bank 0, R36 URTD	Bit Name	URTD7	URTD6	URTD5	URTD4	URTD3	URTD2	URTD1	URTD0
		Power-on	U	U	U	U	U	U	U	U
		/RESET & WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×37	Bank 0, R37 TBPTL	Bit Name	TB7	TB6	TB5	TB4	TB3	TB2	TB1	TB0
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P

Addr.	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0×38	Bank 0, R38 TBPTH	Bit Name	HLB	GP1	GP0	TB12	TB11	TB10	TB9	TB8
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×39	Bank 0, R39 CMP1CR	Bit Name	C1RS	CP1OUT	CMP1COS1	CMP1COS0	CP1NS	CP1PS	CP1NRE	CP1NRDT
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×3C	Bank 0, R3C CMP2CR	Bit Name	C2RS	CP2OUT	CMP2COS1	CMP2COS0	CP2NS	CP2PS	CP2NRE	CP2NRDT
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×43	Bank 0, R43 CPIRLCON	Bit Name	BG2OUT	C2IRL2	C2IRL1	C2IRL0	BG1OUT	C1IRL2	C1IRL1	C1IRL0
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×48	Bank 0, R48 TC1CR	Bit Name	TC1CAP	TC1S	TC1CK1	TC1CK0	TC1M	TC1ES	0	0
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	0	0
0×49	Bank 0, R49 TCR1DA	Bit Name	TCR1DA7	TCR1DA6	TCR1DA5	TCR1DA4	TCR1DA3	TCR1DA2	TCR1DA1	TCR1DA0
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×4A	Bank 0, R4A TCR1DB	Bit Name	TCR1DB7	TCR1DB6	TCR1DB5	TCR1DB4	TCR1DB3	TCR1DB2	TCR1DB1	TCR1DB0
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×4B	Bank 0, R4B T2CR	Bit Name	0	0	TC2ES	TC2M	TC2S	TC2CK2	TC2CK1	TC2CK0
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	0	0	P	P	P	P	P	P
0×4C	Bank 0, R4C TCR2DH	Bit Name	TCR2D15	TCR2D14	TCR2D13	TCR2D12	TCR2D11	TCR2D10	TCR2D9	TCR2D8
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×4D	Bank 0, R4D TCR2DL	Bit Name	TCR2D7	TCR2D6	TCR2D5	TCR2D4	TCR2D3	TCR2D2	TCR2D1	TCR2D0
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×4E	Bank 0, R4E TC3CR	Bit Name	TC3FF1	TC3FF0	TC3S	TC3CK2	TC3CK1	TC3CK0	TC3M1	TC3M0
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P

Addr.	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0×4F	Bank 0, R4F TC3RD	Bit Name	TCR3D7	TCR3D6	TCR3D5	TCR3D4	TCR3D3	TCR3D2	TCR3D1	TCR3D0
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×05	Bank 1, R5 P5PHCR	Bit Name	/PH57	/PH56	/PH55	/PH54	/PH53	/PH52	/PH51	/PH50
		Power-on	1	1	1	1	1	1	1	1
		/RESET & WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×06	Bank 1, R6 P6PHCR	Bit Name	/PH67	/PH66	/PH65	/PH64	/PH63	/PH62	/PH61	/PH60
		Power-on	1	1	1	1	1	1	1	1
		/RESET & WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×07	Bank 1, R7 P7PHCR	Bit Name	/PH77	/PH76	/PH75	/PH74	/PH73	/PH72	/PH71	/PH70
		Power-on	1	1	1	1	1	1	1	1
		/RESET & WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×08	Bank 1, R8 P8PHCR	Bit Name	/PH87	/PH86	/PH85	/PH84	/PH83	/PH82	/PH81	/PH80
		Power-on	1	1	1	1	1	1	1	1
		/RESET & WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×09	Bank 1, R9 P9PHCR	Bit Name	/PH97	/PH96	/PH95	/PH94	/PH93	/PH92	/PH91	/PH90
		Power-on	1	1	1	1	1	1	1	1
		/RESET & WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0B	Bank 1, RB P5PLCR	Bit Name	/PL57	/PL56	/PL55	/PL54	/PL53	/PL52	/PL51	/PL50
		Power-on	1	1	1	1	1	1	1	1
		/RESET & WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0C	Bank 1, RC P6PLCR	Bit Name	/PL67	/PL66	/PL65	/PL64	/PL63	/PL62	/PL61	/PL60
		Power-on	1	1	1	1	1	1	1	1
		/RESET & WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0D	Bank 1, RD P7PLCR	Bit Name	/PL77	/PL76	/PL75	/PL74	/PL73	/PL72	/PL71	/PL70
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0E	Bank 1, RE P8PLCR	Bit Name	/PL87	/PL86	/PL85	/PL84	/PL83	/PL82	/PL81	/PL80
		Power-on	1	1	1	1	1	1	1	1
		/RESET & WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0F	Bank 1, RF P9PLCR	Bit Name	/PL97	/PL96	/PL95	/PL94	/PL93	/PL92	/PL91	/PL90
		Power-on	1	1	1	1	1	1	1	1
		/RESET & WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P

Addr.	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0×11	Bank 1, R11 P5HD/SCR	Bit Name	/H57	/H56	/H55	/H54	/H53	/H52	/H51	/H50
		Power-on	1	1	1	1	1	1	1	1
		/RESET & WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×12	Bank 1, R12 P6HD/SCR	Bit Name	/H67	/H66	/H65	/H64	/H63	/H62	/H61	/H60
		Power-on	1	1	1	1	1	1	1	1
		/RESET & WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×13	Bank 1, R13 P7HD/SCR	Bit Name	/H77	/H76	/H75	/H74	/H73	/H72	/H71	/H70
		Power-on	1	1	1	1	1	1	1	1
		/RESET & WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×14	Bank 1, R14 P8HD/SCR	Bit Name	/H87	/H86	/H85	/H84	/H83	/H82	/H81	/H80
		Power-on	1	1	1	1	1	1	1	1
		/RESET & WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×15	Bank 1, R15 P9HD/SCR	Bit Name	/H97	/H96	/H95	/H94	/H93	/H92	/H91	/H90
		Power-on	1	1	1	1	1	1	1	1
		/RESET & WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×17	Bank 1, R17 P5ODCR	Bit Name	OD57	OD56	OD55	OD54	OD53	OD52	OD51	OD50
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×18	Bank 1, R18 P6ODCR	Bit Name	OD67	OD66	OD65	OD64	OD63	OD62	OD61	OD60
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×19	Bank 1, R19 P7ODCR	Bit Name	OD77	OD76	OD75	OD74	OD73	OD72	OD71	OD70
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×1A	Bank 1, R1A P8ODCR	Bit Name	OD87	OD86	OD85	OD84	OD83	OD82	OD81	OD80
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×1B	Bank 1, R1B P9ODCR	Bit Name	OD97	OD96	OD95	OD94	OD93	OD92	OD91	OD90
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×1D	Bank 1, R1D IRCS	Bit Name	0	0	RCM1	RCM0	0	0	0	0
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P

Addr.	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0×1F	Bank 1, R1F EEPROM CONTROL	Bit Name	RD	WR	EEWE	EEDF	EEPC	0	0	0
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	0	0	0
0×20	Bank 1, R20 EEPROM ADDR	Bit Name	EERA7	EERA6	EERA5	EERA4	EERA3	EERA2	EERA1	EERA0
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×21	Bank 1, R21 EEPROM DATA	Bit Name	EERD7	EERD6	EERD5	EERD4	EERD3	EERD2	EERD1	EERD0
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×23	Bank 1, R23 I2CCR1	Bit Name	Strobe/ Pend	IMS	ISS	STOP	SAR_ EMPTY	ACK	FULL	EMPTY
		Power-on	0	0	0	0	U	U	U	U
		/RESET & WDT	0	0	0	0	U	U	U	U
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×24	Bank 1, R24 I2CCR2	Bit Name	I2CBF	GCEN	0	0	I2CTS1	I2CTS0	0	I2CEN
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	0	0	0	0	P	P	0	P
0×25	Bank 1, R25 I2CSA	Bit Name	SA6	SA5	SA4	SA3	SA2	SA1	SA0	IRW
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×26	Bank 1, R26 I2CDA	Bit Name	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×27	Bank 1, R27 I2CDB	Bit Name	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
		Power-on	0	0	0	0	0	0	0	0
		/RESET &WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×28	Bank 1, R28 I2CA	Bit Name	0	0	0	0	0	0	DA9	DA8
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	0	0	0	0	0	0	P	P
0×2A	Bank 1, R2A PWMER	Bit Name	0	0	0	0	0	0	PWMBE	PWMAE
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	0	0	0	0	0	0	P	P

Addr.	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0×2B	Bank 1, R2B TIMEN	Bit Name	0	0	0	0	0	0	TBEN	TAEN
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	0	0	0	0	0	0	P	P
0×2F	Bank 1, R2F PWMACR	Bit Name	0	0	0	0	TRCBA	0	0	0
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	0	0	0	0	P	0	0	0
0×30	Bank 1, R30 PWMBCR	Bit Name	0	0	0	0	TRCBB	0	0	0
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	0	0	0	0	P	0	0	0
0×32	Bank 1, R32 TACR	Bit Name	0	0	0	0	0	TAP2	TAP1	TAP0
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	0	0	0	0	0	P	P	P
0×33	Bank 1, R33 TBCR	Bit Name	0	0	0	0	0	TBP2	TBP1	TBP0
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	0	0	0	0	0	P	P	P
0×35	Bank 1, R35 TAPRDH	Bit Name	PRDA[9]	PRDA[8]	PRDA[7]	PRDA[6]	PRDA[5]	PRDA[4]	PRDA[3]	PRDA[2]
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×36	Bank 1, R36 TBPRDH	Bit Name	PRDB[9]	PRDB[8]	PRDB[7]	PRDB[6]	PRDB[5]	PRDB[4]	PRDB[3]	PRDB[2]
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×38	Bank 1, R38 TADTH	Bit Name	DTA[9]	DTA[8]	DTA[7]	DTA[6]	DTA[5]	DTA[4]	DTA[3]	DTA[2]
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×39	Bank 1, R39 TBDTH	Bit Name	DTB[9]	DTB[8]	DTB[7]	DTB[6]	DTB[5]	DTB[4]	DTB[3]	DTB[2]
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×3B	BANK 1, R3B PRDxL	Bit Name	0	0	0	0	PRDB[1]	PRDB[0]	PRDA[1]	PRDA[0]
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	0	0	0	0	P	P	P	P
0×3C	Bank 1, R3C DTxL	Bit Name	0	0	0	0	DTB[1]	DTB[0]	DTA[1]	DTA[0]
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	0	0	0	0	P	P	P	P

U : Unknown or don't care **P :** Previous value before reset **t :** Check Table 6-4

6.10.2 Status of RST, T, and P of the Status Register

A reset condition is initiated by the following events:

1. Power-on condition,
2. High-low-high pulse on the /RESET pin, and
3. Watchdog timer time-out.

The values of T and P, listed in Table 6-5 are used to check how the processor wakes up. Table 6-4 shows the events that may affect the status of T and P.

Table 6-4 Values of RST, T and P after Reset

Reset Type	T	P
Power on	1	1
/RESET during Operating mode	*P	*P
/RESET wake-up during Sleep mode	1	0
WDT during Operating mode	0	*P
WDT wake-up during Sleep mode	0	0
Wake-up on pin change during Sleep mode	1	0

*P: Previous status before reset

Table 6-5 Status of T and P Being Affected by Events

Event	T	P
Power on	1	1
WDTC instruction	1	1
WDT time-out	0	*P
SLEP instruction	1	0
Wake-up on pin change during Sleep mode	1	0

*P: Previous value before reset

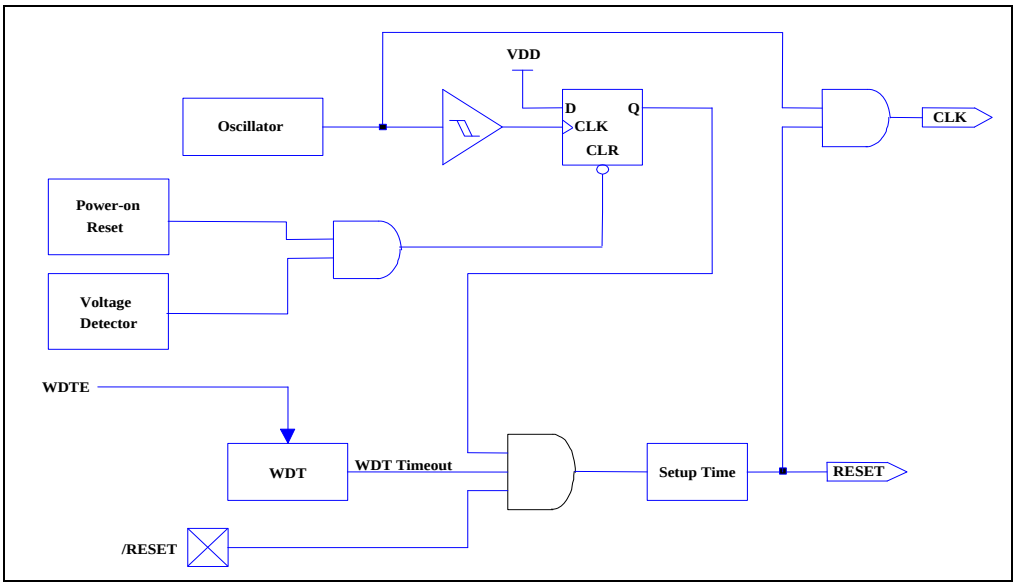


Figure 6-38 Block Diagram of Controller Reset

6.11 Interrupt

The EM78F568N/EM78F668N has 19 interrupts (4 external, 15 internal) listed below:

Interrupt Source		Enable Condition	Int. Flag	Int. Vector	Priority
Internal / External	Reset	-	-	0000	High 0
External	INT	ENI + EXIE=1	EXIF	0003	1
External	Port 6 pin change	ENI +ICIE=1	ICIF	0006	2
Internal	TCC	ENI + TCIE=1	TCIF	0009	3
Internal	LVD	ENI+LVDEN & LVDIE=1	LVDIF	000C	4
External	Comparator 1	ENI+CMP1IE=1	CMP1IF	000F	5
Internal	SPI	ENI + SPIIE=1	SPIIF	0012	6
External	Comparator 2	ENI+CMP2IE=1	CMP2IF	0015	7
Internal	TC1	ENI + TC1IE=1	TC1IF	0018	8
Internal	UART Transmit	ENI + UTIE=1	TBEF	001B	9
Internal	UART Receive	ENI + URIE=1	RBFF	001E	10
Internal	UART Receive error	ENI+UERRIE=1	UERRIF	0021	11
Internal	TC2	ENI + TC2IE=1	TC2IF	0024	12
Internal	TC3	ENI + TC3IE=1	TC3IF	0027	13
Internal	PWMA	ENI+PWMAIE=1	PWMAIF	002A	14
Internal	PWMB	ENI+PWMBIE=1	PWMBIF	002D	15
Internal	AD	ENI + ADIE=1	ADIF	0030	16
Internal	I2C Transmit	ENI+ I2CTIE	I2CTIF	0036	17
Internal	I2C Receive	ENI+ I2CRIE	I2CRIF	0039	18
Internal	I2C Stop	ENI+ I2CSTPIE	I2CSTPIF	003F	19

Bank 0 RC~RF are the interrupt status registers that record the interrupt requests in the relative flags/bits. Bank 0 R1C~R1F is the interrupt mask register. The global interrupt is enabled by the ENI instruction and is disabled by the DISI instruction. When one of the interrupts (enabled) occurs, the next instruction will be fetched from their individual address. The interrupt flag bit must be cleared by instructions before leaving the interrupt service routine and before interrupts are enabled to avoid recursive interrupts.

The flag (except for ICIF bit which is deleted) in the Interrupt Status Register is set regardless of the status of its mask bit or the execution of ENI. The RETI instruction ends the interrupt routine and enables the global interrupt (the execution of ENI).

External interrupt equipped with digital noise rejection circuit (input pulse less than **8 system clock time** is eliminated as noise), **but in Low XTAL oscillator (LXT) mode the noise rejection circuit will be disabled.** When an interrupt (Falling edge) is generated by the External interrupt (when enabled), the next instruction will be fetched from Address 003H.

Before the interrupt subroutine is executed, the contents of ACC and the R3 and R4 register will be saved by hardware. If another interrupt occurs, the ACC, R3 and R4 will be replaced by the new interrupt. After the interrupt service routine is finished, ACC,R3 and R4 will be pushed back.

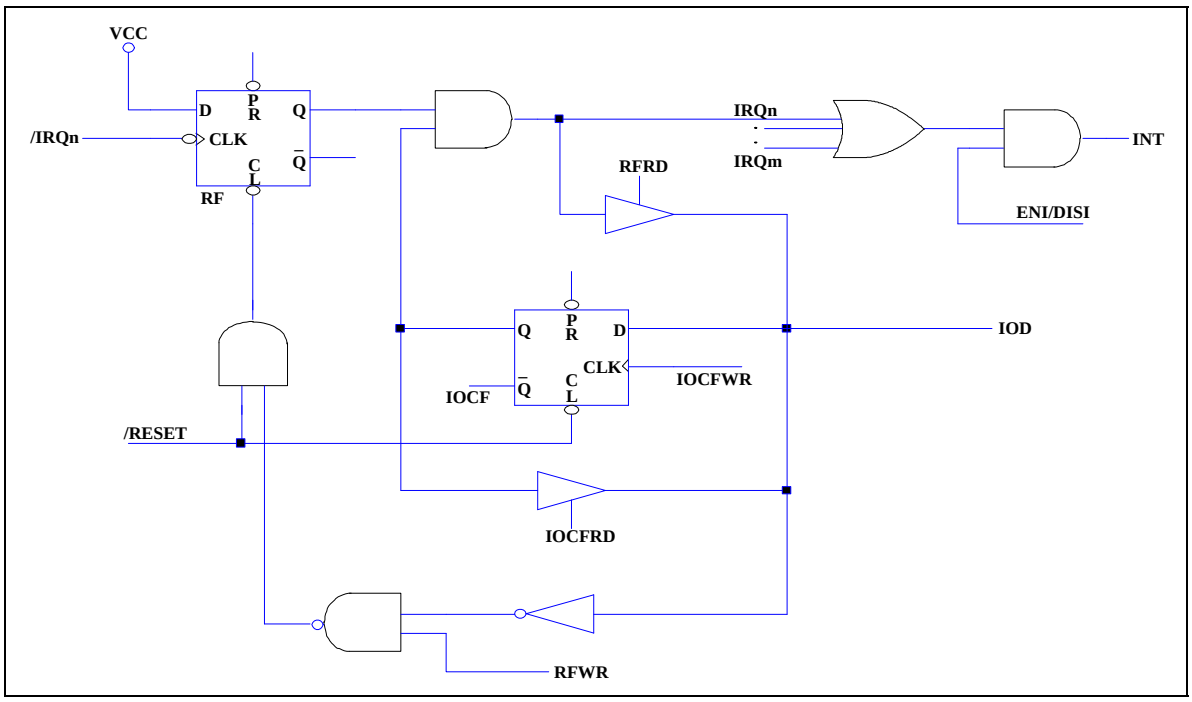


Figure 6-39 Interrupt Input Circuit

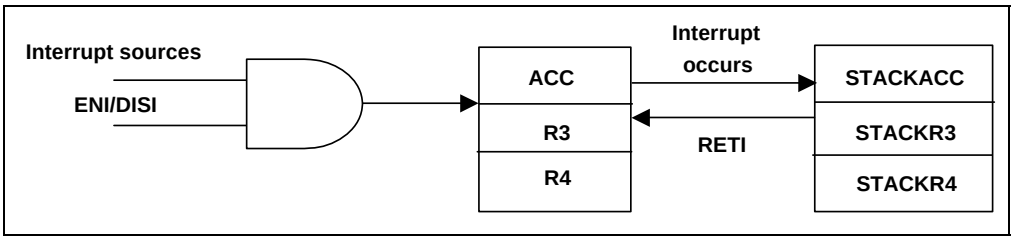


Figure 6-40 Interrupt Backup Diagram

6.12 LVD (Low Voltage Detector)

During power source unstable situation, like external power noise interference or EMS test condition…, situations like such will cause the power to vibrate fiercely. At the time Vdd is unsettled, the voltage may be below the working voltage. When system voltage, Vdd, is below the working voltage, the IC kernel must keep all register status automatically.

LVD property is set at Bank 0 R12, Bits 1, 0. Detailed operation mode is as follows:

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	LVDEN	/LVD	LVD1	LVD0

Bit 1 ~ Bit 0 (LVD1 ~ LVD0): Low Voltage Detect Level Control Bits.

The LVD status and interrupt flag is referred to in Bank 0 RC.

"**1**" means with interrupt request, and "**0**" means no interrupt occurs.

Bit 7 (LVDIF): Low Voltage Detector Interrupt flag.

When LVD1, LVD0 = “0, 0”, Vdd > 2.2V, LVDIF is “0”, Vdd ≤ 2.2V, set LVDIF to “1”. LVDIF is reset to “0” by software.

When LVD1, LVD0 = “0, 1”, Vdd > 3.3V, LVDIF is “0”, Vdd ≤ 3.3V, set LVDIF to “1”. LVDIF is reset to “0” by software.

When LVD1, LVD0 = “1, 0”, Vdd > 4.0V, LVDIF is “0”, Vdd ≤ 4.0V, set LVDIF to “1”. LVDIF is reset to “0” by software.

When LVD1, LVD0 = “1, 1”, Vdd > 4.5V, LVDIF is “0”, Vdd ≤ 4.5V, set LVDIF to “1”. LVDIF is reset to “0” by software.

The following steps are needed to setup the LVD function:

1. Set the LVDEN to “1”, then use Bits 1, 0 (LVD1, LVD0) of Register RB to set the LVD interrupt level
2. Wait for LVD interrupt to occur.
3. Clear the LVD interrupt flag

The internal LVD module uses an internal circuit to fit when you set the LVDEN to enable the LVD module. The current consumption will increase by about 10 μA.

During sleep mode, the LVD module continues to operate. If the device voltage drops slowly and crosses the detect point, the LVDIF bit will be set and the device will not wake-up from Sleep mode. Until the other wake-up source wakes-up the EM78F568N/EM78F668N, the LVD interrupt flag is still set at the prior status.

When the system resets, the LVD flag will be cleared.

Figure 6-41 shows the LVD module that detects the external voltage situation.

When Vdd drops to not below V_{LVD}, LVDIF is kept at “0”.

When Vdd drops below V_{LVD}, LVDIF is set to “1”. If global ENI is enabled, LVDIF will be set to “1”, the next instruction will branched to an interrupt vector. The LVD interrupt flag is cleared to “0” by software.

When Vdd drops below V_{RESET} and is less than 80 μs, the system will keep all the register status and the system halts but oscillation is active. When Vdd drops below V_{RESET} and is more than 80 μs, system Reset will occur.

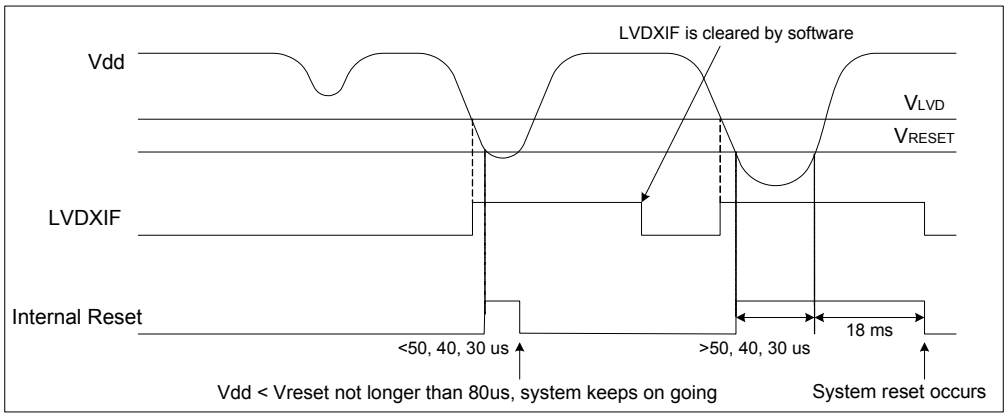


Figure 6-41 LVD Waveform

6.13 Data EEPROM

The Data EEPROM is readable and writable during normal operation for the whole Vdd range. The operation for Data EEPROM is base on a single byte. A write operation makes an erase-then-write cycle to take place on the allocated byte.

The Data EEPROM memory provided high erase and write cycles. A byte write automatically erases the location and write the new value.

6.13.1 Data EEPROM Control Register

6.13.1.1 Bank 1 R1F (EEPROM Control)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RD	WR	EEWE	EEDF	EEPC	0	0	0

Bit 7 (RD): Read control bit

0: do not execute EEPROM read

1: read EEPROM content (RD can be set by software. When read instruction is completed, RD will be cleared by hardware.)

Bit 6 (WR): Write control bit

0: write cycle to the EEPROM is completed.

1: initiate a write cycle (WR can be set by software. When write cycle is completed, WR will be cleared by hardware.)

Bit 5 (EEWE): EEPROM write enable bit

0: Prohibit write to the EEPROM

1: allow EEPROM write cycles

Bit 4 (EEDF): EEPROM detected flag

0: write cycle is completed

1: write cycle is unfinished

Bit 3 (EEPC): EEPROM power down control bit

0: switch of EEPROM

1: EEPROM is operating

Bits 2 ~ 0: unused bit, set to 0 all the time

6.13.1.2 Bank 1 R20 (256 Bytes EEPROM Address)

When accessing the EEPROM data memory, the Bank 1 R20 (256 bytes EEPROM address register) holds the address to be accessed. In accordance with the operation, Bank 1 R21 (256 bytes EEPROM Data register) holds the data to be written, or the data read, at the address in Bank 1 R20.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EERA7	EERA6	EERA5	EERA4	EERA3	EERA2	EERA1	EERA0

Bits 7 ~ 0 (EERA7 ~ EERA0): EEPROM address register

6.13.1.3 Bank 1 R21 (256 Bytes EEPROM Data)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EERD7	EERD6	EERD5	EERD4	EERD3	EERD2	EERD1	EERD0

Bits 7 ~ 0 (EERD7 ~ EERD0): EEPROM data register. Read only.

6.13.1.4 Programming Steps/Example Demonstration

The following are steps to write or read data from the EEPROM:

1) Set the **EEPC** bit of Bank 1 R1F to 1 for enable the EEPROM power.

2) Write the address to EERA8~EERA0 (512 bytes EEPROM address).

3) a.1. Set the **EEWE** bit to 1, if the write function is employed.

a.2. Write the 8-bit data value to be programmed in Bank 1 R21 (256 bytes EEPROM data).

a.3. Set the **WR** bit to 1, then execute write function.

b. Set the **RD** bit to 1, then execute read function.

4) a. Wait for the **EEDF** or **WR** to be cleared.

b. Wait for the **EEDF** to be cleared.

5) For the next conversion, go to Step 2 as required.

6) If user wants to save power and make sure the EEPROM data is not used, clear the **EEPC**.

6.14 Oscillator

6.14.1 Oscillator Modes

The EM78F568N/EM78F668N can be operated in the four different oscillator modes, such as Internal RC oscillator mode (IRC), External RC oscillator mode (ERC), High XTAL oscillator mode (HXT), and Low XTAL oscillator mode (LXT). User can select one of them by programming OSC2, OCS1 and OSC0 in the Code Option register. Table 6-6 depicts how these four modes are defined.

The up-limited operation frequency of the crystal/resonator on the different VDD is listed in Table 6-6.

Table 6-6 Oscillator Modes defined by OSC2 ~ OSC0

XT (XTAL oscillator mode)	0	0	0
HXT (High XTAL oscillator mode)	0	0	1
LXT1 (Low XTAL1 oscillator mode)	0	1	0
LXT2 (Low XTAL2 oscillator mode)	0	1	1
IRC mode, OSCO (P54) act as I/O pin	1	0	0
IRC mode, OSCO (P54) act as RCOUT pin	1	0	1
ERC mode, OSCO (P54) act as I/O pin	1	1	0
ERC mode, OSCO (P54) act as RCOUT pin	1	1	1

In LXT1, LXT2, XT, HXT and ERC mode OSCI and OSCO are used, but cannot be used as normal I/O pin.

In IRC mode, P55 is normal I/O pin.

<**Note**>:1. Frequency range of HXT mode is 20 MHz ~ 6 MHz.

2. Frequency range of XT mode is 6 MHz ~ 1 MHz.

3. Frequency range of LXT1 mode is 1 MHz ~ 100kHz.

4. Frequency range of XT mode is 32kHz.

Table 6-7 Summary of the Maximum Operating Speeds

Conditions	VDD	Max. Fxt. (MHz)
Two cycles with two clocks	2.4	4.0
	3.0	8.0
	5.0	20.0

6.14.2 Crystal Oscillator/Ceramic Resonators (XTAL)

EM78F568N/EM78F668N can be driven by an external clock signal through the OSCI pin as shown in Figure 6-42 below.

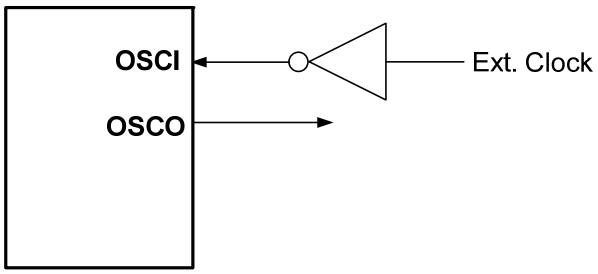


Figure 6-42 External Clock Input Circuit

In most applications, pin OSCI and pin OSCO can be connected with a crystal or ceramic resonator to generate oscillation. Figure 6-43 depicts such a circuit. The same thing applies whether it is in the HXT mode or in the LXT mode. Table 6-8 provides the recommended values of C1 and C2. Since each resonator has its own attribute, user should refer to its specification for appropriate values of C1 and C2. RS, a serial resistor, may be necessary for AT strip cut crystal or low frequency mode.

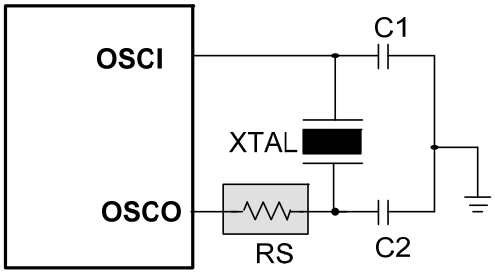


Figure 6-43 Crystal/Resonator Circuit

Table 6-8 Capacitor Selection Guide for Crystal Oscillator or Ceramic Resonator

Oscillator Type	Frequency Mode	Frequency	C1 (pF)	C2 (pF)
Ceramic Resonators	HXT	455kHz	100~150	100~150
		2.0 MHz	20~40	20~40
		4.0 MHz	10~30	10~30
Crystal Oscillator	LXT	32.768kHz	25	15
		100kHz	25	25
		200kHz	25	25
	HXT	455kHz	20~40	20~150
		1.0 MHz	15~30	15~30
		2.0 MHz	15	15
		4.0 MHz	15	15

6.14.3 External RC Oscillator Mode

For some applications that do not need a very precise timing calculation, the RC oscillator (Figure 6-44) offers a lot of cost savings. Nevertheless, it should be noted that the frequency of the RC oscillator is influenced by the supply voltage, the values of the resistor (Rext), the capacitor (Cext), and even by the operation temperature. Moreover, the frequency also changes slightly from one chip to another due to manufacturing process variations.

In order to maintain a stable system frequency, the values of the Cext should not be lesser than 20pF, and that the value of Rext should not be greater than 1 MΩ. If they cannot be kept in this range, the frequency is easily affected by noise, humidity, and leakage.

The smaller the Rext in the RC oscillator, the faster its frequency will be. On the contrary, for very low Rext values, for instance, 1 KΩ, the oscillator becomes unstable because the NMOS cannot discharge the current of the capacitance correctly.

Based on the above reasons, it must be kept in mind that all of the supply voltage, the operation temperature, the components of the RC oscillator, the package types, the way the PCB is layout, will affect the system frequency.

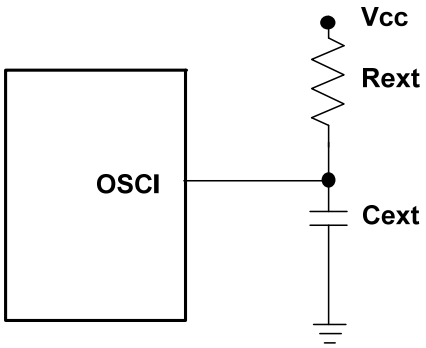


Figure 6-44 Circuit for External RC Oscillator Mode

Table 6-9 RC Oscillator Frequencies

Cext	Rext	Average Fosc 5V, 25°C	Average Fosc 3V, 25°C
20 pF	3.3k	3.5 MHz	3.2 MHz
	5.1k	2.5 MHz	2.3 MHz
	10k	1.30 MHz	1.25 MHz
	100k	140kHz	140kHz
100 pF	3.3k	1.27 MHz	1.21 MHz
	5.1k	850kHz	820kHz
	10k	450kHz	450kHz
	100k	48kHz	50kHz
300 pF	3.3k	560kHz	540kHz
	5.1k	370kHz	360kHz
	10k	196kHz	192kHz
	100k	20kHz	20kHz

Note: 1. *Measured in DIP packages.*
2. *The values are for design reference only.*

6.14.4 Internal RC Oscillator Mode

The EM78F568N/EM78F668N offers a versatile internal RC mode with default frequency value of 4 MHz. Internal RC oscillator mode has other frequencies (16 MHz, 8 MHz and 455kHz) that can be set by Code Option: RCM1 and RCM0. All these four main frequencies can be calibrated by programming the Code Option Bits: C4~C0. Table 6-11 describes a typical instance of the calibration.

Table 6-10 Internal RC Drift Rate (Ta=25°C, VDD=5 V ± 5%, VSS=0V)

Internal RC Frequency	Drift Rate			
	Temperature (-40°C+85°C)	Voltage (2.4V~5.5V)	Process	Total
455kHz	± 5%	± 5%	± 4%	± 14%
4 MHz	± 5%	± 5%	± 4%	± 14%
8 MHz	± 5%	± 5%	± 4%	± 14%
16 MHz	± 5%	± 5%	± 4%	± 14%

Table 6-11 Calibration Selection for Internal RC Mode

Trimming Code					CLK Period	Frequency
C4	C3	C2	C1	C0		
1	1	1	1	1	Period*(1+32%)	F*(1-24.2%)
1	1	1	1	0	Period*(1+30%)	F*(1-23.1%)
1	1	1	0	1	Period*(1+28%)	F*(1-21.9%)
1	1	1	0	0	Period*(1+26%)	F*(1-20.6%)
1	1	0	1	1	Period*(1+24%)	F*(1-19.4%)
1	1	0	1	0	Period*(1+22%)	F*(1-18%)
1	1	0	0	1	Period*(1+20%)	F*(1-16.7%)
1	1	0	0	0	Period*(1+18%)	F*(1-15.3%)
1	0	1	1	1	Period*(1+16%)	F*(1-13.8%)
1	0	1	1	0	Period*(1+14%)	F*(1-12.3%)
1	0	1	0	1	Period*(1+12%)	F*(1-10.7%)
1	0	1	0	0	Period*(1+10%)	F*(1-9.1%)
1	0	0	1	1	Period*(1+8%)	F*(1-7.4%)
1	0	0	1	0	Period*(1+6%)	F*(1-5.7%)
1	0	0	0	1	Period*(1+4%)	F*(1-3.8%)
1	0	0	0	0	Period*(1+2%)	F*(1-2%)
0	0	0	0	0	Period (default)	F (default)
0	0	0	0	1	Period*(1-2%)	F*(1+2%)
0	0	0	1	0	Period*(1-4%)	F*(1+4.2%)

(Continuation)

Trimming Code					CLK Period	Frequency
C4	C3	C2	C1	C0		
0	0	0	1	1	Period*(1-6%)	F*(1+6.4%)
0	0	1	0	0	Period*(1-8%)	F*(1+8.7%)
0	0	1	0	1	Period*(1-10%)	F*(1+11.1%)
0	0	1	1	0	Period*(1-12%)	F*(1+13.6%)
0	0	1	1	1	Period*(1-14%)	F*(1+16.3%)
0	1	0	0	0	Period*(1-16%)	F*(1+19%)
0	1	0	0	1	Period*(1-18%)	F*(1+22%)
0	1	0	1	0	Period*(1-20%)	F*(1+25%)
0	1	0	1	1	Period*(1-22%)	F*(1+28.2%)
0	1	1	0	0	Period*(1-24%)	F*(1+31.6%)
0	1	1	0	1	Period*(1-26%)	F*(1+35.1%)
0	1	1	1	0	Period*(1-28%)	F*(1+38.9%)
0	1	1	1	1	Period*(1-30%)	F*(1+42.9%)

Note: * 1. *These are theoretical values provided for reference only. Actual values depend on the process.*

2. *Similar way of calculation is also applicable for low frequency mode.*

6.15 Power-on Considerations

Any microcontroller is not guaranteed to start to operate properly before the power supply remains at its steady state. The EM78F568N/EM78F668N is equipped with Power-on Voltage Detector (POVD) with a detecting level of 2.0V. It will work well if Vdd can rise quickly enough (50 ms or less). In many critical applications, however, extra devices are still required to assist in solving power-up problems.

6.16 External Power-on Reset Circuit

The circuit shown in Figure 6-45 implements an external RC to produce a reset pulse. The pulse width (time constant) should be kept long enough for Vdd to reached minimum operating voltage. This circuit is used when the power supply has slow rise time. Because the current leakage from the /RESET pin is about $\pm$ 5 μA, it is recommended that R should not be greater than 40K. In this way, the /RESET pin voltage is held below 0.2V. The diode (D) acts as a short circuit at the moment of power down. The capacitor C will discharge rapidly and fully. Rin, the current-limited resistor, will prevent high current or ESD (electrostatic discharge) from flowing to pin /RESET.

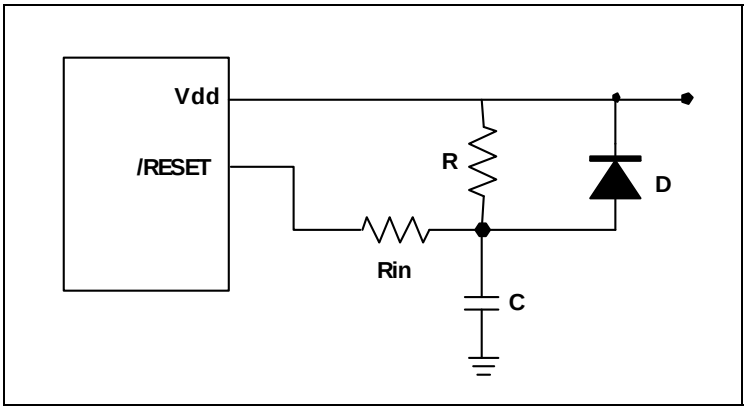


Figure 6-45 External Power-up Reset Circuit

6.17 Residue-Voltage Protection

When battery is replaced, device power (Vdd) is taken off but residue-voltage remains. The residue-voltage may trips below Vdd minimum, but not to zero. This condition may cause a poor power-on reset. Figures 6-46 and 6-47 show how to build a residue-voltage protection circuit.

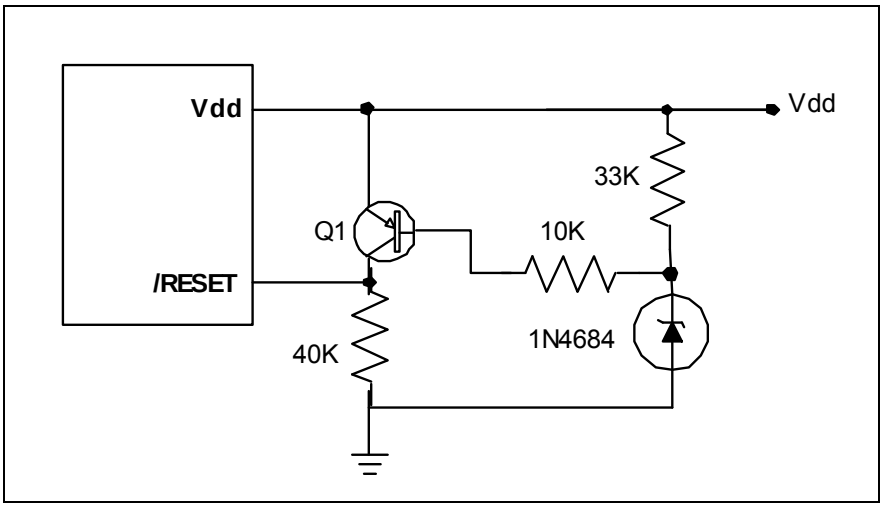


Figure 6-46 Residue Voltage Protection Circuit 1

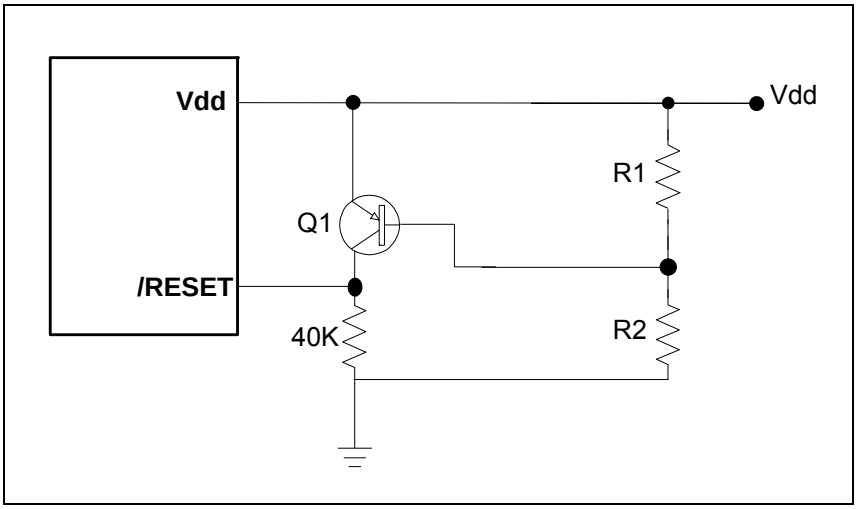


Figure 6-47 Residue Voltage Protection Circuit 2

6.18 Instruction Set

Each instruction in the instruction set is a 15-bit word divided into an OP code and one or more operands. Normally, all instructions are executed within one single instruction cycle (one instruction consists of two oscillator periods), unless the program counter is changed by instruction "MOV R2,A", "ADD R2,A", or by instructions of arithmetic or logic operation on R2 (e.g. "SUB R2,A", "BS(C) R2,6", "CLR R2", ...). In this case, the execution takes two instruction cycles.

If for some reasons, the specification of the instruction cycle is not suitable for certain applications, try modifying the instruction as follows:

(A) Change one instruction cycle to consist of four oscillator periods.

(B) "JMP", "CALL", "RET", "RETL", "RETI", or the conditional skip ("JBS", "JBC", "JZ", "JZA", "DJZ", "DJZA") commands which were tested to be true, are executed within two instruction cycles. The instructions that are written to the program counter also take two instruction cycles.

Case (A) is selected by the Code Option bit, called CLK. One instruction cycle consists of two oscillator clocks if CLK is low, and four oscillator clocks if CLK is high.

In addition, the instruction set has the following features:

(1) Every bit of any register can be set, cleared, or tested directly.

(2) The I/O register can be regarded as general register. That is, the same instruction can operate on the I/O register.

■ Instruction Set Convention:

R = *Register designator that specifies which one of the registers (including operation and general purpose registers) is to be utilized by the instruction.*

b = *Bit field designator that selects the value for the bit located in the register R and which affects the operation.*

k = *8 or 10-bit constant or literal value*

Binary Instruction	Hex	Mnemonic	Operation	Status Affected
000 0000 0000 0000	0000	NOP	No Operation	None
000 0000 0000 0001	0001	DAA	Decimal Adjust A	C
000 0000 0000 0011	0003	SLEP	0 → WDT, Stop oscillator	T, P
000 0000 0000 0100	0004	WDTC	0 → WDT	T, P
000 0000 0001 0000	0010	ENI	Enable Interrupt	None
000 0000 0001 0001	0011	DISI	Disable Interrupt	None
000 0000 0001 0010	0012	RET	[Top of Stack] → PC	None
000 0000 0001 0011	0013	RETI	[Top of Stack] → PC, Enable Interrupt	None
000 0001 rrrr rrrr	01rr	MOV R,A	A → R	None
000 0010 0000 0000	0200	CLRA	0 → A	Z
000 0011 rrrr rrrr	03rr	CLR R	0 → R	Z
000 0100 rrrr rrrr	04rr	SUB A,R	R-A → A	Z, C, DC
000 0101 rrrr rrrr	05rr	SUB R,A	R-A → R	Z, C, DC
000 0110 rrrr rrrr	06rr	DECA R	R-1 → A	Z
000 0111 rrrr rrrr	07rr	DEC R	R-1 → R	Z
000 1000 rrrr rrrr	08rr	OR A,R	A ∨ R → A	Z
000 1001 rrrr rrrr	09rr	OR R,A	A ∨ R → R	Z
000 1010 rrrr rrrr	0Arr	AND A,R	A & R → A	Z
000 1011 rrrr rrrr	0Brr	AND R,A	A & R → R	Z
000 1100 rrrr rrrr	0Crr	XOR A,R	A ⊕ R → A	Z
000 1101 rrrr rrrr	0Drr	XOR R,A	A ⊕ R → R	Z
000 1110 rrrr rrrr	0Err	ADD A,R	A + R → A	Z, C, DC
000 1111 rrrr rrrr	0Frr	ADD R,A	A + R → R	Z, C, DC
001 0000 rrrr rrrr	10rr	MOV A,R	R → A	Z
001 0001 rrrr rrrr	11rr	MOV R,R	R → R	Z
001 0010 rrrr rrrr	12rr	COMA R	/R → A	Z
001 0011 rrrr rrrr	13rr	COM R	/R → R	Z
001 0100 rrrr rrrr	14rr	INCA R	R+1 → A	Z
001 0101 rrrr rrrr	15rr	INC R	R+1 → R	Z

(Continuation)

Binary Instruction	Hex	Mnemonic	Operation	Status Affected
001 0110 rrrr rrrr	16rr	DJZA R	R-1 → A, skip if zero	None
001 0111 rrrr rrrr	17rr	DJZ R	R-1 → R, skip if zero	None
001 1000 rrrr rrrr	18rr	RRCA R	R(n) → A(n-1), R(0) → C, C → A(7)	C
001 1001 rrrr rrrr	19rr	RRC R	R(n) → R(n-1), R(0) → C, C → R(7)	C
001 1010 rrrr rrrr	1Arr	RLCA R	R(n) → A(n+1), R(7) → C, C → A(0)	C
001 1011 rrrr rrrr	1Brr	RLC R	R(n) → R(n+1),R(7) → C, C → R(0)	C
001 1100 rrrr rrrr	1Crr	SWAPA R	R(0-3) → A(4-7), R(4-7) → A(0-3)	None
001 1101 rrrr rrrr	1Drr	SWAP R	R(0-3) ↔ R(4-7)	None
001 1110 rrrr rrrr	1Err	JZA R	R+1 → A, skip if zero	None
001 1111 rrrr rrrr	1Frr	JZ R	R+1 → R, skip if zero	None
010 0bbb rrrr rrrr	2xrr	BC R,b	0 → R(b)	None [2]
010 1bbb rrrr rrrr	2xrr	BS R,b	1 → R(b)	None [3]
011 0bbb rrrr rrrr	3xrr	JBC R,b	if R(b)=0, skip	None
011 1bbb rrrr rrrr	3xrr	JBS R,b	if R(b)=1, skip	None
100 kkkk kkkk kkkk	4kkk	CALL k	PC+1 → [SP], (Page, k) → PC	None
101 kkkk kkkk kkkk	5kkk	JMP k	(Page, k) → PC	None
110 0000 kkkk kkkk	60kk	MOV A,k	k → A	None
110 0100 kkkk kkkk	64kk	OR A,k	A ∨ k → A	Z
110 1000 kkkk kkkk	68kk	AND A,k	A & k → A	Z
110 1100 kkkk kkkk	6Ckk	XOR A,k	A ⊕ k → A	Z
111 0000 kkkk kkkk	70kk	RETL k	k → A,[Top of Stack] → PC	None
111 0100 kkkk kkkk	74kk	SUB A,k	k-A → A	Z, C, DC
111 1100 kkkk kkkk	7Ckk	ADD A,k	k+A → A	Z, C, DC
111 1010 0000 kkkk	7A0k	SBANK k	K->R1(4)	None
111 1010 0100 kkkk	7A4k	GBANK k	K->R1(0)	None
111 1010 1000 kkkk kkk kkkk kkkk kkkk	7A8k kkkk	LCALL k	Next instruction : k kkkk kkkk kkkk PC+1→[SP], k→PC	None
111 1010 1100 kkkk kkk kkkk kkkk kkkk	7ACk kkkk	LJMP k	Next instruction : k kkkk kkkk kkkk K→PC	None
111 1011 rrrr rrrr	7Brr	TBRD R	ROM[(TABPTR)] → R	None

6.19 Code Option

Code Option from SRAM/ROM/OTP/FLASH

Mnemonic	COBS0	-	CLKS0	-	-	LVR1	LVR0	RESETEN	ENWDT	NRHL	NRE	Protect
1	register	-	2CLKS	-	-	High	High	/RESET	Enable	8/fc	Disable	Enable
0	option	-	4CLKS	-	-	Low	Low	P83	Disable	32/fc	Enable	Disable

Bit 14 (COBS0): IRC mode select bit

0: IRC frequency select from code option

1: IRC frequency select from register

Bits 13 ~ 12: unused, set to 0 all the time

Bits 11 (CLKS0): instruction period option bit

Instruction Period	CLKS0
4 clocks	0
2 clocks	1

Bits 8 ~ 7 (LVR1 ~ LVR0)：Low voltage reset enable bit

LVR1, LVR0	VDD Reset Level	VDD Release Level
00	NA	NA
01	2.7V	2.9
10	3.7V	3.9
11	4.2V	4.4

Bit 6 (RESETEN): P83//RST pin select bit

0: P83 pin

1: /RST pin

Bit 5 (ENWDT): WDT enable bit

0: disable WDT

1: enable WDT

Bit 4 (NRHL): noise rejection high/low pulse define bit.

0: pulses equal to 32/fc [s] is regarded as signal

1: pulses equal to 8/fc [s] is regarded as signal

Bit 3 (NREB): noise rejection enable bit

0: enable noise rejection

1: disable noise rejection

Bits 2 ~ 0 (PR2 ~ PR0): product bits

Mnemonic	HLFS	-	SHE	C4	C3	C2	C1	C0	RCM1	RCM0	-	OSC2	OSC1	OSC0	RCOD
1	Green	-	Enable	High	High	High	High	High	High	High	-	High	High	High	Open drain
0	Normal	-	Disable	Low	Low	Low	Low	Low	Low	Low	-	Low	Low	Low	System clock

Bit 14 (HLFS): Initialize the CPU mode

0: normal mode

1: green mode

Bit 13: Unused, set to 1 at all time

0: heavy

1: light

Bit 12 (SHE): System halt enable bit

0: disable

1: enable

Bits 11 ~ 7 (C4 ~ C0): IRC trim bits. These are automatically set by the writer.

Bits 6 ~ 5 (RCM1 ~ RCM0): IRC frequency select

Bit 4: Unused, set to 1 at all time

Bits 3 ~ 1 (OSC2 ~ OSC0): Oscillator mode select bits.

XT (XTAL oscillator mode)	0	0	0
HXT (High XTAL oscillator mode)	0	0	1
LXT1 (Low XTAL1 oscillator mode)	0	1	0
LXT2 (Low XTAL2 oscillator mode)	0	1	1
IRC mode, OSCO (P54) act as I/O pin	1	0	0
IRC mode, OSCO (P54) act as RCOUT pin	1	0	1
ERC mode, OSCO (P54) act as I/O pin	1	1	0
ERC mode, OSCO (P54) act as RCOUT pin	1	1	1

Bit 0 (RCOD): Select bit of Oscillator output or I/O port.

RCOUT	Pin Function
1	OSCO pin is open drain
0	OSCO output system clock (default)

7 DC Electrical Characteristics

Ta=25°C, VDD=5.0V ± 5%, VSS=0V

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Fxt	Crystal: VDD to 3V	Two cycles with two clocks	DC	10 (-)	14 (8)	MHz
	Crystal: VDD to 5V		DC	20 (-)	24 (20)	MHz
	ERC: VDD to 5V	R: 5.1KΩ, C: 100 pF	F±30%	830	F±30%	kHz
	IRC: VDD to 5V	4 MHz, 1 MHz, 8 MHz, 455kHz	F±30%	F	F±30%	Hz
IIL	Input Leakage Current for input pins	VIN = VDD, VSS	–	–	±1	μA
IRC1	IRC: VDD to 5V	RCM0: RCM1=0:0	2.9	4	5.7	MHz
IRCE	Internal RC oscillator error per stage	–	± 4.3	± 4.5	± 4.7	%
IRC2	IRC: VDD to 5V	RCM0:RCM1=1:0	5.8	8	11.4	MHz
IRC3	IRC: VDD to 5V	RCM0:RCM1=0:1	11.6	16	22.8	MHz
IRC4	IRC: VDD to 5V	RCM0:RCM1=1:1	330	455	645	kHz
VIHRC	Input High Threshold Voltage (Schmitt trigger)	OSCI in RC mode	3.9	4	4.1	V
IERC1	Sink current	VI from low to high , VI=5V	21	22	23	mA
VILRC	Input Low Threshold Voltage (Schmitt trigger)	OSCI in RC mode	1.7	1.8	1.9	V
IERC2	Sink current	VI from high to low , VI=2V	16	17	18	mA
IIL	Input Leakage Current for input pins	VIN = VDD, VSS	-1	0	1	μA
VIH1	Input High Voltage (Schmitt trigger)	Ports 5, 6, 7, 8, 9	0.7Vdd	–	Vdd+0.3V	V
VIL1	Input Low Voltage (Schmitt trigger)	Ports 5, 6, 7, 8, 9	-0.3V	–	0.3Vdd	V
VIHT1	Input High Threshold Voltage (Schmitt trigger)	/RESET	0.56Vdd	–	Vdd+0.3V	V
VILT1	Input Low Threshold Voltage (Schmitt trigger)	/RESET	-0.3V	–	0.44Vdd	V
VIHT2	Input High Threshold Voltage (Schmitt trigger)	TCC, INT	0.7Vdd	–	Vdd+0.3V	V
VILT2	Input Low Threshold Voltage (Schmitt trigger)	TCC, INT	-0.3V	–	0.3Vdd	V
VIHX1	Clock Input High Voltage	OSCI in crystal mode	2.9	3.0	3.1	V
VILX1	Clock Input Low Voltage	OSCI in crystal mode	1.7	1.8	1.9	V
IOH1	Output High Voltage (Ports 5, 6, 7, 8, 9)	VOH = VDD – 0.1VDD	–	-4.5	–	mA
IOL1	Output Low Voltage (Ports 5, 6, 7, 8, 9)	VOL = GND + 0.1VDD	–	18	–	mA

(Continuation)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
IOH2	Output High Voltage (high drive)(Ports 5, 6, 7, 8, 9)	VOH = VDD – 0.1VDD	–	-8	–	mA
IOL2	Output Low Voltage (high sink) (Ports 5, 6, 7, 8, 9)	VOL = GND + 0.1VDD	–	32	–	mA
IPH	Pull-high current	Pull-high active, input pin at VSS	–	-75	–	µA
IPL	Pull-low current	Pull-low active, input pin at Vdd	–	40	–	µA
ISB1	Power down current	All input and I/O pins at VDD, Output pin floating, WDT disabled	–	2.0	–	µA
ISB2	Power down current	All input and I/O pins at VDD, Output pin floating, WDT enabled	–	7	–	µA
ICC1	Operating supply current at two clocks	/RESET= 'High', Fosc=32kHz (Crystal type, CLKS="0"), Output pin floating, WDT disabled	–	22	–	µA
ICC2	Operating supply current at two clocks	/RESET= 'High', Fosc=32kHz (Crystal type, CLKS="0"), Output pin floating, WDT enabled	–	27	–	µA
ICC3	Operating supply current at two clocks	/RESET= 'High', Fosc=4MHz (Crystal type, CLKS="0"), Output pin floating, WDT enabled	–	1.6	–	mA
ICC4	Operating supply current at two clocks	/RESET= 'High', Fosc=10MHz (Crystal type, CLKS="0"), Output pin floating, WDT enabled	–	2.2	–	mA

* *These parameters are characterized but not tested.*

* *Data in the Minimum, Typical, Maximum (“Min.”, “Typ.”, ”Max.”) columns are based on characterization results at 25℃. These data are for design reference only and are not tested.*

Data EEPROM Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Tprog	Erase/Write cycle time	Vdd = 2.0~ 5.5V Temperature = -40°C ~ 85°C	–	6	–	ms
Treten	Data Retention	–	–	10	–	Years
Tendu	Endurance time	–	–	1000K	–	Cycles

Program Flash Memory Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Tprog	Erase/Write cycle time	Vdd = 5.0V Temperature = -40 ~ 85°C	–	4	–	ms
Treten	Data Retention		–	10	–	Years
Tendu	Endurance time		–	100K	–	Cycles

A/D Converter Characteristics

Vdd=2.5V to 5.5V, Vss=0V, Ta=25°C

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
VAREF	Analog reference voltage	VAREF-VASS= 2.5V to 5.5V	2.5	-	Vdd	V
VASS	–	–	-	Vss	-	V
VAI	Analog input voltage	–	VASS	-	VAREF	V
IAI1	Ivdd	VAREF = Vdd	1150	1300	1450	μA
	Ivref	–	-10	0	10	μA
IAI2	Ivdd	VAREF = VREF	700	800	900	μA
	Ivref	–	450	500	550	μA
RN	Resolution	VAREF=Vdd	8	9	-	Bits
LN	Linearity error	VAREF=Vdd	0	± 2	+/-4	LSB
DNL	Differential nonlinear error	VAREF=Vdd	0	± 0.5	+/-0.9	LSB
FSE	Full scale error	VAREF=Vdd	± 0	± 1	± 2	LSB
OE	Offset error	VAREF=Vdd	± 0	± 1	± 2	LSB
ZAI	Recommended impedance of analog voltage source	VAREF=Vdd	0	8	10	KΩ
TAD1	A/D clock period	VAREF=Vdd=2.5~5.5V Ta= -40~85°C	4	-	-	μs
TAD2	A/D clock period	VAREF=Vdd=3~5.5V Ta= -40~85°C	1	-	-	μs
TCN	A/D conversion time	VAREF=Vdd	14	-	14	TAD
PSR	Power supply rejection	Vdd=Vdd-10% to Vdd+10%	± 0	-	± 2	LSB

Note: 1. The parameters are characterized but not tested.

2. These parameters are for design guidance only and are not tested.

3. It will not consume any current other than minor leakage current, when A/D is off.

4. The A/D conversion result never decreases with an increase in the input voltage, and has no missing code.

5. Specifications are subject to change without prior notice.

Comparator Electrical Characteristic

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
VOS	Input offset voltage	RL = 5.1K (Note[1])	–	10	–	mV
Vcm	Input common-mode voltages range	(Note [2])	GND	–	VDD	V
ICO	Supply current of Comparator	–	–	200	–	uA
TRS	Response time	Vin(-)=2.5V, Vdd=5V, CL=15p (comparator output load), overdrive=30mV (Note [3])	–	0.7	–	us
TLRS	Large signal response time	Vin(-)=2.5V, Vdd=5V, CL=15p (comparator output load),	–	300	–	ns
VS	Operating range	–	2.5	–	5.5	V

Note: [1]. The output voltage is in the unit gain circuitry and over the full input common-mode range.

[2]. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is VDD.

[3]. The response time specified is a 100 mV input step with 30 mV overdrive.

8 AC Electrical Characteristics

EM78F568N/EM78F668N, 0 ≤ Ta≤ 70°C, VDD=5V, VSS=0V

-40 ≤ Ta ≤ 85°C, VDD=5V, VSS=0V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Dclk	Input CLK duty cycle	–	45	50	55	%
Tins	Instruction cycle time (CLKS:="0")	Crystal type	100	–	DC	ns
		RC type	500	–	DC	ns
Ttcc	TCC input period	–	(Tins+20)/N*	–	–	ns
Tdrh	Device reset hold time	–	11.8	16.8	21.8	ms
Trst	/RESET pulse width	Ta = 25°C	1000	–	–	ns
Twdt	Watchdog timer period	Ta = 25°C	11.8	16.8	21.8	ms
Tset	Input pin setup time	–	–	0	–	ns
Thold	Input pin hold time	–	–	20	–	ns
Tdelay	Output pin delay time	Cload = 20 pF	–	50	–	ns

***N** = *selected prescaler ratio*

NOTE

- *These parameters are theoretical values and have not been tested. These data are for design reference only.*
- *Data under "**Min.**," "**Typ.**," and "**Max.**" columns are based on characterization results at 25°C.*

9 Device Characteristics

The graphs provided in the following pages were derived based on a limited number of samples and are shown here for reference only. The device characteristics illustrated herein are not guaranteed for its accuracy. In some graphs, the data may be out of the specified warranted operating range.

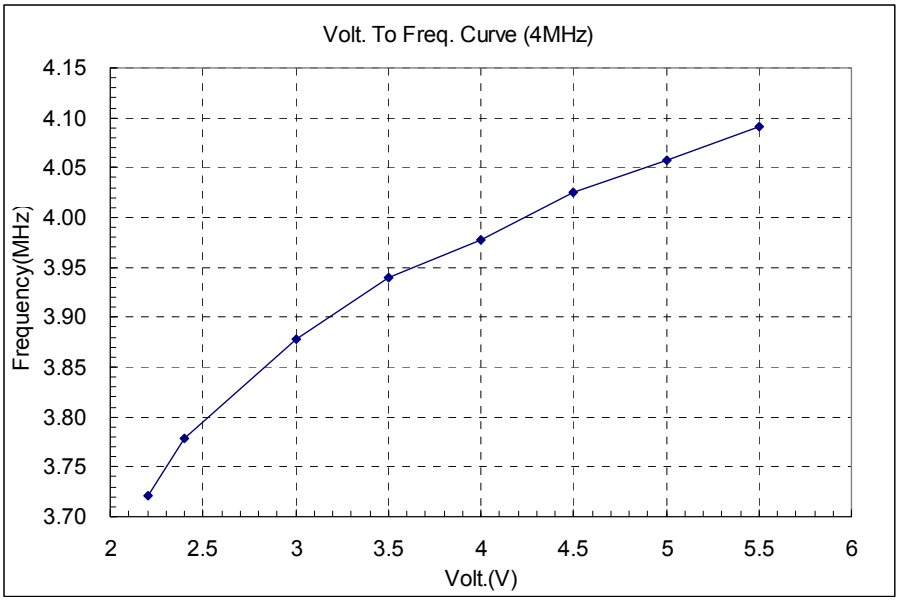


Figure 10-1 Voltage vs. Frequency Curve (4MHz)

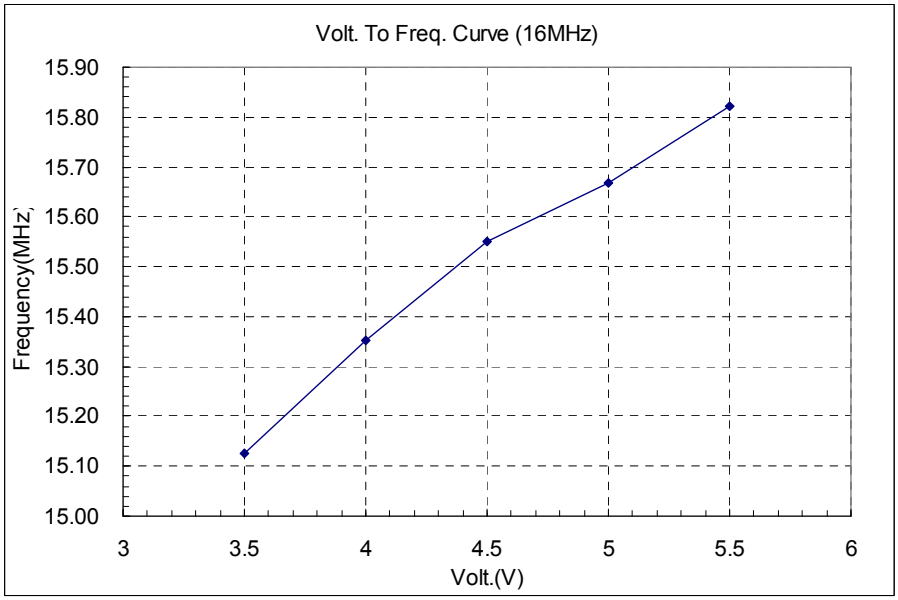


Figure 10-2 Voltage vs. Frequency Curve (16MHz)

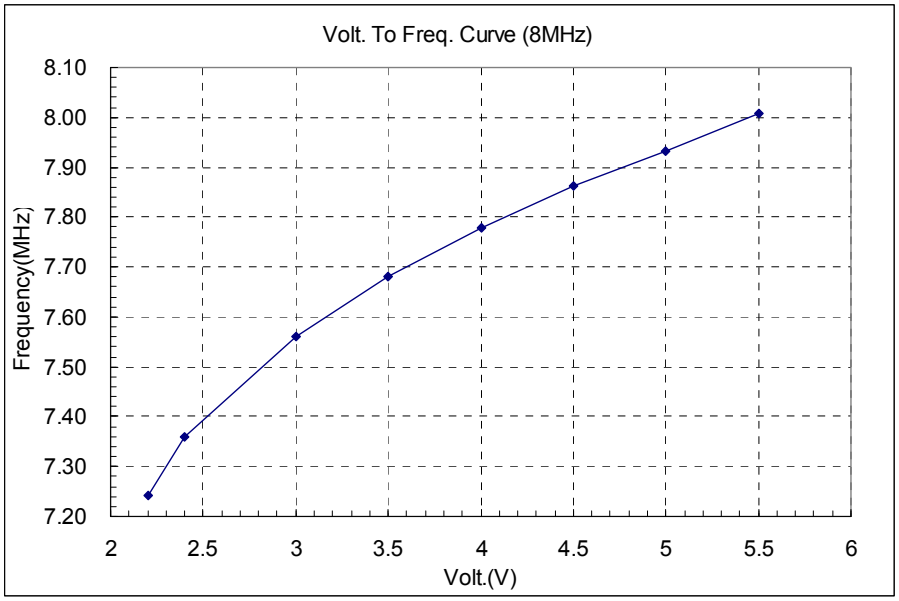


Figure 10-3 Voltage vs. Frequency Curve (8MHz)

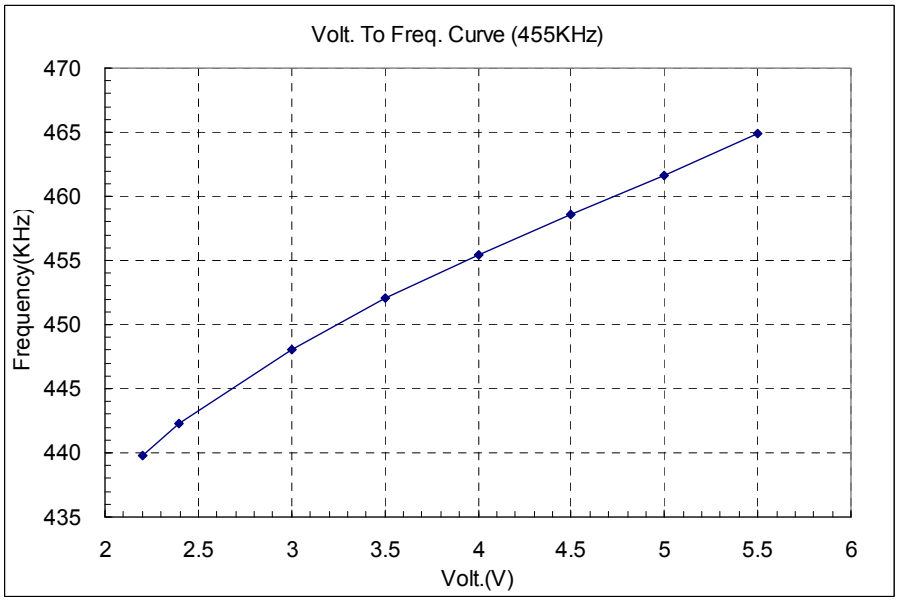


Figure 10-4 Voltage vs. Frequency Curve (455KHz)

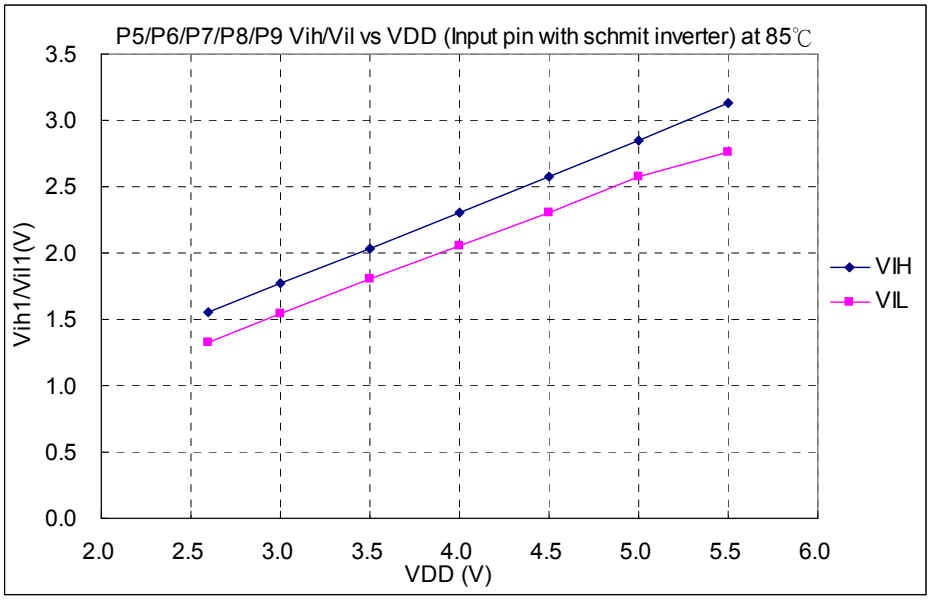


Figure 10-5 VIH/VIL vs. VDD (85°C)

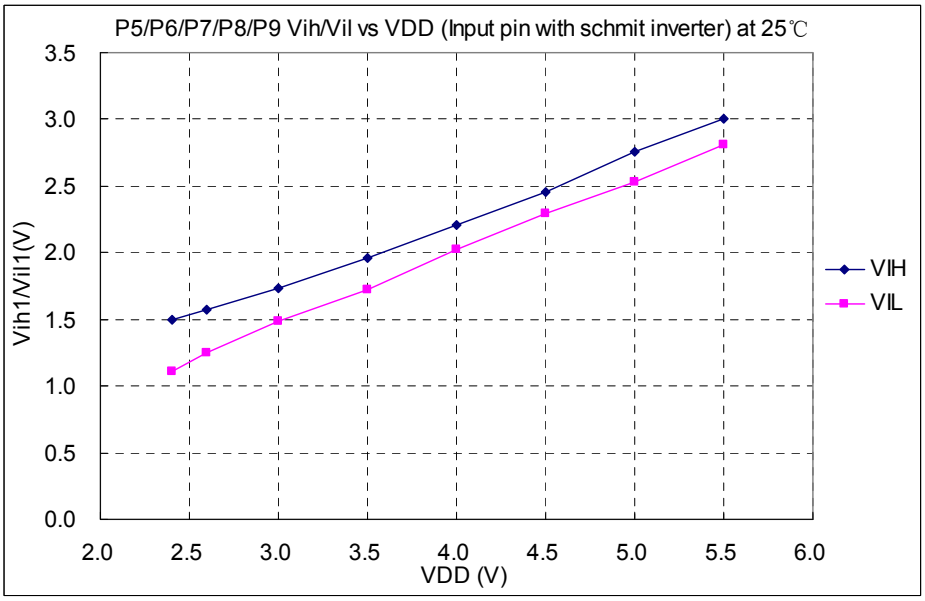


Figure 10-6 VIH/VIL vs. VDD (25°C)

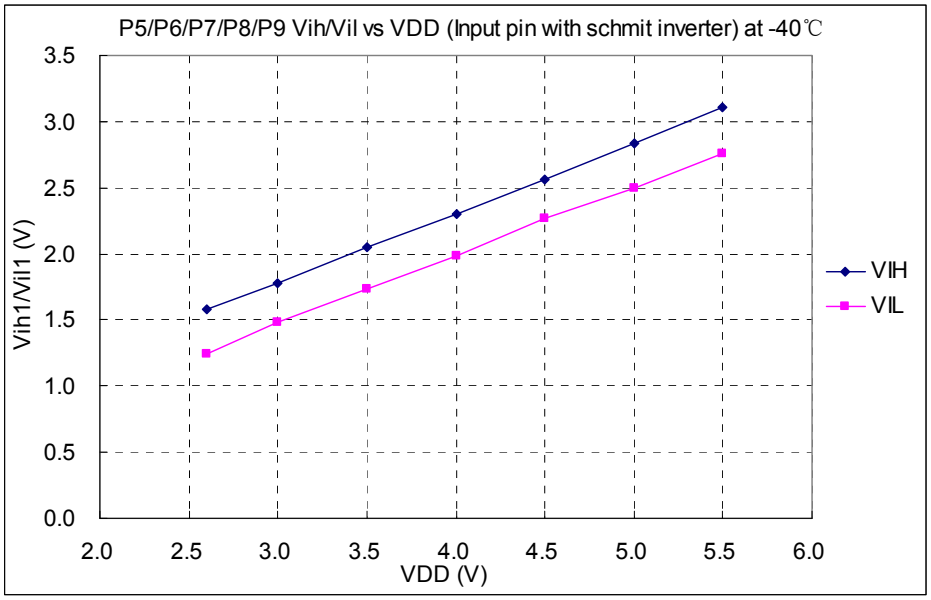


Figure 10-7 VIH/VIL vs. VDD (-40°C)

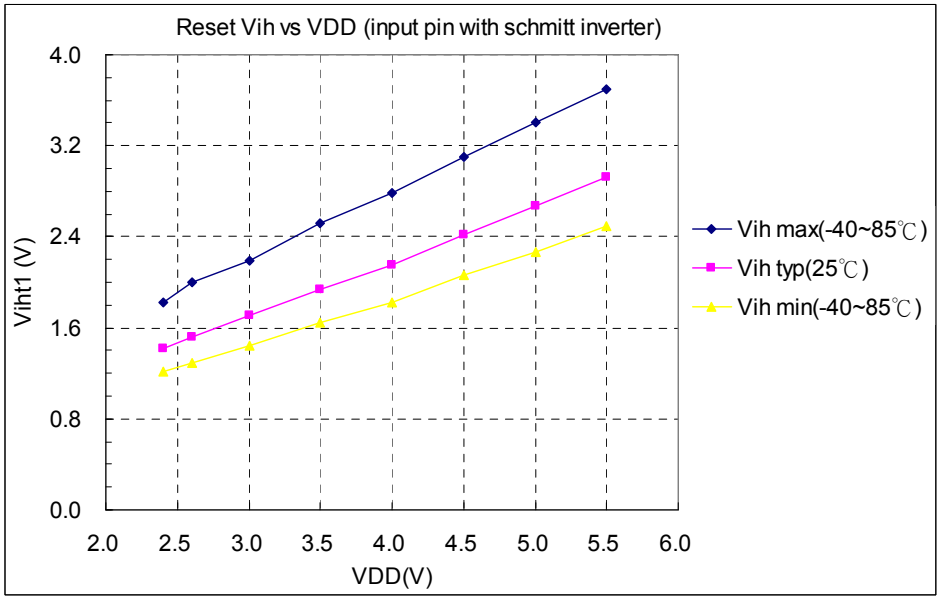


Figure 10-8 VIH of RESET Pin vs. VDD

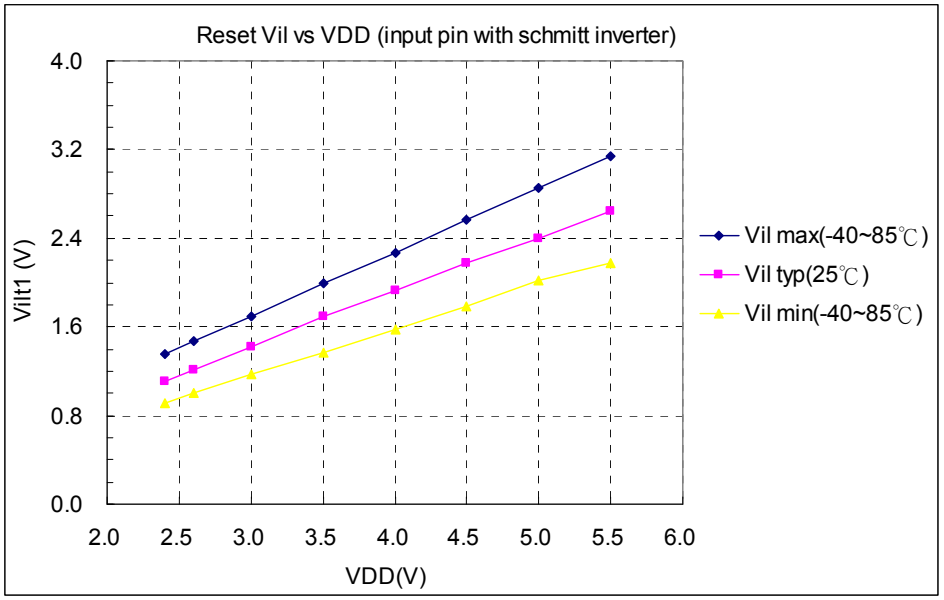


Figure 10-9 VIL of RESET Pin vs. VDD

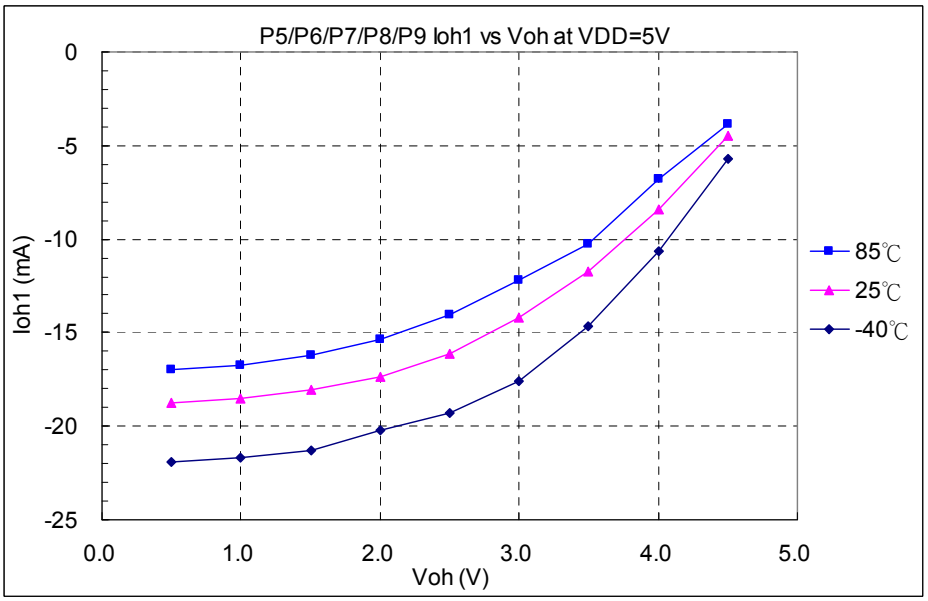


Figure 10-10 VOH vs. IOH, VDD=5V

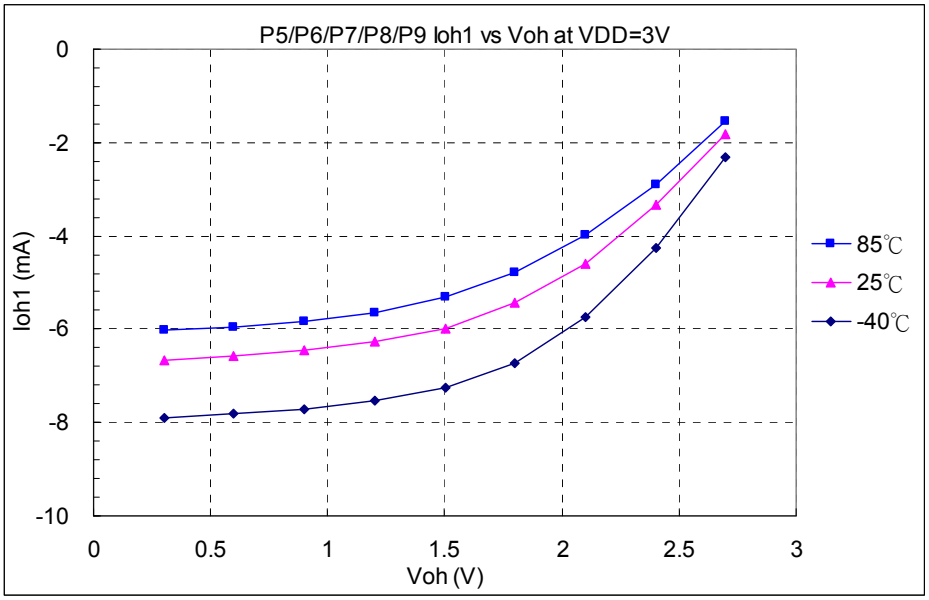


Figure 10-11 VOH vs. IOH, VDD=3V

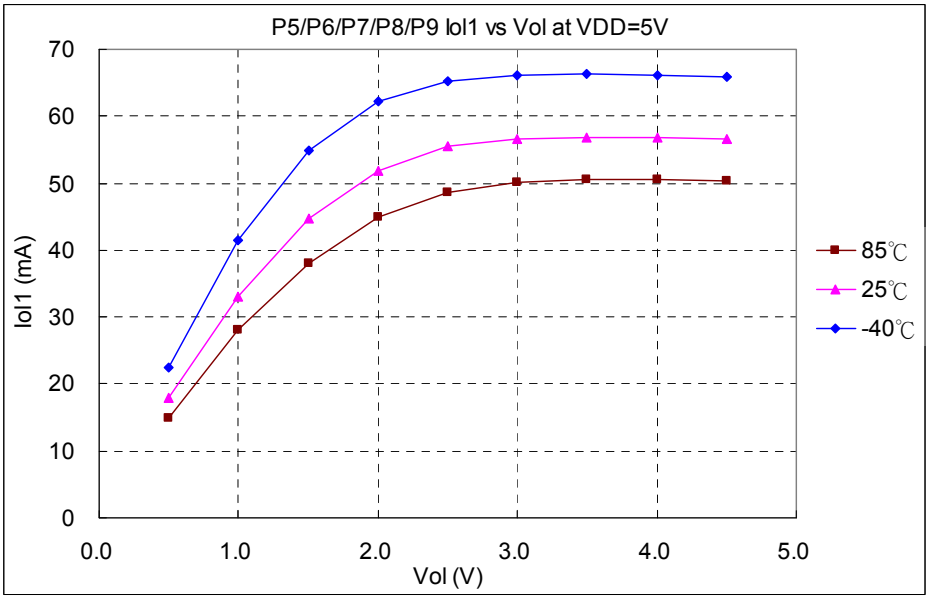


Figure 10-12 VOL vs. IOL1, VDD=5V

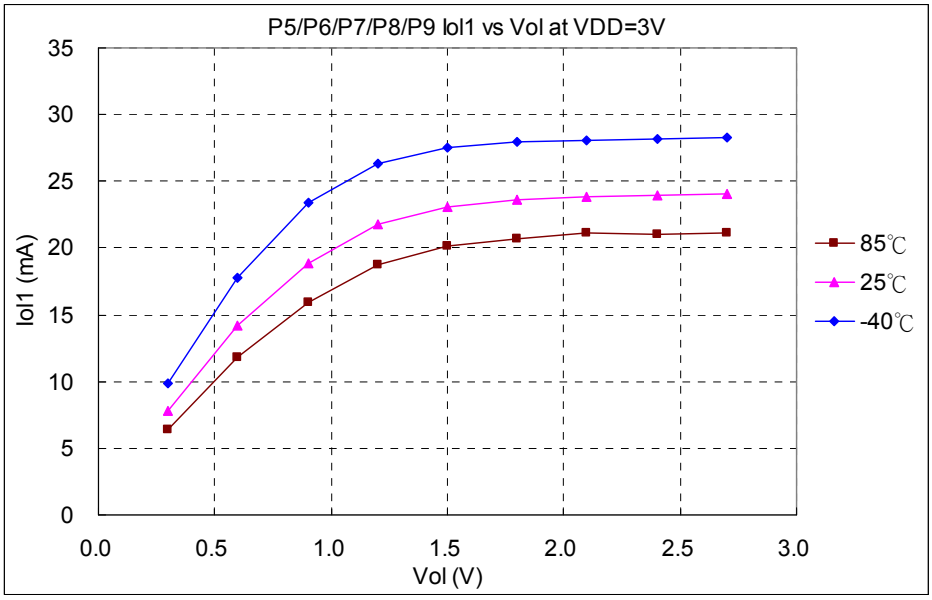


Figure 10-13 VOL vs. IOL1, VDD=3V

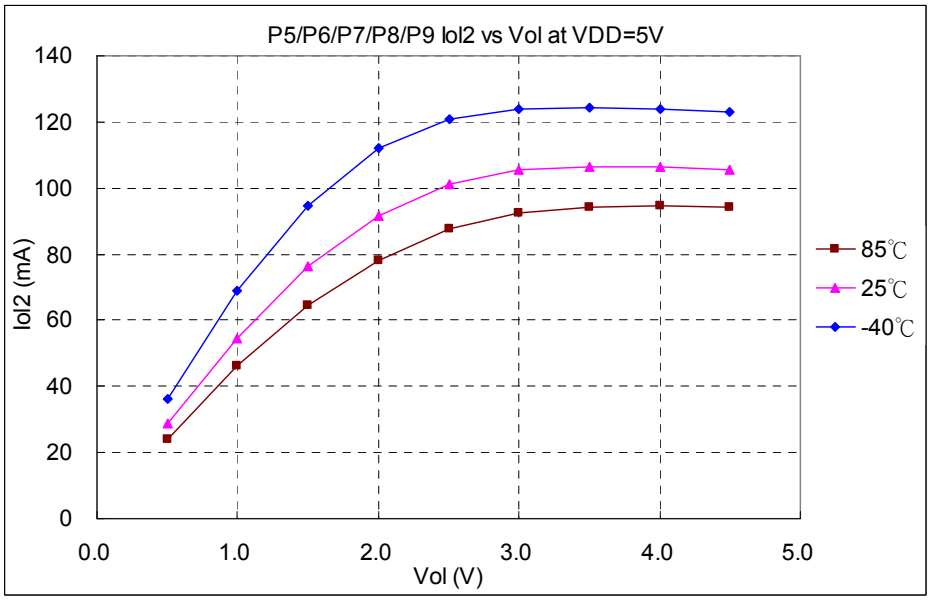


Figure 10-14 VOL of IOL2, VDD=5V

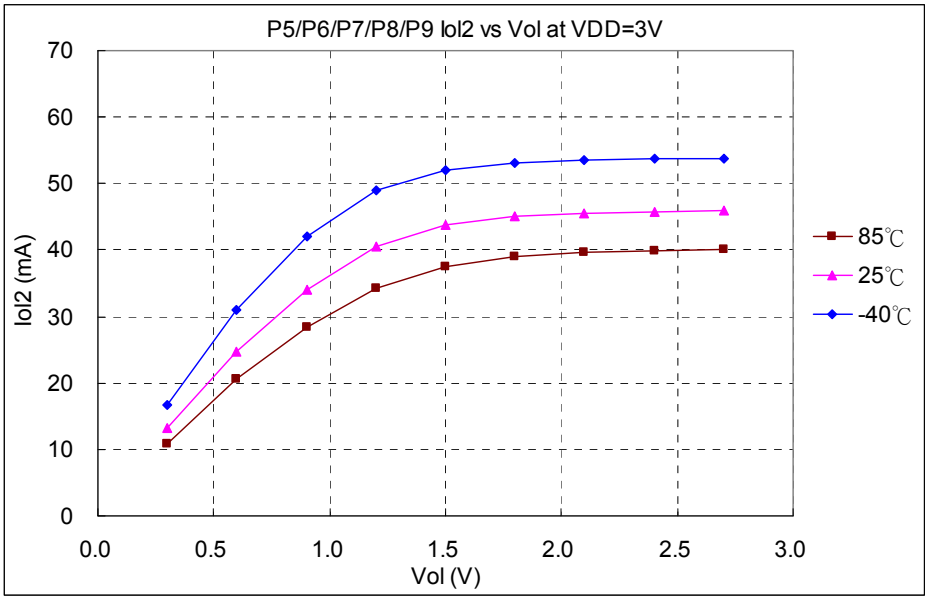


Figure 10-15 VOL of IOL2, VDD=3V

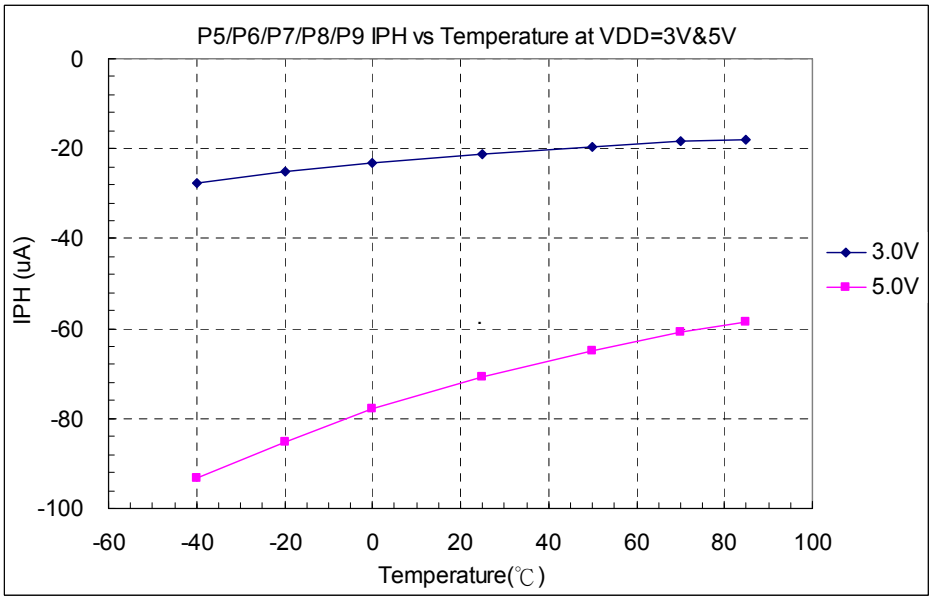


Figure 10-16 IPH vs. Temperature, VDD=3V & 5V

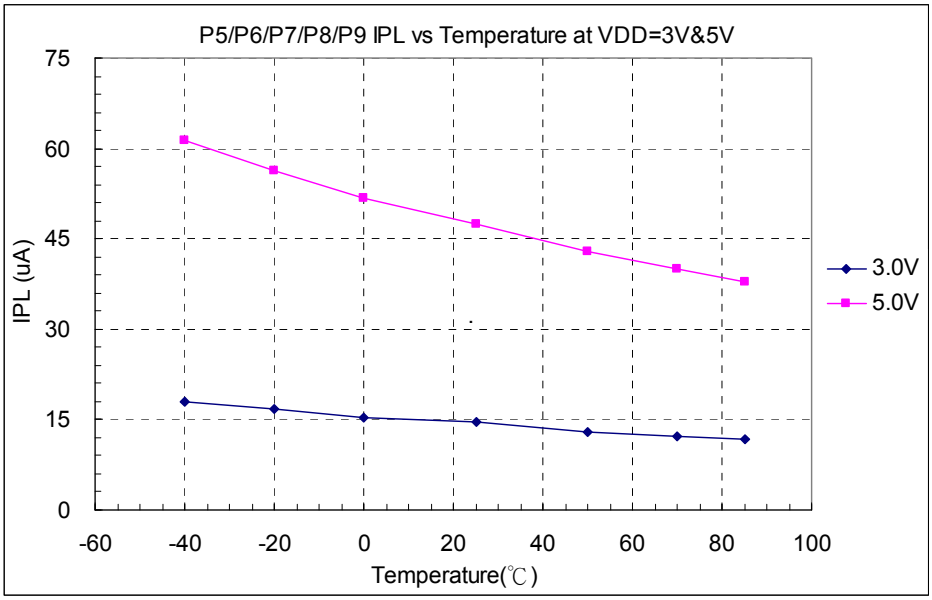


Figure 10-17 IPL vs. Temperature, VDD=3V & 5V

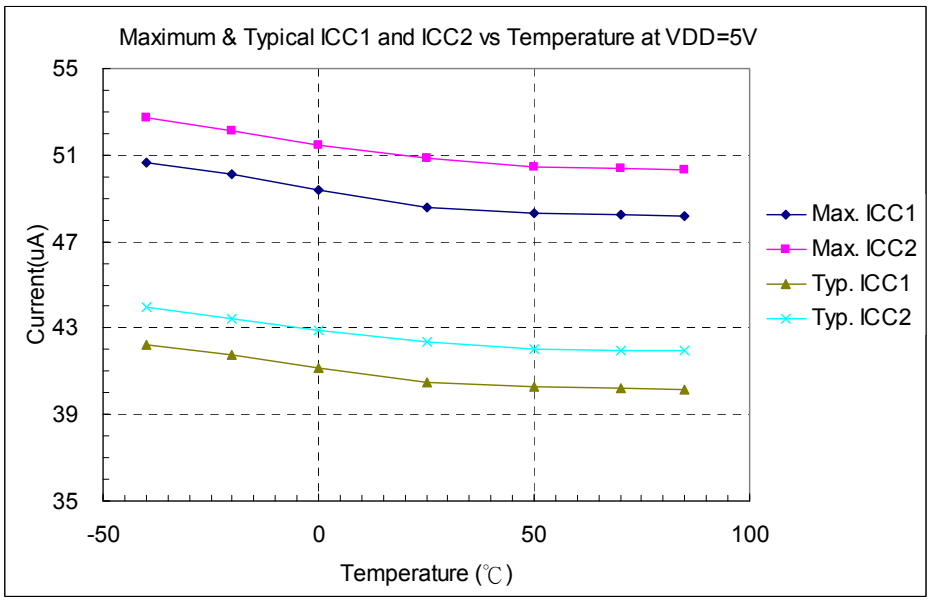


Figure 10-18 ICC1 and ICC2 vs. Temperature, VDD=5V

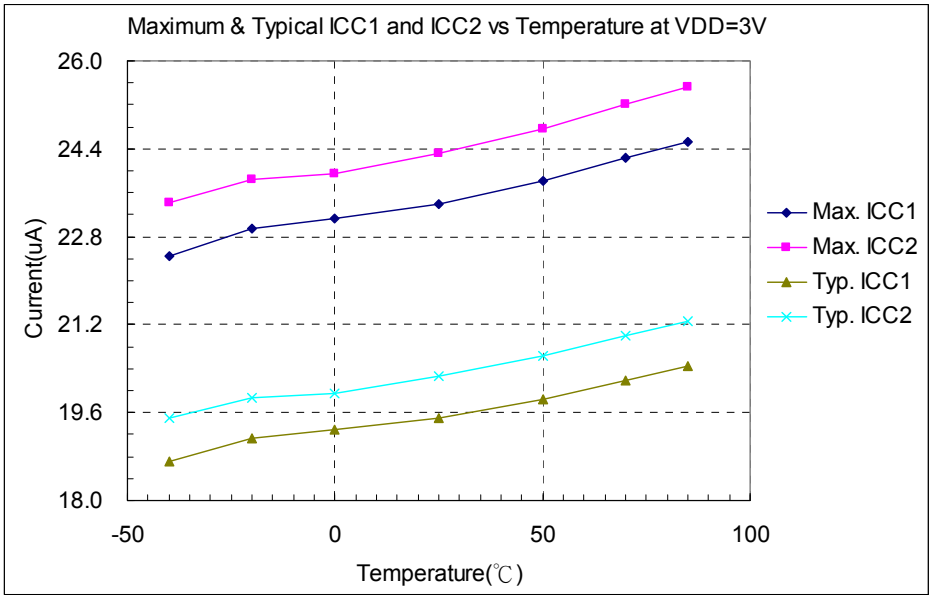


Figure 10-19 ICC1 and ICC2 vs. Temperature, VDD=3V

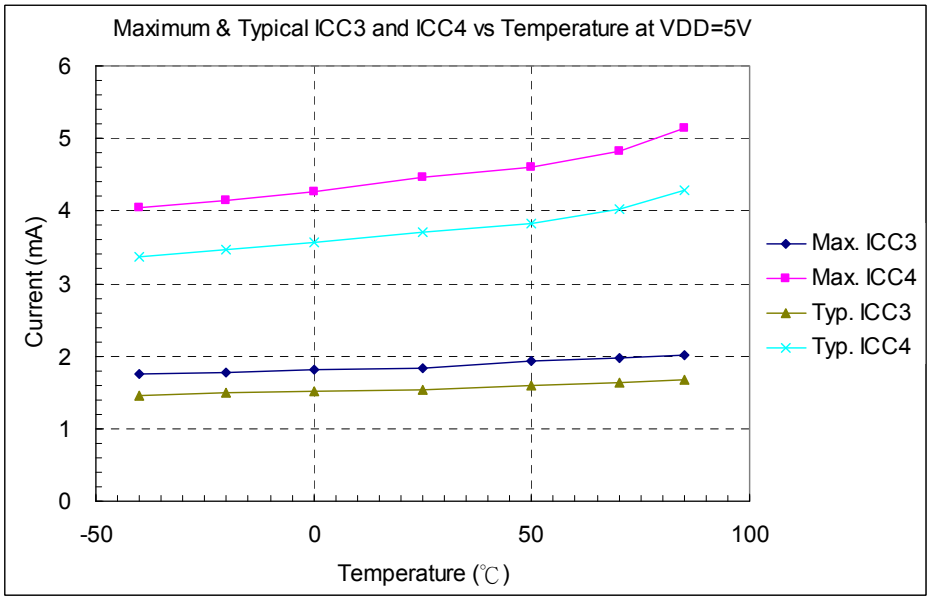


Figure 10-20 ICC3 and ICC4 vs. Temperature, VDD=5V

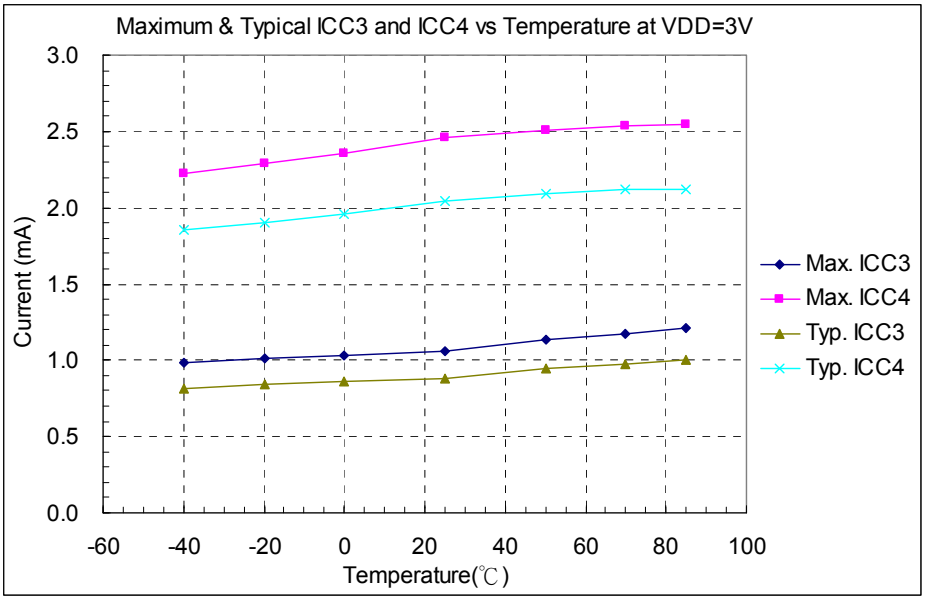


Figure 10-21 ICC3 and ICC4 vs. Temperature, VDD=3V

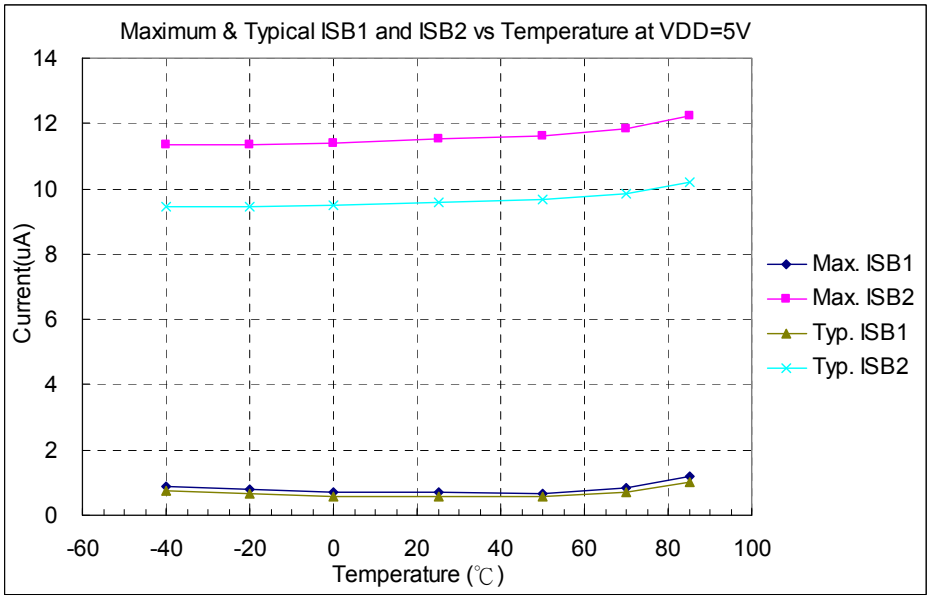


Figure 10-22 ISB1 and ISB2 vs. Temperature, VDD=5V

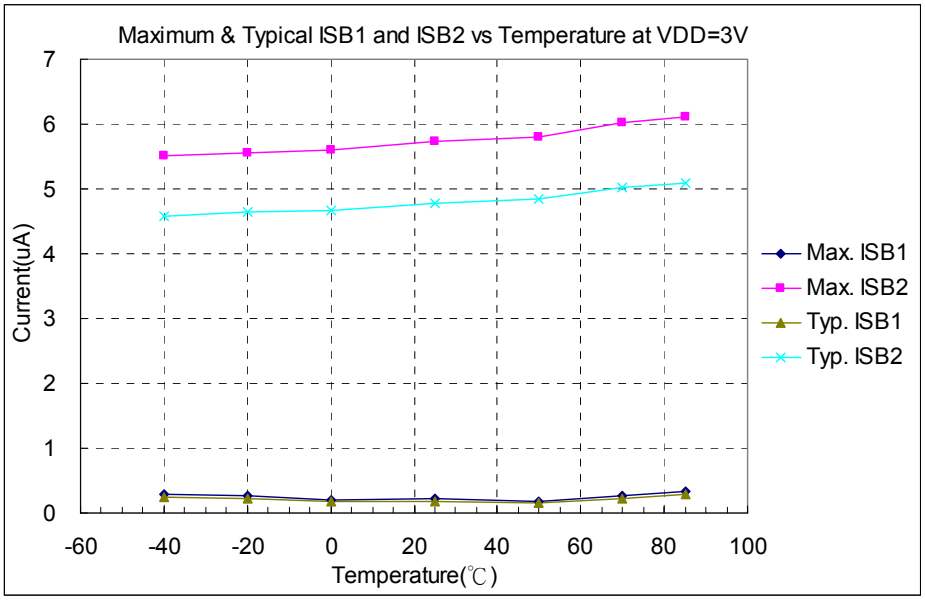


Figure 10-23 ISB1 and ISB2 vs. Temperature, VDD=3V

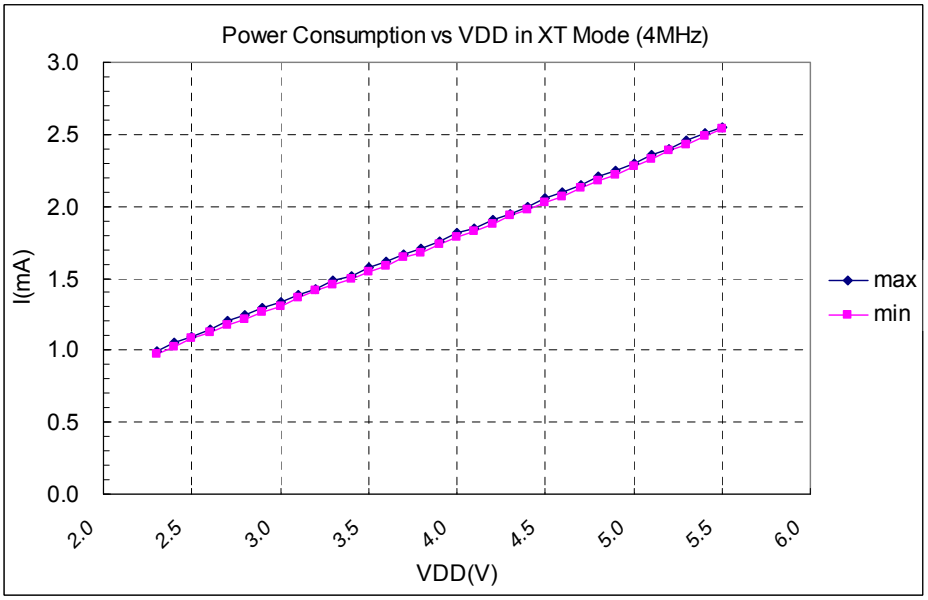


Figure 10-24 Power Consumption in HXT Mode (4MHz)

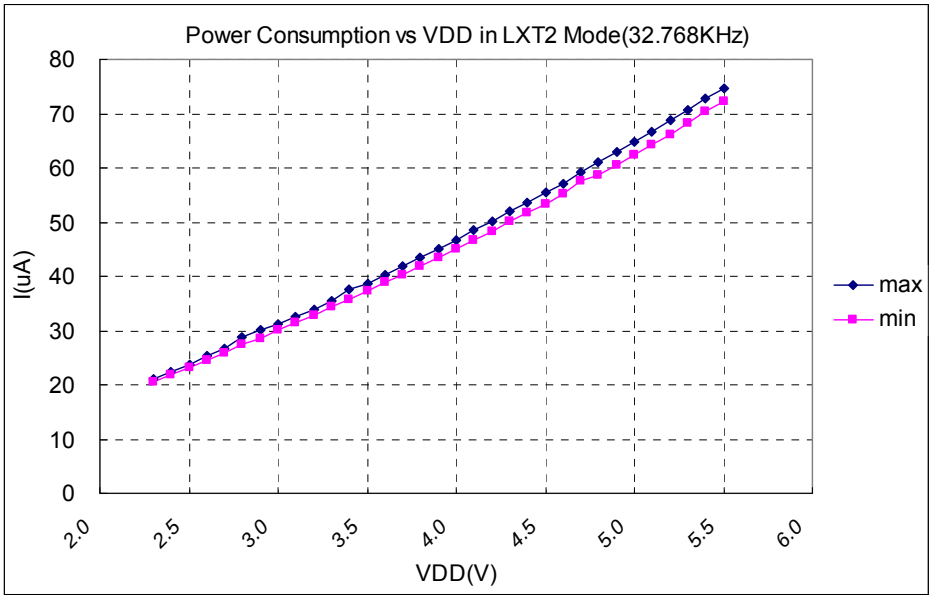


Figure 10-25 Power Consumption in LXT Mode (32768Hz)

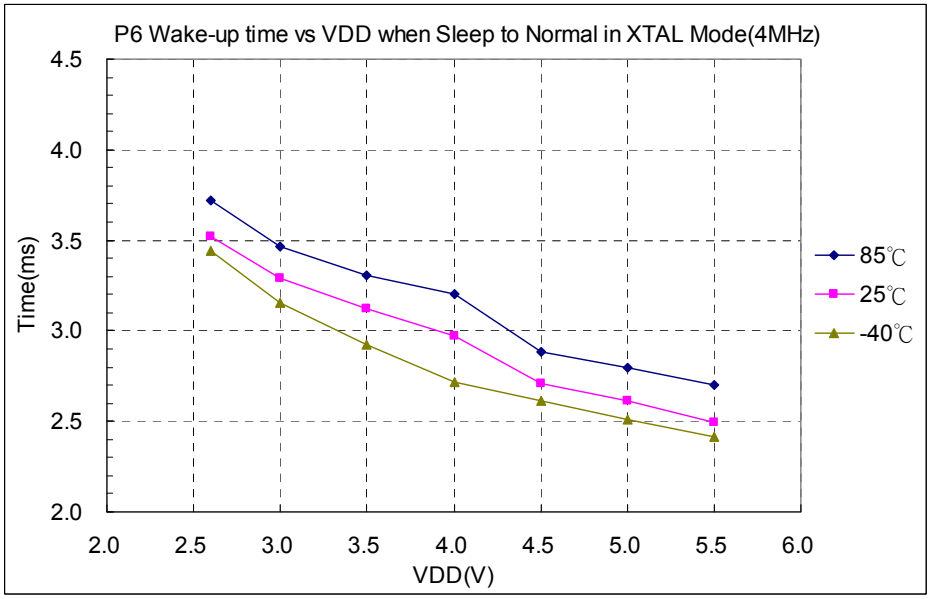


Figure 10-26 P6 Wake-up Time when Sleep to Normal, Crystal mode (Sub. Freq.=16kHz, 4 MHz)

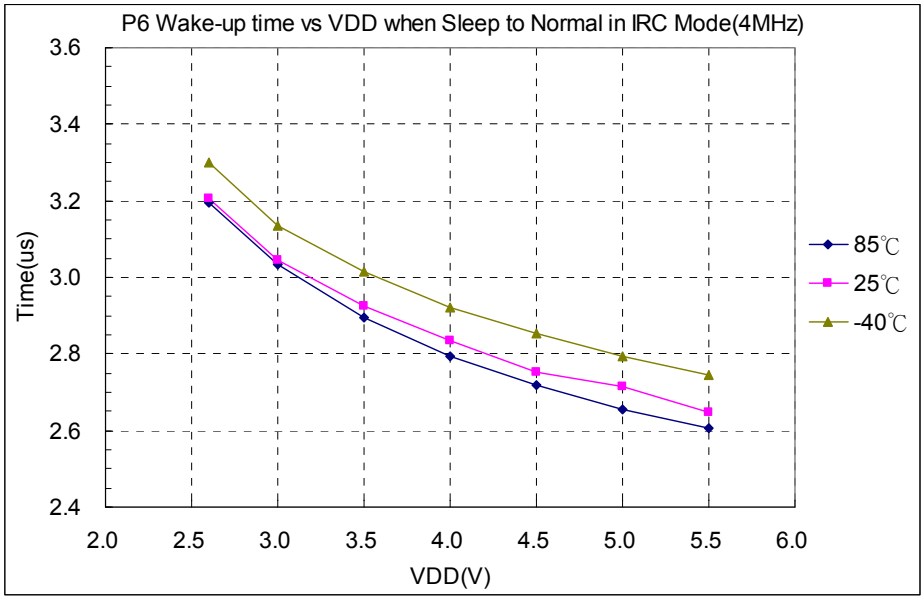


Figure 10-27 P6 Wake-up Time when Sleep to Normal, IRC mode (Sub. Freq.=16kHz, 4 MHz)

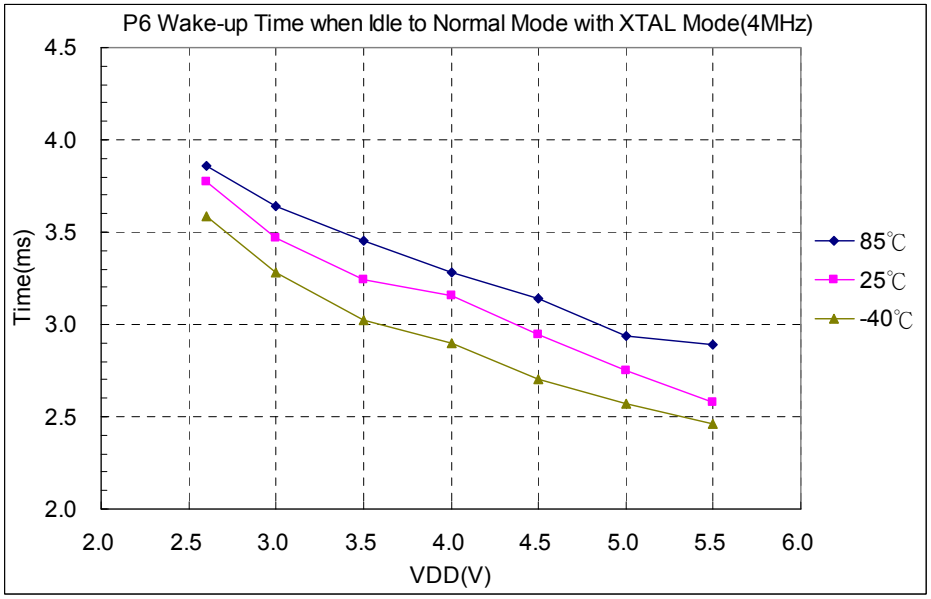


Figure 10-28 P6 Wake-up Time when Idle to Normal, Crystal mode (Sub. Freq.=16kHz, 4 MHz)

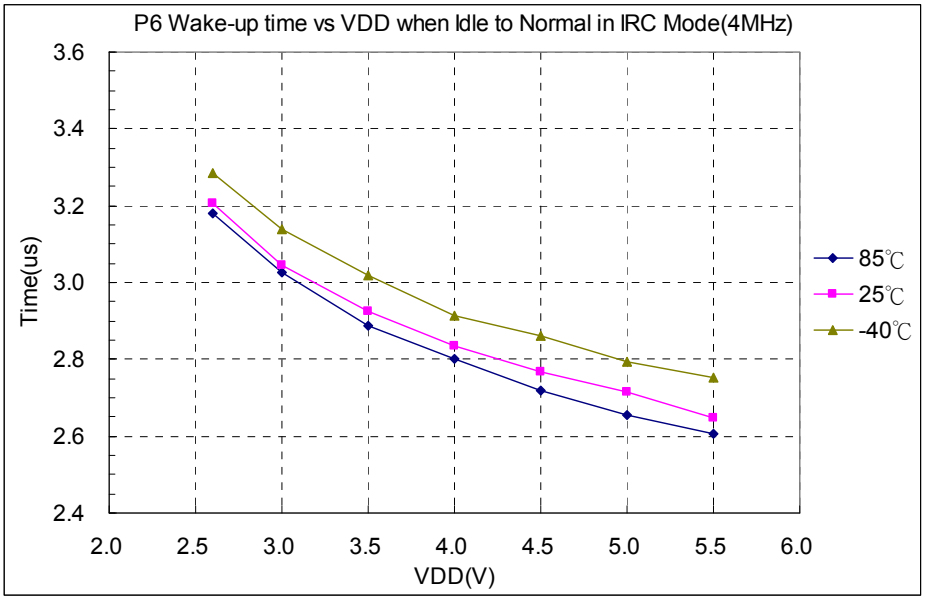


Figure 10-29 P6 Wake-up Time when Idle to Normal, IRC mode (Sub. Freq.=16kHz, 4 MHz)

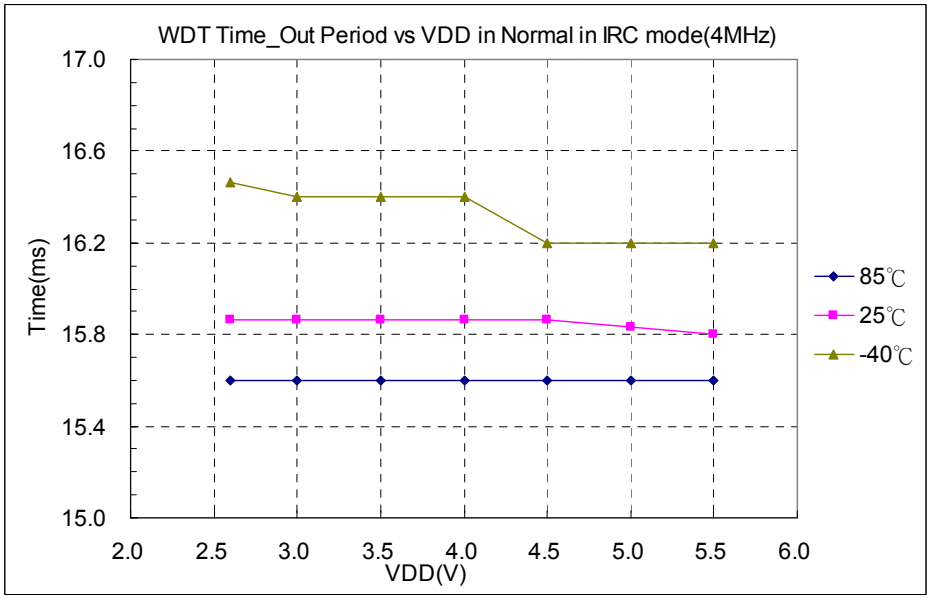


Figure 10-30 WDT Timer Time-out in Normal, IRC Mode (Sub. Freq.=16kHz, 4 MHz)

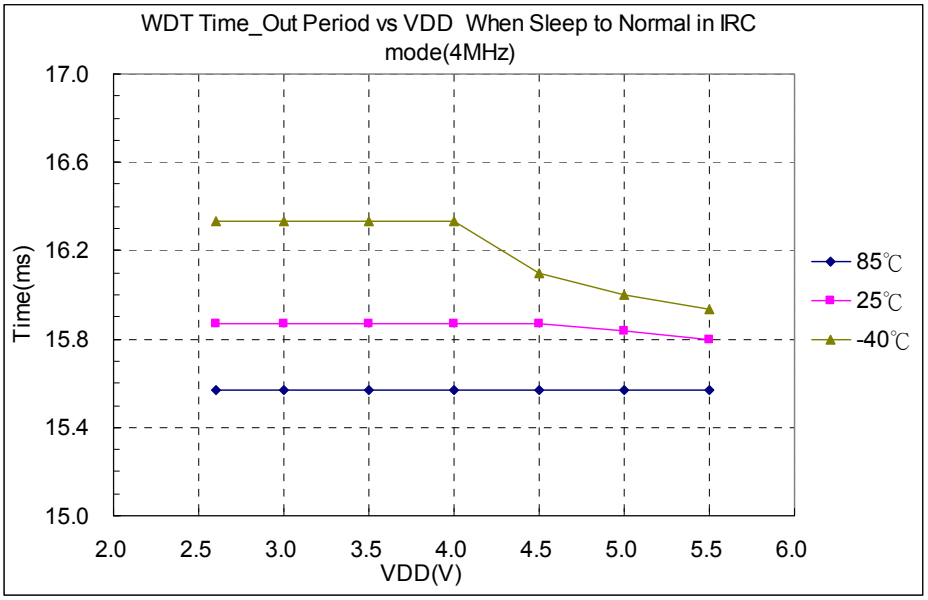


Figure 10-31 WDT Timer Time Out when Sleep to Normal, IRC Mode (4MHz)

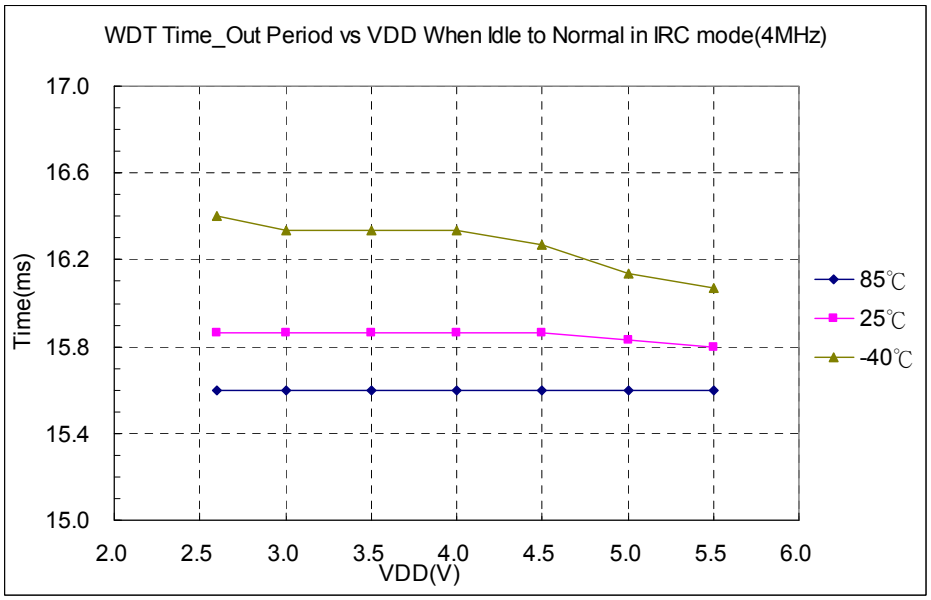


Figure 10-32 WDT Timer Time Out when Idle to Normal, IRC Mode (4MHz)

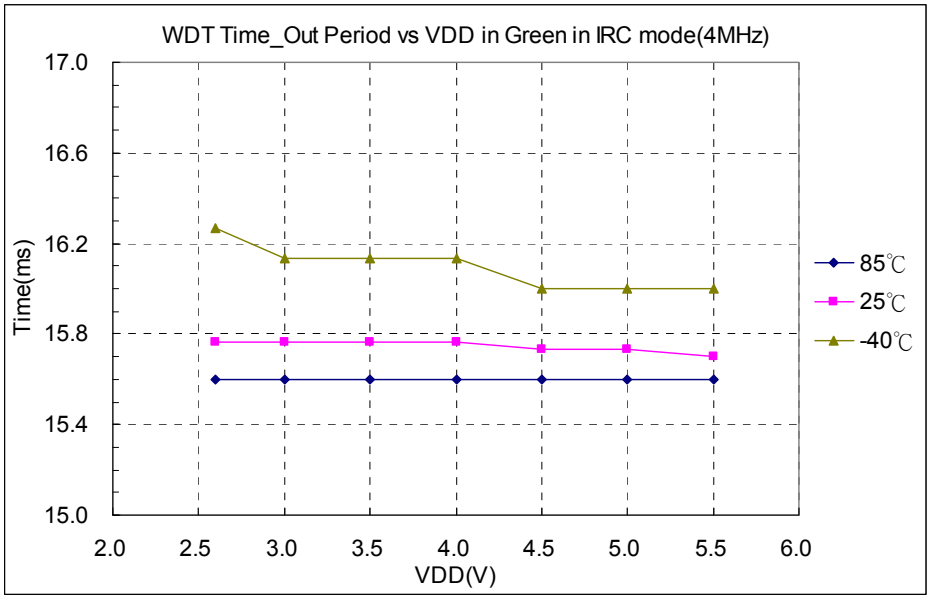


Figure 10-33 WDT Timer Time Out in Green mode, IRC Mode (4MHz)

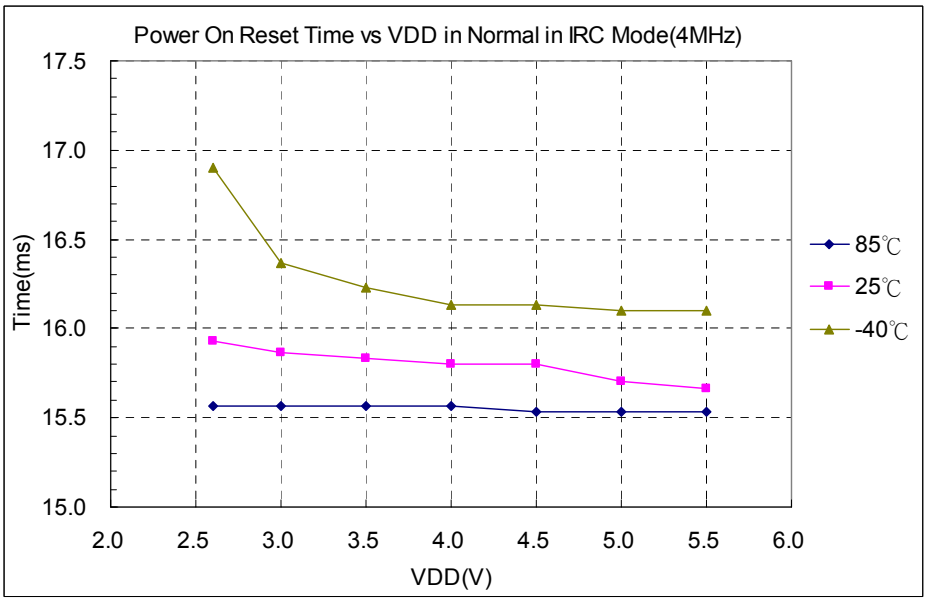


Figure 10-34 Power on Reset Time in Normal, IRC Mode (Sub. Freq.=16kHz, 4 MHz)

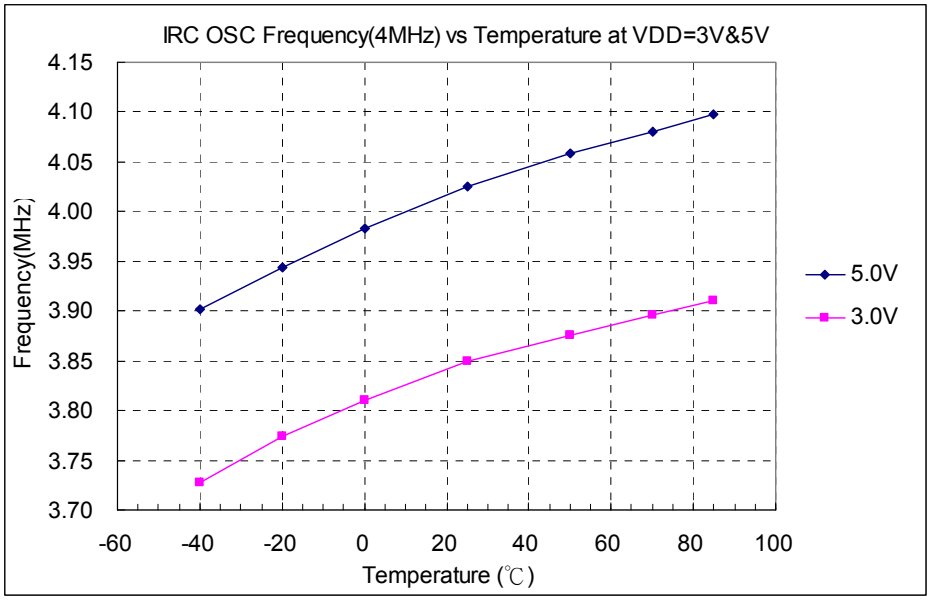


Figure 10-35 IRC OSC Freq, vs. Temp. (4MHz)

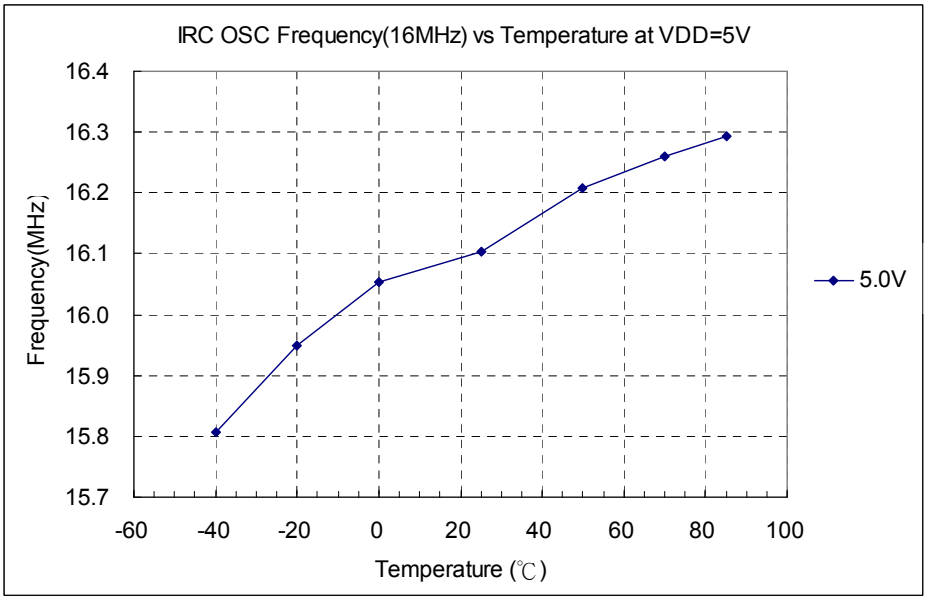


Figure 10-36 IRC OSC Freq, vs. Temp. (16MHz)

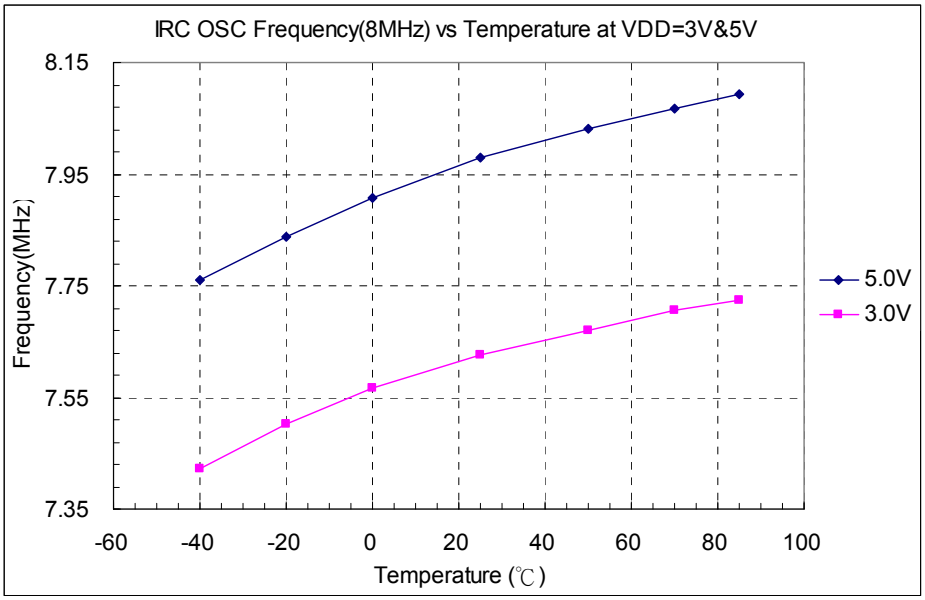


Figure 10-37 IRC OSC Freq, vs. Temp. (8MHz)

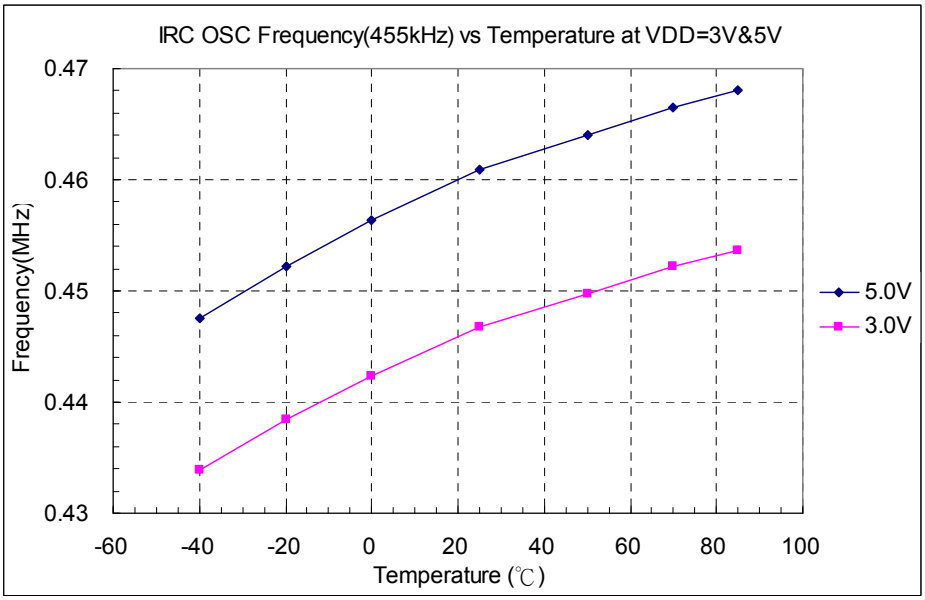


Figure 10-38 IRC OSC Freq, vs. Temp. (455KHz)

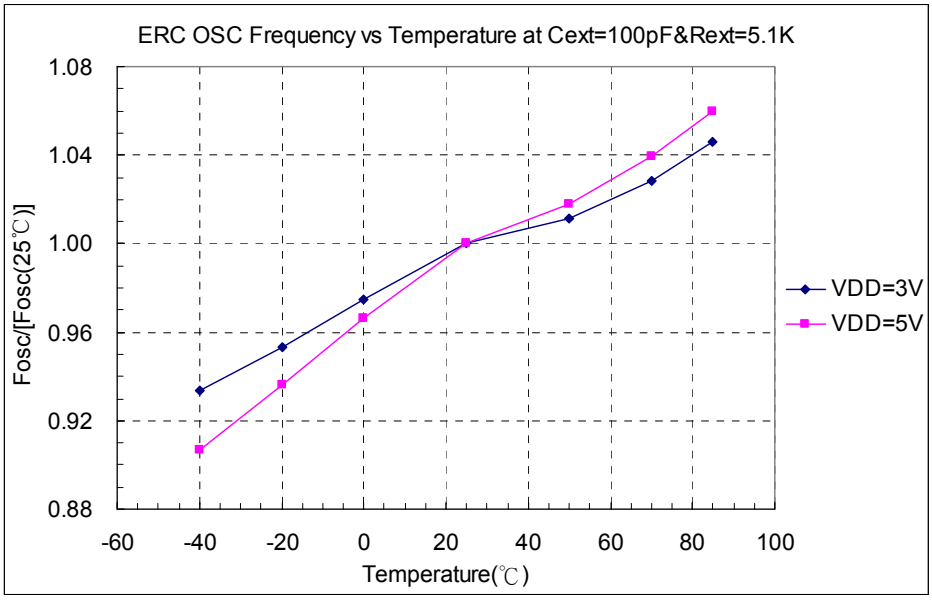


Figure 10-39 ERC OSC Frequency vs. Temp (C_{EXT}=100pf, R_{EXT}=5.1k)

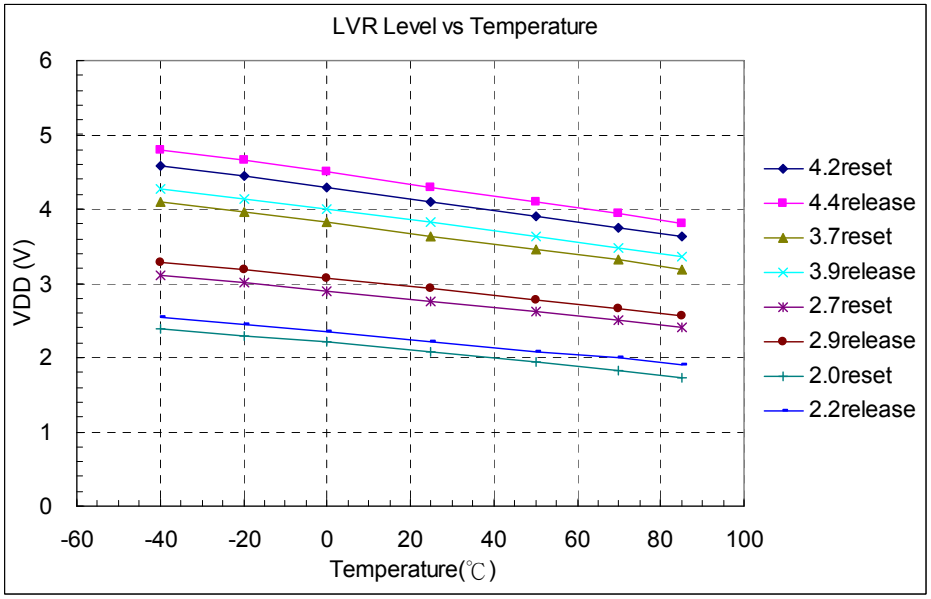


Figure 10-40 LVR Level vs Temperature

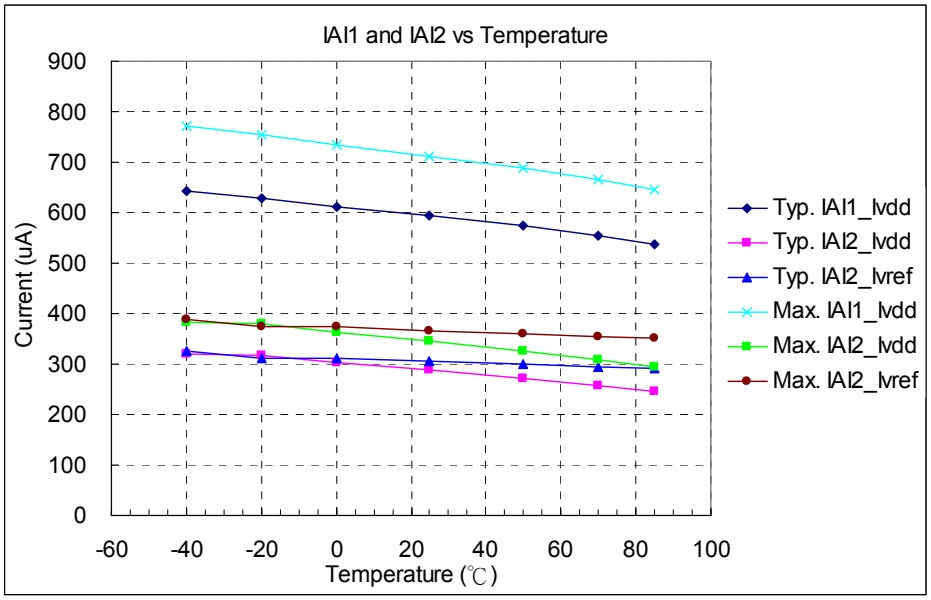


Figure 10-41 Typical & Maximum IAI1 and IAI2 vs Temperature

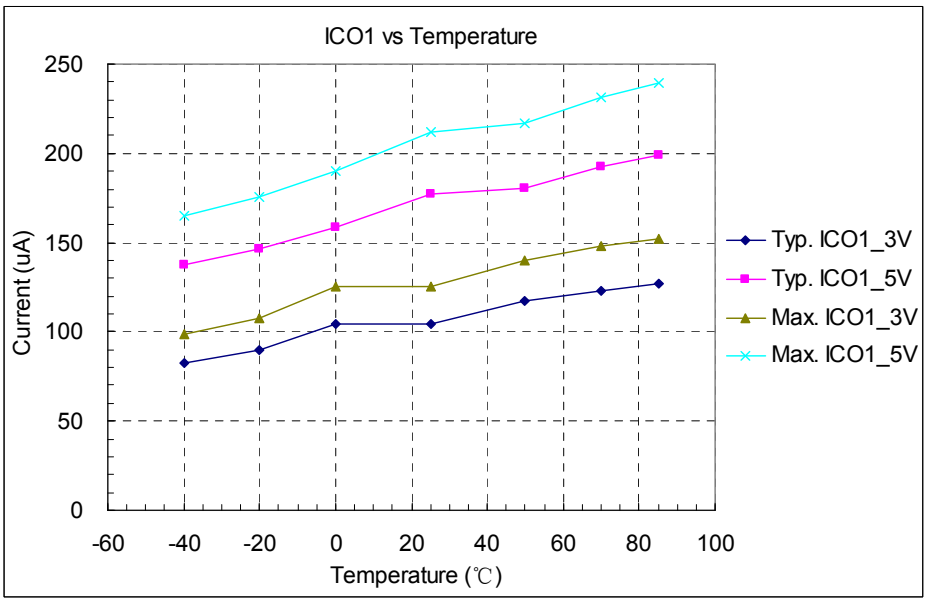


Figure 10-42 Typical & Maximum ICO1 vs Temperature

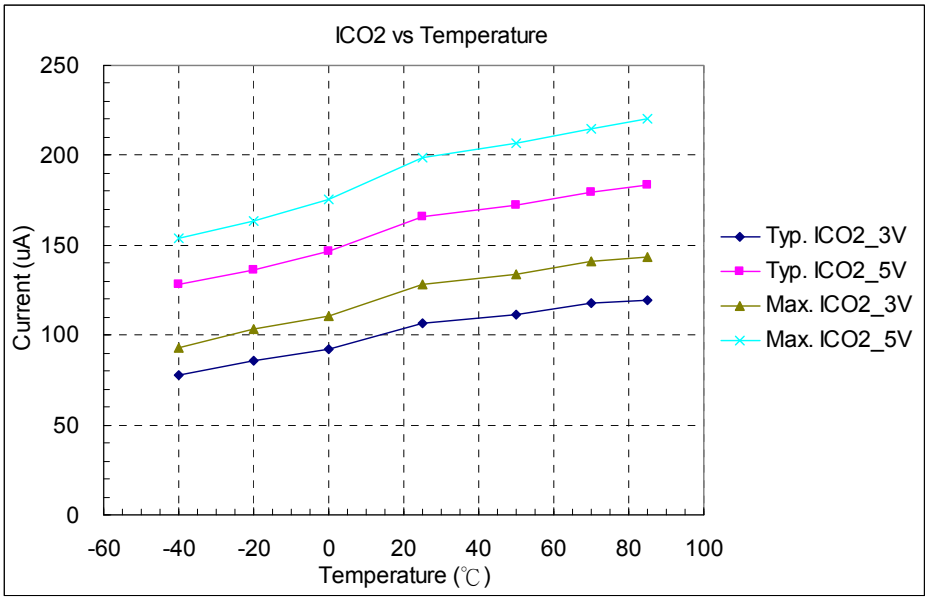


Figure 10-43 Typical and Maximum ICO2 vs Temperature

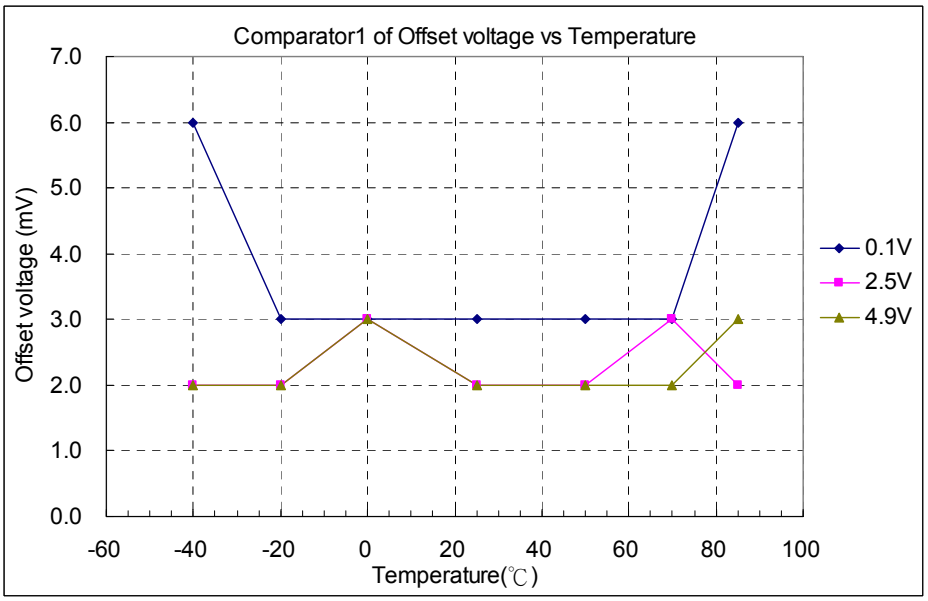


Figure 10-44 Comparator 1 of Offset voltage vs Temperature

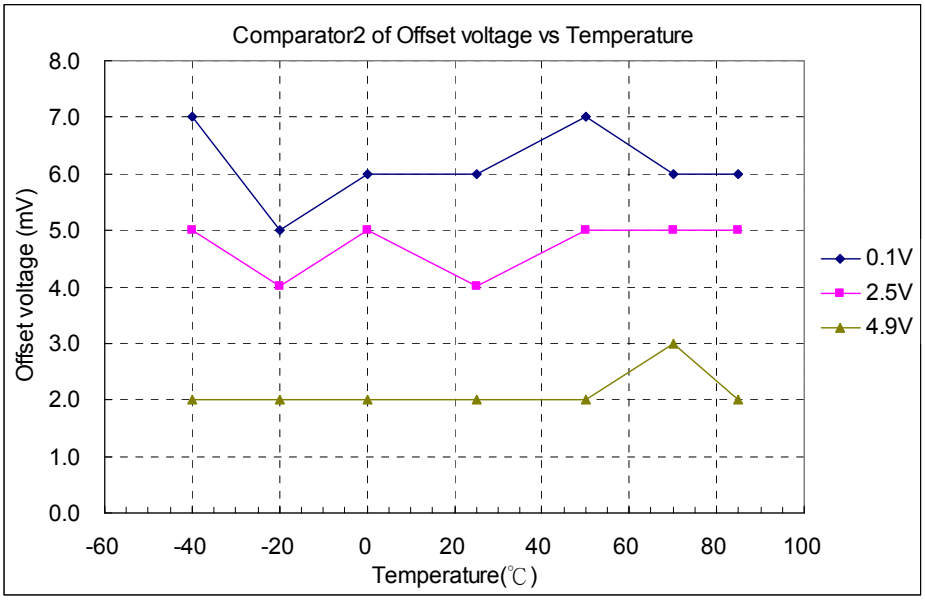
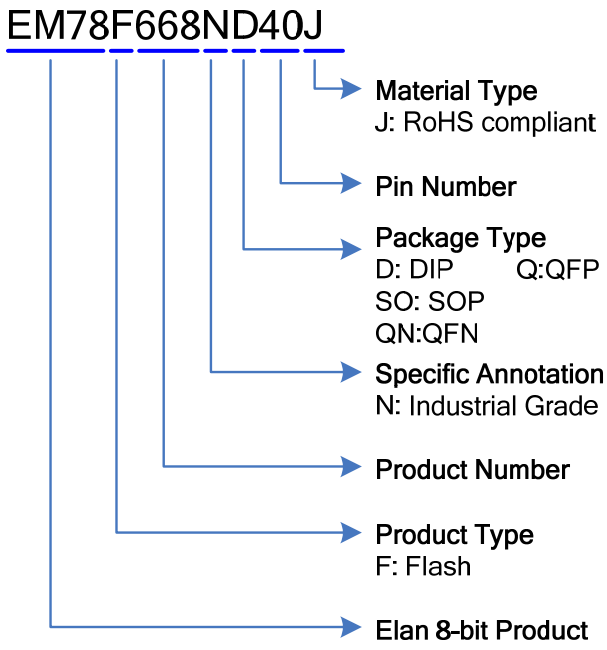


Figure 10-45 Comparator 2 of Offset voltage vs Temperature

APPENDIX

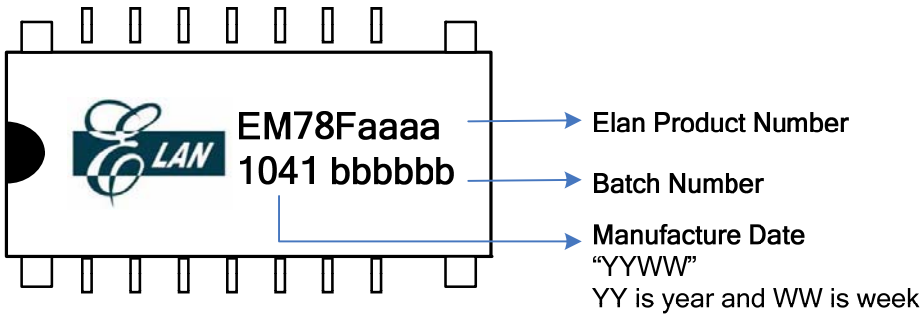
A Ordering and Production Information



For example:

EM78F668ND40J

is EM78F668N with Flash program memory, industrial grade product, in 40-pin DIP 600mil package, and RoHS compliant.



B Package Type

Flash MCU	Package Type	Pin Count	Package Size
EM78F668NK28J/S EM78F568NK28J/S	Skinny DIP	28	300 mil
EM78F668NSO28J/S EM78F568NSO28J/S	SOP	28	300 mil
EM78F668ND40J/S EM78F568ND40J/S	DIP	40	600 mil
EM78F668NQN32J/S EM78F568NQN32J/S	QFN	32	5×5 mm
EM78F668NQ44J/S EM78F568NQ44J/S	QFP	44	10×10 mm

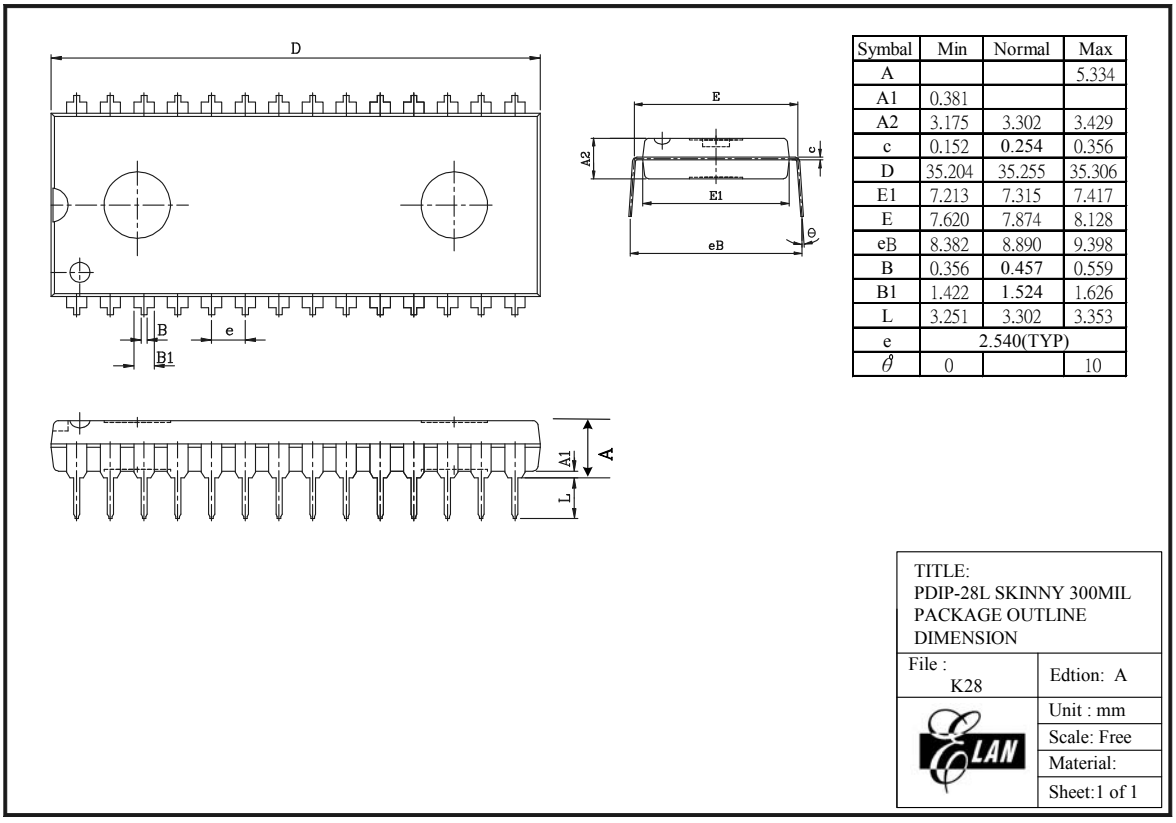
These are Green products which do not contain hazardous substances and comply with the third edition of Sony SS-00259 standard.

The Pb content is less than 100ppm and complies with Sony specifications.

Part No.	EM78F668NxJ/xS
Electroplate type	Pure Tin
Ingredient (%)	Sn: 100%
Melting point (°C)	232°C
Electrical resistivity (μΩ cm)	11.4
Hardness (hv)	8~10
Elongation (%)	>50%

C Packaging Configuration

C.1 EM78F668NK28 / EM78F568NK28

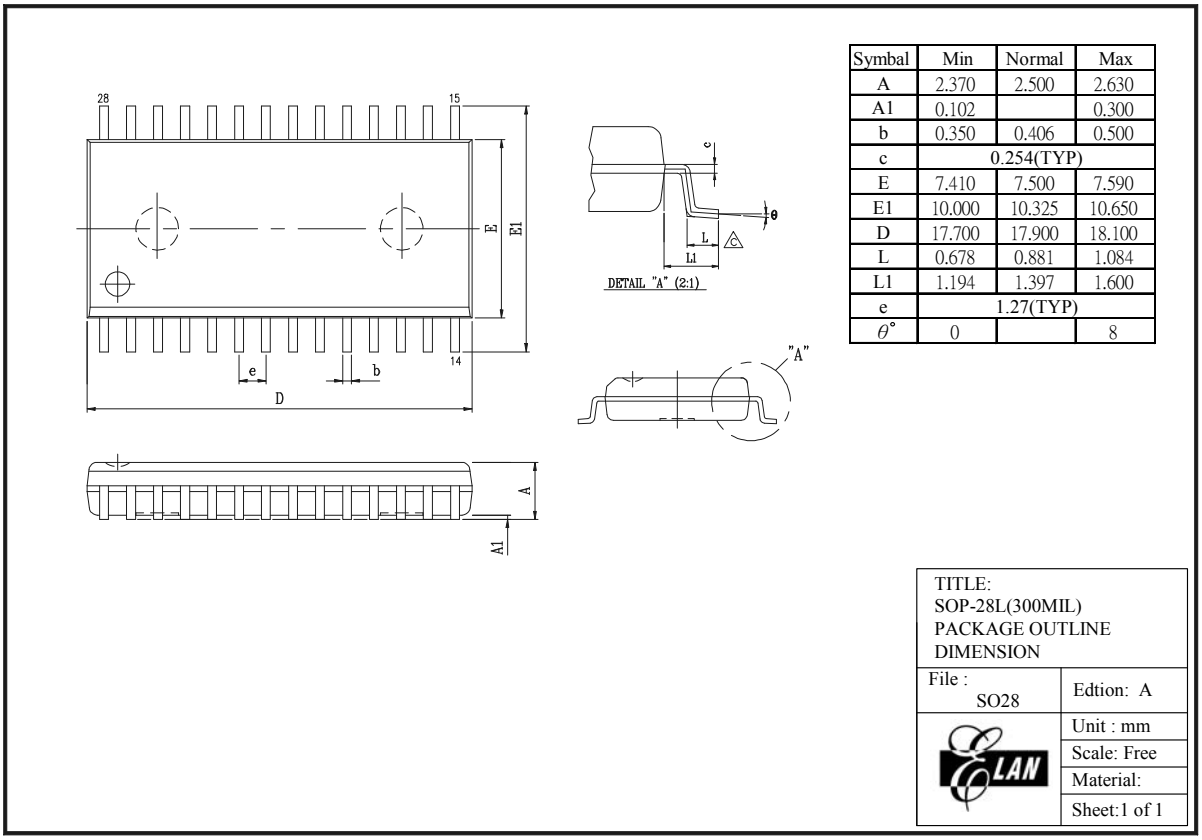


Symbal	Min	Normal	Max
A			5.334
A1	0.381		
A2	3.175	3.302	3.429
c	0.152	0.254	0.356
D	35.204	35.255	35.306
E1	7.213	7.315	7.417
E	7.620	7.874	8.128
eB	8.382	8.890	9.398
B	0.356	0.457	0.559
B1	1.422	1.524	1.626
L	3.251	3.302	3.353
e	2.540(TYP)		
θ	0		10

TITLE: PDIP-28L SKINNY 300MIL PACKAGE OUTLINE DIMENSION	
File : K28	Edtion: A
	Unit : mm
	Scale: Free
	Material:
	Sheet:1 of 1

Figure B-1 EM78F668N 28-pin Skinny DIP Package Type

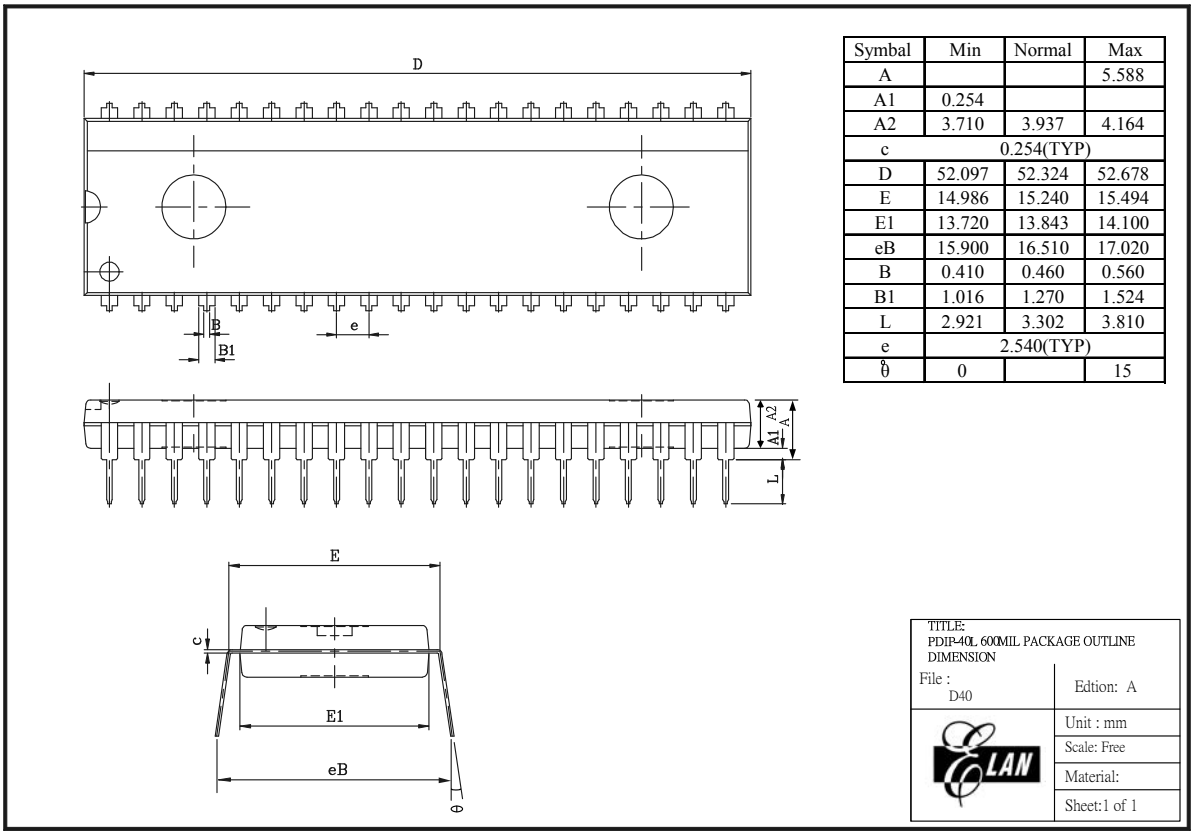
C.2 EM78F668NSO28 / EM78F568NSO28



Symbal	Min	Normal	Max
A	2.370	2.500	2.630
A1	0.102		0.300
b	0.350	0.406	0.500
c	0.254(TYP)		
E	7.410	7.500	7.590
E1	10.000	10.325	10.650
D	17.700	17.900	18.100
L	0.678	0.881	1.084
L1	1.194	1.397	1.600
e	1.27(TYP)		
θ°	0		8

Figure B-2 EM78F668N 28-pin SOP Package Type

C.3 EM78F668ND40 / EM78F568ND40



Symbal	Min	Normal	Max
A			5.588
A1	0.254		
A2	3.710	3.937	4.164
c		0.254(TYP)	
D	52.097	52.324	52.678
E	14.986	15.240	15.494
E1	13.720	13.843	14.100
eB	15.900	16.510	17.020
B	0.410	0.460	0.560
B1	1.016	1.270	1.524
L	2.921	3.302	3.810
e		2.540(TYP)	
θ	0		15

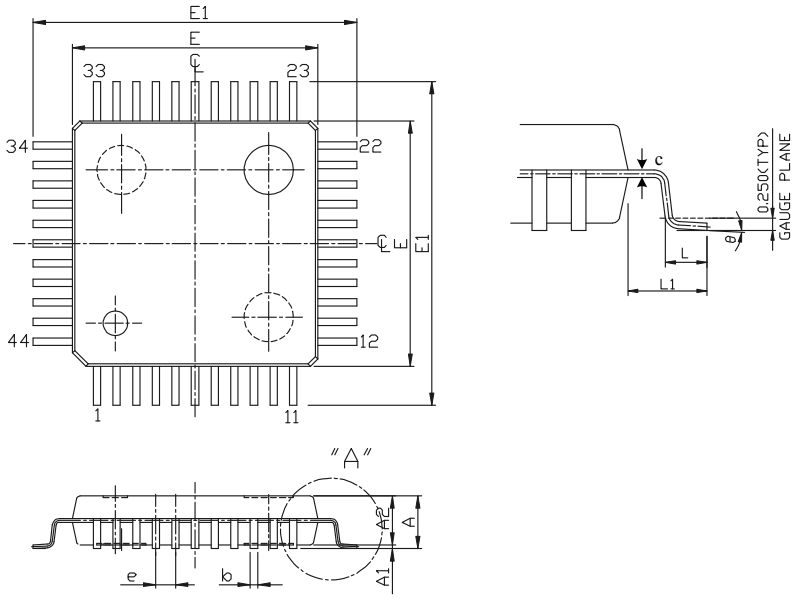
TITLE:
PDIP-40L 600MIL PACKAGE OUTLINE DIMENSION

File : D40 | Edtion: A

Unit : mm
Scale: Free
Material:
Sheet:1 of 1

Figure B-3 EM78F668N 40-pin DIP Package Type

C.4 EM78F668NQ44 / EM78F568NQ44

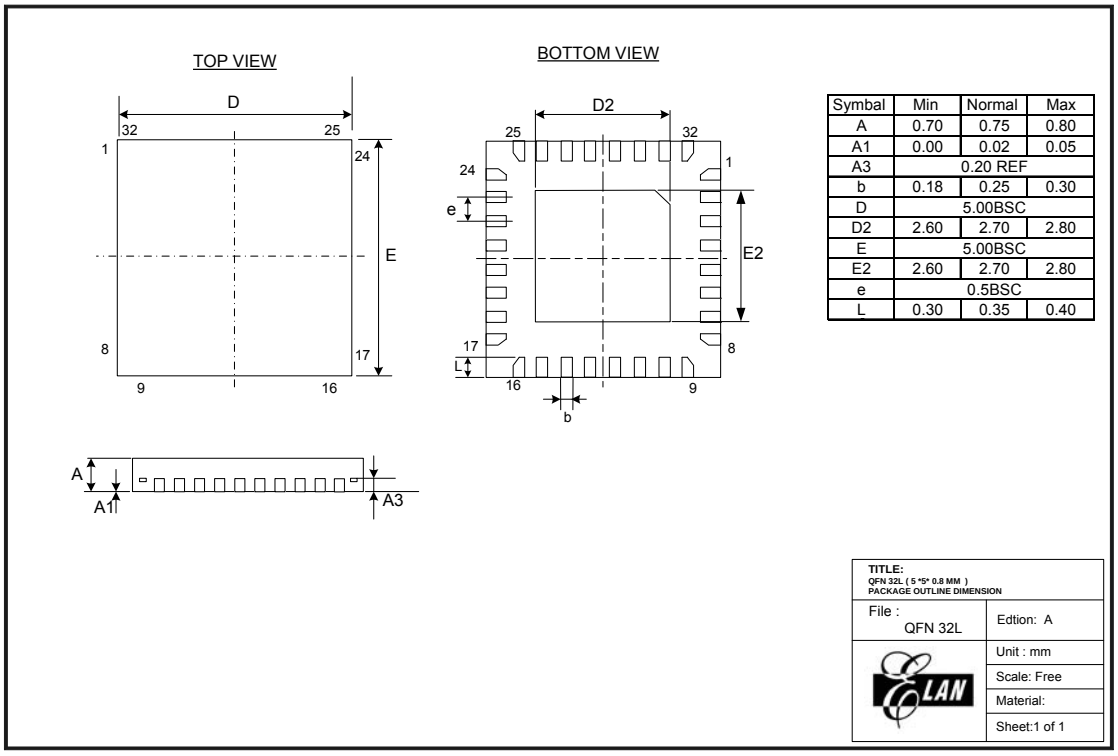


Symbal	Min	Normal	Max
A			2.70
A1	0.15		0.50
A2	1.80	2.00	2.20
b	0.30(TYP)		
c	0.15(TYP)		
E1	13.00	13.20	13.40
E	9.90	10.00	10.10
L	0.73	0.88	1.03
L1	1.50	1.60	1.70
e	0.80(TYP)		
θ°	0		7

TITLE: QFP-44L(10*10 MM) FOOTPRINT 3.2mm PACKAGE OUTLINE DIMENSION	
File : QFP44	Edtion: A
	Unit : mm
	Scale: Free
	Material:
	Sheet:1 of 1

Figure B-4 EM78F668N 44-pin QFP Package Type

C.5 EM78F668NQN32 / EM78F568NQN32



Symbal	Min	Normal	Max
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.20 REF	
b	0.18	0.25	0.30
D		5.00BSC	
D2	2.60	2.70	2.80
E		5.00BSC	
E2	2.60	2.70	2.80
e		0.5BSC	
L	0.30	0.35	0.40

TITLE:
QFN 32L (5 *5* 0.8 MM)
PACKAGE OUTLINE DIMENSION

File : QFN 32L | Edtion: A | Unit : mm | Scale: Free | Material: | Sheet:1 of 1

Figure B-5 EM78F668N 32-pin QFN Package Type

D Quality Assurance and Reliability

Test Category	Test Conditions	Remarks
Solderability	Solder temperature=245±5°C, for 5 seconds up to the stopper using a rosin-type flux	–
Pre-condition	Step 1: TCT, 65°C (15 min)~150°C (15 min), 10 cycles	For SMD IC (such as SOP, QFP, SOJ, etc)
	Step 2: Bake at 125°C, TD (endurance)=24 hrs	
	Step 3: Soak at 30°C/60%，TD (endurance)=192 hrs	
	Step 4: IR flow 3 cycles (Pkg thickness ≥ 2.5 mm or Pkg volume ≥ 350 mm^3 ----225±5°C) (Pkg thickness ≤ 2.5 mm or Pkg volume ≤ 350 mm^3 ----240 ± 5°C)	
Temperature cycle test	-65°C (15 min)~150°C (15 min), 200 cycles	–
Pressure cooker test	TA =121°C, RH=100%, pressure=2 atm, TD (endurance)= 96 hrs	–
High temperature / High humidity test	TA=85°C , RH=85%，TD (endurance) = 168 , 500 hrs	–
High-temperature storage life	TA=150°C, TD (endurance) = 500, 1000 hrs	–
High-temperature operating life	TA=125°C, VCC = Max. operating voltage, TD (endurance) = 168, 500, 1000 hrs	–
Latch-up	TA=25°C, VCC = Max. operating voltage, 150mA/20V	–
ESD (HBM)	TA=25°C, ≥｜± 3KV｜	IP_ND,OP_ND,IO_ND IP_NS,OP_NS,IO_NS IP_PD,OP_PD,IO_PD, IP_PS,OP_PS,IO_PS, VDD-VSS(+),VDD_VSS (-) mode
ESD (MM)	TA=25°C, ≥ ｜± 300V｜	

D.1 Address Trap Detect

An address trap detect is one of the MCU embedded fail-safe functions that detects MCU malfunction caused by noise or the like. Whenever the MCU attempts to fetch an instruction from a certain section of ROM, an internal recovery circuit is auto started. If a noise-caused address error is detected, the MCU will repeat execution of the program until the noise is eliminated. The MCU will then continue to execute the next program.