EM78F704N

8-Bit Microcontroller

Product Specification

DOC. VERSION 1.2

ELAN MICROELECTRONICS CORP.

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Specification Revision History

Doc. Version	Revision Description	Date
1.0	Initial version	2016/01/08
1.1	Modified the on-chip registers (SRAM) size.	2016/02/26
1.2	1. Modified the Package Type in the Features section 2. Modified Appendix A “Ordering and Manufacturing Information”	2016/08/16

1 General Description

The EM78F704N is an 8-bit microprocessor designed and developed with low-power, high-speed CMOS technology and high noise immunity. It has an on-chip 4K×13-bits Electrical Flash Memory and 128 bytes In-system programmable EEPROM. It provides three protection bits to prevent intrusion of user's Flash memory code.

The system application supports up to nine (9) touch keys which is applied to touch sensors.

With its enhanced Flash-ROM feature, the EM78F704N provides a convenient way of developing and verifying user's programs. Moreover, this Flash-ROM device offers the advantages of easy and effective program updates, using development and programming tools. Users can avail of the ELAN Writer to easily program their development codes.

2 Features

- **CPU Configuration**
  - 4K×13 bits Flash memory
  - 134 bytes on-chip registers (SRAM)
  - 128 bytes In-system programmable EEPROM
  - 8-level stacks for subroutine nesting
- **I/O Port Configuration**
  - Two bidirectional I/O ports
  - Up to nine (9) capacitive sensor pins
  - 3 Programmable pull-down I/O pins
  - 3 programmable pull-high I/O pins
- **Operating Voltage Range:**
  - 2.8V~5.5V @ – 25°C ~70°C
- **Operating Frequency Range (base on two clocks):**
  - IRC mode

Internal RC Frequency	Drift Rate			
	Voltage (3.0V ~ 3.6V)	Temperature (-10°C ~ +40°C)	Process	Total
4 MHz	±1%	±1%	±1%	±3%
8 MHz	±1%	±1%	±1%	±3%

- **One 16-bit Timer**
  - TC1 : Timer
- **One 8-bit Timer**
  - TC3 : Timer
- **One channels Analog-to-Digital Converter with 12-bit resolution**
- **Peripheral Configuration**
  - 8-bit real Timer Clock/Counter (TCC) with selective signal sources, trigger edges, and overflow interrupt
  - Power down (Sleep) mode
  - Four programmable Level Voltage Reset (LVR) (LVR) : 3.3V, 3.0V, 2.6V, and 2.0V (POR)
  - Three security registers to prevent intrusion of Flash memory codes
  - One configuration register to accommodate user's requirements
  - Two clocks per instruction cycle
  - High EFT immunity
  - Two sub-frequencies; 128kHz and 16kHz, the 16kHz is provided by dividing the 128kHz
- **Single instruction cycle commands**
- **Programmable free running Watchdog Timer**
- **Package Type:**
  - 24-pin SOP 300mil : EM78F704NSO24

Note: *These are Green Products which do not contain hazardous substances.*

3 Pin Assignment

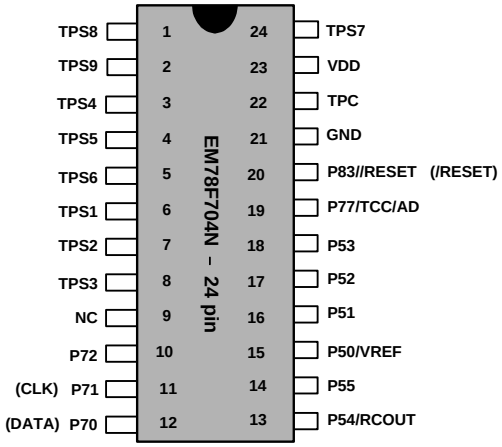


Figure 3-1 EM78F704NSO24

4 Pin Description

Table 1 EM78F704N Pin Description

Legend: ***ST:*** *Schmitt Trigger input* ***AN:*** *Analog Pin*
CMOS: *CMOS*

Name	Function	Input Type	Output Type	Description
P50/VREF	P50	ST	CMOS	Bidirectional I/O pin
	VREF	AN	–	ADC external voltage reference
P51	P51	ST	CMOS	Bidirectional I/O pin
P52	P52	ST	CMOS	Bidirectional I/O pin
P53	P53	ST	CMOS	Bidirectional I/O pin
P54/RCOUT	P54	ST	CMOS	Bidirectional I/O pin
	RCOUT	–	CMOS	Clock output of internal RC oscillator Clock output of external RC oscillator (open-drain)
P55	P55	ST	CMOS	Bidirectional I/O pin
P70 (DATA)	P70	ST	CMOS	Bidirectional I/O pin with programmable pull-high, pull-down
	(DATA)	ST	CMOS	DATA pin for Writer programming
P71 (CLK)	P71	ST	CMOS	Bidirectional I/O pin with programmable pull-high, pull-down
	(CLK)	ST	–	CLOCK pin for Writer programming
P72	P72	ST	CMOS	Bidirectional I/O pin with programmable pull-high, pull-down
P77/TCC/AD	P77	ST	CMOS	Bidirectional I/O pin
	TCC	ST	–	Real Time Clock/Counter clock input
	AD	AN	–	ADC Input
P83//RESET (/RESET)	P83	ST	CMOS	Bidirectional I/O pin
	/RESET	ST	–	Internal pull-high reset pin
	(/RESET)	ST	–	/RESET pin for Writer programming

(Continuation)

Name	Function	Input Type	Output Type	Description
TPS1 ~ TPS9	TPS1 ~ TPS9	AN	AN	Touchkey sensor pins
VDD **(VDD)**	VDD	Power	–	Power
	VDD	Power	–	VDD for Writer programming
VSS **(VSS)**	VSS	Power	–	Ground
	VSS	Power	–	VSS for Writer programming
TPC	TPC	AN	–	1 µF Touchpad capacitor
NC	NC	–	–	TEST pin, No Connection

5 Block Diagram

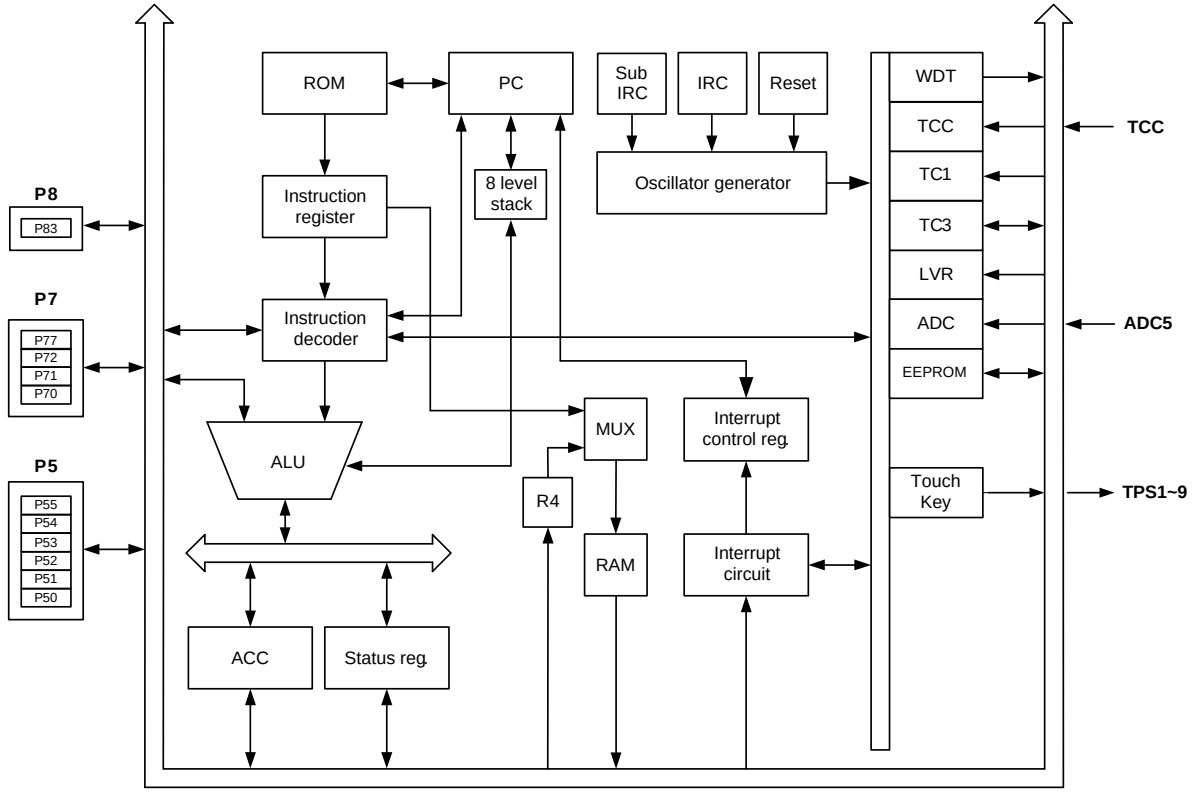


Figure 5-1 EM78F704N Functional Block Diagram

6 Functional Description

6.1 Operational Registers

6.1.1 R0 (Indirect Addressing Register)

R0 is not a physically implemented register. It is used as an indirect addressing pointer. Any instruction using R0 as a pointer actually accesses data pointed by the RAM Select Register (R4).

6.1.2 R1 (Timer Clock/Counter)

R1 is incremented by an external signal edge, which is defined by TE bit (CONT-4) through the TCC pin, or by the instruction cycle clock. It is writable and readable as any other registers. It is defined by resetting PSTE (CONT-3).

The prescaler is assigned to TCC, if the PSTE bit (CONT-3) is reset. The contents of the prescaler counter are cleared only when the TCC register is written with a value.

6.1.3 R2 (Program Counter) and Stack

Depending on the device type, R2 and hardware stack are 10-bit wide. The structure is depicted in Figure 6-1.

The configuration structure generates 4K×13 bits on-chip Flash ROM addresses to the relative programming instruction codes. One program page is 1024 words long.

R2 is set as all “0”s when under a reset condition.

“JMP” instruction allows direct loading of the lower 10 program counter bits. Thus, “JMP” allows PC to go to any location within a page (1K).

“CALL” instruction loads the lower 10 bits of the PC, and then PC+1 is pushed into the stack. Thus, the subroutine entry address can be located anywhere within a page.

“LJMP” instruction allows direct loading of the program counter bits (A0~A11). Thus, “LJMP” allows the PC to go to any location within 4K (2^{12}).

“LCALL” instruction loads the program counter bits (A0~A11), and PC+1 are pushed onto the stack. Thus, the subroutine entry address can be located anywhere within 4K (2^{12}).

“RET” (“RETL k”, “RETI”) instruction loads the program counter with the contents of the top-level stack.

“ADD R2, A” allows a relative address to be added to the current PC, and the ninth and above bits of the PC will increase progressively.

"MOV R2, A" allows loading an address from the "A" register to the lower 8 bits of the PC, and the ninth and tenth bits of the PC remain unchanged.

Any instruction except "ADD R2,A" that is written to R2 (e.g. "MOV R2, A", "BC R2, 6") will cause the ninth bit and the tenth bit (A8~A9) of the PC to remain unchanged.

All instructions are single instruction cycle (fclk/2) except for the instructions that would change the contents of R2 and "LCALL", "LJMP", "TBRD" instruction. The "LCALL", "LJMP" and "TBRD" instructions need two instruction cycles.

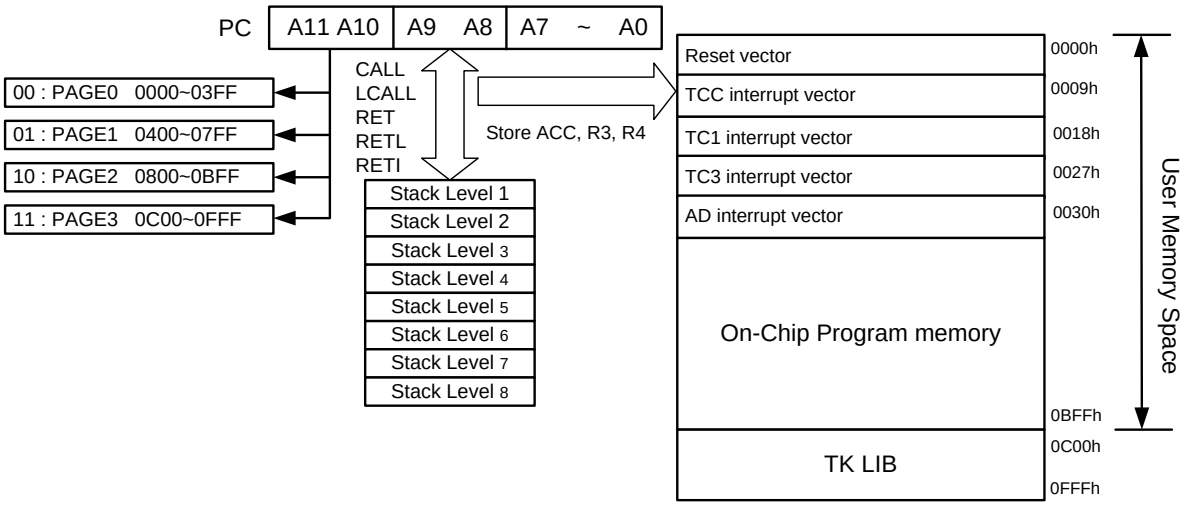


Figure 6-1 Program Counter Organization

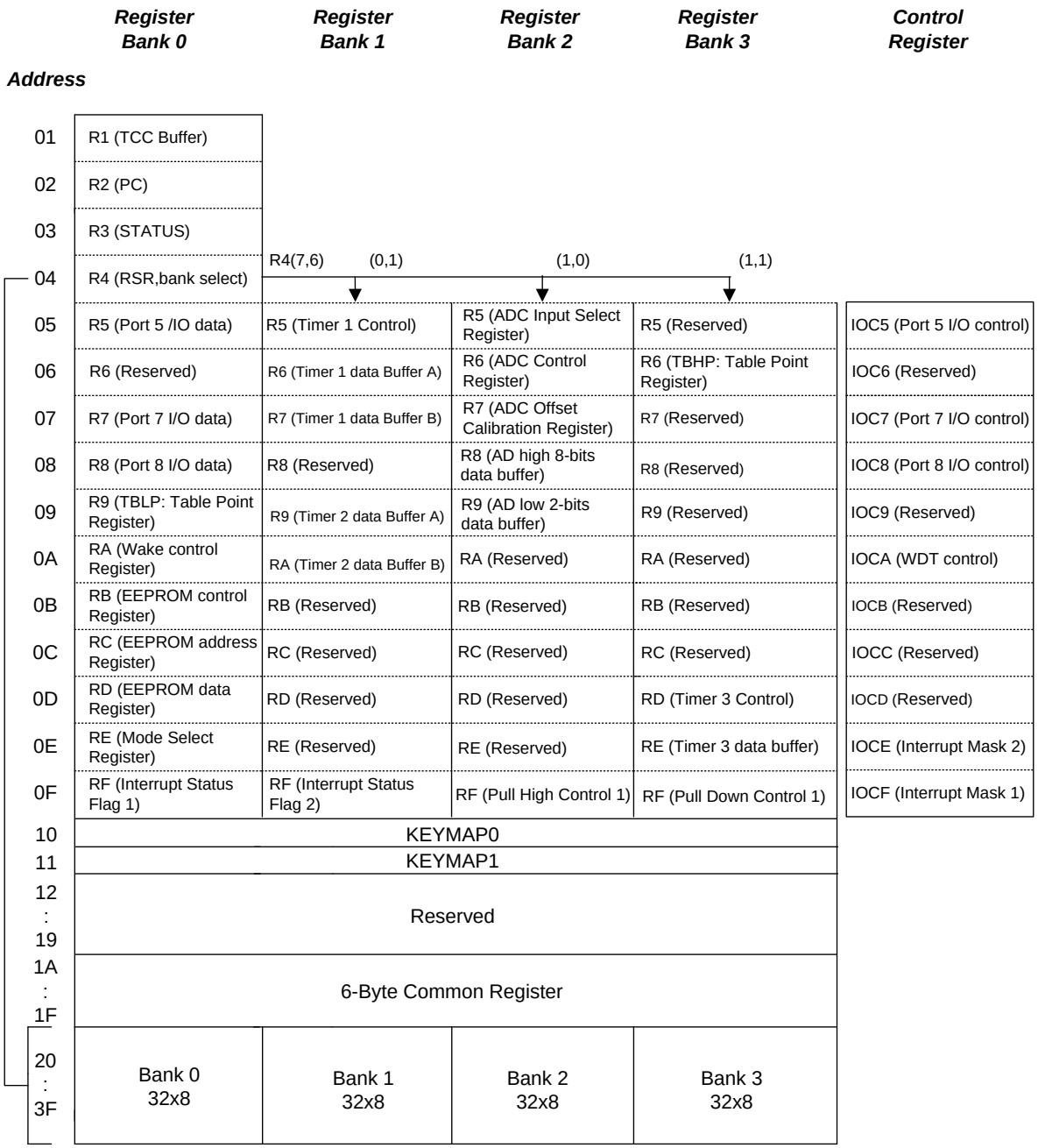


Figure 6-2 Data Memory Configuration

6.1.4 R3 (Status Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
–	–	–	T	P	Z	DC	C

Bits 7 ~ 5: Not used, set to "**0**" at all time

Bit 4 (T): Time-out bit

Set to "**1**" with the "SLEP" and "WDTC" commands, or during power up and reset to "**0**" by WDT time-out.

Bit 3 (P): Power down bit

Set to "**1**" during power on or by a "WDTC" command and reset to "**0**" by a "SLEP" command.

Bit 2 (Z): Zero flag

Set to "**1**" if the result of an arithmetic or logic operation is zero.

Bit 1 (DC): Auxiliary carry flag

Bit 0 (C): Carry flag

6.1.5 R4 (RAM Select Register)

Bits 7 ~ 6: Used to select Bank 0 ~ Bank 3

Bits 5 ~ 0: Used to select registers (Address: 00~3F) in indirect addressing mode.

See the data memory configuration in Figure 6-2.

6.1.6 Bank 0 R5 ~ R8 (Port 5 ~ Port 8)

R5 ~ R8 are I/O registers.

6.1.7 Bank 0 R9 TBPTL (Low byte of Table Pointer Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RBit 7	RBit 6	RBit 5	RBit 4	RBit 3	RBit 2	RBit 1	RBit 0

6.1.8 Bank 0 RA (Wake- up Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	ADWE	-	-	-	–	–

Bits 7 ~ 6: Not used, set to "**0**" at all time

Bit 5 (ADWE): ADC wake-up enable bit

0 : Disable ADC wake-up

1 : Enable ADC wake-up

When ADC completed status is used to enter the interrupt vector or to wake up the EM78F704N from sleep, with A/D conversion running, the ADWE bit must be set to "Enable".

Bits 4 ~ 0: Not used, set to "**0**" at all time

6.1.9 Bank 0 RB (EEPROM Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RD	WR	EEWE	EEDF	EEPC	-	-	-

Bit 7 (RD): Read control register

0 : Does not execute EEPROM read

1 : Read EEPROM content, (RD can be set by software, RD is cleared by hardware after Read instruction is completed)

Bit 6 (WR): Write control register

0 : Write cycle to the EEPROM is completed.

1 : Initiate a write cycle, (WR can be set by software, WR is cleared by hardware after Write cycle is completed)

Bit 5 (EEWE): EEPROM Write Enable bit.

0 : Prohibit write to the EEPROM

1 : Allows EEPROM write cycles

Bit 4 (EEDF): EEPROM Detective Flag

0 : Write cycle is completed

1 : Write cycle is unfinished

Bit 3 (EEPC): EEPROM power-down control bit

0 : Switch off the EEPROM

1 : EEPROM is operating

Bits 2 ~ 0: Not used, set to "**0**" at all time

6.1.10 Bank 0 RC (EEPROM Address)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	EE_A6	EE_A5	EE_A4	EE_A3	EE_A2	EE_A1	EE_A0

Bits 6 ~ 0: EEPROM address

6.1.11 Bank 0 RD (EEPROM Data)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EE_D7	EE_D6	EE_D5	EE_D4	EE_D3	EE_D2	EE_D1	EE_D0

Bits 7 ~ 0: EEPROM data

6.1.12 Bank 0 RE (CPU Operating Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	TIMERSC	CPUS	IDLE-	-			

Bit 7: Not used, set to "**0**" at all time

Bit 6 (TIMERSC): TCC, TC1, TC3 clock source select

0 : Fs. Fs: sub frequency for WDT internal RC time base

1 : Fm. Fm: main-oscillator clock

Bit 5 (CPUS): CPU Oscillator Source Select

0 = Sub-oscillator (fs)

1 = Main oscillator (fosc)

When CPUS=0, the CPU oscillator selects a sub-oscillator and the **main oscillator is stopped**.

Bit 4 (IDLE): Idle Mode Enable Bit. This bit determines the Idle mode status under SLEP instruction.

0 : IDLE="**0**"+SLEP instruction → Sleep mode

1 : IDLE="**1**"+SLEP instruction → Idle mode

■ **CPU Operation Mode**

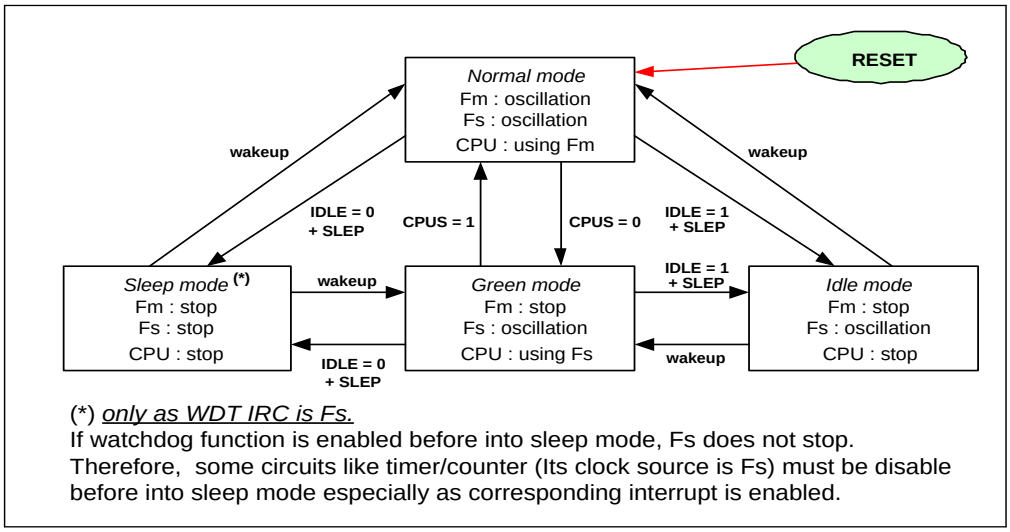


Figure 6-3 CPU Operation Mode

Bits 3 ~ 0: Not used, set to "**0**" at all time

6.1.13 Bank 0 RF (Interrupt Status Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
–	ADIF	-	-	-	-	-	TCIF

Note: ***" 1 "*** *means with interrupt request* ***" 0 "*** *means no interrupt occurs*

Bit 7: Not used, set to "**0**" at all time

Bit 6 (ADIF): Interrupt flag for analog to digital conversion. Set when AD conversion is completed, reset by software.

Bits 5 ~ 1: Not used, set to "**0**" at all time

Bit 0 (TCIF): TCC overflow interrupt flag. Set when TCC overflows, reset by software.

Bank 0 RF can be cleared by instruction but cannot be set.

IOCF is the interrupt mask register.

NOTE
The result of reading Bank 0 RF is the "Logic AND" of Bank 0 RF and IOCF.

6.1.14 R10 (Button Status 0)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Btn7	Btn6	Btn5	Btn4	Btn3	Btn2	Btn1	Btn0

Bits 7 ~ 0 (Btn7 ~ Btn0): There are 8 bits representing Buttons 0 ~ 7 individual status. From the register, to get whether button is touched or untouched.

User can read this register to check the button status.

0 : Button is untouched

1 : Button is touched

6.1.15 R11 (Button Status 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	-	-	Btn8

Bits 7 ~ 1: Unused bits. Read 0 only.

Bit 0 (Btn8): Button 8 status. From the bit to get whether button is touched or untouched. User can read this register to check the button status.

0 : Button is untouched

1 : Button is touched

6.1.16 R12 ~ R17 (Reserved)

These are TK LIB RAM Reserved.

6.1.17 R18 ~ R1F, Bank 0/1/2/3 R20 ~ R3F

These are all 8-bit general-purpose registers.

6.1.18 Bank 1 R5 TC1CR (Timer 1 Control)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	TC1S	-	-	TC1MOD	TCK1CK2	TC1CK1	TC1CK0

Bit 7: Not used, set to "**0**" at all time

Bit 6 (TC1S): Timer1 start control

0 : Stop and clear Timer 1

1 : Start Timer 1

Bits 5 ~ 4: Not used, set to "**0**" at all time

Bit 3 (TC1MOD): Timer Operation Mode Selection Bit

0: Two 8-bit timers

1: Timer 1 and 2 are cascaded as one 16-bit timer. The corresponding control register of 16-bit timer is from Timer 1. TC1DA and TC2DA are low byte. TC1DB and TC2DB are high byte.

Bit 2 ~ Bit 0 (TC1CK2 ~ TC1CK0): Timer1 clock source select

TC1CK2	TC1CK1	TC1CK0	Clock Source	Resolution 8 MHz	Max. time 8 MHz	Resolution 16kHz	Max. time 16kHz
			Normal	F_C=8M	F_C=8M	F_C=16K	F_C=16K
0	0	0	$F_C/2^{23}$	1.05s	19.1hr	145hr	9544hr
0	0	1	$F_C/2^{13}$	1.024ms	67.11s	512ms	33554.432s
0	1	0	$F_C/2^8$	32μs	2.097s	16ms	1048.576s
0	1	1	$F_C/2^3$	1μs	65.536ms	0.5ms	32768ms
1	0	0	$F_C/2^2$	0.5μs	32.768ms	0.25ms	16384ms
1	0	1	$F_C/2$	0.25μs	16.384ms	125μs	8192ms
1	1	0	F_C	125ns	8.192ms	0.0625ms	4096ms
1	1	1	-	-	-	-	-

Bits 1 ~ 0: Not used, set to "**0**" at all time.

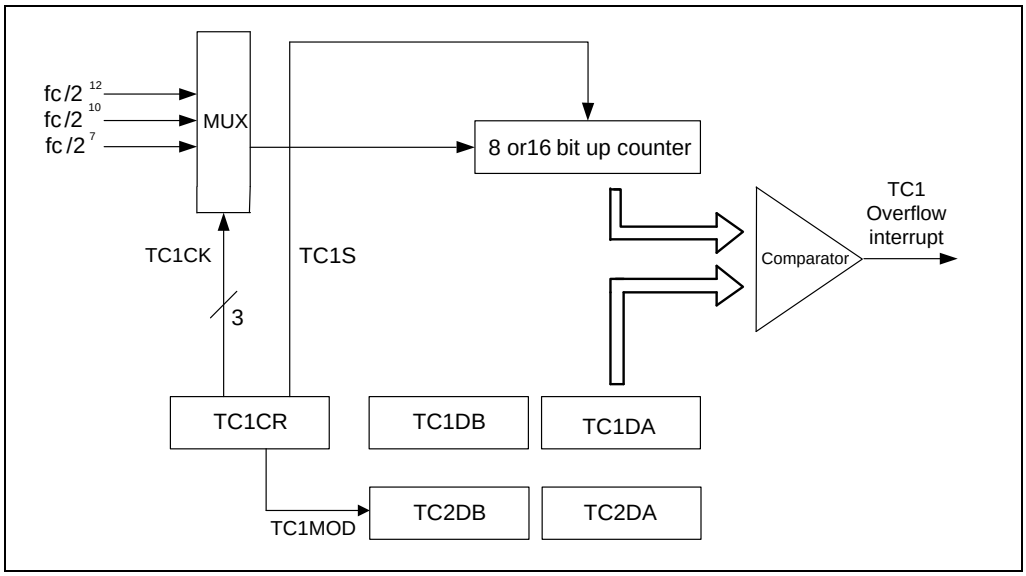


Figure 6-4 Timer 1 Configuration

In Timer mode, counting up is performed using the internal clock. When the contents of the up-counter matched with the TC1DA, interrupt is generated and the counter is cleared. Counting up resumes after the counter is cleared. The current contents of the up-counter are loaded into TC1DB. The timer mode will operate with 16 bits by setting TC1MOD to "1"

6.1.19 Bank 1 R6 TC1DA (Timer 1 Data Buffer A)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TC1DA7	TC1DA6	TC1DA5	TC1DA4	TC1DA3	TC1DA2	TC1DA1	TC1DA0

Bit 7 ~ Bit 0 (TC1DA7 ~ TC1DA0): Data buffer of 8-bit Timer1.

6.1.20 Bank 1 R7 TC1DB (Timer 1 Data Buffer B)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TC1DB7	TC1DB6	TC1DB5	TC1DB4	TC1DB3	TC1DB2	TC1DB1	TC1DB0

Bit 7 ~ Bit 0 (TC1DB7 ~ TC1DB0): Data buffer of 8-bit Timer 1.

6.1.21 Bank 1 R8 (Reserved)

Reserved Register

6.1.22 Bank 1 R9 TC2DA (Timer 2 Data Buffer A)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TC2DA7	TC2DA6	TC2DA5	TC2DA4	TC2DA3	TC2DA2	TC2DA1	TC2DA0

Bits 7~0 (TC2DA7~ TC2DA0): Data buffer of 8-bit Timer 2 cascades with Timer 1 at TC1MOD set to "1"

6.1.23 Bank 1 RA TC2DB (Timer 2 Data Buffer B)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TC2DB7	TC2DB6	TC2DB5	TC2DB4	TC2DB3	TC2DB2	TC2DB1	TC2DB0

Bit 7 ~ Bit 0 (TC2DB7 ~ TC2DB0): Data buffer of 8-bit Timer 2 cascades with Timer 1 at TC1MOD set to "1".

6.1.24 Bank 1 RB ~RE (Reserved)

These are reserved registers.

6.1.25 Bank 1 RF (Interrupt Status Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	TCIF3	–	TCIF1	-	-	-

***Note: " 1 "** means with interrupt request **" 0 "** means no interrupt occurs*

Bits 7~6: Not used, set to "**0**" at all time

Bit 5 (TCIF3): 8-bit Timer 3 interrupt flag. The Interrupt flag is cleared by software.

Bit 4: Not used, set to "**0**" at all time

Bit 3 (TCIF1): 8-bit Timer 1 interrupt flag. The Interrupt flag is cleared by software.

Bits 2~0: Not used, set to "0" at all time

Bank 1 RF can be cleared by instruction but cannot be set.

IOCE is the interrupt mask register.

NOTE
The result of reading Bank 1 RF is the "Logic AND" of Bank 1 RF and IOCE.

6.1.26 Bank 2 R5 AISR (ADC Input Select Register)

The AISR register for ADC pins act as analog input or digital I/O.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	ADE	-	-	-	-	-

Bits 7 ~ 6: Not used, set to "**0**" at all time

Bit 5 (ADE): AD converter enable bit of P77 pin

0 : Disable ADC, P77 functions as I/O pin

1 : Enable ADC to function as analog input pin

Bits 4 ~ 0: Not used, set to "**0**" at all time

6.1.27 Bank 2 R6 ADCON (A/D Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
VREFS	CKR1	CKR0	ADRUN	ADPD	ADIS2	ADIS1	ADIS0

Bit 7 (VREFS): The input source of the Vref of the ADC.

0 : Vref of the ADC is connected to the Internal reference which is selected by Bank 2 R9<5,4>(default value), and the P50/VREF pin carries out the function of P50

1 : Vref of the ADC is connected to P50/VREF

Bit 6 ~ Bit 5 (CKR1 ~ CKR0): The oscillator clock rate of ADC

CKR1/CKR0	Operation Mode	Max. Operation Frequency
00	$F_{OSC}/4$	4 MHz
10	$F_{OSC}/16$	8 MHz

RCM[1:0]*	Frequency (MHz)	Sample and Hold Timing
00	4	8 x T_{AD}
10	8	12 x T_{AD}

Bit 4 (ADRUN): ADC starts to run

0 : Reset upon completion of AD conversion. This bit cannot be reset by software.

1 : A/D conversion is started. This bit can be set by software.

Bit 3 (ADPD): ADC Power-down mode

0 : Switch off the resistor reference to save power even while the CPU is operating.

1 : ADC is operating

Bits 2~0 (ADIS2~ADIS0): AD Input Select Bits

ADIS2	ADIS1	ADIS0	AD Input Pin
1	0	1	AD

6.1.28 Bank 2 R7 ADOC (A/D Offset Calibration Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
–	–	–	–	–	PDE	Reserved	Reserved

Bits 7~3: Not used, set to "**0**" at all time

Bit 2 (PDE): 1/2 VDD Power Detect Enable bit

0 : Disable Power Detect (Default)

1 : Enable Power Detect

PDE	ADIS2	ADIS1	ADIS0	AD Input Select
1	–	–	–	1/2VDD
0	1	0	1	AD

Bits 1~0: Reserved, must be set to "**0**" at all time

6.1.29 Bank 2 R8 ADDH (AD High 8-Bit Data Buffer)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADD11	ADD10	ADD9	ADD8	ADD7	ADD6	ADD5	ADD4

When the A/D conversion is completed, the result which is high 8-bit is loaded into the ADDH. The ADRUN bit is cleared, and the ADIF is set. R8 is read only.

6.1.30 Bank 2 R9 ADDL (AD Low 4-Bit Data Buffer)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	IRVS1	IRVS0	ADD3	ADD2	ADD1	ADD0

Bits 7 ~ 6: Not used, set to "**0**" at all time

Bits 5 ~ 4 (IRVS1~IRVS0): Internal Reference Voltage Selection.

IRVS[1:0]	Reference Voltage
00	AVDD
01	4 V
10	3 V
11	2.5 V

Bits 3 ~ 0: AD low 4-bit data buffer.

6.1.31 Bank 2 RA ~ RE (Reserved)

These are reserved registers.

6.1.32 Bank 2 RF (Pull-high Control Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	/PH72	/PH71	/PH70

Bits 7 ~ 3: Not used, set to "**0**" at all time.

Bit 2 (/PH72): Control bit used to enable pull-high of the P72 pin

0 : Enable internal pull-high

1 : Disable internal pull-high

Bit 1 (/PH71): Control bit used to enable pull-high of the P71 pin.

Bit 0 (/PH70): Control bit used to enable pull-high of the P70 pin.

The RF Register is both readable and writable.

6.1.33 Bank 3 R5 (Reserved)

Reserved Register

6.1.34 Bank 3 R6 TBPTH (High Byte of Table Pointer Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MLB	0	0	0	RBit 11	RBit 10	RBit 9	RBit 8

Bit 7 (MLB): Take MSB or LSB at machine code.

Bits 6 ~ 4: Not used. Set to "**0**" at all time.

Bits 3 ~ 0: Table Pointer Address Bits 11~8.

6.1.35 Bank 3 R7~RC (Reserved)

Reserved Registers

6.1.36 Bank 3 RD TC3CR (Timer 3 Control)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	TC3S	TC3CK2	TC3CK1	TC3CK0	TC3M1	TC3M0

Bits 7 ~ 6: Not used, set to "**0**" at all time

Bit 5 (TC3S): Timer 3 start control

0 : Stop and clear Timer 3

1 : Start Timer 3

Bit 4 ~ Bit 2 (TC3CK2 ~ TC3CK0): Timer3 Clock Source select

TC3CK2	TC3CK1	TC3CK0	Clock Source	Resolution	Max. Time
			Normal	Fc=8M	Fc=8M
0	0	0	$Fc/2^{11}$	250 µs	64 ms
0	0	1	$Fc/2^{7}$	16 µs	4 ms
0	1	0	$Fc/2^{5}$	4 µs	1 ms
0	1	1	$Fc/2^{3}$	1 µs	255 µs
1	0	0	$Fc/2^{2}$	500 ns	127.5 µs
1	0	1	$Fc/2^{1}$	250 ns	63.8 µs
1	1	0	Fc	125 ns	31.9 µs
1	1	1	-	-	-

Bit 1 ~ Bit 0 (TC3M1 ~ TC3M0): Timer 3 operating mode select

TC3M1	TC3M0	Operating Mode
0	0	Timer
other		Reserved

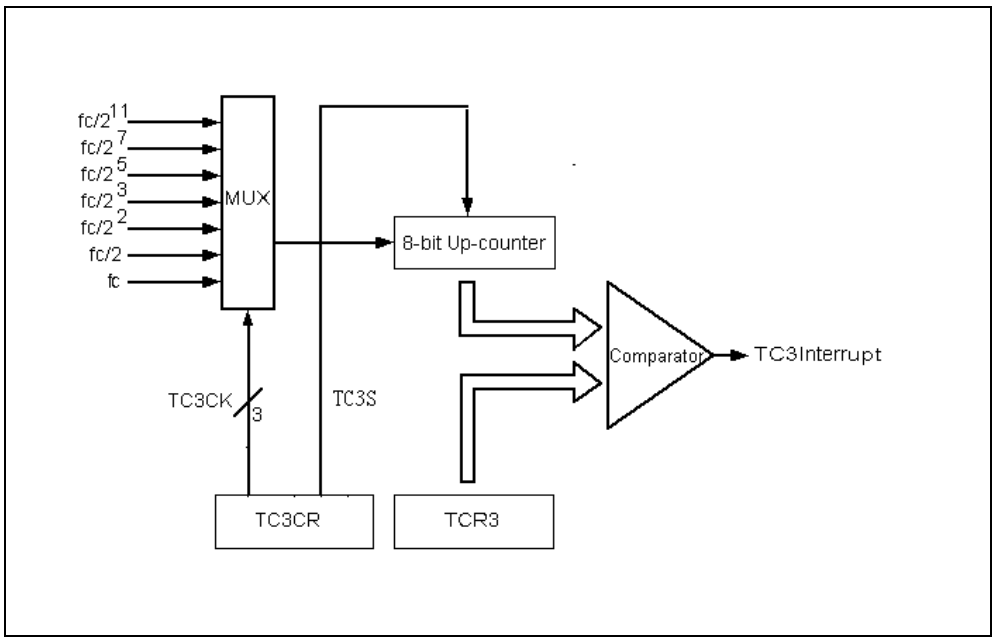


Figure 6-6 Timer3 Configuration

In Timer mode, counting up is performed using internal clock (rising edge trigger). When the contents of the up-counter match the TCR3, then interrupt is generated and the counter is cleared. Counting up resumes after the counter is cleared.

6.1.37 Bank 3 RE TC3D (Timer 3 Data Buffer)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TC3D7	TC3D6	TC3D5	TC3D4	TC3D3	TC3D2	TC3D1	TC3D0

Bit 7 ~ Bit 0 (TC3D7 ~ TC3D0): Data Buffer of 8-bit Timer3

6.1.38 Bank 3 RF (Pull-down Control Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	/PD72	/PD71	/PD70

Bit 7~ Bit 3: Not used, set to "**0**" at all time

Bit 2 (/PD72): Control bit used to enable the P72 pull-down pin

0 : Enable internal pull-down

1 : Disable internal pull-down

Bit 1 (/PD71): Control bit used to enable the P71 pull-down pin

Bit 0 (/PD70): Control bit used to enable the P70 pull-down pin

The RF Register is both readable and writable.

6.2 Special Function Registers

6.2.1 A (Accumulator)

Internal data transfer operation, or instruction operand holding usually involves the temporary storage function of the Accumulator, which is not an addressable register.

6.2.2 CONT (Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	TS	TE	PSTE	PST2	PST1	PST0

Bits 7 ~ 6: Not used, set to "**0**" at all time

Bit 5 (TS): TCC signal source

0 : Internal instruction cycle clock

1 : Transition on the TCC pin

Bit 4 (TE): TCC signal edge

0 : Increment if a transition from low to high takes place on the TCC pin

1 : Increment if a transition from high to low takes place on the TCC pin

Bit 3 (PSTE): Prescaler enable bit for TCC

0 : prescaler disable bit, TCC rate is 1:1

1 : prescaler enable bit, TCC rate is set at Bit 2~Bit 0

Bit 2 ~ Bit 0 (PST 2 ~ PST0): TCC prescaler bits

PST2	PST1	PST0	TCC Rate
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

The CONT register is both readable and writable.

6.2.3 IOC5 ~ IOC8 (I/O Port Control Register)

A value of "**1**" sets the relative I/O pin into high impedance, while "0" defines the relative I/O pin as output.

IOC5, IOC7 and IOC8 registers are both readable and writable.

6.2.4 IOC9 (Reserved)

Reserved registers

6.2.5 IOCA (WDT Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WDTE	-	-	-	PSWE	PSW2	PSW1	PSW0

Bit 7 (WDTE): Control bit used to enable the Watchdog timer

0 : Disable WDT

1 : Enable WDT

WDTE is both readable and writable.

Bits 6~4: Not used, set to "**0**" at all time

Bit 3 (PSWE): Prescaler enable bit for WDT

0 : prescaler disable bit, WDT rate is 1:1

1 : prescaler enable bit, WDT rate is set at Bit 0~Bit 2

Bit 2 ~ Bit 0 (PSW2 ~ PSW0): WDT prescaler bits

PSW2	PSW1	PSW0	WDT Rate
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

6.2.6 IOCB (Reserved)

Reserved Register

6.2.7 IOCC (Reserved)

Reserved Register

6.2.8 IOCD (Reserved)

Reserved Register

6.2.9 IOCE (Interrupt Mask Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
–	–	TCIE3	–	TCIE1	–	–	–

Bits 7~6: Not used, set to "**0**" at all time

Bit 5 (TCIE3): Interrupt enable bit

0 : Disable TCIF3 interrupt

1 : Enable TCIF3 interrupt

Bit 4: Not used, set to "**0**" at all time

Bit 3 (TCIE1): Interrupt enable bit

0: Disable TCIF1 interrupt

1: Enable TCIF1 interrupt

Bits 2~0: Not used, set to "**0**" at all time

6.2.10 IOCF (Interrupt Mask Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
–	ADIE	–	–	–	–	–	TCIE

Bit 7: Not used, set to "**0**" at all time

Bit 6 (ADIE): ADIF interrupt enable bit

0 : Disable ADIF interrupt

1 : Enable ADIF interrupt

When the ADC Complete is used to enter an interrupt vector or enter the next instruction, the ADIE bit must be set to "Enable".

Bits 5 ~ 2: Not used, set to "0" at all time

Bit 1: Not used, set to "1" at all time

Bit 0 (TCIE): TCIF interrupt enable bit

0 : Disable TCIF interrupt

1 : Enable TCIF interrupt

Individual interrupt is enabled by setting its associated control bit in the IOCF to "**1**".

Global interrupt is enabled by the ENI instruction and is disabled by the DISI instruction. The IOCF register is both readable and writable.

6.3 Touch Key Hardware List

Index	Access Direction	Description
0x05	R/W	General configuration
0x09	R	TPERR bit
0x15	R/W	Touch Sensitivity 1 set
0x16	R/W	Touch Sensitivity 2 set
0x17	R/W	Touch Speed set
0x18	R/W	Touch Speed set
0x24	R/W	Button operation mode
0x26	R/W	Button de-bounce
0x30~0x38	R/W	Trigger level adjustment

6.3.1 Index 0x05 : General Configuration

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	ReCal	-	-	-	-	-	-
R-0	R/W-0	R-0	R-0	R-0	R-0	R-0	R-0

Bits 7, 5 ~ 0: Not used bits. Set to "**0**" all the time.

Bit 6 (ReCal): This bit is used to recalibrate the sensor basic capacitance to adjust and compensate capacitance shift due to change of environment. If ReCal bit is set from "**0**" to "**1**", it will recalibrate immediately and then return to "**0**" to complete the process.

0: ReCal completed

1: Execute ReCal

6.3.2 Index 0x09: TPERR Bit

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	TPTR	TPOV	-
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

Bits 7~3, 0 : Not used bits. Set to "**0**" all the time.

Bit 2 (TPTR) : Touch transfer error. Need to increase **Index 0x17, 0x18** Touch transfer time. (See Section Index 0x17, 0x18)

Bit 1 (TPOV) : Touch gain overflow. Need to increase fraction factor of **Index 0x16** Touch Sensitivity 2 (**SST2_FC**). For example; from 1/4 to 1/8 (see Section Index 0x15, 0x16).

6.3.3 Index 0x15: Touch SENSITIVITY 1 SET

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SST1							
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bits 7 ~ 0 (SST1): Touch sensitivity level selection; 0 is lowest, and 255 is highest. For instance thick cover needs higher sensitivity level, while thin cover requires lower level. This setting will also impact Touch execution time, i.e., higher **SST1** needs longer Touch execution time, hence the button response is slower.

6.3.4 Index 0x16: Touch SENSITIVITY 2 SET

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	SST2_FC		
R-0	R-0	R-0	R-0	R-0	R/W-0	R/W-0	R/W-0

Bits 7 ~ 3: Not used bits. Set to "**0**" all the time.

Bits 2 ~ 0 (SST2_FC): Touch sensitivity fraction table select bits with a total of 0~7 levels available selections as shown in the table below. The higher the SST2_FC value, the lower the sensibility will be, while the stability becomes higher. In contrary, the lower the SST2_FC value, the higher is the sensibility will be, while the stability becomes lower. The recommended value is **5** (1/28).

SST2_FC	Description	Note
0	1/2	Highest sensitivity, Lowest stability
1	1/4	
2	1/8	
3	1/16	
4	1/24	
5	1/28	
6	1/32	
7	1/36	Lowest sensitivity, Highest stability

6.3.5 Index 0x17: Touch SPEED 1 SET

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SPP_SE				SPP11	SPP10	SPP9	SPP8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bits 7 ~ 4 (SPP_SE): Touch transfer setup time setting. Each transfer needs an initial setup time, and larger trace (route) requires longer setup time. A total of 16 levels can be set, "**0**" is the shortest and "**15**" is the longest. The longer the setup time, the better the Touch data can be.

$$SPEED\_Setup = (10\mu s + SPP\_SE * 0.5\mu s)$$

Bits 3 ~ 0 (SP11~8): Touch transfer time high 11~8bit**.**

6.3.6 Index 0x18: Touch SPEED2 SET

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SPP7	SPP6	SPP5	SPP4	SPP3	SPP2	SPP1	SPP0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bits 7 ~ 0 (SP7~0): Touch transfer time setting**;** a total of 12 bits (SP11~0) range can be set. 0xFFF is longest and 0x000 is shortest. This parameter relates to layout size of the physical PCB trace. Therefore, the larger the PCB trace is, the longer transfer time it needs.

$$SPEED\_Tran\ sfer = (200\mu s + SPP * 0.5\mu s)$$

6.3.7 Index 0x24: Button Operation Mode

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BtM1	BtM0	SBO	-	-	-	-	-
R/W-0	R/W-0	R/W-0	R-0	R-0	R-0	R-0	R-0

Bits 7 ~ 6 (BtM1 ~ 0): Button mode selection

BtM1	BtM0	Description	Note
0	**0**	Multi-button mode	With serveral buttons enabled, buttons that exceed the set sensitivity trigger level (0x30~0x38) will have their status bit set to “1”.
0	**1**	First button mode	With several buttons enabled, the first button to surpass the set sensitivity trigger level (0x30~0x38) ; will have its status bit set to “1”.
1	**0**	Strong button mode	With several buttons enabled and a number of buttons surpass the set sensitivity trigger level (0x30~0x38) ; the button with the highest sensitivity will have its status bit set to “1”.
1	**1**	×	–

Bit 5 (SBO): This bit selects the Strong button mode options (Strong 1/Strong 2).

0: Strong 1 - If Key A is already pressed; Key B is also considered pressed. If the total keys (except Key B) are **released**, Key B needs to be pressed harder.

1: Strong 2 - If Key A is already pressed, Key B is also considered pressed. If Key B sensitivity is **higher than** Key A, Key B needs to be pressed harder.

NOTE

- *Key A / Key B Sensitivity must be higher than the Trigger Level. Key A / Key B represents different Key Numbers.*

Bits 4 ~ 0: Not used bits. Set to “**0**” all the time.

6.3.8 Index 0x26: Button De-Bounce Control

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-				Bounce Set			
R-0	R-0	R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0

Bits 7 ~ 4: Not used bits. Set to "**0**" all the time.

Bits 3 ~ 0 (Bounce Set): These bits are the bounce time control for buttons. The bounce time mechanism reduces noise interference on button status. The touch button controller provides touch and release de-bounce time control to resist noise effect. The following figure shows an example of detection with bounce Time = 2**;** meaning two consecutive samples are necessary to trigger the key detection or two consecutive samples are necessary to end of detection.

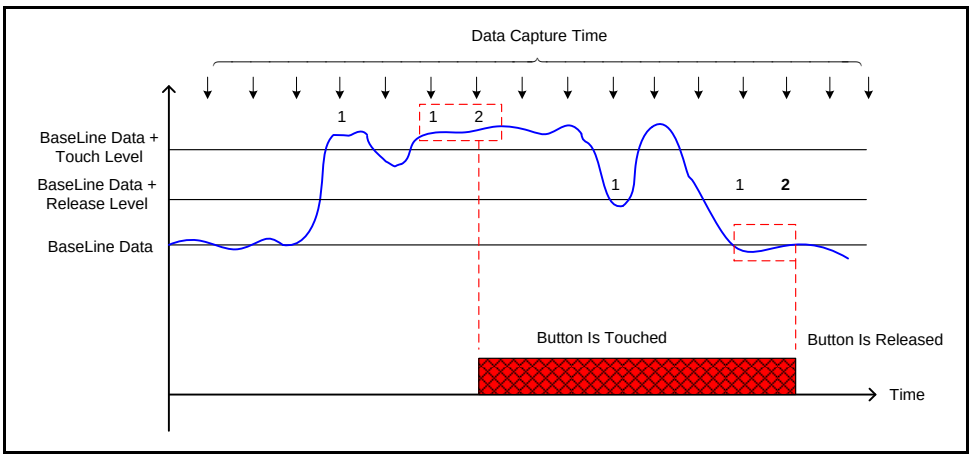


Figure1 Example of Bounce Time Operation

6.3.9 Index 0x30~0x38: Trigger Level Adjustment

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FTN_0~FTN_8							
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

These registers are used to trigger level and obtain button status. If the sensitivity is higher than the level, the relative bit of the button status will be "**1**".

Bits 7 ~ 0 (FTN_X): Adjustment of 8-bit address value is provided for nine keys. The highest setting value is 0xFF, and the lowest is 0x00. The recommended value ranges from 0x00~0x80.

$$1st\ 0x00 \sim 0x80 = (FTN\_X\ *\ 2)$$

6.4 TCC/WDT and Prescaler

There are two 8-bit counters available as prescalers for the TCC and WDT respectively. The PST0~PST2 bits of the CONT register are used to determine the ratio of the prescaler of TCC. Likewise, the PSW0~PSW2 bits of the IOCA register are used to determine the WDT prescaler. The prescaler counter will be cleared by the instructions each time they are written into TCC. The WDT and prescaler will be cleared by the "WDTC" and "SLEP" instructions. Figure 6-9 depicts the circuit diagram of TCC/WDT.

R1 (TCC) is an 8-bit timer/counter. The clock source of TCC can be the internal clock or the external signal input (edge selectable from the TCC pin). If TCC signal source is from the internal clock, TCC will be incremented by 1 at Fc clock (without prescaler). As illustrated in Figure 6-9, selection of Fc depends on the bank 0 RE.6 <TIMERSC>. If TCC signal source is from external clock input, TCC will be incremented by 1 at every falling edge or rising edge of the TCC pin. TCC pin input time length (kept in High or low level) must be greater than 1CLK. The TCC will stop running when sleep mode occurs.

The Watchdog Timer is a free running on-chip RC oscillator. The WDT will keep on running even after the oscillator driver has been turned off (i.e. in sleep mode). During normal operation or sleep mode, a WDT time-out (if enabled) will cause the device to reset. The WDT can be enabled or disabled at any time during normal mode by software programming. Refer to WDTE bit of IOCA register. With no prescaler, the WDT time-out period is approximately 16.5 ms[1] (one oscillator start-up timer period).

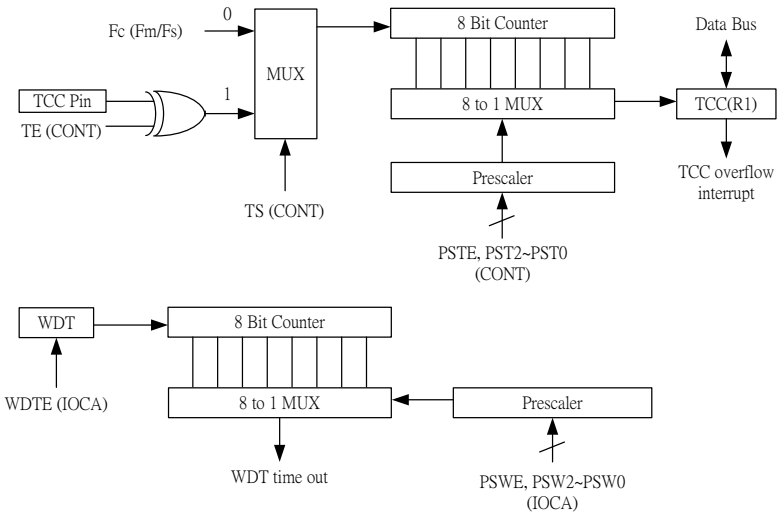


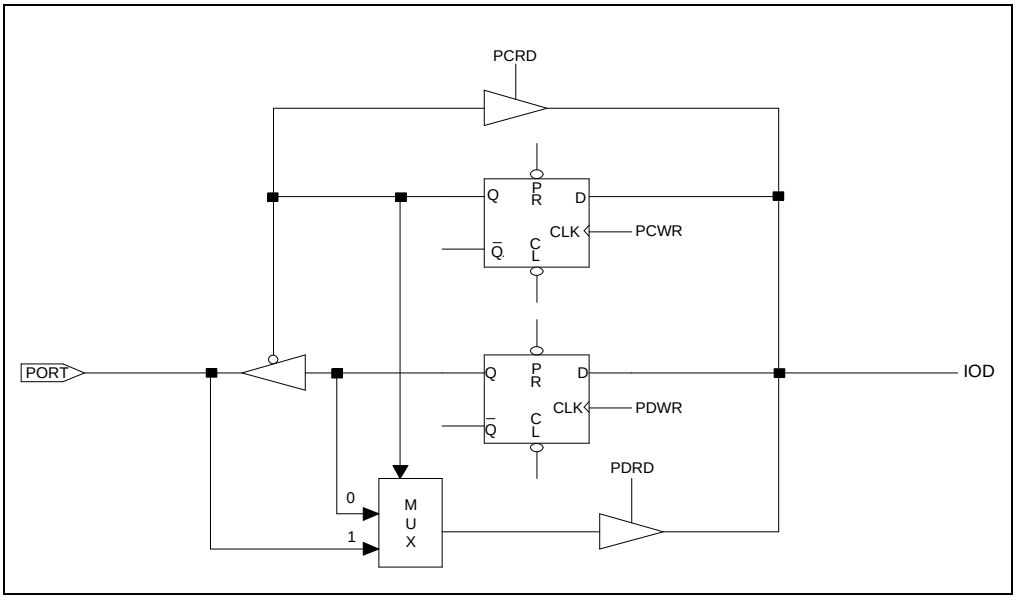
Figure 6-9 TCC and WDT Block Diagram

[1] VDD=5V, WDT time-out period = 16.5ms ± 5% VDD=3V
WDT time-out period = 16.5ms ± 5%.

6.5 I/O Ports

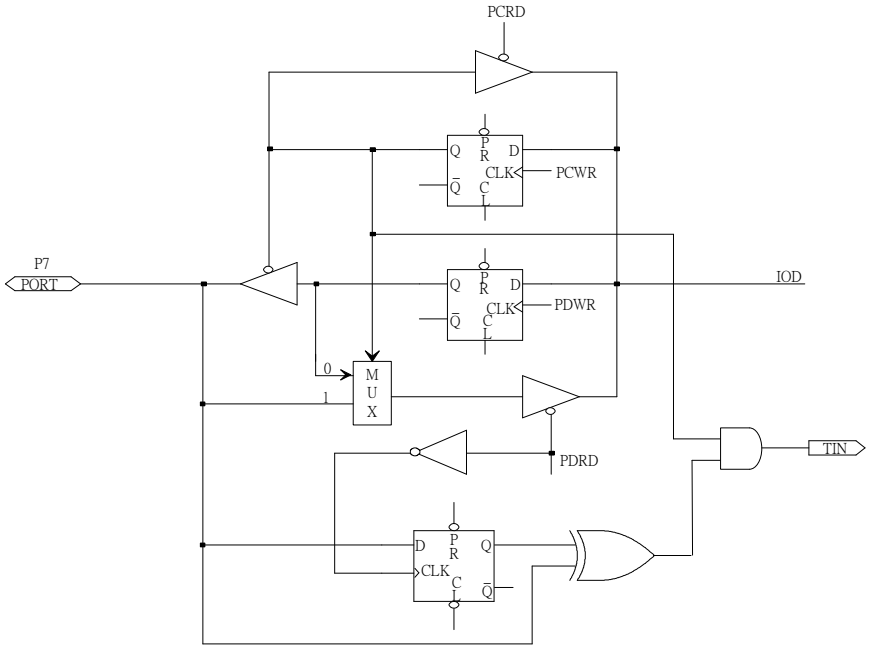
The I/O registers, Ports 5, 7 and 8, are bidirectional tri-state I/O ports. Port 7 can be pulled high internally by software. In addition, Port 7 pins can be pulled down by software. Each I/O pin can be defined as "input" or "output" pin by the I/O control register (IOC5 ~ IOC8).

The I/O registers and I/O control registers are both readable and writable. The I/O interface circuits for Port 5, Port 7 and Port 8 are shown in the following Figures 6-10, and Figure 6-11.



Note: *Pull-down is not shown in the figure.*

Figure 6-10 I/O Port and I/O Control Register Circuit for Ports 5, 7



Note: *Pull-high (down) and Open-drain are not shown in the figure.*

Figure 6-11 I/O Port and I/O Control Register Circuit for P7

6.6 Reset and Wake-up

6.6.1 Reset

A reset is initiated by one of the following events:

(1) Power-on reset

(2) /RESET pin input "low"

(3) WDT time-out (if enabled)

The device is kept in a reset condition for a period of approximately 18ms[2] (one oscillator start-up timer period) after the reset is detected. Once a reset occurs, the following functions are performed.

- The oscillator is running, or will be started.
- The Program Counter (R2) is set to all "0".
- All I/O port pins are configured as input mode (high-impedance state).
- The Watchdog timer and prescaler are cleared.
- When power is switched on, the upper three bits of R3 are cleared.
- The bits of the RB, RC, RD, RD, RE registers are set to their previous status.
- The bits of the Pull-high, Pull-down.
- Bank 0 RF, IOCF registers are cleared.

Sleep (power down) mode is asserted by executing the “SLEP” instruction. While entering sleep mode, WDT (if enabled) is cleared but keeps on running. After a wake-up, in RC mode the wake-up time is 16 clocks.

The controller can be awakened by:

(1) External reset input on /RESET pin

(2) WDT time-out (if enabled)

(3) A/D conversion completed (if ADWE is enabled)

[3] *Vdd = 5V, set up time period = 16.5ms ± 5%*
Vdd = 3V, set up time period = 16.5ms ± 5%

The first two events (1 & 2) will cause the EM78F704N to reset. The T and P flags of R3 can be used to determine the source of the reset (wake-up). Event 3 is considered the continuation of program execution and the global interrupt ("ENI" or "DISI" being executed) determines whether or not the controller branches to the interrupt vector following wake-up. If ENI is executed before SLEP, the instruction will begin to execute from address 0x30, after wake-up. If DISI is executed before SLEP, the execution will restart from the instruction right next to SLEP after wake-up. All throughout the sleep mode, wake-up time is150 µs.

One or more of the above Events 3 can be enabled before entering into sleep mode but is awakened only by one of the events.

[a] If WDT is enabled before SLEP, all of the RE bit is disabled. Hence, the EM78F704N can be awakened only by Event 1 or 2. Refer to Section 6.6 *Interrupt* for further details.

[b] If AD conversion completed is used to wake-up EM78F704N and ADWE bit of the RA register is enabled before SLEP, the WDT must be disabled by software. Hence, the EM78F704N can be waken-up only by Event 3.

6.6.2 Summary of Wake-up and Interrupt Modes Operation

All categories under Wake-up and Interrupt modes are summarized below.

The controller can be awakened from Sleep mode and Idle mode. The Wake-up signals are listed as follows.

Wake-up Signal	Sleep Mode	Idle Mode	Green Mode	Normal Mode
TCC overflow interrupt	x	Wake-up + interrupt (if interrupt is enabled) + next instruction	Interrupt (if interrupt is enabled) or next instruction	Interrupt (if interrupt is enabled) or next instruction
AD conversion complete interrupt	If enable ADWE bit Wake-up + interrupt (if interrupt is enabled) + next instruction **Fs and Fm don't stop**	If enable ADWE bit Wake-up + interrupt (if interrupt is enabled) + next instruction **Fs and Fm don't stop**	Interrupt (if interrupt is enabled) or next instruction **Fs and Fm don't stop**	Interrupt (if interrupt is enabled) or next instruction
TC2 interrupt	x	Wake-up + interrupt (if interrupt is enabled) + next instruction	Interrupt (if interrupt is enabled) or next instruction	Interrupt (if interrupt is enabled) or next instruction
TC3 interrupt	x	Wake-up + interrupt (if interrupt is enabled) + next instruction	Interrupt (if interrupt is enabled) or next instruction	Interrupt (if interrupt is enabled) or next instruction
WDT Time out	RESET	RESET	RESET	RESET
Low Voltage Reset	RESET	RESET	RESET	RESET

After wake up:

1. If interrupt is enabled → interrupt+ next instruction

2. If interrupt is disabled → next instruction

6.6.3 Summary of Register Initial Values

Legend: ***x:*** *Not used* ***P:*** *Previous value before reset*
U: *Unknown or don't care* ***t:*** *Check tables under Section 6.5.4*

Addr	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x05	IOC5	Bit Name	-	-	C55	C54	C53	C52	C51	C50
		Power-on	1	0	1	1	1	1	1	1
		/RESET and WDT	1	0	1	1	1	1	1	1
		Wake-up from Pin Change	P	0	P	P	P	P	P	P
0x07	IOC7	Bit Name	C77	-	-	-	-	C72	C71	C70
		Power-on	1	0	0	1	1	1	1	1
		/RESET and WDT	1	0	0	1	1	1	1	1
		Wake-up from Pin Change	P	0	0	P	P	P	P	P
0x08	IOC8	Bit Name	-	-	-	-	C83	-	-	-
		Power-on	0	0	0	0	1	0	0	0
		/RESET and WDT	0	0	0	0	1	0	0	0
		Wake-up from Pin Change	0	0	0	0	P	0	0	0
N/A	CONT	Bit Name	-	-	TS	TE	PSTE	PST2	PST1	PST0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x00	R0 (IAR)	Bit Name	IAR7	IAR6	IAR5	IAR4	IAR3	IAR2	IAR1	IAR0
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x01	R1 (TCC)	Bit Name	TCC7	TCC6	TCC5	TCC4	TCC3	TCC2	TCC1	TCC0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x02	R2 (PC)	Bit Name	A7	A6	A5	A4	A3	A2	A1	A0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x03	R3 (SR)	Bit Name	-	-	-	T	P	Z	DC	C
		Power-on	0	0	0	1	1	U	U	U
		/RESET and WDT	0	0	0	t	t	P	P	P
		Wake-up from Pin Change	0	0	0	t	t	P	P	P
0x04	R4 (RSR)	Bit Name	RSR7	RSR6	RSR5	RSR4	RSR3	RSR2	RSR1	RSR0
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P

(Continuation)

Addr	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x05	P5 (Bank 0)	Bit Name	-	-	P55	P54	P53	P52	P51	P50
		Power-on	1	0	1	1	1	1	1	1
		/RESET and WDT	1	0	1	1	1	1	1	1
		Wake-up from Pin Change	P	0	P	P	P	P	P	P
0x07	P7 (Bank 0)	Bit Name	P77	-	-	-	-	P72	P71	P70
		Power-on	1	0	0	1	1	1	1	1
		/RESET and WDT	1	0	0	1	1	1	1	1
		Wake-up from Pin Change	P	0	0	P	P	P	P	P
0x08	P8 (Bank 0)	Bit Name	-	-	-	-	P83	-	-	-
		Power-on	0	0	0	0	1	0	0	0
		/RESET and WDT	0	0	0	0	1	0	0	0
		Wake-up from Pin Change	0	0	0	0	P	0	0	0
0X09	R9 (Bank 0)	Bit Name	RBit7	RBit6	RBit5	RBit4	RBit3	RBit2	RBit1	RBit0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x0A	RA (Bank 0)	Bit Name	-	-	ADWE	-	-	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	0	0	P	0	0	0	0	0
0X0B	RB (ECR) (Bank 0)	Bit Name	RD	WR	EEWE	EEDF	EEPC	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	P	P	P	P	P	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	0	0	0
0X0C	RC (Bank 0)	Bit Name	-	EE_A6	EE_A5	EE_A4	EE_A3	EE_A2	EE_A1	EE_A0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	P	P	P	P	P	P	P
		Wake-up from Pin Change	0	P	P	P	P	P	P	P
0X0D	RD (Bank 0)	Bit Name	EE_D7	EE_D6	EE_D5	EE_D4	EE_D3	EE_D2	EE_D1	EE_D0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0X0E	RE (Bank 0)	Bit Name	-	TIMERSC	CPUS	IDLE	-	-	-	-
		Power-on	0	1	1	1	0	0	0	0
		/RESET and WDT	0	1	1	1	0	0	0	0
		Wake-up from Pin Change	0	P	P	P	0	0	0	0
0x0F	RF (ISR) (Bank 0)	Bit Name	-	ADIF	-	-	-	-	-	TCIF
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	0	P	0	0	0	0	0	P
0x5	R5 (Bank 1)	Bit Name	-	TC1S	-	-	TC1MOD	TCK1CK2	TC1CK1	TC1CK0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	0	P	0	0	P	P	P	P

(Continuation)

Addr	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x5	R5 (Bank 1)	Bit Name	-	TC1S	-	-	TC1MOD	TCK1CK2	TC1CK1	TC1CK0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	0	P	0	0	P	P	P	P
0x6	R6 (Bank 1)	Bit Name	TC1DA7	TC1DA6	TC1DA5	TC1DA4	TC1DA3	TC1DA2	TC1DA1	TC1DA0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0X7	R7 (Bank 1)	Bit Name	TC1DB7	TC1DB6	TC1DB5	TC1DB4	TC1DB3	TC1DB2	TC1DB1	TC1DB0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x9	R9 (Bank 1)	Bit Name	TC2DA7	TC2DA6	TC2DA5	TC2DA4	TC2DA3	TC2DA2	TC2DA1	TC2DA0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0XA	RA (Bank 1)	Bit Name	TC2DB7	TC2DB6	TC2DB5	TC2DB4	TC2DB3	TC2DB2	TC2DB1	TC2DB0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0XF	RF (Bank 1)	Bit Name	-	-	TCIF3	-	TCIF1	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	0	0	P	0	P	0	0	0
0x05	R5 (Bank 2)	Bit Name	-	-	ADE5	-	-	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	0	0	P	0	0	0	0	0
0x06	R6 (Bank 2)	Bit Name	VREFS	CKR1	CKR0	ADRUN	ADPD	ADIS2	ADIS1	ADIS0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P

(Continuation)

Addr	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x7	R7 (Bank 2)	Bit Name	-	-	-	-	-	PDE	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	0	0	0	0	0	P	0	0
0x8	R8 (Bank 2)	Bit Name	ADD11	ADD10	ADD9	ADD8	ADD7	ADD6	ADD5	ADD4
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x9	R9 (Bank 2)	Bit Name	-	-	IRVS1	IRVS0	ADD3	ADD2	ADD1	ADD0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	0	0	P	P	P	P	P	P
0x0F	RF (Bank 2)	Bit Name	-	-	-	-	-	/PH72	/PH71	/PH70
		Power-On	0	0	0	0	1	1	1	1
		/RESET and WDT	0	0	0	0	1	1	1	1
		Wake-up from Pin Change	0	0	0	0	P	P	P	P
0X06	R6 (Bank 3)	Bit Name	MLB	-	-	-	RBit 11	RBit 10	RBit 9	RBit 8
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	0	0	0	P	P	P	P
0XD	RD (Bank 3)	Bit Name	-	-	TC3S	TC3CK2	TC3CK1	TC3CK0	TC3M1	TC3M0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0XE	RE (Bank 3)	Bit Name	TC3D7	TC3D6	TC3D5	TC3D4	TC3D3	TC3D2	TC3D1	TC3D0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0XF	RF (Bank 3)	Bit Name	-	-	-	-	-	/PD72	/PD71	/PD70
		Power-on	0	0	0	0	1	1	1	1
		/RESET and WDT	0	0	0	0	1	1	1	1
		Wake-up from Pin Change	0	0	0	0	P	P	P	P

(Continuation)

Addr	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0A	IOCA	Bit Name	WDTE	-	-	-	PSWE	PSW2	PSW1	PSW0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	0	0	0	P	P	P	P
0x0E	IOCE	Bit Name	-	-	TCIE3	-	TCIE1	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	0	0	P	0	P	0	0	0
0x0F	IOCF	Bit Name	-	ADIE	-	-	-	-	-	TCIE
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	0	P	0	0	0	0	0	P
0x18~ 0x2F	R18~ R2F	Bit Name	R7	R6	R5	R4	R3	R2	R1	R0
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P

6.6.4 Status of RST, T, and P of the Status Register

A reset condition is initiated by the following events:

1. Power-on condition
2. High-low-high pulse on /RESET pin
3. Watchdog timer time-out

The values of T and P, listed in the first table below are used to check how the processor wakes up. The second table shows the events that may affect the status of T and P.

■ **Values of RST, T and P after Reset**

Reset Type	T	P
Power on	1	1
/RESET during Operating mode	*P	*P
/RESET wake-up during Sleep mode	1	0
WDT during Operating mode	0	*P
WDT wake-up during Sleep mode	0	0

***P:** Previous status before reset*

■ **Status of T and P Being Affected by Events**

Event	T	P
Power on	1	1
WDTC instruction	1	1
WDT time-out	0	*P
SLEP instruction	1	0

***P:** Previous value before reset*

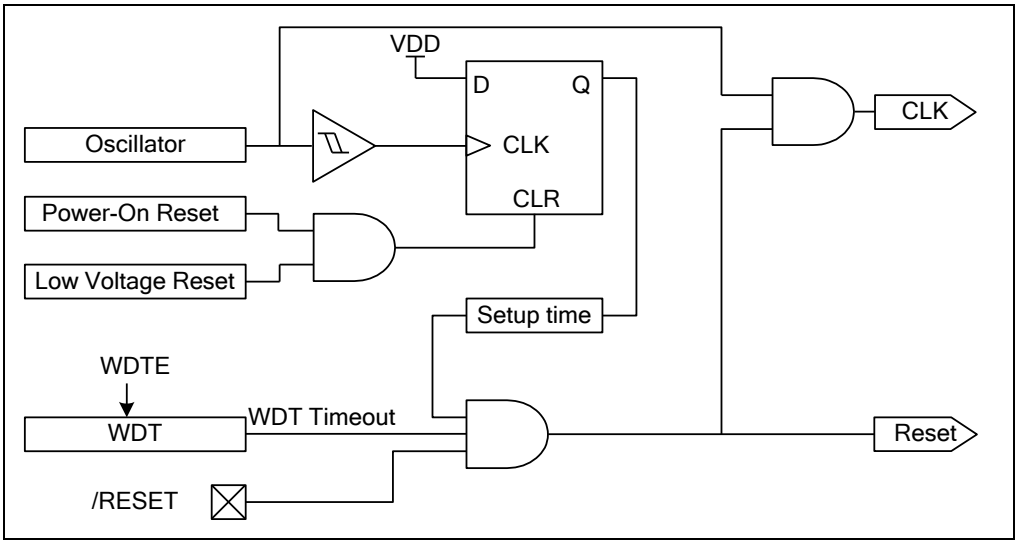


Figure 6-13 Controller Reset Block Diagram

6.7 Interrupt

The EM78F704N has four interrupts (0 external, four internal) as listed below:

Interrupt Source		Enable Condition	Int. Flag	Int. Vector	Priority
Internal / External	Reset	-	-	0000	High 0
Internal	TCC	ENI + TCIE=1	TCIF	0009	1
Internal	TC1	ENI + TCIE1=1	TCIF1	0018	2
Internal	TC3	ENI + TCIE3=1	TCIF3	0027	3
Internal	AD	ENI + ADIE=1	ADIF	0030	4

RF is interrupt status register that records the interrupt requests in the relative flags/ bits. IOCF is interrupt mask register. The global interrupt is enabled by the ENI instruction and is disabled by the DISI instruction. When one of the enabled interrupts occur, the next instruction will be fetched from their individual address. The interrupt flag bit must be cleared by instructions before leaving the interrupt service routine and before interrupts are enabled to avoid recursive interrupts.

The flag in the Interrupt Status Register (RF) is set regardless of the status of its mask bit or the execution of ENI. The RETI instruction ends the interrupt routine and enables the global interrupt (the execution of ENI).

Before the interrupt subroutine is executed, the contents of ACC and the R3 and R4 register will be saved by hardware. If another interrupt occurred, the ACC, R3 and R4 will be replaced by the new interrupt. After the interrupt service routine is finished, ACC, R3 and R4 will be pushed back.

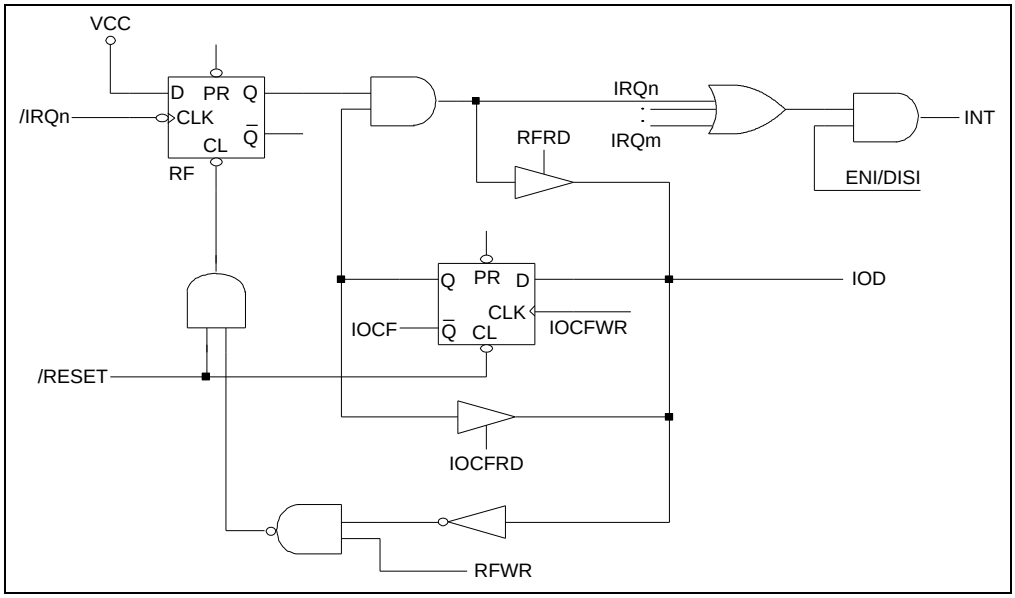


Figure 6-14 Interrupt Input Circuit

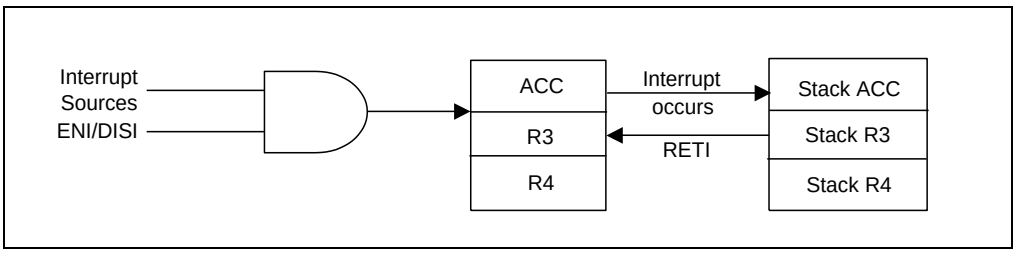


Figure 6-15 Interrupt Back-up Diagram

6.8 Data EEPROM

The Data EEPROM is readable and writable during normal operation over the whole Vdd range. The operation for Data EEPROM is based on a single byte. A write operation makes an erase-then-write cycle to take place on the allocated byte.

The Data EEPROM memory provides high erase and write cycles. A byte write automatically erases the location and writes the new value.

6.8.1 Data EEPROM Control Register

6.8.1.1 RB (EEPROM Control Register)

The EECR (EEPROM Control Register) is the control register for configuring and initiating the control register status.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RD	WR	EEWE	EEDF	EEPC	-	-	-

Bit 7 (RD): Read control register

0 : Does not execute EEPROM read

1 : Read EEPROM content, (RD can be set by software, RD is cleared by hardware after Read instruction is completed)

Bit 6 (WR): Write control register

0 : Write cycle to the EEPROM is completed.

1 : Initiate a write cycle, (WR can be set by software, WR is cleared by hardware after Write cycle is completed)

Bit 5 (EEWE): EEPROM Write Enable bit

0 : Write to the EEPROM is prohibited.

1 : Allows EEPROM write cycles

Bit 4 (EEDF): EEPROM Detect Flag

0 : Write cycle is completed

1 : Write cycle is unfinished

Bit 3 (EEPC): EEPROM power-down control bit

0 : Switch off the EEPROM

1 : EEPROM is operating

Bits 2 ~ 0: Not used, set to "**0**" at all time

6.8.1.2 RC (128 Bytes EEPROM Address)

When accessing the EEPROM data memory, the RC (128 bytes EEPROM address register) holds the address to be accessed. In accordance with the operation, the RD (128 bytes EEPROM Data register) holds the data to be written, or the data read, at the address in RC.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	EE_A6	EE_A5	EE_A4	EE_A3	EE_A2	EE_A1	EE_A0

Bit 7: Not used, set to "**0**" at all time.

Bits 6 ~ 0: 128 bytes EEPROM address

6.8.1.3 RD (256 Bytes EEPROM Data)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EE_D7	EE_D6	EE_D5	EE_D4	EE_D3	EE_D2	EE_D1	EE_D0

Bits 7 ~ 0: 128 bytes EEPROM data

6.8.2 Programming Step / Example Demonstration

6.8.2.1 Programming Step

Follow these steps to write to or read data from the EEPROM:

Step 1 Set the RB.EEPC bit to "**1**" to enable the EEPROM power.

Step 2 Write the address to RC (128 bytes EEPROM address).

1. (a) Set the RB.EEWE bit to 1, if the write function is employed.

   (b) Write the 8-bit data value to be programmed in the RD (256 bytes EEPROM data)

   (c) Set the RB.WR bit to "**1**", then execute the write function.

2. Set the RB.READ bit to "**1**", after which, execute the read function.

Step 3 Wait for the RB.EEDF or RB.WR to be cleared

Step 4 For the next conversion, go to Step 2 as required.

Step 5 If you want to save power, make sure the EEPROM data is not used by clearing the RB.EEPC.

6.8.2.2 Example Demonstration Programs

```
; Define the control register and write data to EEPROM
RC == 0x0C
RB == 0x0B
RD == 0x0D
Read == 0x07
WR == 0x06
EEWE == 0x05
EEDF == 0x04
EEPC == 0x03

BS RB, EEPC       ; Set the EEPROM power on
MOV A,@0x0A
MOV RC,A          ; Assign the address from EEPROM
BS RB, EEWE       ; Enable the EEPROM write function
MOV A,@0x55
MOV RD,A          ; Set the data for EEPROM
BS RB,WR          ; Write value to EEPROM
JBC RB,EEDF       ; Check whether the EEPROM bit is completed or not
JMP $-1
```

6.9 Analog-to-Digital Converter (ADC)

The analog-to-digital circuitry consists of a 9-bit analog multiplexer, three control registers (AISR/R5 (Bank 2), ADCON/R6 (Bank 2), ADOC/R7 (Bank 2), two data registers (ADDH, ADDL/R8, R9) and an ADC with 12-bit resolution. The analog reference voltage (Vref) and analog ground are connected via separate input pins. The functional block diagram of the ADC is shown below.

The ADC module utilizes successive approximation to convert the unknown analog signal into a digital value. The result is fed to the ADDH and ADDL. Input channels are selected by the analog input multiplexer via the ADCON register Bits ADIS2, ADIS1 and ADIS0.

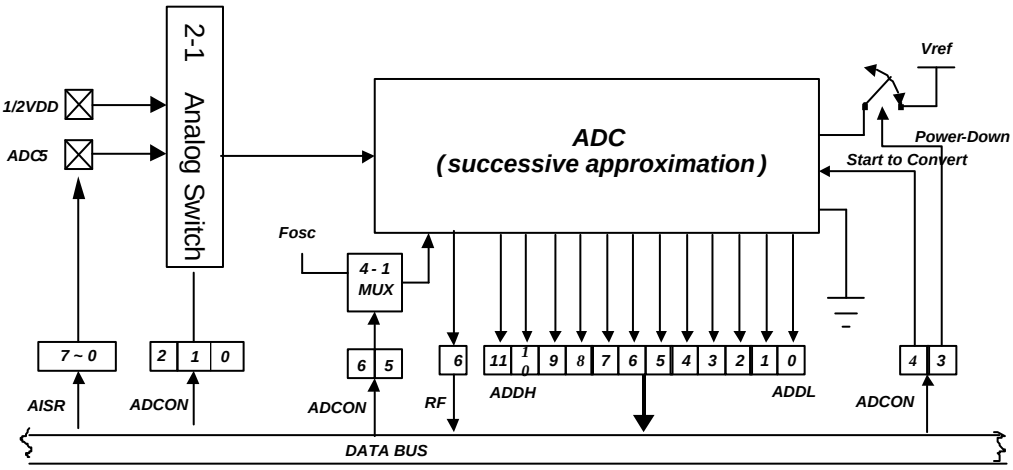


Figure 6-16 Functional Block Diagram of Analog-to-Digital Conversion

6.9.1 ADC Control Register (AISR/R5, ADCON/R6, ADOC/R7)

6.9.2 Bank 2 R5 AISR (ADC Input Select Register)

The AISR register defines the ADC pins as analog input or as digital I/O.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	ADE5	-	-	-	-	-

Bits 7~6: Not used, set to "**0**" at all time

Bit 5 (ADE5): AD converter enable bit of P77 pin

0 : Disable ADC5, P77 functions as I/O pin

1 : Enable ADC5 to function as analog input pin

Bits 4~0: Not used, set to "**0**" at all time

6.9.3 Bank 2 R6 ADCON (A/D Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
VREFS	CKR1	CKR0	ADRUN	ADPD	ADIS2	ADIS1	ADIS0

Bit 7 (VREFS): Input source of the Vref of the ADC.

0 : Vref of the ADC is connected to the internal reference which is selected by Bank 2 R9<5,4> (default value), and the P50/VREF pin carries out the function of P50

1 : Vref of the ADC is connected to P50/VREF

Bit 6 ~ Bit 5 (CKR1 ~ CKR0): Prescaler of oscillator clock rate of ADC

CKR1/CKR0	Operation Mode	Max. Operation Frequency
00	$F_{OSC}/4$	4 MHz
10	$F_{OSC}/16$	8 MHz

Bit 4 (ADRUN): ADC starts to run

0 : Reset upon completion of AD conversion. This bit cannot be reset by software.

1 : A/D conversion is started. This bit can be set by software.

Bit 3 (ADPD): ADC Power-down mode

0 : Switch off the resistor reference to save power even while the CPU is operating

1 : ADC is operating

Bits 2~0 (ADIS2~ADIS0): AD Input Select Bits

ADIS2	ADIS1	ADIS0	AD Input Pin
1	0	1	AD5

6.9.4 Bank 2 R7 ADOC (A/D Offset Calibration Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	PDE	Reserved	Reserved

Bits 7~3: Not used, set to "**0**" at all time.

Bit 2 (PDE): 1/2 VDD Power Detect Enable bit.

0: Disable Power Detect (Default)

1: Enable Power Detect.

PDE	ADIS2	ADIS1	ADIS0	AD Input Select
1	x	x	x	1/2VDD
0	1	0	1	AD5

Bits 1~0: Reserved, must be set to "**0**" at all time.

6.9.5 ADC Data Buffer (ADDH, ADDL/R8, R9)

When the A/D conversion is completed, the result is loaded to the ADDH, ADDL. The ADRUN bit is cleared, and the ADIF is set.

6.9.6 A/D Sampling Time

The accuracy, linearity, and speed of the successive approximation A/D converter are dependent on the properties of the ADC. The source impedance and the internal sampling impedance directly affect the time required to charge the sample holding capacitor. The application program controls the length of the sample time to meet the specified accuracy. Generally speaking, the program should wait for 2μs for each KΩ of the analog source impedance and at least 2μs for the low- impedance source. The maximum recommended impedance for analog source is 10KΩ at Vdd=5V. After the analog input channel is selected, this acquisition time must be done before the conversion can be started.

RCM[1:0]*	Frequency (MHz)	Sample and Hold Timing
00	4	8 x T_{AD}
10	8	12 x T_{AD}

6.9.7 A/D Conversion Time

CKR0 and CKR1 select the conversion time (Tct), in terms of instruction cycles. This allows the MCU to run at the maximum frequency without sacrificing the accuracy of A/D conversion. For the EM78F704N, the conversion time per bit is 1µs. The table below shows the relationship between Tct and the maximum operating frequencies.

■ **Tct vs. Maximum Operation Frequency**

CKR0: CKR1	Operation Mode	Max. Operating Frequency	Max. Conversion Rate Per Bit	Max. Conversion Rate (12bit)
00	Fosc/4	4 MHz	1 MHz (1 µs)	(12+8)*1µs=20µs (50kHz)
10	Fosc/16	8 MHz	0.5 MHz (2 µs)	(12+12)*2µs=48µs (20.8kHz)

NOTE

- *The pin that is not used as analog input can be used as regular input or output pin.*
- *During conversion, do not perform output instruction to maintain precision for all of the pins.*

6.9.8 A/D Operation During Sleep Mode

In order to obtain a more accurate ADC value and reduced power consumption, the A/D conversion remains operational during sleep mode. As the SLEP instruction is executed, all the MCU operations will stop except for the Oscillator, TCC, TC1, TC3, and A/D conversion.

The AD Conversion is considered completed when:

1 ADRUN Bit of R6 Register is cleared to "**0**".

2 Wake-up from A/D Conversion remains in operation during Sleep Mode.

The result is fed to the ADDATA, ADOC when the conversion is completed. If the ADWE is enabled, the device will wake up. Otherwise, the A/D conversion will be shut off, no matter what the status of the ADPD bit is.

6.9.9 Programming Steps/Considerations

6.9.9.1 Programming Steps

Follow the following steps to obtain data from the ADC:

1. Write to the 1 bit (ADE5) on the R5 (AISR) register to define the characteristics of R6: Digital I/O, analog channels, and voltage reference pin.
2. Write to the R6/ADCON register to configure the AD module:
   a. Select A/D input channel (ADIS1 ~ ADIS0).
   b. Define the A/D conversion clock rate (CKR1 ~ CKR0).
   c. Select the input source of the VREFS of the ADC.
   d. Set the ADPD bit to "**1**" to begin sampling.
3. Set the ADWE bit, if the wake-up function is employed.
4. Set the ADIE bit, if the interrupt function is employed.
5. Put "ENI" instruction, if the interrupt function is employed.
6. Set the ADRUN bit to "**1**".
7. Wait for wake-up or when ADRUN bit is cleared to "**0**".
8. Read ADDATA, ADOC the conversion data register.
9. Clear the interrupt flag bit (ADIF) when A/D interrupt function occurs.
10. For the next conversion, repeat from Step 1 or Step 2 as required. At least 2 Tct is required before the next acquisition starts.

NOTE

To obtain an accurate value, it is necessary to avoid any data transition on the I/O pins during AD conversion.

6.9.9.2 Sample Demonstration Programs

```
; To define the General Registers
R_0 == 0                    ; Indirect addressing register
PSW == 3                    ; Status register
PORT5 == 5
PORT7 == 7
RE== 0XE                    ; Wake-up control resister
RF== 0XF                    ; Interrupt status register

; To define the Control Register
IOC50 == 0X5                ; Control Register of Port 5
IOC70 == 0X7                ; Control Register of Port 7
C_INT== 0XF                 ; Interrupt Control Register
```

```
; ADC Control Registers
ADDATA == 0x8              ; The contents are the results of ADC
AISR == 0x08               ; ADC output select register
ADCON == 0x6               ; 7    6    5    4    3    2    1    0
                           VREFS  CKR1  CKR0  ADRUN  ADPD
                             –    ADIS1 ADIS0

; To define bits
; In ADCON
ADRUN == 0x4               ; ADC is executed as the bit is set
ADPD == 0x3                ; Power Mode of ADC

; Program Starts
ORG 0                      ; Initial address
JMP INITIAL
ORG 0x30                   ; Interrupt vector
(User program)
CLR RF                     ; To clear the ADIF bit
BS ADCON  , ADRUN          ; To start to execute the next AD
                           ; conversion if necessary
RETI

INITIAL:
MOV A      , @0B00100000   ; To define P77 as an analog input
MOV AISR   , A
MOV A      , @0B00001101   ; To select P77 as an analog input
                           ; channel, and AD power on
MOV ADCON  , A             ; To define P77 as an input pin and
                           ; set clock rate at fosc/16
En_ADC:
MOV A      , @0B1XXXXXXX   ; To define P77 as an input pin, and
                           ; the others are dependent
                           ; on applications
IOW PORT7
MOV A      , @0BXXXX1XXX   ; Enable the ADWE wake-up function
                           ; of ADC, "X" by application
MOV RE     , A
MOV A      , @0BXXXX1XXX   ; Enable the ADIE interrupt function
                           ; of ADC, "X" by application
IOW C_INT

ENI                        ; Enable the interrupt function
BS ADCON   , ADRUN         ; Start to run the ADC
; If the interrupt function is ; employed, the following three lines
; may be ignored
POLLING:
JBC ADCON  , ADRUN         ; To check the ADRUN bit ; continuously
JMP                        ; ADRUN bit will be reset as the AD
POLLING                    ; conversion is completed
;
(User program)
;
```

6.10 Timer 1

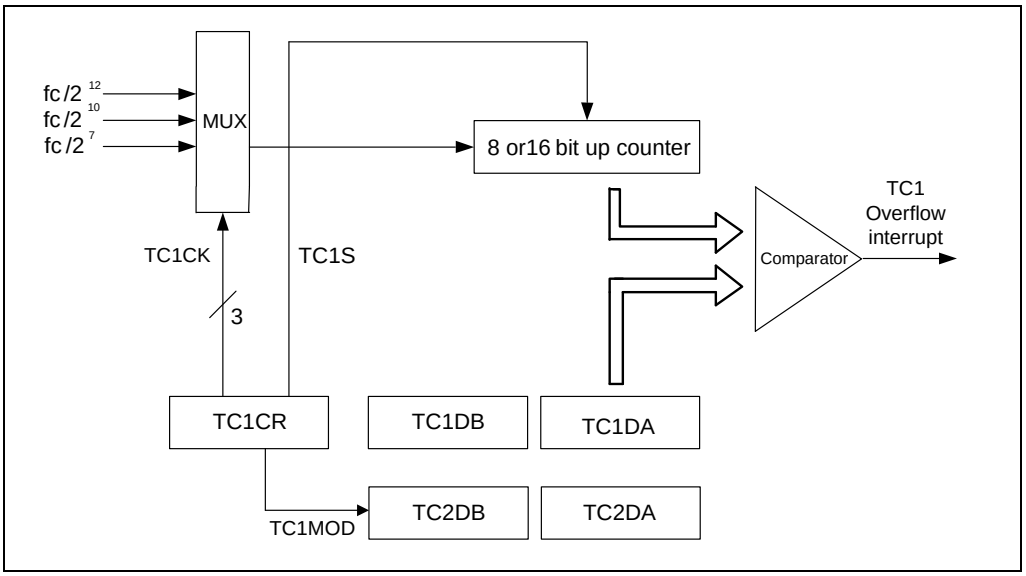


Figure 6-17 Timer 1 Configuration

In Timer mode, counting up is performed using an internal clock. When the contents of the up-counter matched the TC1DA, then interrupt is generated and the counter is cleared. Counting up resumes after the counter is cleared. The current contents of the up-counter are loaded into TC1DB. The timer mode will operate with 16bits by setting TC1MOD to “1”

6.11 Timer 3

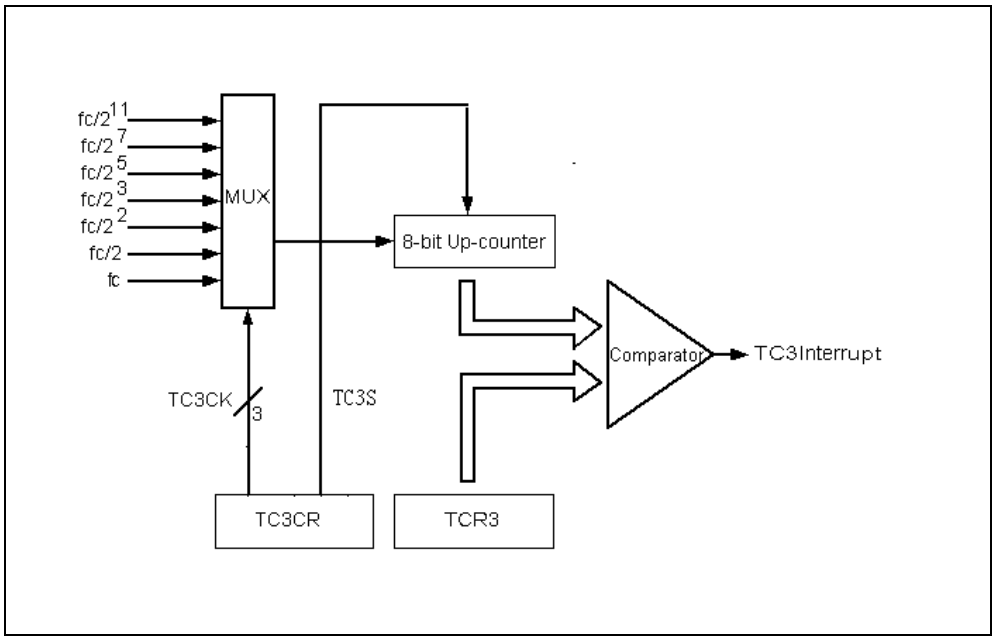


Figure 6-19 Timer 3 Mode Configuration

■ Timer Mode

In Timer mode, counting up is performed using the internal clock (rising edge trigger). When the contents of the up-counter matched with TCR3, interrupt is generated and the counter is cleared. Counting up resumes after the counter is cleared.

6.12 Oscillator

6.12.1 Oscillator Modes

The device can be operated in Internal RC oscillator mode (IRC). User can select one of such modes by programming OSC2, OCS1, and OSC0 in the Code Option register. The following table depicts how these four modes are defined.

■ **Oscillator Modes defined by OSC2 ~ OSC0**

Mode	OSC2	OSC1	OSC0
IRC mode, OSCO (P54) act as I/O pin	**1**	**0**	**0**
IRC mode, OSCO (P54) act as RCOUT pin	**1**	**0**	**1**
Reserve	**Other**		

In IRC mode, P55 is used as normal I/O pin. The maximum operating frequency of the crystal/resonator on the different VDD is shown below:

6.12.2 Internal RC Oscillator Mode

EM78F704N offers a versatile internal RC mode with default frequency value of 4 MHz. The Internal RC oscillator mode has other frequencies (8 MHz). All these four main frequencies can be calibrated by programming the Code Option (Word 1) bits, C6~C0. The table describes a typical instance of the calibration.

■ **Internal RC Drift Rate (Ta=25°C, VDD=5 V ± 5%, VSS=0V)**

Internal RC	Drift Rate			
	Temperature (-40°C~85°C)	Voltage (2.2V~5.5V)	Process	Total
4 MHz	± 2%	± 3.5%	± 1%	± 6.5%
8 MHz	± 2%	± 3.5%	± 1%	± 6.5%

6.13 Code Option Register

The EM78F704N has a Code Option Word that is not part of the normal program memory. The option bits cannot be accessed during normal program execution.

Code Option Register and Customer ID Register arrangement distribution:

Word 0	Word 1	Word 2
Bit 12~Bit 0	Bit 12~Bit 0	Bit 12~Bit 0

6.13.1 Code Option Register (Word 0)

Word 0													
Bit	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Mnemonic	**-**	**-**	**-**	**RESETEN**	**-**	**-**	**ENWDT**	**OSC2**	**OSC1**	**OSC0**	**PR2**	**PR1**	**PR0**
1	-	-	-	Enable	-	-	Enable	High	High	High	High	High	High
0	-	-	-	Disable	-	-	Disable	Low	Low	Low	Low	Low	Low
default	0	1	0	0	0	0	0	1	0	0	0	0	0

Bits 12 ~ 10: Not used, always set to "**010**"

Bit 9 (RESETEN): Reset Pin Enable Bit

1 : Enable, P83//RESET=>RESET pin.

0 : Disable, P83//RESET=>P83 (default)

Bits 8 ~ 7: Not used, always set to "**0**"

Bit 6 (ENWDT): Watchdog timer enable bit

1 : Enable

0 : Disable

Bits 5 ~ 3 (OSC2 ~ OSC0): Oscillator Mode Selection bits

Mode	OSC2	OSC1	OSC0
IRC mode, P54 act as I/O pin	**1**	**0**	**0**
IRC mode, P54 act as RCOUT pin	**1**	**0**	**1**

Bits 2 ~ 0 (PR2 ~ PR0): Protect Bit. PR2~PR0 are protect bits, protect type is as follows:

PR2	PR1	PR0	Protect
1	1	1	Enable
0	0	0	Disable

6.13.2 Code Option Register (Word 1)

Word 1													
Bit	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Mnemonic	**-**	**TCEN**	**C6**	**C5**	**C4**	**C3**	**C2**	**C1**	**C0**	**RCM1**	**RCM0**	**LVR1**	**LVR0**
1	**-**	TCC	High	High	High	High	High	High	High	High	High	High	High
0	**-**	P77	Low	Low	Low	Low	Low	Low	Low	Low	Low	Low	Low
Default	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit 12: Not used, always set to "**0**"

Bit 11 (TCEN): TCC enable bit

0 : P77/TCC is set as P77

1 : P77/TCC is set as TCC

Bits 10 ~ 4 (C6 ~ C0): Internal RC mode calibration bits. (IRC frequency auto calibration)

Bits 3 ~ 2 (RCM1 ~ RCM0): RC mode selection bits

RCM 1	RCM 0	*Frequency (MHz)
0	**0**	4
1	**0**	8

Bits 1 ~ 0 (LVR1 ~ LVR0): Low voltage reset enable bits

LVR1	LVR0	Reset Level	Release Level
0	**0**	NA	NA
0	**1**	2.5V	2.6V
1	**0**	2.9V	3.0V
1	**1**	3.2V	3.3V

Note: *LVR1, LVR0="**0, 0**": LVR disabled, power-on reset point of EM78F704N is 2.4V.*

*LVR1, LVR0="**0, 1**": If Vdd < 2.9V, the EM78F704N will reset.*

*LVR1, LVR0="**1, 0**": If Vdd < 3.2V, the EM78F704N will reset.*

*LVR1, LVR0="**1, 1**": If Vdd < 3.9V, the EM78F704N will reset.*

6.13.3 Code Option Register (Word 2)

Word 2													
Bit	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Mnemonic	**SC4**	**SC3**	**SC2**	**SC1**	**SC0**	**-**	**-**	**-**	**SFS**	**IRE**	**-**	**-**	**-**
1	High	High	High	High	High	-	-	-	128kHz	Enable	-	-	-
0	Low	Low	Low	Low	Low	-	-	-	16kHz	Disable	-	-	-
Default	0	0	0	0	0	1	0	0	0	0	0	0	0

Bits 12 ~ 8 (SC4 ~ SC0): Calibrator of sub frequency (WDT frequency auto calibration)

Bits 7 ~ 5: Not used, always set to "**100**"

Bits 4 (SFS): Sub-frequency select.

0: 16kHz (WDT frequency)

1: 128kHz

Bit 3 (IRE): IRC Regulator Enable bit

0: Disable regulator for saving power but more error of IRC.

1: Enable regulator for improving IRC accurately but more power consumed.

Bits 2 ~ 0: Not used, always set to "**0**"

6.14 Power-on Considerations

Any microcontroller is not guaranteed to start to operate properly before the power supply stays has stabilized. The EM78F704N has an on-chip Power-on Voltage Detector (POVD) with a detecting level of 2.0V. It will work well if Vdd can rise quickly enough (50ms or less). In many critical applications, however, extra devices are still required to assist in solving power-up problems.

6.15 External Power-on Reset Circuit

The circuit shown in Figure 6-24 uses an external RC to generate a reset pulse. The pulse width (time constant) should be kept long enough for Vdd to reached minimum operation voltage. This circuit is used when the power supply has slow rise time. Because the current leakage from the /RESET pin is ± 5μA, it is recommended that R should not be greater than 40K. In this way, the /RESET pin voltage is held below 0.2V. The diode (D) functions as a short circuit at the moment of power down.

The capacitor C will discharge rapidly and fully. Rin, the current-limited resistor, will prevent high current or ESD (electrostatic discharge) from flowing to pin /RESET.

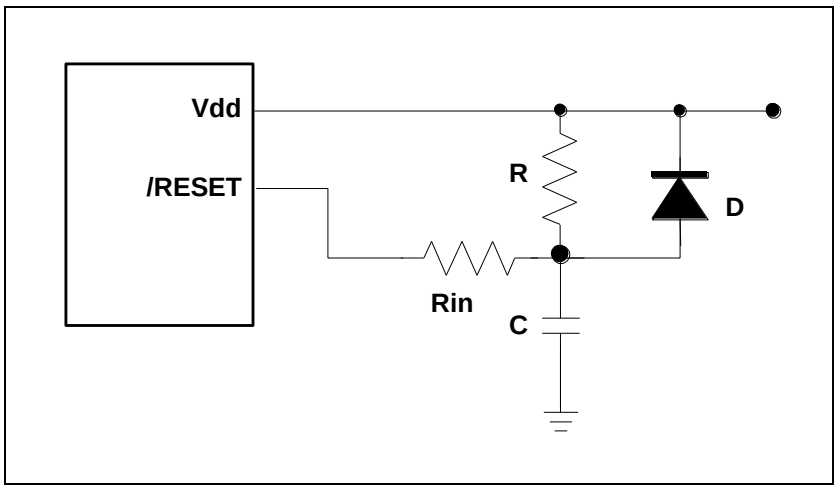


Figure 6-24 External Power-up Reset Circuit

6.16 Residue-Voltage Protection

When battery is replaced, device power (Vdd) is taken off but residue-voltage remains. The residue-voltage may trip below Vdd minimum, but not to zero. This condition may cause a poor power-on reset. Figure 6-25 and Figure 6-26 show how to build a residue-voltage protection circuits.

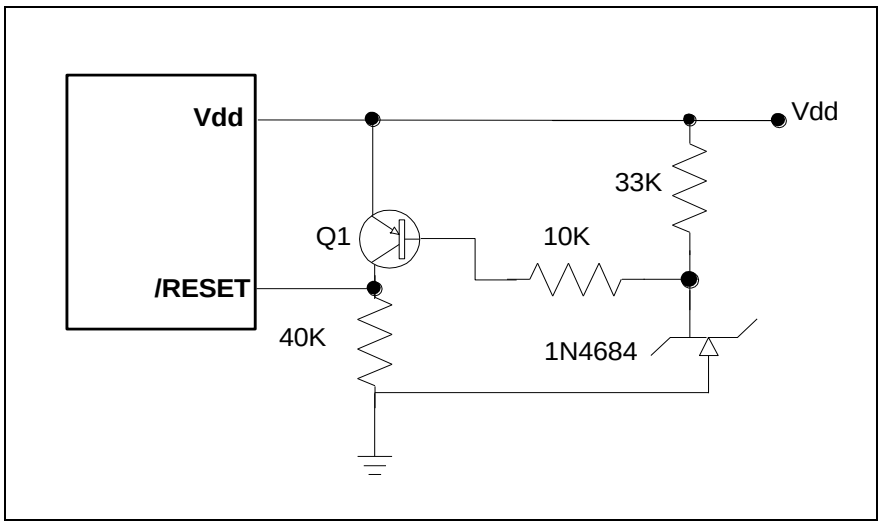


Figure 6-25 Circuit 1 for the Residue Voltage Protection

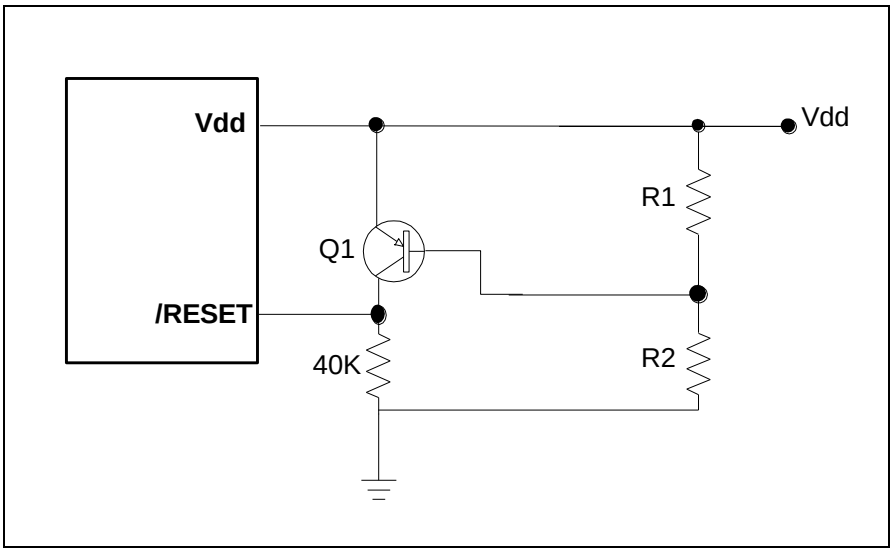


Figure 6-26 Circuit 2 for the Residue Voltage Protection

6.17 Instruction Set

Each instruction in the instruction set is a 13-bit word divided into an OP code and one or more operands. Normally, all instructions are executed within one single instruction cycle (one instruction consists of two oscillator periods), unless the program counter is changed by instruction "MOV R2,A", "ADD R2,A", or by instructions of arithmetic or logic operation on R2 (e.g. "SUB R2,A", "BS(C) R2,6", "CLR R2", ····). In this case, the execution takes two instruction cycles.

If for some reasons, the specification of the instruction cycle is not suitable for certain applications, try modifying the instruction as follows:

(A) "JMP", "CALL", "RET", "RETL", "RETI" commands are executed with one instruction cycle, the conditional skip ("JBS", "JBC", "JZ", "JZA", "DJZ", "DJZA") commands which were tested to be true, are executed within two instruction cycles. The instructions that are written to the program counter also take two instruction cycles.

In addition, the instruction set has the following features:

(1) Every bit of any register can be set, cleared, or tested directly.

(2) The I/O register can be regarded as general register. That is, the same instruction can operate on the I/O register.

■ Instruction Set Table:

The following symbols are used in the following table:

*"**R**" Register designator that specifies which one of the registers (including operation and general purpose registers) is to be utilized by the instruction.*

*"**b**" Bit field designator that selects the value for the bit located in the register R and which affects the operation.*

*"**K**" 8 or 10-bit constant or literal value*

Mnemonic	Operation	Status Affected
NOP	No Operation	None
DAA	Decimal Adjust A	C
CONTW	A → CONT	None
SLEP	0 → WDT, Stop oscillator	T, P
WDTC	0 → WDT	T, P
IOW R	A → IOCR	None[1]
ENI	Enable Interrupt	None
DISI	Disable Interrupt	None
RET	[Top of Stack] → PC	None
RETI	[Top of Stack] → PC, Enable Interrupt	None
CONTR	CONT → A	None
IOR R	IOCR → A	None[1]
MOV R,A	A → R	None
CLRA	0 → A	Z
CLR R	0 → R	Z
SUB A,R	R-A → A	Z, C, DC
SUB R,A	R-A → R	Z, C, DC
DECA R	R-1 → A	Z
DEC R	R-1 → R	Z
OR A,R	A ∨ R → A	Z
OR R,A	A ∨ R → R	Z
AND A,R	A & R → A	Z
AND R,A	A & R → R	Z
XOR A,R	A ⊕ R → A	Z
XOR R,A	A ⊕ R → R	Z
ADD A,R	A + R → A	Z, C, DC
ADD R,A	A + R → R	Z, C, DC
MOV A,R	R → A	Z
MOV R,R	R → R	Z
COMA R	/R → A	Z
COM R	/R → R	Z
INCA R	R+1 → A	Z
INC R	R+1 → R	Z

[1] *This instruction is applicable to IOC5~IOC7, IOCA ~ IOCF only.*

Mnemonic	Operation	Status Affected
DJZA R	R-1 → A, skip if zero	None
DJZ R	R-1 → R, skip if zero	None
RRCA R	R(n) → A(n-1), R(0) → C, C → A(7)	C
RRC R	R(n) → R(n-1), R(0) → C, C → R(7)	C
RLCA R	R(n) → A(n+1), R(7) → C, C → A(0)	C
RLC R	R(n) → R(n+1), R(7) → C, C → R(0)	C
SWAPA R	R(0-3) → A(4-7), R(4-7) → A(0-3)	None
SWAP R	R(0-3) ↔ R(4-7)	None
JZA R	R+1 → A, skip if zero	None
JZ R	R+1 → R, skip if zero	None
BC R,b	0 → R(b)	None[2]
BS R,b	1 → R(b)	None[3]
JBC R,b	if R(b)=0, skip	None
JBS R,b	if R(b)=1, skip	None
CALL k	PC+1 → [SP], (Page, k) → PC	None
JMP k	(Page, k) → PC	None
MOV A,k	k → A	None
OR A,k	A ∨ k → A	Z
AND A,k	A & k → A	Z
XOR A,k	A ⊕ k → A	Z
RETL k	k → A, [Top of Stack] → PC	None
SUB A,k	k-A → A	Z, C, DC
ADD A,k	k+A → A	Z, C, DC
BANK k	K → R4(7:6)	None
LCALL k	Next instruction : k kkkk kkkk kkkk PC+1→[SP], k→PC4	None
LJMP k	Next instruction : k kkkk kkkk kkkk k→PC4	None
TBRD R	If Bank 3 R6.7=0, machine code (7:0) → R Else machine code (12:8) → R(4:0), R(7:5)=(0,0,0)	None

[2] *This instruction is not recommended for interrupt status register operation.*

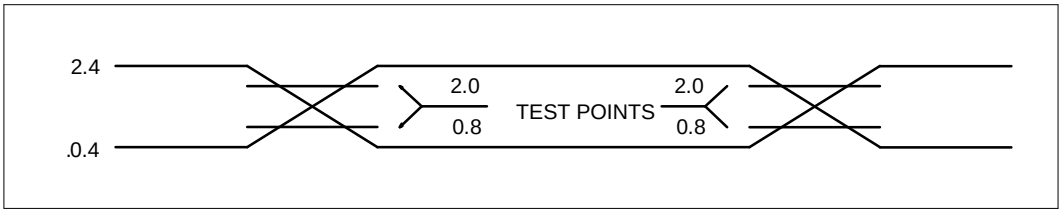
[3] *This instruction cannot operate under interrupt status register.*

6.18 Macro

Syntax:	TKHW_EN MACRO
Description:	EM78F704N Touch Key Hardware Enable **Method:** If Enable Touch Hardware, ENI instruction and TKHW_EN must be enable.
Example:	;Enable Touch Key Hardware ENI TKHW_EN
Syntax:	TKHW_DIS MACRO
Description:	EM78F704N Touch Key Hardware Disable **Method:** If Disable Touch Hardware, DISI instruction and TKHW_DIS must be enable.
Example:	;Disable Touch Key Hardware DISI TKHW_DIS
Syntax:	TK_WRITE MACRO INDEX , DATA
Description:	EM78F704N Touch Key Hardware writes value. **Method:** User Change The touch key hardware parameter by TK_WRITE.
Example:	;TK Strong-2 KEY Mode (INDEX 0x24 written 0XA0) TK_WRITE 0x24,0XA0
Syntax:	TK_READ MACRO INDEX
Description:	EM78F704N Touch Key Hardware read value. **Method:** User Read The touch key hardware parameter by TK_READ.
Example:	;Read Touch Key Mode (Bank2) ReadData → User define variable BANK 2 TK_READ 0x24 MOV ReadData,A
Syntax:	TK_ IDLETIME MACRO TIME,REPEAT
Description:	EM78F704N Touch Key Hardware at TK_IDLE **Method:** TIME: *_500ms*: Touch will run at TK_IDLE for about 500ms, then wake-up to scan all buttons. *_250ms*: Touch will run at TK_IDLE for about 250ms, then wake-up to scan all buttons. *_125ms*: Touch will run at TK_IDLE for about 125ms, then wake-up to scan all buttons. *_62ms*: Touch will run at TK_IDLE for about 62.5ms, then wake-up to scan all buttons. *_32ms:* Touch will run at TK_IDLE for about 32ms, then wake-up to scan all buttons._ REPEAT: *_REPYES*: The Touch key Hardware always at TK_IDLE. *_REPNO*: Touch key Hardware return TK_NORMAL, when any Touch Key pressed. **Note:** TK_IDLE: Touch key Hardware wait TIME up, and wake-up to scan all buttons. TK_NORMAL: Touch key Hardware always scan all buttons.
Example:	;TK SET IDLETIME TK_IDLETIME _250ms,_REPYES

7 Timing Diagrams

AC Test Input/Output Waveform



AC Testing: Input are driven at 2.4V for logic “1” and 0.4V for logic “0”.

Timing measurements are made at 2.0V for logic “1”, and 0.8V for logic “0”.

Figure 7-1 AC Test Timing Diagram

Reset Timing (CLK=“0”)

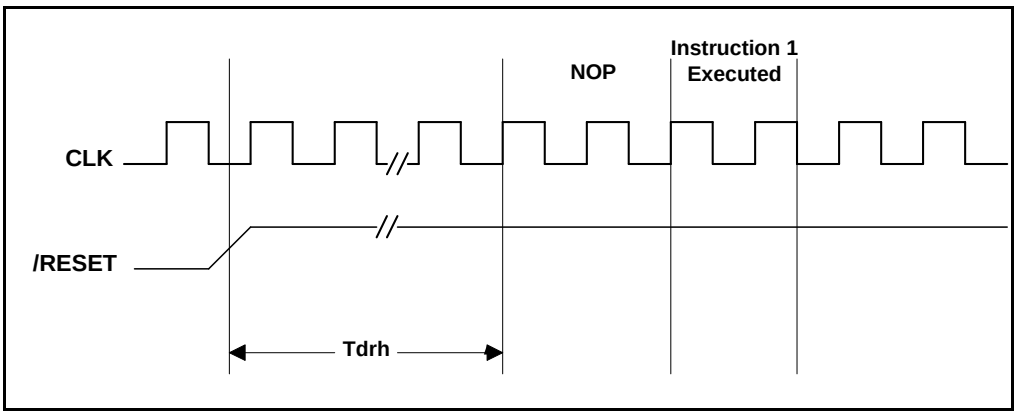


Figure 7-2 Reset Timing Diagram

TCC Input Timing (CLKS=”0”)

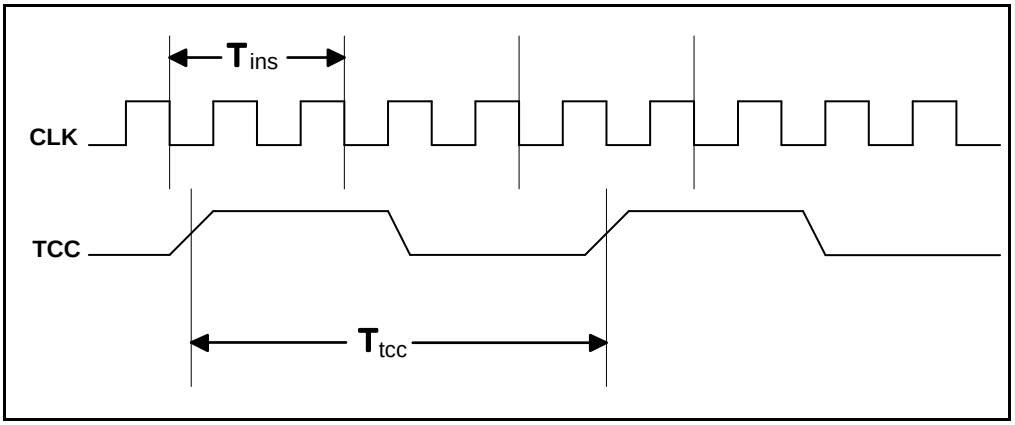


Figure 7-3 TCC Input Timing Diagram

8 Absolute Maximum Ratings

■ **EM78F704N**

Items	Rating		
Temperature under bias	-40°C	to	85°C
Storage temperature	-65°C	to	150°C
Working voltage	2.8	to	5.5V
Working frequency	DC	to	8 MHz*
Input voltage	Vss-0.3V	to	Vdd+0.5V
Output voltage	Vss-0.3V	to	Vdd+0.5V

Note: **These parameters are theoretical values and have not been tested.*

9 DC Electrical Characteristics

VDD=5.0V, VSS=0V, Ta=25°C

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Fxt	IRC: VDD to 5 V	4 MHz, 8 MHz	F±30%	F	F±30%	Hz
IIL	Input Leakage Current for input pins	VIN = VDD, VSS	-	-	±1	μA
VIH1	Input High Voltage (Schmitt Trigger)	Ports 5, 7, 8	-	0.7VDD	-	V
VIL1	Input Low Voltage (Schmitt Trigger)	Ports 5, 7, 8	-	0.3VDD	-	V
VIHT1	Input High Threshold Voltage (Schmitt Trigger)	/RESET	-	0.7VDD	-	V
VILT1	Input Low Threshold Voltage (Schmitt trigger)	/RESET	-	0.3VDD	-	V
VIHT2	Input High Threshold Voltage (Schmitt Trigger)	TCC	-	0.7VDD	-	V
VILT2	Input Low Threshold Voltage (Schmitt Trigger)	TCC	-	0.3VDD	-	V

Note: ** The parameters are theoretical and have not been tested or verified.*

** Data in the Minimum, Typical, Maximum ("Min.", "Typ.", "Max.") column are based on hypothetical results at 25℃. These data are for design guidance only.*

(Continuation)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
IOH1	High Drive Current (Ports 5, 7, 8)	VOH = 0.9VDD	-2.5	-	-	mA
IOL1	Low Sink Current (Ports 5, 7, 8)	VOL = 0.1VDD	10	-	-	mA
IPH	Pull-high current	Pull-high active, input pin at VSS	-	-	-95	μA
IPL	Pull-low current	Pull-low active, input pin at Vdd	-	-	40	μA
LVR1	Low voltage reset level 1 (2.6V)	Ta = 25°C	2.13	2.6	3.07	V
		Ta = -40°C ~ 85°C	1.72	2.6	3.46	V
LVR2	Low voltage reset level 1 (3.0V)	Ta = 25°C	2.48	3.0	3.51	V
		Ta = -40°C ~ 85°C	2.05	3.0	3.93	V
LVR3	Low voltage reset level 1 (3.3V)	Ta = 25°C	2.72	3.3	3.86	V
		Ta = -40°C ~ 85°C	2.25	3.3	4.3	V
ISB1	Power down current	All input and I/O pins at VDD, output pin floating, WDT disabled	-	3	5	μA
ISB2	Power down current	All input and I/O pins at VDD, output pin floating, WDT enabled	-	-	10	μA
ICC1	Operating supply current at two clocks	/RESET= 'High', Fosc=4 MHz, output pin floating, WDT enabled	-	-	4.55	mA
ICC2	Operating supply current at two clocks	/RESET= 'High', Fosc=8 MHz, output pin floating, WDT enabled	-	-	6	mA

NOTE

- *The above parameters are theoretical values only and have not been tested or verified.*
- *Data under the "**Min.**", "**Typ.**", and "**Max.**" (Minimum, Typical, and Maximum) columns are based on hypothetical results at 25°C. These data are for design reference only.*

9.1 Data EEPROM Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Tprog	Erase/Write cycle time	Vdd = 2.8V~ 5.5V Temperature = -40°C ~ 85°C	-	-	-	ms
Treten	Data Retention		-	10	-	Years
Tendu	Endurance time		-	100K	-	Cycles

9.2 Program Flash Memory Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Tprog	Erase/Write cycle time	Vdd = 5.0V Temperature = -40°C ~ 85°C	-	-	-	ms
Treten	Data Retention		-	10	-	Years
Tendu	Endurance time		-	100K	-	Cycles

9.3 A/D Converter Characteristics

VDD=5.0V, VSS=0V, Ta=25°C

Parameter	Symbol	Test Conditions	Type			Unit
			Min.	Typ.	Max.	
Operating Range	Vdd	For 5.5V Fs=100kHz, Fin=2kHz, For 2.8V Fs=50kHz, Fin=1kHz	2.8	-	5.5	V
	V_{REFT}		2.8	-	Vdd	V
Current Consumption	Ivdd	V_{REFT}= Vdd=5.5V, Fs=100kHz, Fin=2kHz	-	-	0.5	mA
	Iref		-	-	50	μA
Standby Current	Isb		-	-	0.1	μA
ZAI	ZAI		-	-	10k	Ω
SNR	SNR	V_{REFT}= Vdd=3.3V, Fs=100kHz, Fin=2kHz	70	-	-	dBc
THD	THD	V_{REFT}= Vdd=3.3V, Fs=100kHz, Fin=2kHz	-	-	-70	dBc
SNDR	SNDR	V_{REFT}= Vdd=3.3V, Fs=100kHz, Fin=2kHz	68	-	-	dBc
Worst Harmonic	WH	V_{REFT}= Vdd=3.3V, Fs=100kHz, Fin=2kHz	-	-	-73	dBc
SFDR	SFDR	V_{REFT}= Vdd=3.3V, Fs=100kHz, Fin=2kHz	73	-	-	dBc
Offset Error	OE	V_{REFT}= Vdd=3.3V, Fs=100kHz	-	-	± 4	LSB
Gain Error	GE	V_{REFT}= Vdd=3.3V, Fs=100kHz	-	-	± 8	LSB
DNL	DNL	V_{REFT}= Vdd=3.3V, Fs=100kHz, Fin=2kHz	-	-	± 1	LSB
INL	INL	V_{REFT}= Vdd=3.3V, Fs=100kHz, Fin=2kHz	-	-	± 4	LSB
Conversion Rate	Fs1	Vdd=2.8~5.5V, Fin=2kHz	100	-	-	K SPS
Power Supply Rejection Ratio	PSRR	V_{REFT}=2.8V, SVREF="0"or"1", Vdd=2.8V ~ 5.5V, Fs=50kHz, Vin=0V ~ 2.8V	-	-	2	LSB

Note: *[1]These parameters are hypothetical (not tested) and are provided for design reference only.*

[2]There is no current consumption when ADC is off other than minor leakage current.

[3]The A/D conversion result will not decrease with an increase in the input voltage, and has no missing code.

[4]These parameters are subject to change without prior notice.

10 AC Electrical Characteristics

EM78F704N, 0 ≤ Ta ≤ 70°C, VDD=5V, VSS=0V

-40 ≤ Ta ≤ 85°C, VDD=5V, VSS=0V

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Dclk	Input CLK duty cycle	–	45	50	55	%
Tins	Instruction cycle time (CLKS="0")	RC type	500	–	DC	ns
Ttcc	TCC input period	–	(Tins+20)/N*	–	–	ns
Tdrh	Device reset hold time	–	11.8	16.8	21.8	ms
Trst	/RESET pulse width	Ta = 25°C	2000	–	–	ns
Twdt	Watchdog timer period	Ta = 25°C	11.8	16.8	21.8	ms
Tset	Input pin setup time	–	–	0	–	ns
Thold	Input pin hold time	–	–	20	–	ns
Tdelay	Output pin delay time	Cload=20pF	–	50	–	ns

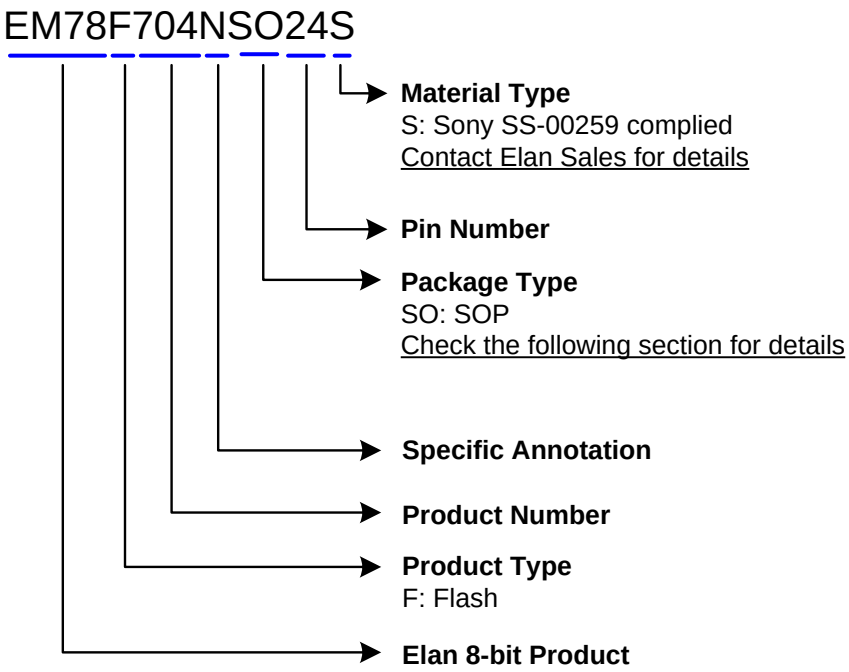
Note: These parameters are theoretical values and have not been tested. Such parameters are for design reference only.

Data in the Minimum, Typical, Maximum (“Min.”, “Typ.”, ”Max.”) columns are based on characterization results at 25°C.

* N = selected prescaler ratio

APPENDIX

A Ordering and Manufacturing Information

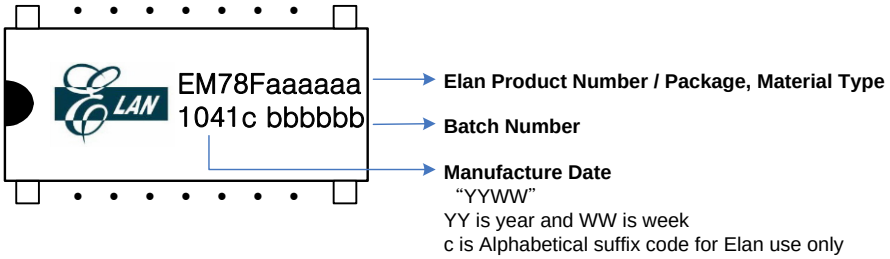


For example:

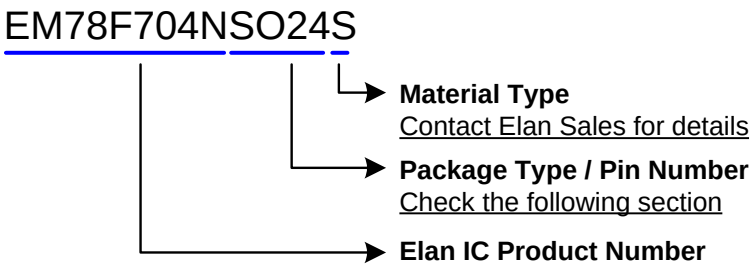
EM78F704NSO24S

is EM78F704N with Flash program memory product,
in 24-pin SOP 300mil package with Sony SS-00259 complied

IC Mark



Ordering Code



B Package Type

Flash MCU	Package Type	Pin Count	Package Size
EM78F704NSO24	SOP	24	300 mil

These are Green products which do not contain hazardous substances and comply with the third edition of Sony SS-00259 standard.

Pb contents should be less than 100ppm and complies with Sony specifications.

Part No.	EM78F704NS
Electroplate type	Pure Tin
Ingredient (%)	Sn:100%
Melting point (°C)	232°C
Electrical resistivity (μΩ cm)	11.4
Hardness (hv)	8~10
Elongation (%)	>50%

C Package Information

C.1 EM78F704NSO24 300mil

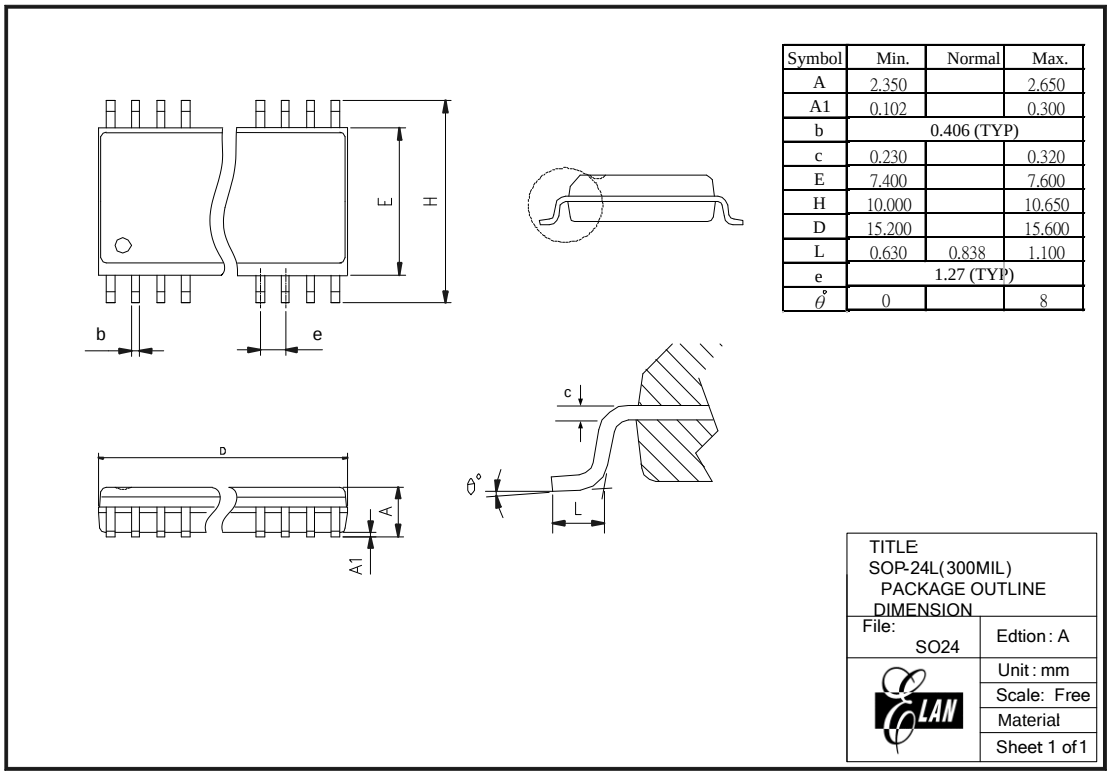


Figure B-1 EM78F704N 24-Pin SOP Package Type

D Quality Assurance and Reliability

Test Category	Test Conditions	Remarks
Solderability	Solder temperature=245±5°C, for 5 seconds up to the stopper using a rosin-type flux	–
Pre-condition	Step 1: TCT, 65°C (15mins)~150°C (15mins), 10 cycles	For SMD IC (such as SOP, QFP, SOJ, etc.)
	Step 2: Bake at 125°C, TD (endurance)=24 hrs	
	Step 3: Soak at 30°C/60%，TD (endurance)=192 hrs	
	Step 4: IR flow 3 cycles (Pkg thickness ≥ 2.5mm or Pkg volume ≥ 350mm^3 ----225±5°C) (Pkg thickness ≤ 2.5mm or Pkg volume ≤ 350mm^3 ----240±5°C)	
Temperature cycle test	-65°C (15mins)~150°C (15mins), 200 cycles	–
Pressure cooker test	TA =121°C, RH=100%, pressure=2 atm, TD (endurance)= 96 hrs	–
High temperature / High humidity test	TA=85°C , RH=85%，TD (endurance) = 168 , 500 hrs	–
High-temperature storage life	TA=150°C, TD (endurance) = 500, 1000 hrs	–
High-temperature operating life	TA=125°C, VCC = Max. operating voltage, TD (endurance) = 168, 500, 1000 hrs	–
Latch-up	TA=25°C, VCC = Max. operating voltage, 150mA/20V	–
ESD (HBM)	TA=25°C, ≥｜± 3KV｜	IP_ND,OP_ND,IO_ND IP_NS,OP_NS,IO_NS IP_PD,OP_PD,IO_PD, IP_PS,OP_PS,IO_PS, VDD-VSS(+),VDD_VSS (-) mode
ESD (MM)	TA=25°C, ≥ ｜± 300V｜	

C.1 Address Trap Detect

An address trap detect is one of the MCU embedded fail-safe functions that detects MCU malfunction caused by noise or the like. Whenever the MCU attempts to fetch an instruction from a certain section of ROM, an internal recovery circuit is auto started. If a noise-caused address error is detected, the MCU will repeat execution of the program until the noise is eliminated. The MCU will then continue to execute the next program.