EM78P134N

8-Bit Microcontroller with OTP ROM

Product Specification

DOC. VERSION 1.6

ELAN MICROELECTRONICS CORP.

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Specification Revision History

Doc. Version	Revision Description	Date
1.0	Initial version	2008/08/11
1.1	Modified the package type description	2008/11/04
1.2	Added description of RC Bit 7	2008/11/12
1.3	Corrected some description error	2009/02/02
1.4	Modified the DC electrical characteristics	2009/03/23
1.5	Modified the operation voltage range	2009/08/10
1.6	Added SSOP10 package type	2010/06/02

1 General Description

The EM78P134N is an 8-bit microprocessor designed and developed with low-power and high-speed CMOS technology. It has an on-chip 1K×13-bit Electrical One Time Programmable Read Only Memory (OTP-ROM). It provides three protection bits to prevent intrusion of user's OTP memory code as well as from unwanted external accesses. Several code option bits are available to meet user's requirements.

With its enhanced OTP-ROM feature, the EM78P134N provides a convenient way of developing and verifying user's programs. Moreover, this OTP device offers the advantages of easy and effective program updates, using development and programming tools. User can avail of the ELAN Writer to easily program his development code.

2 Features

- CPU Configuration
  - 1K×13 bits on-chip ROM
  - 48×8 bits on-chip registers (SRAM, general purpose)
  - 5-level stacks for subroutine nesting
  - Less than 1.5 mA at 5V/IRC 4 MHz
  - Typically 15 μA, at 3V/32kHz
  - Typically 1 μA, during Sleep mode
  - 3 programmable Level Voltage Reset (LVR): 4.0V, 3.3V 2.4V
  - Power-on Reset (POR): 1.8V
- I/O Port Configuration
  - 1 bidirectional I/O port : P6
  - Wake-up port : P6
  - 3 programmable pull-down I/O pins
  - 7 programmable pull-high I/O pins
  - 7 programmable open-drain I/O pins
  - External interrupt : P60
- Operating Voltage Range:

  Operating voltage: 2.1V~5.5V at 0°C ~70°C (commercial)

  Operating voltage: 2.3V~5.5V at -40°C ~85°C (industrial)
- Operating Frequency range (base on 2 clocks):
  - Crystal Mode:

    DC~20MHz/2clks @ 5V

    DC~8MHz/2clks @ 3V

    DC~4MHz/2clks @ 2.1V
  - ERC Mode:

    DC~16 MHz/2clks @ 4.5V

    DC~12 MHz/2clks @ 4V

    DC~4MHz/2clks @ 2.1V
  - Internal RC Drift Rate:

    (Ta=25°C, VDD=5V ± 5%, VSS=0V)

Internal RC Frequency	Drift Rate			
	Temperature (-40℃~85℃)	Voltage (2.0V~5.5V)	Process	Total
455kHz	± 5%	± 5%	±3%	± 13%
4 MHz	± 5%	± 5%	±3%	± 13%
8 MHz	± 5%	± 5%	±3%	± 13%
16 MHz	± 6%	± 5%	±3%	± 14%

- Peripheral Configuration
  - 8-bit real time clock/counter (TCC) with selective signal sources, trigger edges, and overflow interrupt
  - One comparator (typical offset voltage 10mV when input voltage range 0.5V~4.5V) with Cin+/internal Vref level select and Cin- 3 channel switch.
  - One Pulse Width Modulation (PWM) with 10-bit resolution
  - High EFT immunity
  - Power down mode (Sleep mode)
- Five available Interrupts:
  - TCC overflow interrupt
  - Input-port status changed interrupt (wake-up from sleep mode)
  - External interrupt
  - PWM period match completion
  - Comparator output change interrupt
- Other Features
  - Programmable prescaler of oscillator set-up time
  - One security register to prevent intrusion of user's OTP memory code
  - One configuration register to match user's requirements
  - Two clocks per instruction cycle
  - TBRD instruction
- Package Type:
  - 10-pin MSOP 118mil : EM78P134NMS10J
  - 10-pin SSOP 150mil : EM78P134NSS10J

Note: *These are all Green products that do not contain hazardous substances.*

3 Pin Assignment

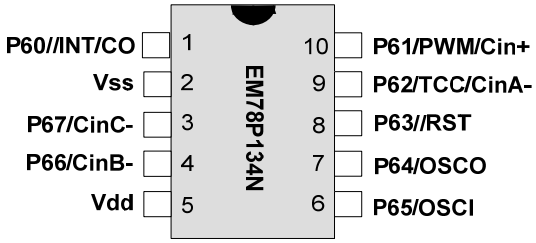


Figure 3-1 EM78P134NMS10J

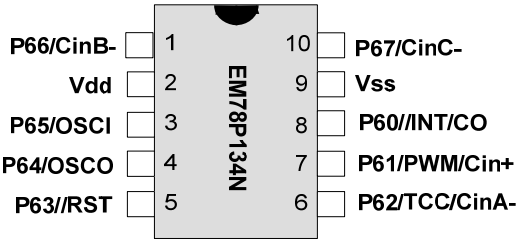


Figure 3-2 EM78P134NSS10 J

4 Pin Description

4.1 EM78P134N – 10 pins

Symbol	Pin No.	Type	Function
P60~P67	1, 3, 4, 6~10	I/O	8-bit general purpose input/output pins. Default value at power-on reset. Can be pulled-high by software control. P60~P62 can be pulled-down by software control. P63 is open drain for output port.
INT	1	I	External interrupt pin triggered by a falling edge.
PWM	10	O	Pulse width modulation output.
/RST	8	I	General-purpose Input only. If it remains at logic low, the device will be reset. Wake-up from sleep mode when pin status changes. Voltage on /RESET must not exceed Vdd during normal mode.
CINA- CINB- CINC- CIN1+ CO	9 4 3 10 1	I I I I O	"-" : the input pin of Vin- of the comparator. Select by CMPCON II (RC) "+" : the input pin of Vin+ of the comparator. Can use External/Internal Voltage input. Pin CO is the comparator output. Set by CMPCON I(RB).
TCC	9	I	Real time clock/counter with Schmitt Trigger input pin. It must be tied to VDD or VSS if not in use.
OSCI	6	I	Crystal type: Crystal input terminal or external clock input pin. RC type: RC oscillator input pin
OSCO	7	O	Crystal type: Output terminal for crystal oscillator or external clock input pin. RC type: Clock output with a duration of one instruction cycle time. The prescaler is determined by the CONT register. External clock signal input.
VDD	5	–	Power supply
VSS	2	–	Ground

5 Functional Description

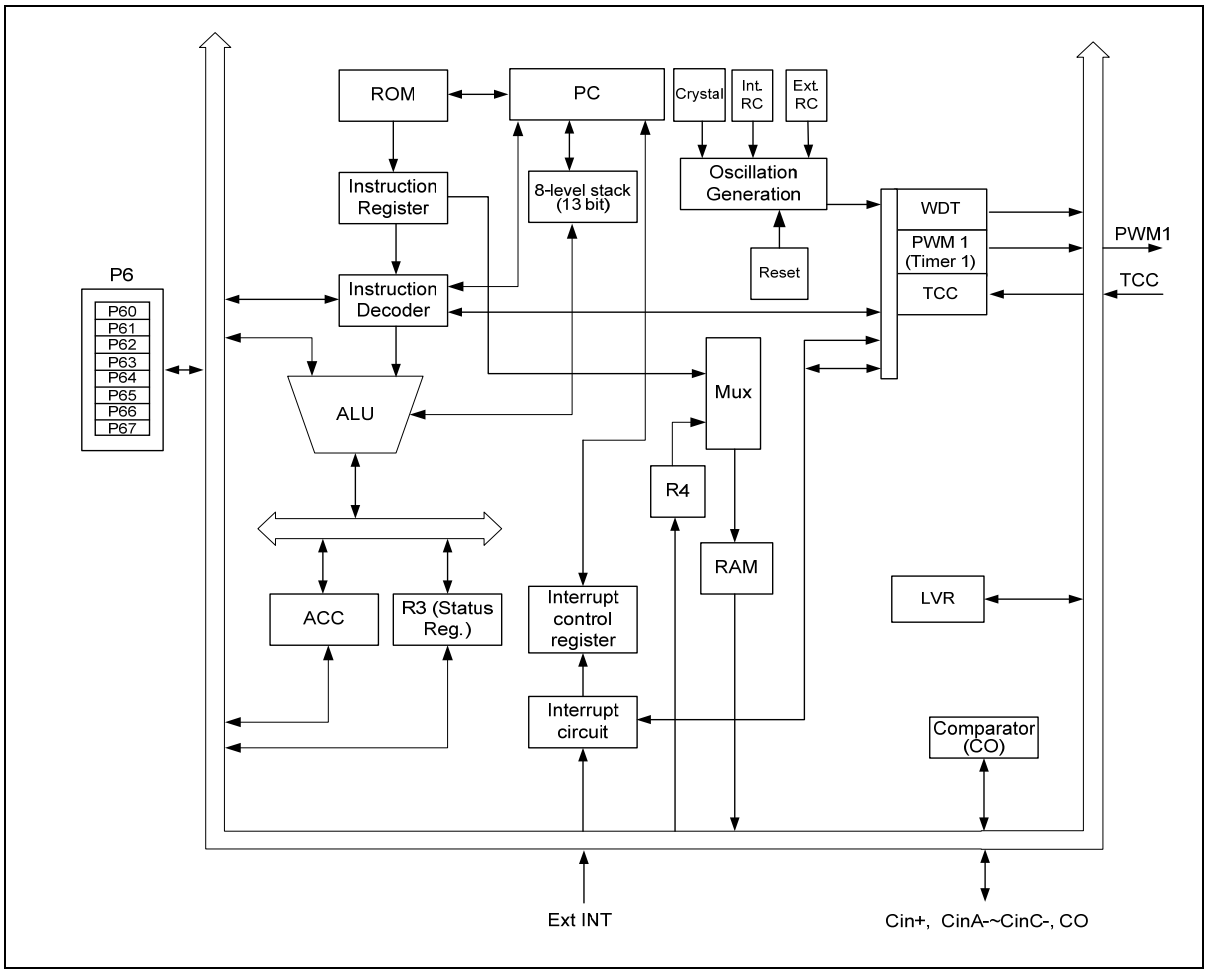


Figure 5-1 Functional Block Diagram

5.1 Operational Registers

5.1.1 R0 (Indirect Addressing Register)

R0 is not a physically implemented register. It is used as an indirect addressing pointer. Any instruction using R0 as a pointer actually accesses data pointed by the RAM Select Register (R4).

5.1.2 R1 (Timer Clock/Counter)

- Incremented by an external signal edge, through the TCC pin, or by the instruction cycle clock.
- External signal of TCC trigger pulse width must be greater than one instruction.
- The signals to increase the counter are determined by Bit 4 and Bit 5 of the CONT register.
- Writable and readable as any other registers.

5.1.3 R2 (Program Counter) and Stack

- Depending on the device type, R2 and hardware stack are 10-bit wide. The structure is depicted in the following figure.

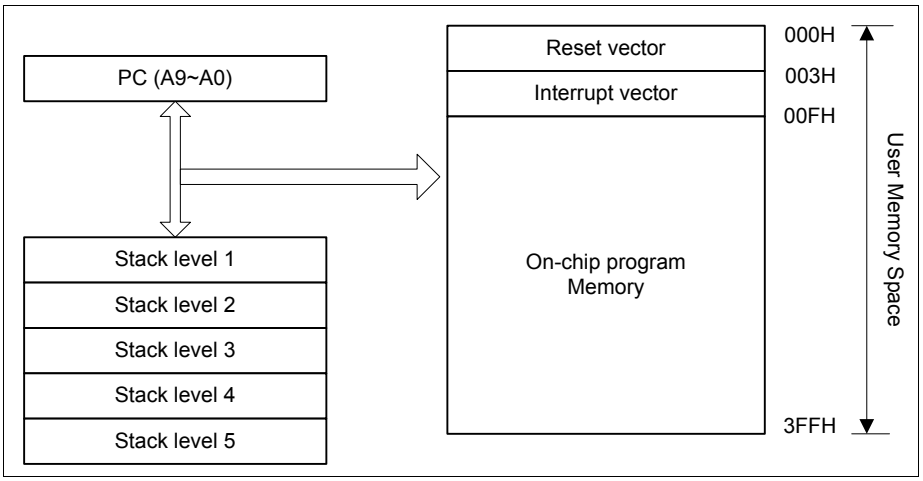


Figure 5-2 Program Counter Organization

- The configuration structure generates 1K×13 bits on-chip OTP ROM addresses to the relative programming instruction codes. One program page is 1024 words long.
- R2 is set as all "0" when under Reset condition.
- "JMP" instruction allows direct loading of the lower 10 program counter bits. Thus, "JMP" allows the PC to go to any location within a page.

- "CALL" instruction loads the lower 10 bits of the PC, and then PC+1 is pushed onto the stack. Thus, the subroutine entry address can be located anywhere within a page.
- "RET" ("RETL k", "RETI") instruction loads the program counter with the contents of the top-level stack.
- "ADD R2,A" allows the contents of 'A' to be added to the current PC, and the ninth and tenth bits of the PC will increase progressively.
- "MOV R2, A" allows loading of an address from the "A" register to the lower 8 bits of the PC, and the ninth and tenth bits of the PC will remain unchanged.
- Any instruction except "ADD R2,A" written to R2 (e.g. "MOV R2, A", "BC R2, 6",·etc.) will cause the ninth bit and the tenth bit (A8 ~ A9) of the PC to remain unchanged.
- All instructions are single instruction cycle (fclk/2 or fclk/4) except for instructions that would change the contents of R2. Such instructions will need one more instruction cycle.
- The Data Memory Configuration is as follows:

Address	R PAGE Registers		IOC PAGE Registers	
00	R0			
01	R1	(TCC)	CONT	(Control Register)
02	R2	(PC)		
03	R3	(Status)		
04	R4	(RSR)		
05	Unused	(-)	Unused	(-)
06	R6	(Port 6)	IOC6	(I/O Port Control Register)
07	R7 (TBLP:Table Point Register)		IOC7	(TMRH: PWM timer)
08	R8 (TBHP:Table Point Register)		IOC8	(TIMEL: PWM timer)
09	R9 (Unused)		IOC9	(PRDL: PWM period)
0A	RA (PWM Control Register)		IOCA	(DTL: Duty cycle of PWM)
0B	RB (Comparator Control Register I)		IOCB	(Pull-down Register)
0C	RC (Comparator Control Register II)		IOCC	(Open-drain Register)
0D	RD (System Control Register)		IOCD	(Pull-high Register)
0E	RE (Wake-up Control Register)		IOCE	(WDT Control Register)
0F	RF (Interrupt Status Register)		IOCF	(Interrupt Mask Register)
10 : 3F	General Registers			

5.1.4 R3 (Status Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RST	GP1	GP0	T	P	Z	DC	C

Bit 7 (RST): Bit for reset type (read only)

0: Set to 0 if the device wakes up from other reset type

1: Set to 1 if the device wakes up from sleep mode on a pin change

Bits 6 ~ 5 (GP1 ~ 0): General purpose read/write bits.

Bit 4 (T): Time-out bit.

Set to 1 with the "SLEP" and "WDTC" command, or during power up and reset to 0 by WDT time-out.

Bit 3 (P): Power down bit.

Set to 1 during power-on or by a "WDTC" command and reset to 0 by a "SLEP" command.

NOTE

Bit 4 and Bit 3 (T and P) are read only.

Bit 2 (Z): Zero flag.

Set to "1" if the result of an arithmetic or logic operation is zero.

Bit 1 (DC): Auxiliary carry flag

Bit 0 (C): Carry flag

5.1.5 R4 (RAM Select Register)

Bits 7 ~ 6 are general-purpose read/write bits. See the Data Memory Configuration.

Bits 5 ~ 0 are used to select registers (Address: 10~3F) in the indirect addressing mode.

5.1.6 R5 (Unused)

5.1.7 R6 (Port 6)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P67	P66	P65	P64	P63	P62	P61	P60

Bits 7 ~ 0 (P67 ~ P60): I/O data registers, user can use the IOC6 to define each bit as input/output.

5.1.8 R7 (TBLP : Table Point Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TBA7	TBA6	TBA5	TBA4	TBA3	TBA2	TBA1	TBA0

Bits 7 ~ 0 (TBA7 ~ TBA0): Table Point Address Bits 7 ~ 0.

5.1.9 R8 (TBHP : Table Point Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
HLB	0	0	0	0	0	TBA9	TBA8

Bit 7 (HLB): Take MSB or LSB as machine code.

0: LSB of machine code.

1: MSB of machine code.

Bits 6 ~ 2 (Unused): Unused bits, set to 0 all the time

Bits 1 ~ 0 (TBA9 ~ TBA8): Table Point Address Bits 9 ~ 8.

5.1.10 R9 (Unused)

5.1.11 RA (PWMCON : PWM Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	PWME	TEN	TP2	TP1	TP0

Bits 7 ~ 5 (Unused): Unused bits, set to 0 all the time.

Bit 4 (PWME): PWM enable bit

0: PWM is off (default value), and its related pin carries out the P61 function.

1: PWM is on, and its related pin is automatically set to output.

NOTE

The P61/PWM/Cin+ pin priority is as follows:

P61/CO/PWM Priority		
High	Medium	Low
Cin+	PWM	P61

Bit 3 (TEN): TMR enable bit

0: TMR is off (default value)

1: TMR is on

Bits 2 ~ 0 (TP2 ~ TP0): TMR clock prescaler bits

TP2	TP1	TP0	Prescale
0	0	0	1:1 (default)
0	0	1	1:2
0	1	0	1:4
0	1	1	1:8
1	0	0	1:16
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

5.1.12 RB (CMPCON I : Comparator Control Register I)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ACOS1	ACOS0	BCOS1	BCOS0	CCOS1	CCOS0	DCOS1	DCOS0

Bits 7 ~ 0(XCOS1 ~ XCOS0): Comparator Select bits

XCOS1	XCOS0	Function Description
0	0	Comparator is not used. P50, P60, P61, P62, P66, and P67 functions as normal I/O pins.
1	1	
0	1	Used as Comparator and P60 functions as normal I/O pin *1
1	0	Used as Comparator and P60 funcions as Comparator output pin (CO) *1

*1: For Cin+ and Cin- definition, refer to RC control register.

NOTE

The P60//INT/CO pin priority is as follows:

P61/PWM/Cin+ Priority		
High	Medium	Low
CO	/INT	P60

5.1.13 RC (CMPCON II : Comparator Control Register II)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CRS	CIRL2	CIRL1	CIRL0	CPOUT	COE	CRCS1	CRCS0

Bit 7 (CRS): Comparator reference voltage source select bit. When comparator disables, this bit must also be set to 0.

0: Disable internal voltage reference, CIN+ external source (default value) If the comparator is disabled, P61/PWM/CIN+ pin acts as I/O.

1: Enable internal voltage reference. P61/PWM/CIN+ pin acts as I/O.

Bits 6 ~ 4 (CIRL2 ~ CIRL0): Comparator internal reference level

CIRL2	CIRL1	CIRL0	Voltage Level (V)
0	0	0	0.1VDD
0	0	1	0.15VDD
0	1	0	0.2VDD
0	1	1	0.3VDD
1	0	0	0.4VDD
1	0	1	0.45VDD
1	1	0	0.5VDD
1	1	1	0.6VDD

Bit 3 (CPOUT): Result of the comparator output.

Bit 2 (COE): Comparator enable bit (RB effect when this bit = 1)

0: Comparator function is disabled (default value)

1: Comparator function is enabled

Bits 1 ~ 0 (CRCS1 ~ CRCS0): Comparator CIN- channel switch

CRCS1	CRCS0	Prescale
0	0	P62/TCC/CinA- is set as CinA- pin (default)
0	1	P66/CinB- is set as CinB- pin
1	0	P67/CinC- is set as CinC- pin
1	1	Reserved

NOTE

The P62/TCC/CinA- Pin Priority is as follows:

P62/TCC/CinA- Priority		
High	Medium	Low
CinA-	TCC	P62

5.1.14 RD (System Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TIMERSC	CPUS	IDLE	0	0	0	0	0

Bit 7 (TIMERSC): TCC, TMR clock source select

0: Fs, sub frequency for WDT internal RC time base

1: Fm, main-oscillator clock

Bit 6 (CPUS): CPU Oscillator Source Select

0: sub-oscillator (fs)

1: main oscillator (fosc)

When CPUS=0, the CPU oscillator selects the sub-oscillator and the main oscillator is stopped.

Bit 5 (IDLE): Idle mode enable bit.

0: IDLE=”0”+SLEP instruction → sleep mode

1: IDLE=”1”+SLEP instruction → idle mode

■ **CPU Operation Mode**

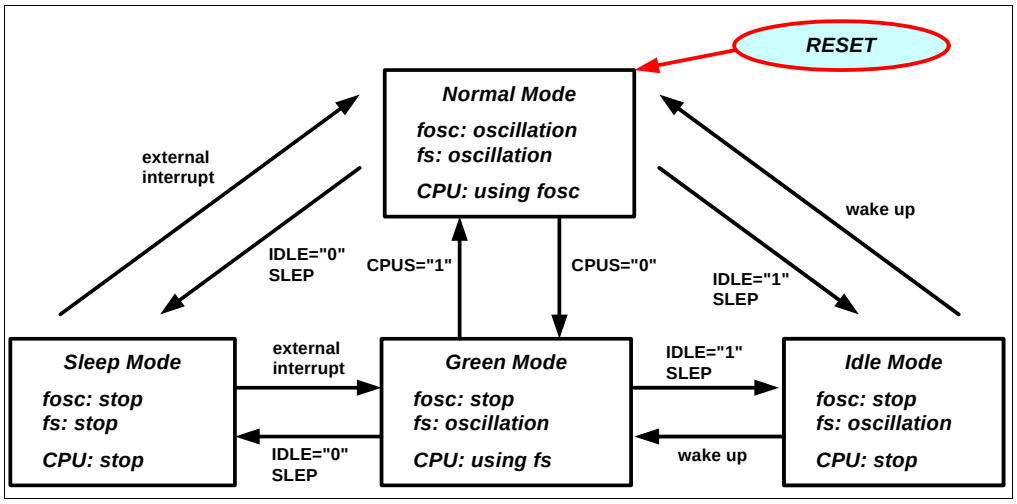


Figure 5-3 CPU Operation Mode

Bits 4 ~ 0 (Unused): Unused bits, set to 0 all the time.

5.1.15 RE (WUCR: Wake-up Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	CMPWE	ICWE	0

Bits 7 ~ 3 (Unused): Unused bits, set to 0 all the time.

Bit 2 (CMPWE): Comparator wake-up enable bit

0: Disable Comparator wake up

1: Enable Comparator wake up

When the Comparator output status change is used to enter an interrupt vector or to wake-up the EM78P134N from sleep mode, the CMPWE bit must be set to “Enable“.

Bit 1 (ICWE): Port 6 input change to wake-up status enable bit.

0: Disable Port 6 input change to wake-up status

1: Enable Port 6 input change wake-up status

When the Port 6 Input Status Change is used to enter an interrupt vector or to wake-up the EM78P134N from sleep mode, the ICWE bit must be set to “Enable“.

Bit 0 (Unused): Unused bit, set to 0 all the time.

5.1.16 RF (Interrupt Status Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	PWMIF	CMPIF	EXIF	ICIF	TCIF

"**1**" means there is an interrupt request "**0**" means no interrupt occurs.

Bits 7 ~ 5 (Unused): Unused bits, set to 0 all the time.

Bit 4 (PWMIF): PWM (Pulse Width Modulation) interrupt flag. Set when a selected duration is reached. Reset by software.

Bit 3 (CMPIF): Comparator interrupt flag. Set when a change occurs in the Comparator output. Reset by software.

Bit 2 (EXIF): External interrupt flag. Set by a falling edge on the /INT pin, reset by software.

Bit 1 (ICIF): Port 6 input status changed interrupt flag. Set when Port 6 input changes, reset by software.

Bit 0 (TCIF): TCC overflow interrupt flag. Set when TCC overflows, reset by software.

- RF can be cleared by instruction but cannot be set.
- IOCF is the interrupt mask register.
- Note that the result of reading RF is the "logic AND" of RF and IOCF.

5.1.17 R10 ~ R3F

- All of these are 8-bit general-purpose registers.

5.2 Special Purpose Registers

5.2.1 A (Accumulator)

Internal data transfer operation, or instruction operand holding usually involves the temporary storage function of the Accumulator, which is not an addressable register.

5.2.2 CONT (Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTE	INT	TS	TE	PSTE	PST2	PST1	PST0

Bit 7 (INTE): INT signal edge

0: interrupt occurs at a rising edge of the INT pin

1: interrupt occurs at a falling edge of the INT pin

Bit 6 (INT): Interrupt enable flag

0: masked by DISI or hardware interrupt

1: enabled by ENI/RETI instructions

Bit 5 (TS): TCC signal source

0: internal instruction cycle clock, P62 is a bidirectional I/O pin.

1: transition on the TCC pin

NOTE

The P62/TCC/CinA- Pin Priority is as follows:

P62/TCC/CinA- Priority		
High	**Medium**	**Low**
CinA-	**TCC**	**P62**

Bit 4 (TE): TCC signal edge

0: increment if a transition from low to high takes place on the TCC pin

1: increment if a transition from high to low takes place on the TCC pin

Bit 3 (PSTE): Prescaler enable bit for TCC

0: prescaler disable bit. TCC rate is 1:1.

1: prescaler enable bit. TCC rate is set at Bit 2 ~ Bit 0.

Bits 2 ~ 0 (PST2 ~ PST0): TCC prescaler bits

PST2	PST1	PST0	TCC Rate
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

5.2.3 IOC5 (Unused)

5.2.4 IOC6 (I/O Port Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IOC67	IOC66	IOC65	IOC64	IOC63	IOC62	IOC61	IOC60

Bits 7 ~ 0 (IOC67 ~ IOC60): I/O direction control register

0: defines the relative I/O pin as output

1: puts the relative I/O pin into high impedance

5.2.5 IOC7 (TMRH: Most Significant Bits of the PWM Timer)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	TMR[9]	TMR[8]	PRD[9]	PRD[8]	DT[9]	DT[8]

Bits 7 ~ 6 (unused): unused bits, set to 0 all the time.

Bits 5 ~ 4 (TMR[9]~TMR[8]): most significant bits of the PWM timer, read-only bit.

Bits 3 ~ 2 (PRD[9]~PRD[8]): most significant bits of the PWM time period.

Bits 1 ~ 0 (DT[9]~DT[8]): most significant bits of the PWM duty cycle.

5.2.6 IOC8 (TMRL: Least Significant Byte of the PWM Timer)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TMR[7]	TMR[6]	TMR[5]	TMR[4]	TMR[3]	TMR[2]	TMR[1]	TMR[0]

The content of IOC8 is read-only.

5.2.7 IOC9 (PRDL: Least Significant Byte of the PWM Time Period)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PRD[7]	PRD[6]	PRD[5]	PRD[4]	PRD[3]	PRD[2]	PRD[1]	PRD[0]

The content of IOC9 is the time period (time base) of PWM. The PWM frequency is the reverse of the period. Most Significant Bits (Bits 9, 8) of the PWM Period Cycle are located in IOC7<3, 2>.

5.2.8 IOCA (DTL: Least Significant Byte of the PWM Duty Cycle)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DT[7]	DT[6]	DT[5]	DT[4]	DT[3]	DT[2]	DT[1]	DT[0]

A specified value keeps the PWM output to remain high until the value matches with TMR.

5.2.9 IOCB (Pull-down Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	/PD62	/PD61	/PD60	0	0	0	0

Bit 7 (unused): Unused bit, set to 0 all the time.

Bit 6 (/PD62): Control bit used to enable pull-down of the P62 pin.

0: Enable internal pull-down

1: Disable internal pull-down

Bit 5 (/PD61): Control bit used to enable pull-down of the P61 pin.

Bit 4 (/PD60): Control bit used to enable pull-down of the P60 pin.

Bits 3 ~ 0 (/PD53): Unused bits, set to 0 all the time.

The IOCB Register is both readable and writable.

5.2.10 IOCC (Open-drain Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OD67	OD66	OD65	OD64	0	OD62	OD61	OD60

Bit 7 (OD67): Control bit used to enable open-drain of the P67 pin.

0: Disable open-drain output

1: Enable open-drain output

Bit 6 (OD66): Control bit used to enable open-drain of the P66 pin.

Bit 5 (OD65): Control bit used to enable open-drain of the P65 pin.

Bit 4 (OD64): Control bit used to enable open-drain of the P64 pin.

Bit 3 (unused): Unused bit, set to 0 all the time.

Bit 2 (OD62): Control bit used to enable open-drain of the P62 pin.

Bit 1 (OD61): Control bit used to enable open-drain of the P61 pin.

Bit 0 (OD60): Control bit used to enable open-drain of the P60 pin.

The IOCC Register is both readable and writable.

5.2.11 IOCD (Pull-high Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/PH67	/PH66	/PH65	/PH64	0	/PH62	/PH61	/PH60

Bit 7 (/PH67): Control bit used to enable pull-high of the P67 pin.

0: Enable internal pull-high

1: Disable internal pull-high

Bit 6 (/PH66): Control bit used to enable pull-high of the P66 pin.

Bit 5 (/PH65): Control bit used to enable pull-high of the P65 pin.

Bit 4 (/PH64): Control bit used to enable pull-high of the P64 pin.

Bit 3 (unused): Unused bit, set to 0 all the time.

Bit 2 (/PH62): Control bit used to enable pull-high of the P62 pin.

Bit 1 (/PH61): Control bit used to enable pull-high of the P61 pin.

Bit 0 (/PH60): Control bit used to enable pull-high of the P60 pin.

The IOCD Register is both readable and writable.

5.2.12 IOCE (WDT Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WDTE	EIS	PSWE	PSW2	PSW1	PSW0	0	0

Bit 7 (WDTE): Control bit used to enable the Watchdog Timer

0: Disable WDT

1: Enable WDT

WDTE is both readable and writable.

Bit 6 (EIS): Control bit used to define the function of the P60 (/INT) pin

0: P60, normal I/O pin

1: /INT, external interrupt pin. In this case, the I/O control bit of P60 (Bit 0 of IOC6) must be set to "1"

NOTE

- *When EIS is "0," the path of the /INT pin is masked. When EIS is "1," the status of the /INT pin can also be read by way of reading Port 6 (R6). Refer to Figure 6-5 (I/O Port and I/O Control Register Circuit for P60 (/INT)) in Section 6.4 (I/O Ports).*
- *The EIS is both readable and writable.*

Bit 5 (PSWE): prescaler enable bit for WDT

0: prescaler disable bit. WDT rate is 1:1

1: prescaler enable bit. WDT rate is set at Bit 4~Bit 2

Bits 4 ~ 2 (PSW2 ~ PSW0): WDT prescaler bits.

PSW2	PSW1	PSW0	WDT Rate
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

Bits 1 ~ 0: unused bits, set to 0 all the time.

5.2.13 IOCF (Interrupt Mask Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	PWMIE	CMPIE	EXIE	ICIE	TCIE

Bits 7 ~ 5: Unused bits, set to 0 all the time.

Bit 4 (PWMIE): PWMIF interrupt enable bit

0: Disable PWM interrupt

1: Enable PWM interrupt

Bit 3 (CMPIE): CMPIF interrupt enable bit

0: Disable CMPIF interrupt

1: Enable CMPIF interrupt

When the Comparator output status change is used to enter an interrupt vector or to enter the next instruction, the CMPIE bit must be set to "Enable".

Bit 2 (EXIE): EXIF interrupt enable bit.

0: disable EXIF interrupt

1: enable EXIF interrupt

Bit 1 (ICIE): ICIF interrupt enable bit.

0: Disable ICIF interrupt

1: Enable ICIF interrupt

Bit 0 (TCIE): TCIF interrupt enable bit.

0: Disable TCIF interrupt

1: Enable TCIF interrupt

The IOCF register is both readable and writable.

5.3 TCC/WDT and Prescaler

There are two 8-bit counters available as prescalers for the TCC and WDT respectively. The PST0 ~ PST2 bits of the CONT register are used to determine the ratio of the TCC prescaler, and the PSW0 ~ PSW2 bits of the IOCE0 register are used to determine the WDT prescaler. The prescaler counter is cleared by the instructions each time such instructions are written into the TCC. The WDT and prescaler will be cleared by the "WDTC" and "SLEP" instructions. Figure 5-4 depicts the block diagram of TCC/WDT.

TCC (R1) is an 8-bit timer/counter. The TCC clock source can be an internal clock or external signal input (edge selectable from the TCC pin). If the TCC signal source is from an internal clock, TCC will increase by 1 at every 1/Fc clock (without prescaler). If TCC signal source is from the external clock input, TCC will increase by 1 at every falling edge or rising edge of the TCC pin. The TCC pin input time length (kept at High or Low level) must be greater than 1CLK.

The watchdog timer is a free running on-chip RC oscillator. The WDT will keep on running even when the oscillator driver has been turned off (i.e., in sleep mode). During normal operation or sleep mode, a WDT time-out (if enabled) will cause the device to reset. The WDT can be enabled or disabled any time during normal mode through software programming. Refer to WDTE bit of the IOCE0 register. Without prescaler, the WDT time-out duration is approximately 18 ms.[1]

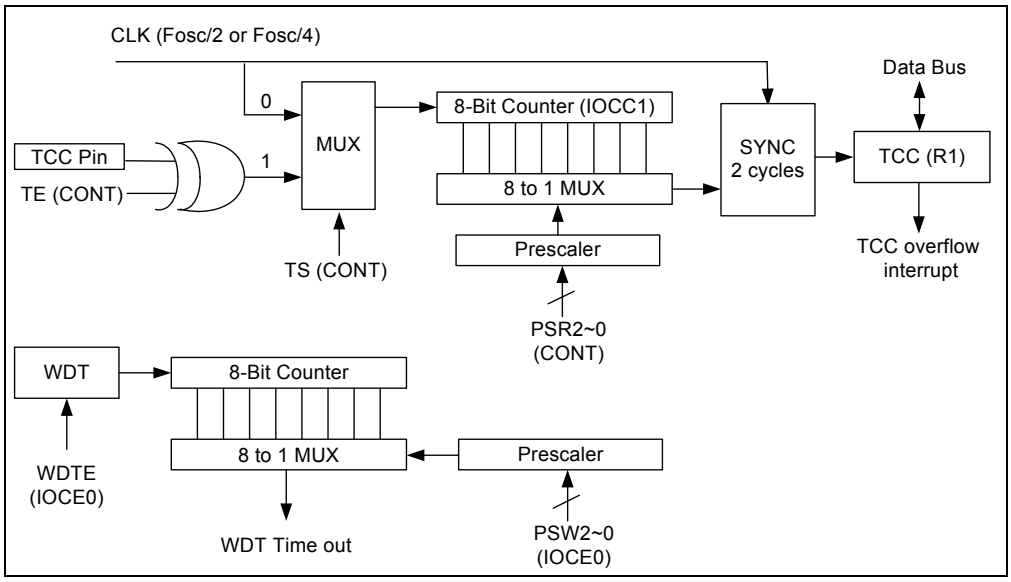
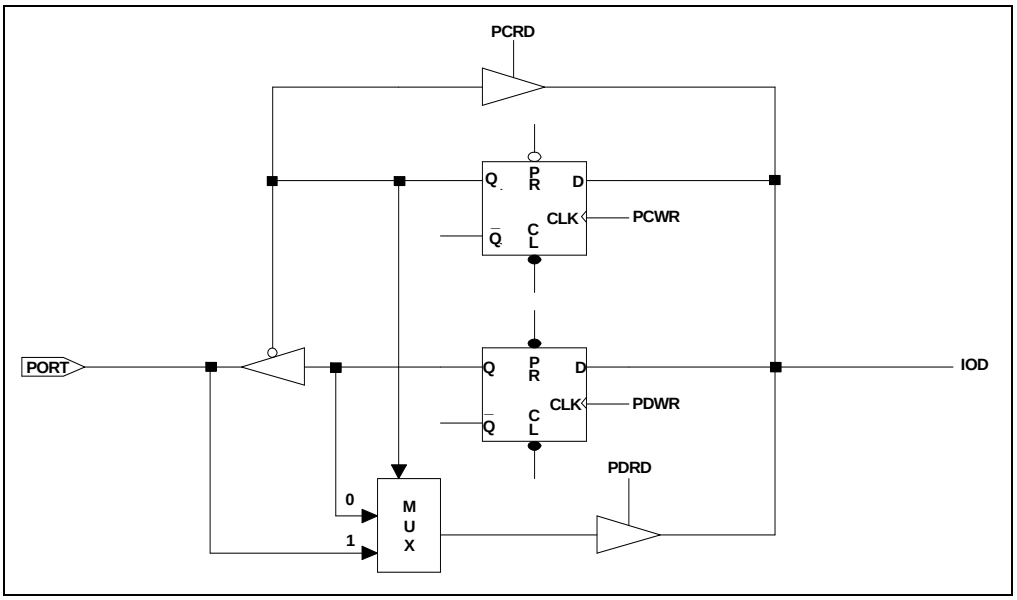


Figure 5-4 TCC and WDT Block Diagram

[1] VDD=5V, Setup time period = 16.5ms ± 30%.
VDD=3V, Setup time period = 18ms ± 30%.

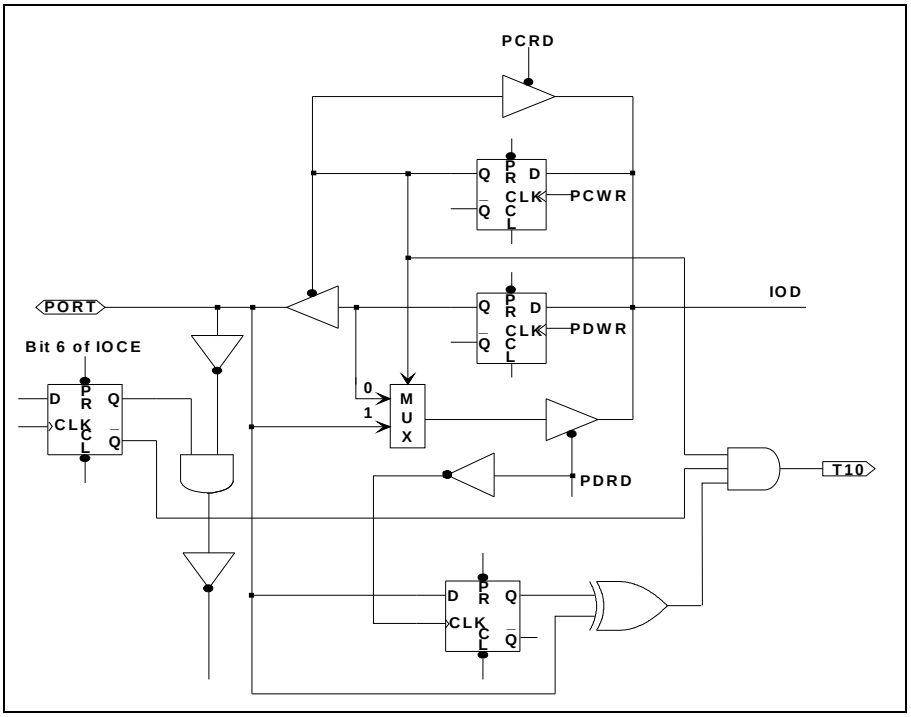
5.4 I/O Ports

The I/O registers, Port 6, is bidirectional tri-state I/O port. Port 6 can be pulled-high internally by software except P63. In addition, Port 6 can also have open-drain output by software except P63. Input status changed interrupt (or wake-up) function is available from Port 6. P62 ~ P60 pins can be pulled-down by software. Each I/O pin can be defined as "input" or "output" pin by the I/O control register (IOC6) except P63. The I/O registers and I/O control registers are both readable and writable. The I/O interface circuits for Port 6 are shown in Figure 5-5, Figure 5-6 and Figure 5-7 respectively.



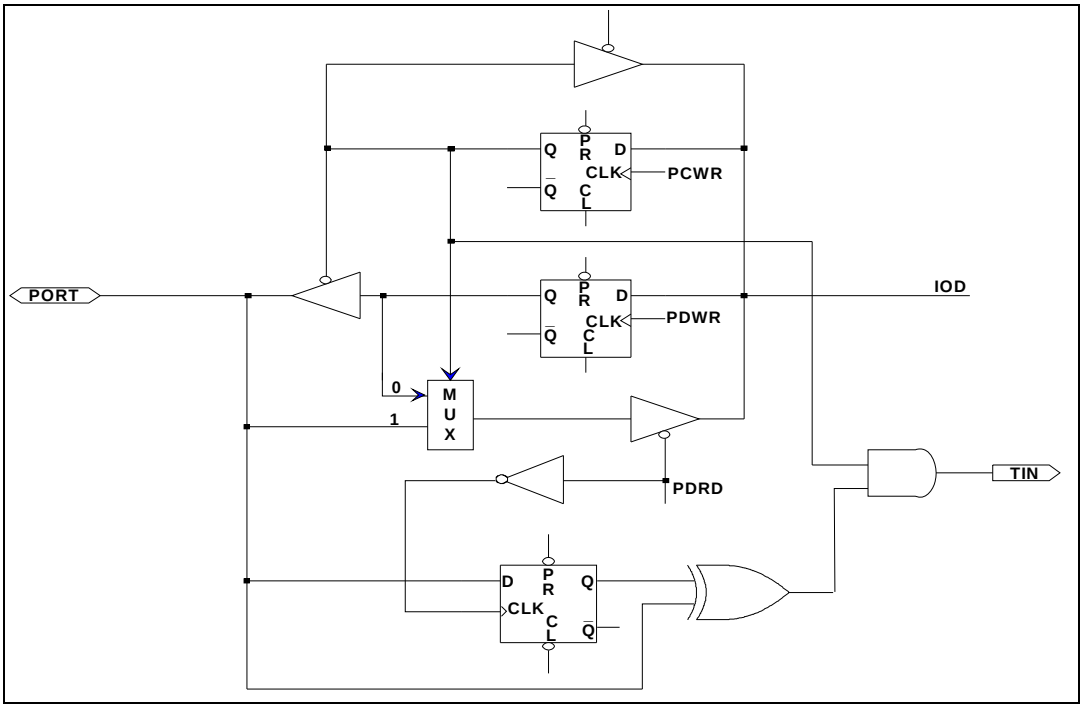
Note: Pull-down is not shown in the figure.

Figure 5-5 The Circuit of I/O Port and I/O Control Register for Port 6



Note: Pull-high (down), open-drain is not shown in the figure.

Figure 5-6 Circuit of I/O Port and I/O Control Register for P60(/INT)



Note: Pull-high (down), open-drain is not shown in the figure.

Figure 5-7 Circuit of I/O Port and I/O Control Register for P61~P67

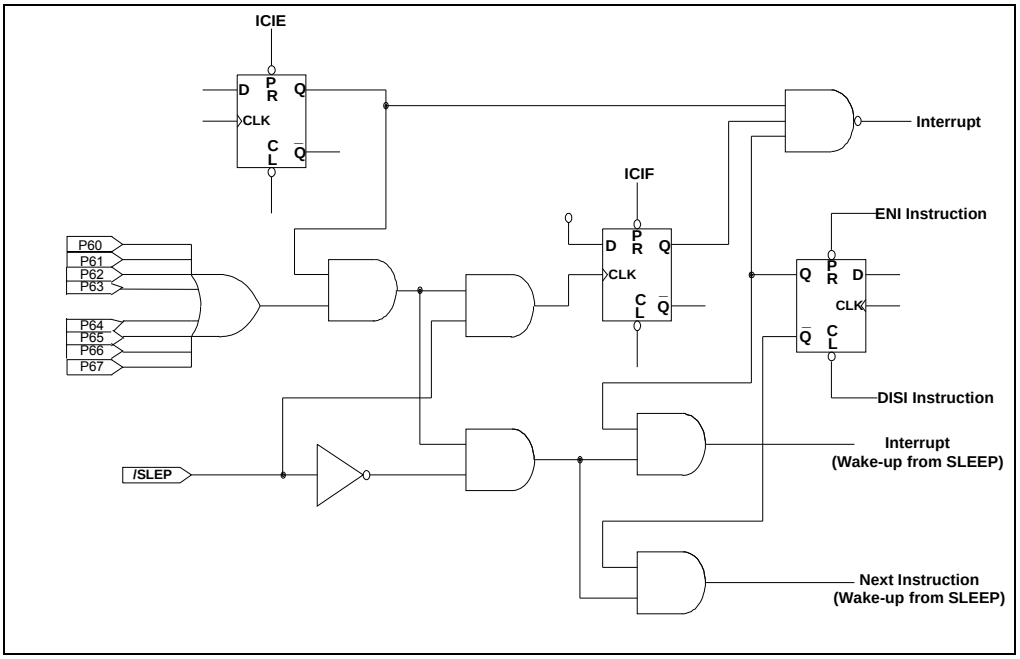


Figure 5-8 Block Diagram of I/O Port 6 with input Change Interrupt/Wake-up

Table 5-1 Usage of Port 6 Input Change Wake-up/Interrupt Function

Usage of Port 6 Input Status Change Wake-up/Interrupt	
(I) Wake-up from Port 6 Input Status Change (a) Before Sleep 1. Disable WDT 2. Read I/O Port 6 (MOV R6,R6) 3. Execute "ENI" or "DISI" 4. Enable interrupt (Set IOCF.1) 5. Execute "SLEP" instruction (b) After Wake-up 1. IF "ENI" → Interrupt vector (006H) 2. IF "DISI" → Next instruction	(II) Port 6 Input Status Change Interrupt 1. Read I/O Port 6 (MOV R6,R6) 2. Execute "ENI" 3. Enable interrupt (Set IOCF.1) 4. IF Port 6 change (interrupt) → Interrupt Vector (006H)

5.5 Reset and Wake-up

5.5.1 Reset

Input Status Change

(1) Power-on reset

(2) /RESET pin input "low"

(3) WDT time-out (if enabled)

The device is kept in a reset condition for a period of approximately 18 ms[2] (one oscillator start-up timer period) after a reset is detected. Once a reset occurs, the following functions are performed.

- The oscillator is running, or will be started.
- The Program Counter (R2) is set to all "0".
- All I/O port pins are configured as input mode (high-impedance state).
- The Watchdog timer and prescaler are cleared.
- When power is switched on, the upper 3 bits of R3 are cleared.
- The bits of the CONT register are set to all "1" except for Bit 6 (INT flag).
- The bits of the IOCB register are set to all "1".
- The IOCC register is cleared.
- The bits of the IOCD register are set to all "1".
- Bit 7 of the IOCE register is set to "1", and Bits 6~0 are cleared
- Bits 0 ~ 4 of RF and Bits 0 ~ 4 of IOCF register are cleared.

Sleep (power down) mode is attained by executing the “SLEP” instruction. While entering sleep mode, WDT (if enabled) is cleared but keeps on running. The controller can be waken up by:

(1) External reset input on the /RESET pin

(2) WDT time-out (if enabled), or

(3) Port 6 input status changes (if enabled).

The first two cases will cause the EM78P134N to reset. The T and P flags of R3 can be used to determine the source of the reset (wake-up). The last case is considered a continuation of program execution and the global interrupt ("ENI" or "DISI" being executed) determines whether or not the controller branches to the interrupt vector following a wake-up. If ENI is executed before SLEP, the instruction will begin to execute from the interrupt vector address after a wake-up. If DISI is executed before SLEP, the operation will restart from the instruction right next to SLEP after a wake-up.

[2] Vdd = 5V, set up time period = 16.5ms ± 30%
Vdd = 3V, set up time period = 18ms ± 30%

Only one of Cases 2 and 3 can be enabled before entering sleep mode. That is,

[a] if Port 6 input status changed interrupt is enabled before SLEP, WDT must be disabled by software. However, the WDT bit in the option register remains enabled. Hence, the EM78P134N can be awakened only by Case 1 or 3.

[b] if WDT is enabled before SLEP, Port 6 Input Status Change Interrupt must be disabled. Hence, the EM78P134N can be awakened only by Case 1 or 2. Refer to the section on *Interrupt*.

If Port 6 Input Status Changed Interrupt is used to wake-up the EM78P134N (Case [a] above), the following instructions must be executed before SLEP:

```
MOV             A, @xxxx1110b   ; Select WDT prescaler,
                                ; the prescaler  must be set over
                                ; 1:1
CONTW
WDTC                            ; Clear WDT and prescaler
MOV             A, @0xxxxxxxb   ; Disable WDT
IOW             RE
MOV             R6, R6          ; Read Port 6
MOV             A, @00000x1xb   ; Enable Port 6 input change
                                ; interrupt
IOW             RF
ENI (or DISI)                   ; Enable (or disable) global
                                ; interrupt
SLEP                            ; Sleep
```

NOTE

1. *After waking up from sleep mode, the WDT is automatically enabled. The WDT enable/disable operation after waking up from sleep mode should be properly defined in the software.*
2. *To avoid a reset from occurring when the Port 6 Input Status Changed Interrupt enters into an interrupt vector or is used to wake-up the MCU, the WDT prescaler must be set above the 1:1 ratio.*

5.5.2 Wake-up and Interrupt Modes Operation Summary

All categories under wake-up and interrupt modes are summarized below.

The controller can be waken-up from sleep mode and idle mode. The wake-up signals are listed as follows:

After wake up:

Wake-up Signal	Sleep Mode	Idle Mode	Green Mode	Normal Mode
External interrupt	×	Wake-up + interrupt (if interrupt is enabled) + next instruction	Interrupt (if interrupt is enabled) or next instruction	Interrupt (if interrupt is enabled) or next instruction
Port 6 pin change	If ICWE bit is enabled Wake-up + interrupt (if interrupt is enabled) + next instruction	If ICWE bit is enabled Wake-up + interrupt (if interrupt is enabled) + next instruction	Interrupt (if interrupt is enabled) or next instruction	Interrupt (if interrupt is enabled) or next instruction
TCC overflow interrupt	×	Wake-up + interrupt (if interrupt is enabled) + next instruction	Interrupt (if interrupt is enabled) or next instruction	Interrupt (if interrupt is enabled) or next instruction
Comparator interrupt	If CMPWE bit is enabled Wake-up + interrupt (if interrupt is enabled) + next instruction	If CMPWE bit is enabled Wake-up + interrupt (if interrupt is enabled) + next instruction	Interrupt (if interrupt is enabled) or next instruction	Interrupt (if interrupt is enabled) or next instruction
PWM (When TMR matches PRD)	×	Wake-up + interrupt (if interrupt is enabled) + next instruction	Interrupt (if interrupt is enabled) or next instruction	Interrupt (if interrupt is enabled) or next instruction
WDT Time out	RESET	RESET	RESET	RESET
Low Voltage Reset	RESET	RESET	RESET	RESET

Note: 1. If interrupt is enabled → interrupt+ next instruction
2. If interrupt is disabled → next instruction

Signal	Sleep Mode	Normal Mode
TCC Overflow	N/A	**DISI + IOCF0 (TCIE) Bit 0 = 1**
		Next Instruction+ Set RF (TCIF) = 1
		ENI + IOCF0 (TCIE) Bit 0 = 1
		Interrupt Vector (0x09)+ Set RF (TCIF) = 1
Port 6 Input Status Change	**RE (ICWE) Bit 1 = 0, IOCF0 (ICIE) Bit 1 = 0**	**IOCF0 (ICIE) Bit 1 = 0**
	Oscillator, TCC and TIMERX are stopped. Port 6 input status change wake up is invalid.	Port 6 input status change interrupt is invalid
	RE (ICWE) Bit 1 = 0, IOCF0 (ICIE) Bit 1 = 1	
	Set RF (ICIF) = 1, Oscillator, TCC and TIMERX are stopped. Port 6 input status change wake up is invalid.	
	RE (ICWE) Bit 1 = 1, IOCF0 (ICIE) Bit 1 = 0	
	Wake-up+ Next Instruction Oscillator, TCC and TIMERX are stopped.	
	RE (ICWE) Bit 1 = 1, DISI + IOCF0 (ICIE) Bit 1 = 1	**DISI + IOCF0 (ICIE) Bit 1 = 1**
	Wake-up+ Next Instruction+ Set RF (ICIF) = 1 Oscillator, TCC and TIMERX are stopped.	Next Instruction+ Set RF (ICIF) = 1
	RE (ICWE) Bit 1=1, ENI + IOCF0 (ICIE) Bit 1 = 1	**ENI + IOCF0 (ICIE) Bit 1 = 1**
	Wake-up+ Interrupt Vector (0x06)+ Set RF (ICIF)=1 Oscillator, TCC and TIMERX are stopped.	Interrupt Vector (0x06)+ Set RF (ICIF)=1
INT Pin	N/A	**DISI + IOCF0 (EXIE) Bit 3 = 1**
		Next Instruction+ Set RF (EXIF) = 1
		ENI + IOCF0 (EXIE) Bit 3 = 1
		Interrupt Vector (0x03)+ Set RF (EXIF)=1
PWM (When TMR matches PRD)	N/A	**DISI + IOCF0 (PWMIE)=1**
		Next Instruction+ Set RF (PWMIF) = 1
		ENI + IOCF0 (PWMIE)=1
		Interrupt Vector (0x0F)+ Set RF (PWMIF) = 1
Comparator (Comparator Output Status Change)	**RE (CMPWE) Bit 2 = 0, IOCF0 (CMPIE) Bit 2 = 0**	**IOCF0 (CMPIE) Bit 7 = 0**
	Comparator output status change wake-up is invalid. Oscillator, TCC and TMR are stopped.	Comparator output status change interrupt is invalid.
	RE (CMPWE) Bit 2 = 0, IOCF0 (CMPIE) Bit 2 = 1	
	Set RF (CMPIF) = 1, Comparator output status change wake up is invalid. Oscillator, TCC and TMR are stopped.	
	RE (CMPWE) Bit 2 = 1, IOCF0 (CMPIE) Bit 2 = 0	
	Wake-up+ Next Instruction, Oscillator, TCC and TMR are stopped.	
	RE (CMPWE) Bit 2=1, DISI + IOCF0 (CMPIE) Bit 2 = 1	**DISI + IOCF0 (CMPIE) Bit 7 = 1**
	Wake-up+ Next Instruction+ Set RF (CMPIF) = 1, Oscillator, TCC and TMR are stopped.	Next Instruction+ Set RF (CMPIF) = 1
	RE (CMPWE) Bit 2 = 1, ENI + IOCF0 (CMPIE) Bit 2 = 1	**ENI + IOCF0 (CMPIE) Bit 7 = 1**
	Wake-up+ Interrupt Vector (0x0C)+ Set RF (CMPIF)=1 Oscillator, TCC and TMR are stopped.	Interrupt Vector (0x0C)+ Set RF (CMPIF) = 1
WDT Time Out IOCE (WDTE) Bit 7 = 1	Wake-up+ Reset (Address 0x00)	Reset (Address 0x00)

Table 5-2 Summary of the Initialized Register Values

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
N/A	IOC5 (unused)	Bit Name	×	×	×	×	×	×	×	×
		Power-on	0	0	1	1	1	1	1	1
		/RESET and WDT	0	0	1	1	1	1	1	1
		Wake-up from Pin Change	0	0	P	P	P	P	P	P
N/A	IOC6	Bit Name	C67	C66	C65	C64	C63	C62	C61	C60
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×05	R5 (unused)	Bit Name	×	×	×	×	×	×	×	×
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×06	P6	Bit Name	P67	P66	P65	P64	P63	P62	P61	P60
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×07	R7 (TBPL)	Bit Name	-	-	-	-	-	-	-	-
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	CONT	Bit Name	INTE	INT	TS	TE	PSTE	PST2	PST1	PST0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	0	P	P	P	P	P	P
0×00	R0 (IAR)	Bit Name	-	-	-	-	-	-	-	-
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0×01	R1 (TCC)	Bit Name	-	-	-	-	-	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×02	R2 (PC)	Bit Name	-	-	-	-	-	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	N	P	P	P
0×03	R3 (SR)	Bit Name	RST	GP1	GP0	T	P	Z	DC	C
		Power-on	0	0	0	1	1	U	U	U
		/RESET and WDT	0	0	0	t	t	P	P	P
		Wake-up from Pin Change	1	P	P	t	t	P	P	P
0×04	R4 (RSR)	Bit Name	GP1	GP0	-	-	-	-	-	-
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×08 ~ 0×09	R8 ~ R9	Bit Name	-	-	-	-	-	-	-	-
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0A	RA (PWMCON)	Bit Name	-	-	-	PWME	T1EN	T1P2	T1P1	T1P0
		Power-on				0	0	0	0	0
		/RESET and WDT				0	0	0	0	0
		Wake-up from Pin Change				P	P	P	P	P
0×0B	RB (CMPCON I)	Bit Name	ACOS1	ACOS0	BCOS1	BCOS0	CCOS1	CCOS0	DCOS1	DCOS0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0×0C	RC (CMPCON II)	Bit Name	CRS	CIRL2	CIRL1	CIRL0	CPOUT	COE	CRCS1	CRCS0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0D	RD	Bit Name	TIMERSC	CPUS	IDLE	-	-	-	-	-
		Power-on	0	1	1	0	0	0	0	0
		/RESET and WDT	0	1	1	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0E	RE (WUCR)	Bit Name	-	-	-	-	-	CMPWE	ICWE	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0F	RF	Bit Name	-	-	-	PWMIF	EXIF	CMPIF	ICIF	TCIF
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOC7	Bit Name	-	-	TMR[9]	TMR[8]	PRD[9]	PRD[8]	DT[9]	DT[8]
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOC8 (TMRL)	Bit Name	TMR[7]	TMR[6]	TMR[5]	TMR[4]	TMR[3]	TMR[2]	TMR[1]	TMR[0]
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOC9 (PRDL)	Bit Name	PRD[7]	PRD[6]	PRD[5]	PRD[4]	PRD[3]	PRD[2]	PRD[1]	PRD[0]
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
N/A	IOCA (DTL)	Bit Name	DT[7]	DT[6]	DT[5]	DT[4]	DT[3]	DT[2]	DT[1]	DT[0]
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOCB	Bit Name	0	/PD62	/PD61	/PD60	0	0	0	0
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOCC	Bit Name	OD67	OD66	OD65	OD64	×	OD62	OD61	OD60
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOCD	Bit Name	/PH67	/PH66	/PH65	/PH64	×	/PH62	/PH61	/PH60
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOCE	Bit Name	WDTE	EIS	PSWE	PSW2	PSW1	PSW0	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOCF	Bit Name	-	-	-	PWMIE	EXIE	CMPIE	ICIE	TCIE
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×10 ~ 0×3F	R10~R3F	Bit Name	-	-	-	-	-	-	-	-
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P

Legend: **×:** Not used **U:** Unknown or don't care **P:** Previous value before reset **-:** not defined

5.5.3 /RESET Configuration

Refer to Figure 5-8 when the reset bit in the Option word is programmed to 0, the external /RESET is enabled. When programmed to 1, the internal /RESET is enabled, tied to the internal Vdd and the pin is defined as P63.

5.5.4 Status of RST, T, and P of the Status Register

A reset condition is initiated by the following events:

1. Power-on condition
2. High-low-high pulse on /RESET pin
3. Watchdog timer time-out

The values of RST, T and P, listed in Table 5-2 are used to check how the processor wakes up.

Table 5-4 shows the events which may affect the status of RST, T and P.

Table 5-3 Values of RST, T and P after Reset

Reset Type	RST	T	P
Power on	0	1	1
/RESET during Operating mode	0	*P	*P
/RESET wake-up during Sleep mode	0	1	0
WDT during Operating mode	0	0	P
WDT wake-up during Sleep mode	0	0	0
Wake-up on pin change during Sleep mode	1	1	0

*P: Previous status before reset

Table 5-4 Status of RST, T and P being Affected by Events

Event	RST	T	P
Power on	0	1	1
WDTC instruction	*P	1	1
WDT time-out	0	0	*P
SLEP instruction	*P	1	0
Wake-up on pin change during Sleep mode	1	1	0

*P: Previous value before reset

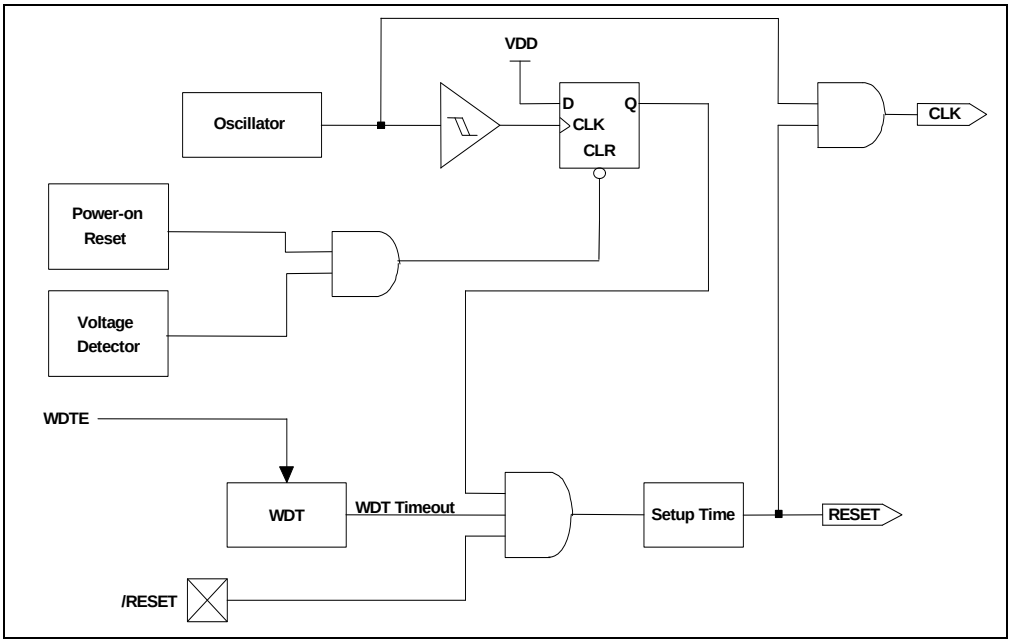


Figure 5-9 Controller Reset Block Diagram

5.6 Interrupt

The EM78P134N has five interrupts as listed below:

(1) TCC overflow interrupt

(2) Port 6 Input Status Change Interrupt

(3) External interrupt [(P60, /INT) pin]

(4) When TMR matches with PRD respectively in PWM

(5) When the comparators output changes

Before the Port 6 Input Status Changed Interrupt is enabled, reading Port 6 (e.g. "MOV R6, R6") is necessary. Each pin of Port 6 will have this feature if its status changes. Any pin configured as output or P60 pin configured as /INT, is excluded from this function. The Port 6 Input Status Changed Interrupt can wake up the EM78P134N from sleep mode if Port 6 is enabled prior to going into sleep mode by executing SLEP instruction. When the device wakes-up, the controller will continue to execute the program in-line if the global interrupt is disabled. If the global interrupt is enabled, it will branch to the interrupt Vector 006H.

RF is the interrupt status register that records the interrupt requests in the relative flags/bits. IOCF is an interrupt mask register. The global interrupt is enabled by the ENI instruction and is disabled by the DISI instruction. When one of the interrupts (enabled) occurs, the next instruction will be fetched from interrupt vector address. Once in the interrupt service routine, the source of an interrupt can be determined by polling the flag bits in RF. The interrupt flag bit must be cleared by instructions before leaving the interrupt service routine, prior to enabling interrupts to avoid recursive interrupts.

The flag (except ICIF bit) in the Interrupt Status Register (RF) is set regardless of the status of its mask bit or the execution of ENI. Note that the outcome of RF will be the logic AND of RF and IOCF (refer to Figure 5-9). The RETI instruction ends the interrupt routine and enables the global interrupt (execution of ENI).

When an interrupt is generated by the Timer clock / counter (if enabled), the next instruction will be fetched from Address 009H, and 00FH (TCC and Timer 1 respectively).

Before an interrupt subroutine is executed, the contents of ACC and the R3 and R4 registers will be saved by the hardware. If another interrupt occurs, ACC, R3, and R4 will be replaced by the new interrupt. After the interrupt service routine is completed, ACC, R3, and R4 registers are restored.

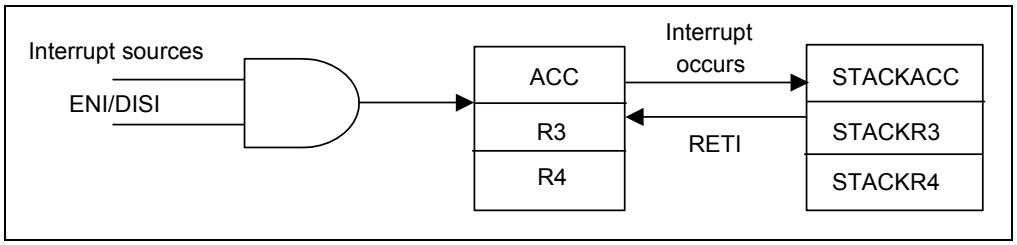


Figure 5-10 Interrupt Backup Diagram

In EM78P134N, each individual interrupt source has its own interrupt vector as depicted in the table below.

Interrupt Vector	Interrupt Status	Priority*
003H	External interrupt	1
006H	Port 6 pin change	2
009H	TCC overflow interrupt	3
00CH	Comparator interrupt	4
00FH	Timer 1 (PWM) overflow interrupt	5

*Priority **:** 1 = highest ; 5 = lowest priority

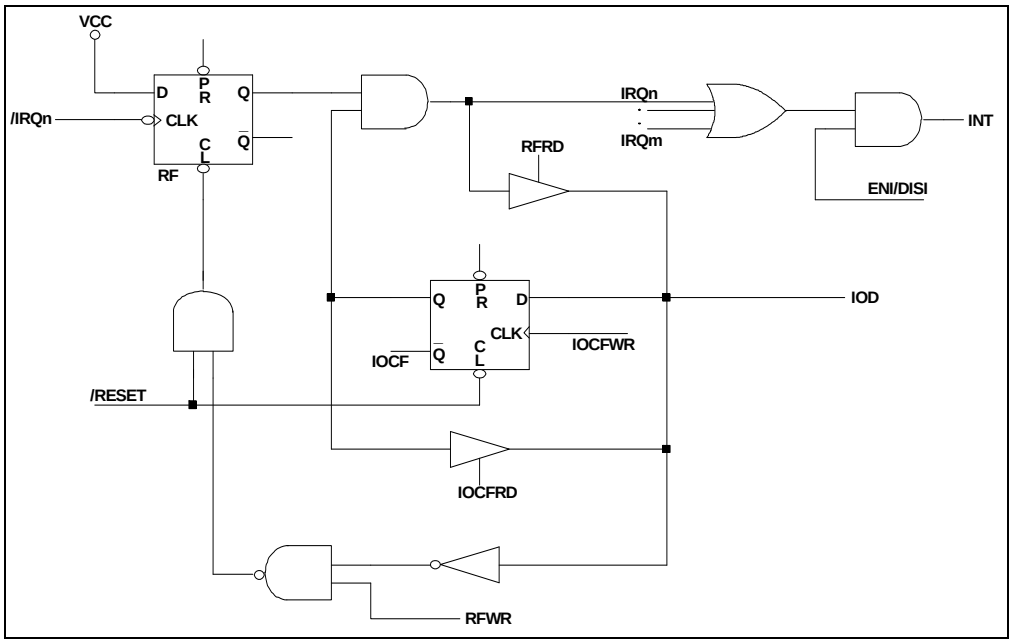


Figure 5-11 Interrupt input Circuit

5.7 PWM (Pulse Width Modulation)

5.7.1 Overview

In PWM mode, the PWM pins produce up to a 10-bit resolution PWM output (see the functional block diagram below). A PWM output consists of a time period and a duty cycle, and it keeps the output high. The baud rate of the PWM is the inverse of the time period. Figure 5-13 *PWM Output Timing* depicts the relationships between a time period and a duty cycle.

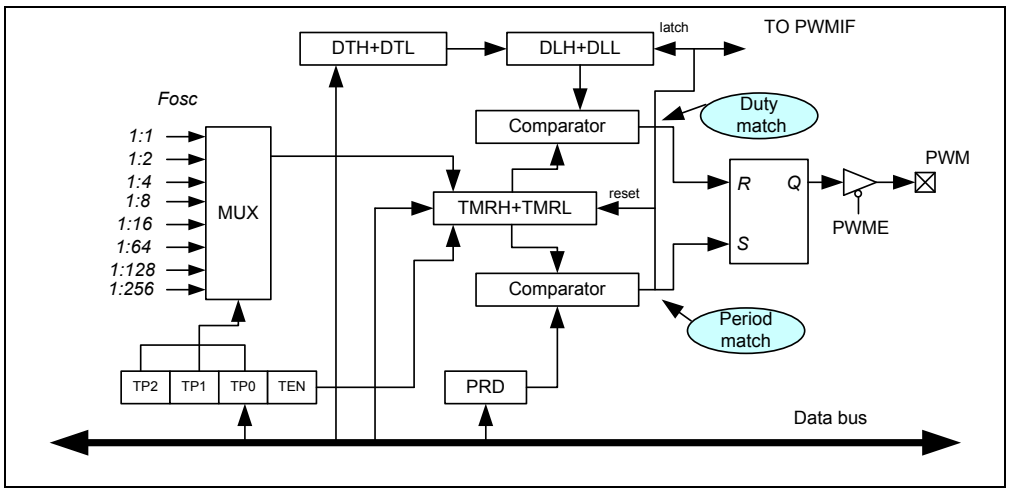


Figure 5-12 PWM Functional Block Diagram

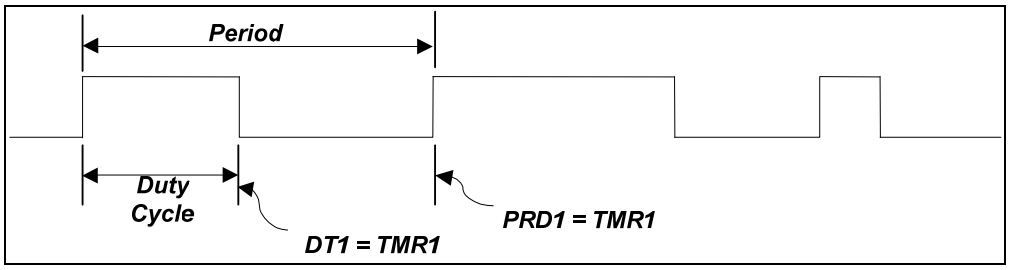


Figure 5-13 PWM Output Timing

5.7.2 Increment Timer Counter (TMRX: TMRH/TMRL)

TMRX are 10-bit clock counters with programmable prescalers. They are designed for the PWM module as baud rate clock generators. TMRX can be read only. If employed, they can be turned off for power saving by setting the T1EN Bit [RB<3>] to 0.

5.7.3 PWM Time Period (PRDX: TMRH/PRDL)

The PWM time period is defined by writing to the PRDL register. When TMRX is equal to PRDX, the following events occur on the next increment cycle**:**

- TMRX is cleared
- The PWMX pin is set to 1
- The PWM duty cycle is latched from DT to DTL

NOTE

The PWM output will not be set, if the duty cycle is 0

- The PWMIF pin is set to 1

The following formula describes how to calculate the PWM Time Period**:**

$$Period = (PRDX + 1) \times \left(\frac{1}{F_{OSC}}\right) \times (TMRX \ \ prescale\ value)$$

Example:

PRDX = 49; Fosc = 4 MHz; TMRX (0, 0, 0) = 1 : 1,

Then

$$Period = (49+1) \times \left(\frac{1}{4M}\right) \times = 12.5\,\mu s$$

5.7.4 PWM Duty Cycle (DTX: TMRH/DTL)

The PWM duty cycle is defined by writing to the DTX register, and is latched from DTX to DLX while TMRX is cleared. When DLX is equal to TMRX, the PWMX pin is cleared. DTX can be loaded anytime. However, it cannot be latched into DLX until the current value of DLX is equal to TMRX.

The following formula describes how to calculate the PWM duty cycle**:**

$$Duty\ cycle\ =\ (DTX)\ \times\ \left(\frac{1}{F_{OSC}}\right)\ \times\ (TMRX\ \ prescale\ value)$$

Example:

DTX = 10; **Fosc = 4 MHz;** **TMRX (0, 0, 0) = 1 : 1,**

Then

$$Duty\ cycle\ =\ (10)\ \times\ \left(\frac{1}{4M}\right)\ \times\ =\ 2.5\,\mu s$$

5.7.5 Comparator

Changing the output status while a match occurs will set the TMRIF flag at the same time.

5.7.6 PWM Programming Process/Steps

Load PRD with the PWM time period.

1. Load DT with the PWM Duty Cycle.
2. Enable interrupt function by writing IOCF0, if required.
3. Set PWMX pin to be output by writing a desired value to RB.
4. Load a desired value to IOC9 with TMR prescaler value and enable both PWM and TMR.

5.8 Timer

5.8.1 Overview

The Timer (TMRX) is a 10-bit clock counter with programmable prescalers. It is designed for the PWM module as baud rate clock generator. TMRX can be read only. The Timer will stop running when sleep mode occurs.

5.8.2 Function Description

The following figure shows the TMRX block diagram followed by descriptions of its signals and blocks**:**

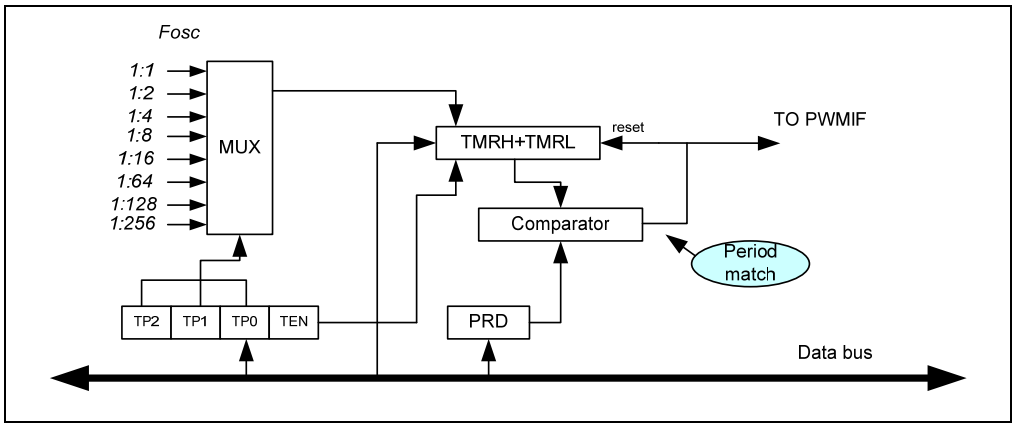


Figure 5-14 TMRX Block Diagram

Fosc: Input clock

Prescaler (TP2, TP1 and TP0): The Options 1:1, 1:2, 1:4, 1:8, 1:16, 1:64, 1:128, and 1:256 are defined by TMR. It is cleared when any type of reset occurs.

TMR (TMRH/TMRL): Timer register; TMR is increased until it matches with PRD, and then is reset to 1 (default valve).

PRD: PWM time period register.

Comparator: Reset TMR while a match occurs. The TMRIF flag is set at the same time.

5.8.3 Programming the Related Registers

When defining TMR, refer to the operation of its related registers as shown in the table below. It must be noted that the PWM bits must be disabled if their related TMR are employed. That is, Bit 4 of the PWMCON register must be set to '0'.

5.8.3.1 TMR Related Control Registers

Addr.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0B	PWMCON/RB	CPOUT	COS1	COS0	PWME	TEN	TP2	TP1	TP0

5.8.4 Timer Programming Process/Steps

1. Load PRD with the Timer duration
2. Enable interrupt function by writing IOCF0, if required
3. Load a desired TMR prescaler value to PWMCON, enable TMR and disable PWM

5.9 Comparator

The EM78P134N has one comparator comprising of five analog inputs and one output. The comparator can be utilized to wake up the EM78P134N from sleep mode. The comparator circuit diagram is depicted in the figure below.

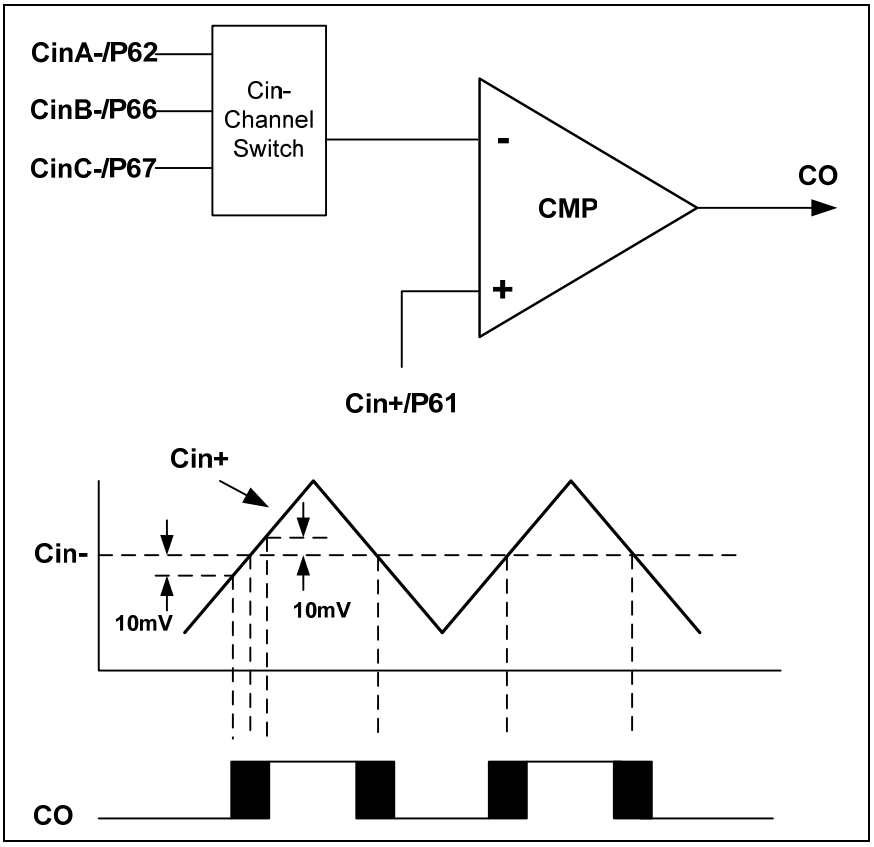


Figure 5-15 Comparator Circuit Diagram and Operating Mode

5.9.1 External Reference Signal

The analog signal that is presented at CinX– is compared to the signal at Cin+, and the digital output (CO) of the comparator is adjusted accordingly by taking the following notes into considerations:

NOTE

- *The reference signal must be between Vss and Vdd.*
- *The reference voltage can be applied to either pin of the comparator.*
- *Threshold detector applications may be of the same reference.*
- *The comparator can operate from the same or different reference sources.*

5.9.2 Comparator Outputs

- The compared result is stored in the CPOUT of RB.
- The comparator outputs are sent to CO (P60) by programming Bit 1, Bit 0<COS1, COS0> of the RB register to <1, X>. See Section 6.2.6, *RB* for Comparator select bits function description.

NOTE

- *The CO and PWM of the P60/INT/CO pins cannot be used at the same time.*
- *The P60/INT/CO pin priority is as follows:*

P60/INT/CO Priority		
High	Medium	Low
CO	INT	P60

The following figure shows the Comparator Output block diagram.

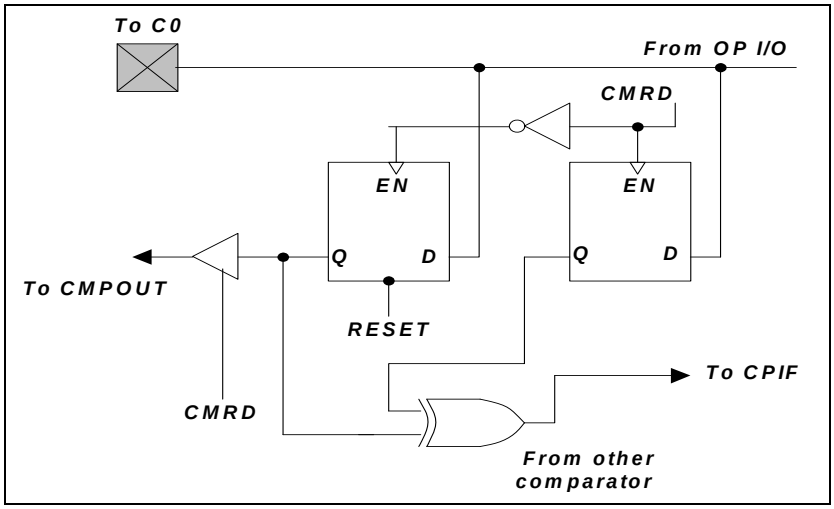


Figure 5-16 Comparator Output Configuration

5.9.3 Comparator Interrupt

- CMPIE (IOCF0.3) must be enabled for the “ENI” instruction to take effect.
- Interrupt is triggered whenever a change occurs on the comparator output pin.
- The actual change on the pin can be determined by reading the Bit CPOUT, RB<2>.
- CMPIF (RF.3), the comparator interrupt flag, can only be cleared by software.

5.9.4 Wake-up from Sleep Mode

- If enabled, the comparator remains active and the interrupt remains functional, even in Sleep mode.
- If a mismatch occurs, the interrupt will wake up the device from Sleep mode.
- Power consumption should be taken into consideration for the benefit of energy conservation.
- If the function is not implemented during Sleep mode, turn off the comparator before entering into sleep mode.

5.10 Oscillator

5.10.1 Oscillator Modes

The EM78P134N can be operated in four different oscillator modes, such as High Crystal oscillator mode (HXT), Low Crystal oscillator mode (LXT), External RC oscillator mode (ERC), and RC oscillator mode with Internal RC oscillator mode (IRC). One of the four modes can be selected by programming the OSC3, OSC2, OCS1, and OSC0 in the Code Option register.

The Oscillator modes defined by OSC3, OSC2, OCS1, and OSC0 are described below.

Oscillator Modes	OSC3	OSC2	OSC1	OSC0
ERC[1] (External RC oscillator mode); P64/OSCO funcions as P64	0	0	0	0
ERC[1] (External RC oscillator mode); P64/OSCO functions as OSCO	0	0	0	1
IRC[2] (Internal RC oscillator mode); P64/OSCO functions as P64	0	0	1	0
IRC[2] (Internal RC oscillator mode); P64/OSCO funtions as OSCO	0	0	1	1
LXT1 (Frequency range of LXT1 mode is 100kHz ~ 1 MHz)	0	1	0	0
HXT1 (Frequency range of HXT mode is 12 MHz ~ 20 MHz)	0	1	0	1
LXT2 (Frequency range of XT mode is 32kHz)	0	1	1	0
HXT2 (Frequency range of XT mode is 6 MHz ~ 12 MHz)	0	1	1	1
XT (Frequency range of XT mode is 1 MHz ~ 6 MHz) (default)	1	1	1	1

[1] In ERC mode, OSCI is used as oscillator pin. OSCO/P64 is defined by code option Word 0 Bit 9 ~ Bit 6.

[2] In IRC mode, P65 is normal I/O pin. OSCO/P64 is defined by code option Word 0 Bit 9 ~ Bit 6.

The maximum operating frequency limit of crystal/resonator at different VDDs, are as follows:

Conditions	VDD	Max. Freq. (MHz)
Two clocks	2.3	4
	4.5	16

5.10.2 Crystal Oscillator/Ceramic Resonators (Crystal)

The EM78P134N can be driven by an external clock signal through the OSCO pin as illustrated below.

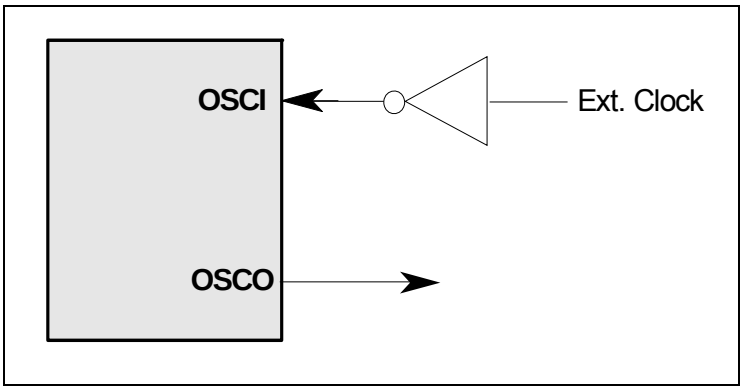


Figure 5-17 External Clock Input Circuit

In most applications, Pin OSCI and Pin OSCO can be connected with a crystal or ceramic resonator to generate oscillation. Figure 5-18 depicts such a circuit. The same applies to the HXT mode and the LXT mode.

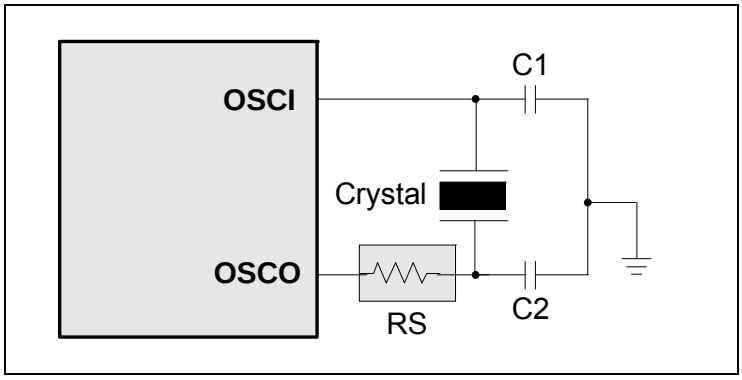


Figure 5-18 Crystal/Resonator Circuit

The following table provides the recommended values for C1 and C2. Since each resonator has its own attribute, refer to the resonator specifications for appropriate values of C1 and C2. RS, a serial resistor, may be required for AT strip cut crystal or low frequency mode.

Capacitor selection guide for crystal oscillator or ceramic resonators:

Oscillator Type	Frequency Mode	Frequency	C1 (pF)	C2 (pF)
Ceramic Resonators	HXT	455kHz	100~150	100~150
		2.0 MHz	20~40	20~40
		4.0 MHz	10~30	10~30
Crystal Oscillator	LXT	32.768kHz	25	15
		100kHz	25	25
		200kHz	25	25
	HXT	455kHz	20~40	20~150
		1.0 MHz	15~30	15~30
		2.0 MHz	15	15
		4.0 MHz	15	15

5.10.3 External RC Oscillator Mode

For some applications that do not require precise timing calculation, the RC oscillator (Figure 5-19) offers effective cost savings. Nevertheless, it should be noted that the frequency of the RC oscillator is influenced by the supply voltage, the values of the resistor (Rext), the capacitor (Cext), and even by the operation temperature. Moreover, the frequency also changes slightly from one chip to another due to manufacturing process variations.

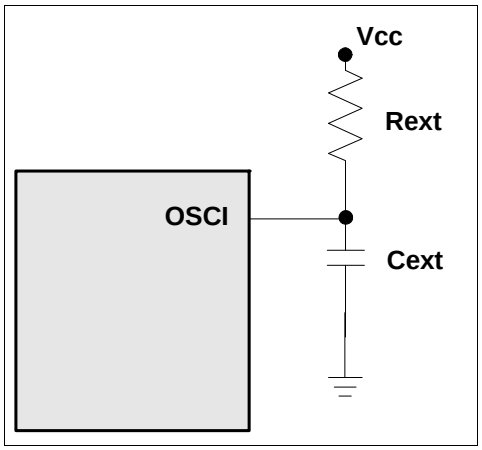


Figure 5-19 External RC Oscillator Mode Circuit

In order to maintain a stable system frequency, the values of the Cext should be no less than 20pF, and the value of Rext should not be greater than 1MΩ. If the frequency cannot be kept within this range, it can be affected easily by noise, humidity, and leakage.

The smaller the Rext in the RC oscillator is, the faster its frequency will be. On the contrary, for very low Rext values, for instance, 1 KΩ, the oscillator will become unstable because the NMOS cannot discharge the capacitance current correctly.

Based on the above reasons, it must be kept in mind that all the supply voltage, the operation temperature, the components of the RC oscillator, the package type, and the PCB layout, have certain effects on the system frequency.

The RC Oscillator frequencies:

Cext	Rext	Average Fosc 5V, 25°C	Average Fosc 3V, 25°C
20 Pf	3.3k	3.5 MHz	3.0 MHz
	5.1k	2.4 MHz	2.2 MHz
	10k	1.27 MHz	1.24 MHz
	100k	140kHz	143kHz
100 Pf	3.3k	1.21 MHz	1.18 MHz
	5.1k	805kHz	790kHz
	10k	420kHz	418kHz
	100k	45kHz	46kHz
300 Pf	3.3k	550kHz	526kHz
	5.1k	364kHz	350kHz
	10k	188kHz	185kHz
	100k	20kHz	20kHz

Note: [1]: Measured based on DIP packages.
[2]: The values are for design reference only.
[3]: The frequency drift is ± 30%

5.10.4 Internal RC Oscillator Mode

The EM78P134N offers a versatile internal RC mode with default frequency value of 4 MHz. Internal RC oscillator mode has other frequencies (16 MHz, 8 MHz, and 455kHz) that can be set by Code Option (Word 1), RCM1, and RCM0. The Table below describes the EM78P134N internal RC drift with voltage, temperature, and process variations.

Internal RC Drift Rate (Ta=25°C, VDD=5V ± 5%, VSS=0V)

Internal RC Frequency	Drift Rate			
	Temperature (-40°C ~+85°C)	Voltage (2.3V~5.5V)	Process	Total
16 MHz	± 6%	± 5%	± 3%	± 14%
8 MHz	± 5%	± 5%	± 3%	± 13%
4 MHz	± 5%	± 5%	± 3%	± 13%
455kHz	± 5%	± 5%	± 3%	± 13%

Note: These are theoretical values which are provided for reference only. Actual values may vary depending on the actual process.

Table 5-5 Calibration Selection for Internal RC Mode

C4	C3	C2	C1	C0	*Frequency (MHz)
0	0	0	0	0	(1-24.2%) × F
0	0	0	0	1	(1-23.1%) × F
0	0	0	1	0	(1-21.9%) × F
0	0	0	1	1	(1-20.6%) × F
0	0	1	0	0	(1-19.4%) × F
0	0	1	0	1	(1-18%) × F
0	0	1	1	0	(1-16.7%) × F
0	0	1	1	1	(1-15.3%) × F
0	1	0	0	0	(1-13.8%) × F
0	1	0	0	1	(1-12.3%) × F
0	1	0	1	0	(1-10.7%) × F
0	1	0	1	1	(1-9.1%) × F
0	1	1	0	0	(1-7.4%) × F
0	1	1	0	1	(1-5.7%) × F
0	1	1	1	0	(1-3.8%) × F
0	1	1	1	1	(1-2%) × F
1	1	1	1	1	F (default)
1	1	1	1	0	(1+2%) × F
1	1	1	0	1	(1+4.2%) × F
1	1	1	0	0	(1+6.4%) × F
1	1	0	1	1	(1+8.7%) × F
1	1	0	1	0	(1+11.1%) × F
1	1	0	0	1	(1+13.6%) × F
1	1	0	0	0	(1+16.3%) × F
1	0	1	1	1	(1+19%) × F
1	0	1	1	0	(1+22%) × F
1	0	1	0	1	(1+25%) × F
1	0	1	0	0	(1+28.2%) × F
1	0	0	1	1	(1+31.6%) × F
1	0	0	1	0	(1+35.1%) × F
1	0	0	0	1	(1+38.9%) × F
1	0	0	0	0	(1+42.9%) × F

* These are theoretical values which are provided for reference only. Actual values may vary depending on the actual process.

5.11 Power-on Considerations

Any microcontroller is not warranted to start operating properly before the power supply has stabilized to a steady state. The EM78P134N has a built-in Power-on Reset (POR) with reset level range of 1.7V to 1.9V. The circuitry eliminates the extra external reset circuit. It will work well if Vdd rises quickly enough (50ms or less). However, under critical applications, extra devices are still required to assist in solving power-on problems.

5.11.1 External Power-on Reset Circuit

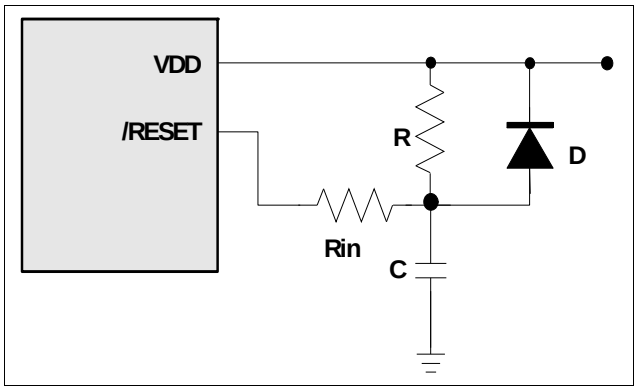


Figure 5-20 External Power-on Reset Circuit

The circuits shown in the figure implement an external RC to produce a reset pulse. The pulse width (time constant) should be kept long enough to allow Vdd to reach the minimum operating voltage. This circuit is used when the power supply has a slow power rise time. Because the current leakage from the /RESET pin is ± 5 μA, it is recommended that R should not be greater than 40K. This way, the voltage at Pin /RESET is held below 0.2V. The diode (D) functions as a short circuit at power-down. The "C" capacitor is discharged rapidly and fully. Rin, the current-limited resistor, prevents high current discharge or ESD (electrostatic discharge) from flowing into Pin /RESET.

5.11.2 Residual Voltage Protection

When the battery is replaced, device power (Vdd) is removed but residual voltage remains. The residual voltage may trip below Vdd minimum, but not to zero. This condition may cause a poor power-on reset. Figure 5-21 and Figure 5-22 show how to create a protection circuit against residual voltage.

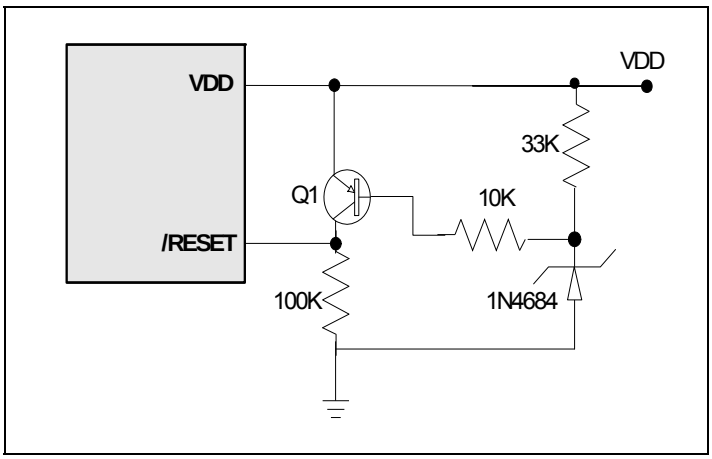


Figure 5-21 Residual Voltage Protection Circuit 1

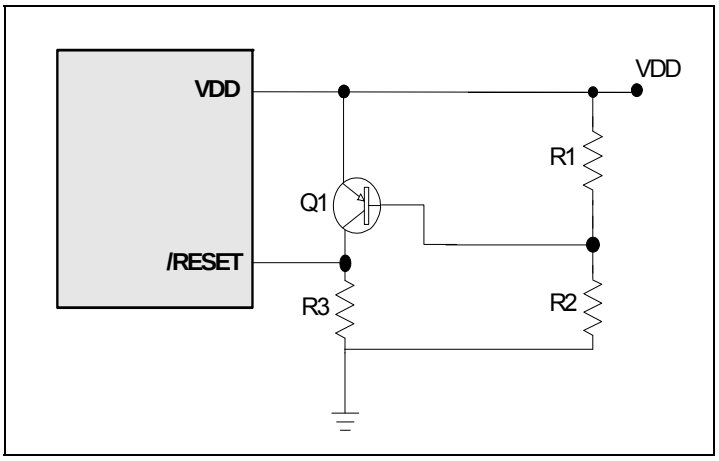


Figure 5-22 Residual Voltage Protection Circuit 2

5.12 Code Option Register

The EM78P134N has Code Option words that are not part of the normal program memory. The option bits cannot be accessed during normal program execution.

Code Option Register and Customer ID Register arrangement distribution:

Word 0	Word 1	Word 2
Bit 12~Bit 0	Bit 12~Bit 0	Bit 12~Bit 0

5.12.1 Code Option Register (Word 0)

Word 0													
Bit	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mnemonic	0	CLKS	TYPE1	TYPE0	LVR1	LVR0	RESETDG	ENWDT	NRHL	NRE	PR2	PR1	PR0
1	-	4CLKS	High	High	High	High	Disable	Disable	32/fc	Disable	Disable		
0	-	2LCKS	Low	Low	Low	Low	Enable	Enable	8/fc	Enable	Enable		

Bit 12: unused bit, set to 0 all the time.

Bit 11 (CLKS): Instruction period selection bit

0: Two oscillator periods

1: Four oscillator periods

Refer to the Instruction Set section.

Bits 10 ~ 9 (TYPE1 ~ TYPE0): these bits must always be set to 0 for EM78P134N

Bits 8 ~ 7 (LVR1 ~ LVR0): Low Voltage Reset enable bits

LVR1, LVR0	VDD Reset Level	VDD Release Level
11	NA (Power-on Reset)	
10	2.4V	2.6V
01	3.3V	3.5V
00	4.0V	4.2V

Bit 6 (RESETDG): Reset pin delete glitch function

0: Enable

1: Disable

Bit 5 (ENWDT): Watchdog timer enable bit.

0: Enable Watchdog timer

1: Disable Watchdog timer

NOTE

This bit must enable the WDTE register (IOCE register). Bit 7 must be disabled when Port 6 pin change wake-up function is used.

Bit 4 (NRHL): Noise rejection high/low pulse defined bit

0: Pulses equal to 8/fc [s] are regarded as signal

1: Pulses equal to 32/fc [s] are regarded as signal

Bit 3 (NRE): Noise rejection enable bit

0: disable noise rejection

1: enable noise rejection

Bits 2 ~ 0 (PR2 ~ PR0): Protect Bits

5.12.2 Code Option Register (Word 1)

Word 1													
Bit	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mnemonic	HLP	C4	C3	C2	C1	C0	RCM1	RCM0	OSC3	OSC2	OSC1	OSC0	RCOUT
1	Low	High	High	High	High	High	High	High	High	High	High	High	System clock
0	High	Low	Low	Low	Low	Low	Low	Low	Low	Low	Low	Low	Open drain

Bit 12 (HLP): high/low power mode

0: Low power mode

1: High power mode (default)

Bits 11 ~ 7 (C4 ~ C0): Calibrator of internal RC mode. These bits must always be set to "1" only (auto calibration)

Bits 6 ~ 5 (RCM1 ~ RCM0): RC mode selection bits

RCM 1	RCM 0	Frequency (MHz)
1	1	4
1	0	16
0	1	8
0	0	455kHz

Bits 4 ~ 1(OSC3 ~ OSC0): Oscillator mode selection bits

Oscillator Modes	OSC3	OSC2	OSC1	OSC0
ERC[1] (External RC oscillator mode); P64/OSCO funcions as P64	0	0	0	0
ERC[1] (External RC oscillator mode); P64/OSCO functions as OSCO	0	0	0	1
IRC[2] (Internal RC oscillator mode); P64/OSCO functions as P64	0	0	1	0
IRC[2] (Internal RC oscillator mode); P64/OSCO funtions as OSCO	0	0	1	1
LXT1 (Frequency range of LXT1 mode is 100kHz ~ 1 MHz)	0	1	0	0
HXT1 (Frequency range of HXT mode is 12 MHz ~ 20 MHz)	0	1	0	1
LXT2 (Frequency range of XT mode is 32kHz)	0	1	1	0
HXT2 (Frequency range of XT mode is 6 MHz ~ 12 MHz)	0	1	1	1
XT (Frequency range of XT mode is 1 MHz ~ 6 MHz) (default)	1	1	1	1

Bit 0 (RCOUT): Selection bit of Oscillator output or I/O port.

RCOUT	Pin Function
0	OSCO pin is open drain
1	OSCO output system clock (default)

5.12.3 Customer ID Register (Word 2)

Word 2													
Bit	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mnemonic	1	1	CMP_DE	1	RESETEN	EFT_SEL	SUT0	1	1	1	1	1	1
1	-	-	High	-	P63	Long	18ms	-	-	-	-	-	-
0	-	-	Low	-	/RST	Short	4.5ms	-	-	-	-	-	-

Bit 12 (Unused): unused bit, set to 1 all the time

Bit 11 (Unused): unused bit, set to 1 all the time

Bit 10 (CMP_DE): comparator de-glitch enable bit

0: disable

1: enable

Bit 9 (Unused): unused bit, set to 1 all the time

Bit 8 (RESETEN): P63//RST pin select bit

0: P63//RST set to /RST pin

1: P63//RST set to P63 pin

Bit 7 (EFT_SEL): EFT hold time selection

0: short hold time 8 μs × 16

1: long hold time 8 μs × 64

Bit 6 (SUT0): set up time select bit

0: 4.5 ms

1: 18 ms

Bit 5~Bit 0: unused bit, set to 1 all the time

5.13 Instruction Set

Each instruction in the instruction set is a 13-bit word divided into an OP code and one or more operands. Normally, all instructions are executed within one single instruction cycle (one instruction consists of 2 oscillator periods), unless the program counter is changed by instruction "MOV R2,A", "ADD R2,A", or by instructions of arithmetic or logic operation on R2 (e.g. "SUB R2,A", "BS(C) R2,6", "CLR R2", etc.). In this case, the execution takes two instruction cycles.

If for some reasons, the specification of the instruction cycle is not suitable for certain applications, try modifying the instruction as follows:

(A) Modify one instruction cycle to consist of 4 oscillator periods.

(B) Execute within two instruction cycles the "JMP", "CALL", "RET", "RETL", "RETI" commands, or the conditional skip ("JBS", "JBC", "JZ", "JZA", "DJZ", "DJZA") which were tested to be true. The instructions that are written to the program counter, should also take two instruction cycles.

Case (A) is selected by the Code Option bit, called CLKS. One instruction cycle will consist of two oscillator clocks if CLKS is Low, and four oscillator clocks if CLKS is high.

Note that once the 4 oscillator periods within one instruction cycle is selected under Case (A), the internal clock source to TCC should be CLK=Fosc/4 , instead of Fosc/2 as illustrated in Figure 5-3.

In addition, the instruction set has the following features:

(1) Every bit of any register can be set, cleared, or tested directly.

(2) The I/O register can be regarded as general register. That is, the same instruction can operate on the I/O register.

Convention:

R = Register designator that specifies which one of the registers (including operation and general purpose registers) is to be utilized by the instruction.

b = Bit field designator that selects the value for the bit located in the register R and which affects the operation.

k = 8 or 10-bit constant or literal value

Binary Instruction	Hex	Mnemonic	Operation	Status Affected
0 0000 0000 0000	0000	NOP	No Operation	None
0 0000 0000 0001	0001	DAA	Decimal Adjust A	C
0 0000 0000 0010	0002	CONTW	A → CONT	None
0 0000 0000 0011	0003	SLEP	0 → WDT, Stop oscillator	T, P
0 0000 0000 0100	0004	WDTC	0 → WDT	T, P
0 0000 0000 rrrr	000r	IOW R	A → IOCR	None[1]
0 0000 0001 0000	0010	ENI	Enable Interrupt	None
0 0000 0001 0001	0011	DISI	Disable Interrupt	None
0 0000 0001 0010	0012	RET	[Top of Stack] → PC	None
0 0000 0001 0011	0013	RETI	[Top of Stack] → PC, Enable Interrupt	None
0 0000 0001 0100	0014	CONTR	CONT → A	None

Binary Instruction	Hex	Mnemonic	Operation	Status Affected
0 0000 0001 rrrr	001r	IOR R	IOCR → A	None[1]
0 0000 01rr rrrr	00rr	MOV R,A	A → R	None
0 0000 1000 0000	0080	CLRA	0 → A	Z
0 0000 11rr rrrr	00rr	CLR R	0 → R	Z
0 0001 00rr rrrr	01rr	SUB A,R	R-A → A	Z, C, DC
0 0001 01rr rrrr	01rr	SUB R,A	R-A → R	Z, C, DC
0 0001 10rr rrrr	01rr	DECA R	R-1 → A	Z
0 0001 11rr rrrr	01rr	DEC R	R-1 → R	Z
0 0010 00rr rrrr	02rr	OR A,R	A ∨ VR → A	Z
0 0010 01rr rrrr	02rr	OR R,A	A ∨ VR → R	Z
0 0010 10rr rrrr	02rr	AND A,R	A & R → A	Z
0 0010 11rr rrrr	02rr	AND R,A	A & R → R	Z
0 0011 00rr rrrr	03rr	XOR A,R	A ⊕ R → A	Z
0 0011 01rr rrrr	03rr	XOR R,A	A ⊕ R → R	Z
0 0011 10rr rrrr	03rr	ADD A,R	A + R → A	Z, C, DC
0 0011 11rr rrrr	03rr	ADD R,A	A + R → R	Z, C, DC
0 0100 00rr rrrr	04rr	MOV A,R	R → A	Z
0 0100 01rr rrrr	04rr	MOV R,R	R → R	Z
0 0100 10rr rrrr	04rr	COMA R	/R → A	Z
0 0100 11rr rrrr	04rr	COM R	/R → R	Z
0 0101 00rr rrrr	05rr	INCA R	R+1 → A	Z
0 0101 01rr rrrr	05rr	INC R	R+1 → R	Z
0 0101 10rr rrrr	05rr	DJZA R	R-1 → A, skip if zero	None
0 0101 11rr rrrr	05rr	DJZ R	R-1 → R, skip if zero	None

Binary Instruction	Hex	Mnemonic	Operation	Status Affected
0 0110 00rr rrrr	06rr	RRCA R	R(n) → A(n-1),R(0) → C, C → A(7)	C
0 0110 01rr rrrr	06rr	RRC R	R(n) → R(n-1),R(0) → C, C → R(7)	C
0 0110 10rr rrrr	06rr	RLCA R	R(n) → A (n+1),R(7) → C, C → A(0)	C
0 0110 11rr rrrr	06rr	RLC R	R(n) → R (n+1), R(7) → C, C → R(0)	C
0 0111 00rr rrrr	07rr	SWAPA R	R(0-3) → A (4-7), R(4-7) → A(0-3)	None
0 0111 01rr rrrr	07rr	SWAP R	R(0-3) ↔ R(4-7)	None
0 0111 10rr rrrr	07rr	JZA R	R+1 → A, skip if zero	None
0 0111 11rr rrrr	07rr	JZ R	R+1 → R, skip if zero	None
0 100b bbrr rrrr	0xxx	BC R,b	0 → R(b)	None[2]
0 101b bbrr rrrr	0xxx	BS R,b	1 → R(b)	None[3]
0 110b bbrr rrrr	0xxx	JBC R,b	if R(b)=0, skip	None
0 111b bbrr rrrr	0xxx	JBS R,b	if R(b)=1, skip	None
1 00kk kkkk kkkk	1kkk	CALL k	PC+1 → [SP], (Page, k) → PC	None
1 01kk kkkk kkkk	1kkk	JMP k	(Page, k) → PC	None
1 1000 kkkk kkkk	18kk	MOV A,k	k → A	None
1 1001 kkkk kkkk	19kk	OR A,k	A ∨ k → A	Z
1 1010 kkkk kkkk	1Akk	AND A,k	A & k → A	Z
1 1011 kkkk kkkk	1Bkk	XOR A,k	A ⊕ k → A	Z
1 1100 kkkk kkkk	1Ckk	RETL k	k → A, [Top of Stack] → PC	None
1 1101 kkkk kkkk	1Dkk	SUB A,k	k-A → A	Z, C, DC
1 1110 0000 0001	1E01	INT	PC+1 → [SP],001H → PC	None
1 1111 kkkk kkkk	1Fkk	ADD A,k	k+A → A	Z, C, DC
1 1110 11rr rrrr	1Err	TBRD R	If R8 Bit7=0, Machine code (7:0) → R Else machine code (12:8) → R	None

Note: [1] This instruction is applicable to IOC5~IOCF only.

[2] This instruction is not recommended for RF operation.

[3] This instruction cannot operate under RF.

6 Absolute Maximum Ratings

Items	Rating		
Temperature under bias	-40°C	to	85°C
Storage temperature	-65°C	to	150°C
Input voltage	-0.3V	to	+6.0V
Output voltage	-0.3V	to	+6.0V
Working Voltage	2.5V	to	5.5V
Working Frequency	DC	to	20 MHz

7 Electrical Characteristics

7.1 DC Electrical Characteristics

Ta= 25°C, VDD= 5.0V ± 5%, VSS= 0V

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Fxt	Crystal: VDD to 2.3V	Two cycles with two clocks	DC	–	4.0	MHz
Fxt	Crystal: VDD to 3V	Two cycles with two clocks	DC	–	8.0	MHz
Fxt	Crystal: VDD to 5V	Two cycles with two clocks	DC	–	20.0	MHz
ERC	RC: VDD to 5V	R: 5KΩ, C: 39 pF	F-30%	1500	F+30%	kHz
IIL	Input Leakage Current for input pins	VIN = VDD, VSS	–	–	±1	μA
VIH1	Input High Voltage (Schmitt Trigger)	Ports 5, 6	0.7Vdd	–	Vdd+0.3V	V
VIL1	Input Low Voltage (Schmitt Trigger)	Ports 5, 6	-0.3V	–	0.3Vdd	V
VIHT1	Input High Threshold Voltage (VDD=5.0V)	/RESET, TCC (Schmitt trigger)	0.7Vdd	–	Vdd+0.3V	V
VILT1	Input Low Threshold Voltage (VDD=5.0V)	/RESET, TCC (Schmitt trigger)	-0.3V	–	0.3Vdd	V
VIHX1	Clock Input High Voltage (VDD=5.0V)	OSCI	2.9	3.0	3.1	V
VILX1	Clock Input Low Voltage (VDD=5.0V)	OSCI	1.7	1.8	1.9	V
VIHT2	Input High Threshold Voltage (VDD=3.0V)	/RESET, TCC (Schmitt trigger)	0.7Vdd	–	Vdd+0.3V	V
VILT2	Input Low Threshold Voltage (VDD=3.0V)	/RESET, TCC (Schmitt trigger)	-0.3V	–	0.3Vdd	V
IOH1	Output High Voltage (Ports 5, 6)	VOH = 0.9VDD	–	-9	–	mA
IOL1	Output Low Voltage (Ports 5, 6)	VOL = 0.1VDD	–	24	–	mA
IPH	Pull-high current	Pull-high active, input pin at VSS	-70	-75	-80	μA
IPL	Pull-low current	Pull-low active, input pin at Vdd	35	40	45	μA

Symbol	Parameter	Condition	Min	Typ	Max	Unit
ISB1	Power down current	All input and I/O pins at VDD, Output pin floating, WDT disabled	0.6	2.0	2.5	μA
ISB2	Power down current	All input and I/O pins at VDD, Output pin floating, WDT enabled	6	7	8	μA
ICC1	Operating supply current at two clocks	/RESET= 'High', Fosc=32kHz (Crystal type, CLKS="0") Output pin floating, WDT enabled	25	27	29	μA
ICC2	Operating supply current at two clocks	/RESET= 'High', Fosc=4MHz (IRC type, CLKS="0"), Output pin floating, WDT enabled	1.2	1.4	1.6	mA
ICC3	Operating supply current at two clocks	/RESET= 'High', Fosc = 4 MHz (Crystal type, CLKS="0"), Output pin floating, WDT enabled	2.4	2.6	3	mA
ICC4	Operating supply current at two clocks	/RESET= 'High', Fosc = 10 MHz (Crystal type, CLKS="0"), Output pin floating, WDT enabled	2.4	2.6	3	mA

Internal RC Electrical Characteristics (Ta = 25°C, VDD = 5 V, VSS = 0V)

Internal RC	Drift Rate				
	Temperature	Voltage	Min.	Typ.	Max.
4 MHz	25°C	5V	3.88 MHz	4 MHz	4.12 MHz
8 MHz	25°C	5V	7.76 MHz	8 MHz	8.24 MHz
16 MHz	25°C	5V	15.52 MHz	16 MHz	16.48 MHz
455kHz	25°C	5V	441.3kHz	455kHz	468.7kHz

Internal RC Electrical Characteristics (Ta = -40 ~85°C, VDD = 2.2~5.5 V, VSS = 0V)

Internal RC	Drift Rate				
	Temperature	Voltage	Min.	Typ.	Max.
4 MHz	-40 ~85°C	2.2V~5.5V	3.48 MHz	4 MHz	4.52 MHz
8 MHz	-40 ~85°C	2.2V~5.5V	6.96 MHz	8 MHz	9.04 MHz
16 MHz	-40 ~85°C	2.2V~5.5V	13.92 MHz	16 MHz	18.08 MHz
455kHz	-40 ~85°C	2.2V~5.5V	395.85kHz	455kHz	514.15kHz

LVR (Low Voltage Reset) Electrical Characteristics

Symbol	Parameter	Condition	Min.*	Typ.	Max.**	Unit
LVR1	LVR1 Voltage reset level (Schmitt trigger)	Vdd=5V	–	–	–	V
LVR2	LVR2 Voltage reset level (Schmitt trigger)	Vdd=5V	2.4 ± 0.2	–	2.6 ± 0.2	V
LVR3	LVR3 Voltage reset level (Schmitt trigger)	Vdd=5V	3.3 ± 0.2	–	3.5 ± 0.2	V
LVR4	LVR4 Voltage reset level (Schmitt trigger)	Vdd=5V	4.0 ± 0.2	–	4.2 ± 0.2	V

Note: * VDD Voltage from High to Low.

** VDD Voltage from Low to High.

7.2 Comparator Characteristics

Vdd = 5.0V, Vss=0V, Ta = -40 to 85°C

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
SR	Slew rate	–	0.1	0.2	–	V/μs
Vos	Input offset voltage	RL=5.1K, (Note 1)	1	10	15	mV
IVR	Input voltage range	Vdd =5.0V, V_{SS} = 0.0V	0.5	–	4.5	V
OVS	Output voltage swing	Vd =5.0V, V_{SS} = 0.0V, RL=10KΩ	0	0.2	0.3	V
			4.7	4.8	5	
Ico	Supply current of Comparator	–	–	300	–	μA
Vs	Operating range	–	2.5	–	5.5	V

Note: 1. These parameters are hypothetical (not tested), provided here for design reference only.

2. These parameters are subject to change without prior notice.

7.3 AC Electrical Characteristics

Ta=-40°C ~ 85°C, VDD=5V ± 5%, VSS=0V

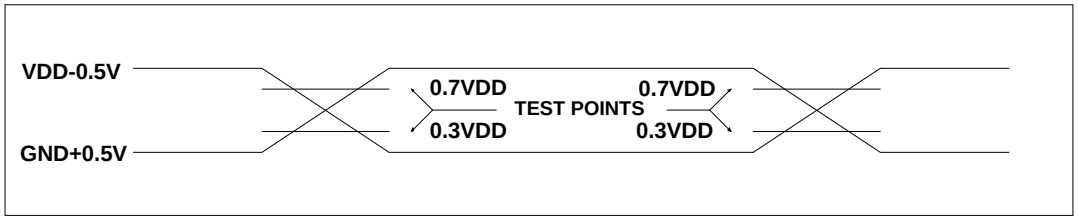
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Dclk	Input CLK duty cycle	–	45	50	55	%
Tins	Instruction cycle time (CLKS="0")	Crystal type	100	–	DC	ns
		RC type	500	–	DC	ns
Ttcc	TCC input period	–	(Tins+20)/N*	–	–	ns
Tdrh	Device reset hold time	Ta = 25°C TXAL, SUT0=1	17.6-30%	17.6	17.6+30%	ms
Trst	/RESET pulse width	Ta = 25°C	2000	–	–	ns
Twdt1*	Watchdog timer period	Ta = 25°C SUT0=1	17.6-30%	17.6	17.6+30%	ms
Twdt2*	Watchdog timer period	Ta = 25°C SUT0=0	4.5-30%	4.5	4.5+30%	ms
Tset	Input pin setup time	–	–	0	–	ns
Thold	Input pin hold time	–	–	20	–	ns
Tdelay	Output pin delay time	Cload=20pF	–	50	–	ns

Note: 1. N = selected prescaler ratio

2. Twdt1**:** The Option Word 1 SUT0 is used to define the oscillator set-up time. In Crystal mode, the WDT timeout length is the same as the set-up time (18ms).
3. Twdt2: The Option Word 1 SUT0 is used to define the oscillator set-up time. In Crystal mode, the WDT timeout length is the same as set-up time (4.5ms).
4. These parameters are hypothetical (not tested) and are provided for design reference only.
5. Data under Minimum, Typical, and Maximum (Min., Typ., and Max.) columns are based on hypothetical results at 25°C. These data are for design reference use only.
6. The Watchdog timer duration is determined by Code Option Word 1 (Bit 6, Bit 5).

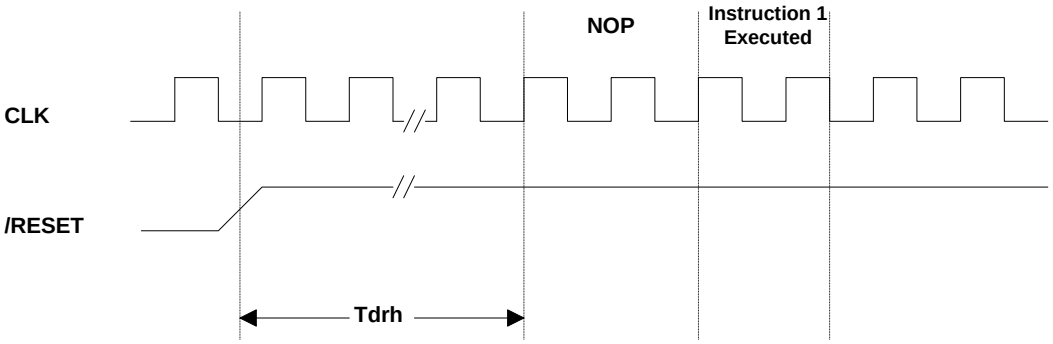
8 Timing Diagram

AC Test Input/Output Waveform



AC Testing: Input is driven at VDD-0.5V for logic "1" and GND+0.5V for logic "0". Timing measurements are made at 0.7VDD for logic "1" and 0.3VDD for logic "0"

RESET Timing (CLK="0")



TCC Input Timing (CLKS="0")