EM78P141

8-Bit Microprocessor with OTP ROM

Product Specification

DOC. VERSION 1.1

ELAN MICROELECTRONICS CORP.
December 2009

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APPENDIX

Specification Revision History

Doc. Version	Revision Description	Date
0.9	Preliminary version	2008/10/25
1.0	Initial released version	2009/03/12
1.1	1. Added EM78P141MS10J/S package type. 2. Modified Section 6.5.1.3 *Register Initial Values After Reset.* 3. Delete IOCB0 and IOCC0 registers. 4. Modified Absolute Maximum Ratings.	2009/12/16

1 General Description

The EM78P141 is an 8-bit microprocessor designed and developed with low-power and high-speed CMOS technology. It is equipped has an on-chip 1K×13-bit Electrical One Time Programmable Read Only Memory (OTP-ROM). It provides a protection bit to prevent intrusion of user's code. Three Code option words are also available to meet user's requirements.

With its enhanced OTP-ROM feature, the EM78P141 provides a convenient way of developing and verifying user's programs. Moreover, this MCU offers the advantages of easy and effective program updates with the use of ELAN development and programming tools. You can also avail yourself with ELAN Writer to easily program your development code.

2 Features

- CPU configuration
  - 1K×13 bits on-chip ROM
  - 48×8 bits on-chip registers (SRAM)
  - 8-level stacks for subroutine nesting
  - 4 programmable level voltage detector (LVD): 4.5V, 4.0V, 3.3V, 2.2V
  - 3 programmable level voltage reset (LVR): 4.0V, 3.5V, 2.7V
  - Less than 1.5 mA at 5V/4MHz
  - Typically 15 µA, at 3V/32kHz
  - Typically 2 µA, during Sleep mode
- I/O port configuration
  - 1 bidirectional I/O ports
  - Wake-up port: P5
  - 7 Programmable pull-down I/O pins
  - 7 programmable pull-high I/O pins
  - 7 programmable open-drain I/O pins
  - External interrupt: P52
- Operating voltage range
  - Operating voltage: 2.1V~5.5V (Commercial)
  - Operating temperature: 0°C ~70°C (Commercial)
- Operating frequency range
  - Crystal mode:
    DC~16MHz/2clks @4.5V
    DC~8MHz/2clks @ 3V
    DC~4MHz/2clks @ 2.1V
  - ERC mode:
    DC~16 MHz/2clks @ 4.5V
    DC~12 MHz/2clks @ 4V
    DC~4 MHz/2clks @ 2.1V
  - IRC mode:
    Oscillation mode: 4 MHz, 8 MHz, 16 MHz, & 455kHz

Internal RC Frequency	Drift Rate			
	Temperature (0℃ ~70℃)	Voltage (2.3V~5.5V)	Process	Total
4 MHz	± 3%	± 5%	± 3%	± 11%
8 MHz	± 3%	± 5%	± 3%	± 11%
16 MHz	± 3%	± 5%	± 3%	± 11%
455kHz	± 3%	± 5%	± 3%	± 11%

All the four main frequencies can be trimmed by programming with four calibrated bits in the ICE143 Simulator. OTP is auto trimmed by ELAN Writer.

- Peripheral configuration
  - 8-bit real time clock/counter (TCC) with selective signal sources, trigger edges, and overflow interrupt
  - 7-channel Analog-to-Digital Converter with 10-bit resolution in Vref mode
  - Two Pulse Width Modulation (PWM) with 8-bit resolution, each provides 8-bit real time clock/counter function and supports 16-bit cascaded mode from these two independent ones
  - One pair of comparators (Offset voltage: 5mV, max offset voltage: 10mV)
  - Power-down (Sleep) mode
  - High EFT immunity
- Seven available interrupts:
  - TCC overflow interrupt
  - Input-port status changed interrupt (wake-up from Sleep mode)
  - External interrupt
  - ADC completion interrupt
  - PWM period match completion
  - Comparators status change interrupt
  - Low voltage detector interrupt
- Programmable free running Watchdog Timer
  - Two clocks per instruction cycle
  - Watchdog timer 16.5ms ± 30% in Vdd = 5V at 25°C (WDTPS=1 in Option pin)
  - Watchdog timer 18ms ± 30% in Vdd = 3V at 25°C (WDTPS=1 in Option pin)
  - Watchdog timer 4.2ms ± 30% in Vdd = 5V at 25°C (WDTPS=0 in Option pin)
  - Watchdog timer 4.5ms ± 30% in Vdd = 3V at 25°C (WDTPS=0 in Option pin)
- Package type:
  - 10-pin MSOP 118 mil: EM78P141MS10J/S

NOTE

These are Green products which do NOT contain hazardous substances.

3 Pin Assignment

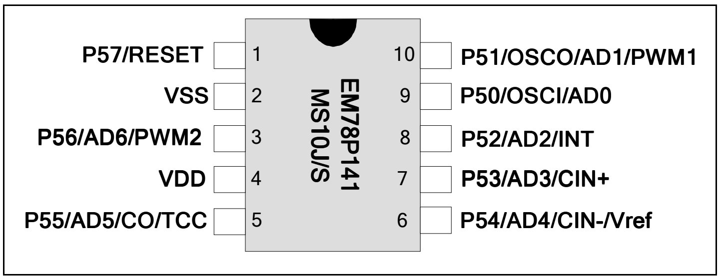


Figure 3-1 EM78P141MS10J/S Pin Assignment

4 Pin Description

4.1 EM78P141MS10J/S Pin Description

Symbol	Pin No.	Type	Function
P50~P57	5,3,1,10 7,9,8,6	I/O	Bidirectional 8-bit input/output pins P50~P56 can be used as pull-high, pull-down, and as open-drain by software programming.
OSCI / ERCin	9	I	External clock crystal resonator oscillator input pin External RC oscillator clock input pin
OSCO/RCOUT	10	O	Clock output from crystal oscillator Clock output from internal RC oscillator
TCC	5	I	Real time clock/counter, Schmitt trigger input pin. Must be tied to VDD or VSS if not in use.
/RESET	1	I	Schmitt trigger input pin. If this pin remains at logic low, the controller is reset.
CIN-, CIN+CO	6, 7, 5	I/O	P54 can act as CIN- of a comparator P53 can act as CIN+ of a comparator P55 can act as CO of a comparator
VREF	6	I	P54 can be used as external reference for ADC.
ADC0~ADC6	9,10,8,7 6,5,3	I/O	P50~P56 can be used as 7-channel 10-bit resolution A/D converter
/INT	8	I	P52 can be used as external interrupt pin triggered by a falling edge.
PWM1/PWM2	10, 3	O	P51 & P56 can be used as Pulse Width Modulation output
VDD	4	–	Power supply
VSS	2	–	Ground

5 Block Diagram

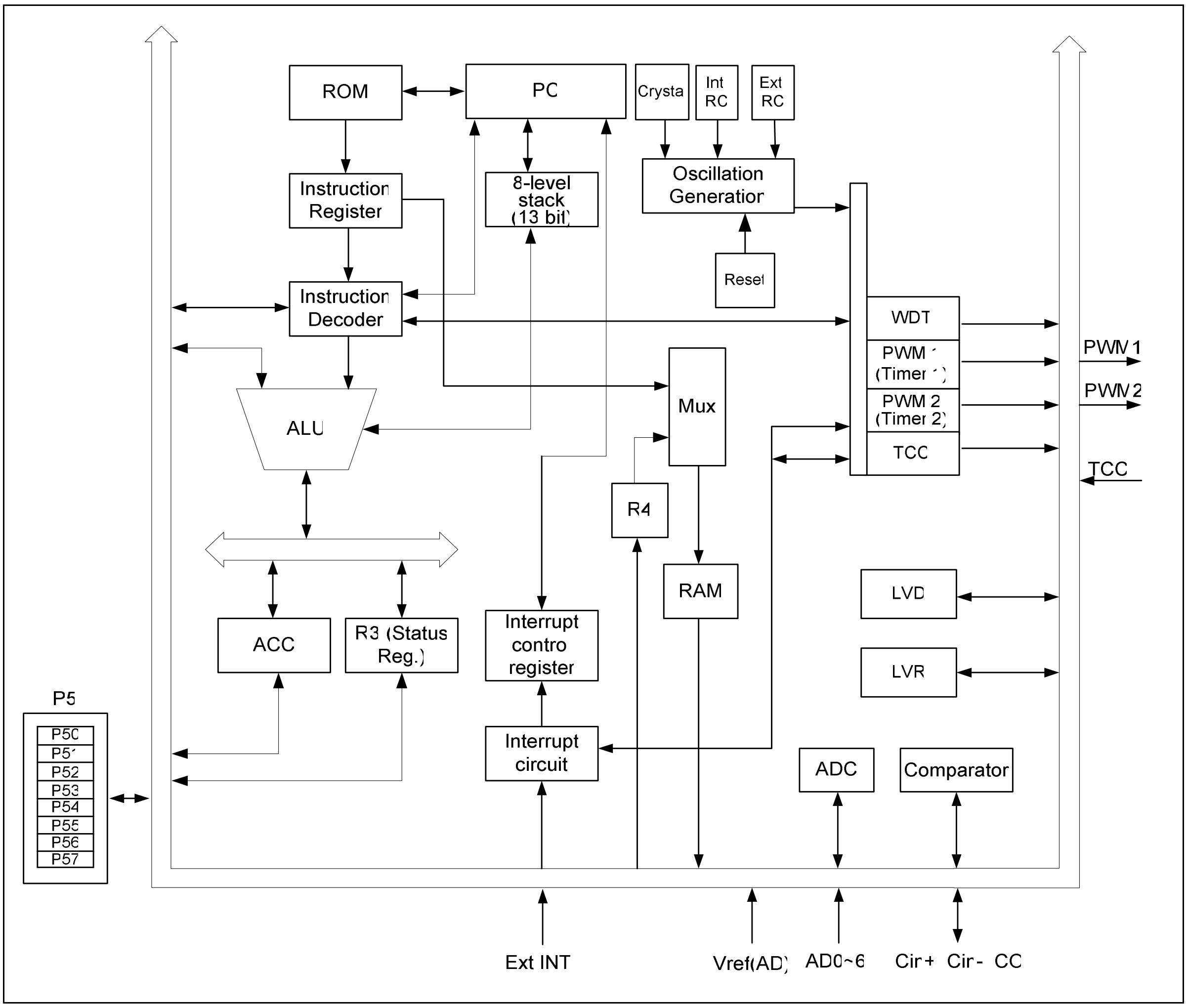


Figure 5-1 EM78P141 Functional Block Diagram

6 Functional Description

6.1 Operational Registers

6.1.1 R0 (Indirect Address Register)

R0 is not a physically implemented register. It is used as an indirect address pointer. Any instruction using R0 as a pointer, actually accesses the data pointed by the RAM Select Register (R4).

6.1.2 R1 (Time Clock/Counter)

- Increased by an external signal edge which is defined by the TE bit (CONT-4) through the TCC pin, or by the instruction cycle clock.
- Writable and readable as any other registers
- The TCC prescaler counter (CONT) is assigned to TCC
- The contents of the CONT register is cleared
  - when a value is written to the TCC register
  - when a value is written to the TCC prescaler bits (Bits 3, 2, 1, & 0 of the CONT register)
  - during power-on reset, /RESET, or WDT time out reset

6.1.3 R2 (Program Counter) and Stack

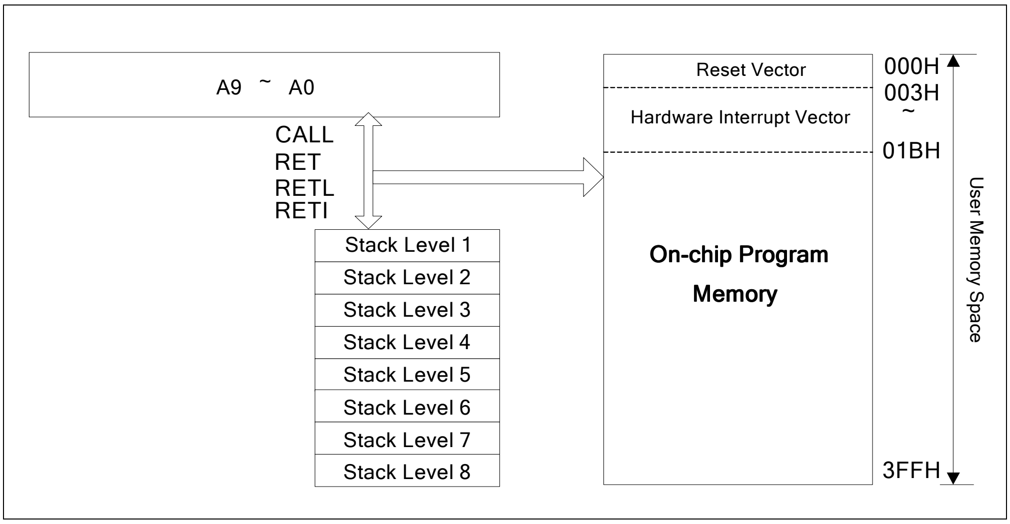


Figure 6-1 Program Counter Organization

- R2 and hardware stacks are 10-bit wide. The structure is depicted in the table under Section 6.1.3.1, *Data Memory Configuration*.

- The configuration structure generates 1K×13 bits on-chip ROM addresses to the relative programming instruction codes. One program page is 1024 words long.
- The contents of R2 are all set to "**0**"s when a reset condition occurs.
- "JMP" instruction allows direct loading of the lower 10 program counter bits. Thus, "JMP" allows the PC to jump to any location within a page.
- "CALL" instruction loads the lower 10 bits of the PC, and then PC+1 is pushed onto the stack. Thus, the subroutine entry address can be located anywhere within a page.
- "RET" ("RETL k", "RETI") instruction loads the program counter with the contents of the top of stack.
- "ADD R2, A" allows a relative address to be added to the current PC, and the ninth and above bits of the PC will increase progressively.
- "MOV R2, A" allows loading of an address from the "A" register to the lower 8 bits of the PC, and the ninth and tenth bits (A8 ~ A9) of the PC will remain unchanged.
- Any instruction (except “ADD R2,A”) that is written to R2 (e.g., "MOV R2, A", "BC R2, 6", etc.) will cause the ninth bit and the tenth bit (A8 ~ A9) of the PC to remain unchanged.
- All instructions are single instruction cycle (fclk/2).

6.1.3.1 Data Memory Configuration

Address	R PAGE registers	IOCX0 PAGE Registers	IOCX1 PAGE registers
00	**R0** (Indirect Addressing Register)	Reserve	Reserve
01	**R1** (Time Clock Counter)	Reserve	Reserve
02	**R2** (Program Counter)	Reserve	Reserve
03	**R3** (Status Register)	Reserve	Reserve
04	**R4** (RAM Select Register)	Reserve	Reserve
05	**R5** (Port 5)	**IOC50** (I/O Port Control Register)	**IOC51** (PWMCON : PWM Control Register)
06	**R6** (LVD Control Register)	**IOC60** (Pull-high Control Register)	**IOC61** (TMRCON : Timer Control Register)
07	**R7** (MCSR)	**IOC70** (Pull-down Control Register)	**IOC71** (PRD1 : PWM1 Time Period)
08	**R8** (ADC Input Select Register	**IOC80** (Open-drain Control Register)	**IOC81** (PRD2 : PWM2 Time Period)
09	**R9** (ADC Control Register)	**IOC90** (Comparator Control Register)	**IOC91** (DT1 : PWM1 Duty Cycle)
0A	**RA** (ADC Offset Calibration Register)	**IOCA0** Reserve	**IOCA1** (DT2 : PWM2 Duty Cycle)
0B	**RB** (The converted value Bit 9~Bit 2 of ADDATAH)	**IOCB0** Reserve	**IOCB1** (TMR1 : PMW1 Timer)
0C	**RC** (The converted value Bit 1~Bit 0 of ADDATAL)	**IOCC0** Reserve	**IOCC1** (TMR2 : PWM2 Timer)
0D	**RD** (THLP: LSB of Table Point Register)	**IOCD0** (Code Option Control Register)	**IOCD1** (Wake-up Control Register)
0E	**RE** (TBHP: MSB of Table Point Register)	**IOCE0** (Code Option Control Register)	**IOCE1** (WDT Control Register)
0F	**RF** (Interrupt Status Register)	**IOCF0** (Interrupt Mask Register 1)	Reserve
10 : 1F	General Registers		
20 : 3F	General Registers		

6.1.4 R3 (Status Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RST	IOCS	-	T	P	Z	DC	C

Bit 7 (RST): Bit of reset type

Set to "**1**" if wake-up from Sleep mode on pin change, comparator status change, or AD conversion completed. Set to "**0**" if wake-up from other reset types.

Bit 6 (IOCS): Select the Segment of IO control register

0: Segment 0 (IOC50 ~ IOCF0) selected

1: Segment 1 (IOC51 ~ IOCF1) selected

Bit 5: **Not used (reserved)**

Bit 4 (T): Time-out bit. Set to "**1**" by the "SLEP" and "WDTC" commands or during power on and reset to "**0**" by WDT time-out. For further details see Section 6.5.2, *The T and P Status under Status Register.*

Bit 3 (P): Power-down bit. Set to "**1**" during power-on or by a "WDTC" command and reset to "**0**" by a "SLEP" command (see Section 6.5.2, *The T and P status under Status Register* for more details).

> **NOTE**
> *Bit 4 and Bit 3 (T and P) are read only.*

Bit 2 (Z): Zero flag. Set to "**1**" if the result of an arithmetic or logic operation is zero.

Bit 1 (DC): Auxiliary carry flag

Bit 0 (C): Carry flag

6.1.5 R4 (RAM Select Register)

Bit 7: Not used bit. Set to '**0**' all the time.

Bit 6: Not used bit. Set to '**0**' all the time.

Bits 5~0: Used to select a register (Address: 00~0F, 10~3F) in indirect addressing mode (see table under Section 6.1.3.1, *Data Memory Configuration*).

6.1.6 R5 (Port 5)

R5 are I/O registers.

6.1.7 R6 (LVD Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
'0'	LVDIF	/LVD	LVDIE	LVDWE	LVDEN	LVD1	LVD0

Bit 7: Not used bit. Read as '**0**' all the time.

Bit 6 (LVDIF): Low Voltage Detector interrupt flag. LVDIF is reset to "**0**" by software.

Bit 5 (/LVD): Low voltage Detector state. This is a read only bit. When the VDD pin voltage is lower than LVD voltage interrupt level (selected by LVD1 and LVD0), this bit is cleared.

0: Low voltage is detected

1: Low voltage is not detected or LVD function is disabled

Bit 4 (LVDIE): Low voltage detector interrupt enable bit

0: Disable low voltage detector interrupt

1: Enable low voltage detector interrupt

> **NOTE**
> - *R6<4> register is both readable and writeable.*
> - *Individual interrupt is enabled by setting its associated control bit in R6<4> to "**1**".*
> - *Global interrupt is enabled by the ENI instruction and is disabled by the DISI instruction. Refer to Figure 6-6b (Interrupt Input Circuit) in Section 6.6 (Interrupt)*

Bit 3 (LVDWE): Low voltage detector wake-up enable bit

0: Disable Low voltage detect wake-up

1: Enable Low voltage detect wake-up

Bit 2 (LVDEN): Low voltage detector enable bit

0: Disable Low voltage detector function

1: Enable Low voltage detector function

Bits 1 ~0: Low voltage detector level bits.

LVDEN	LVD1, LVD0	LVD Voltage Interrupt Level	/LVD
1	11	Vdd ≤ 2.2V	0
		Vdd > 2.2V	1
1	10	Vdd ≤ 3.3V	0
		Vdd > 3.3V	1
1	01	Vdd ≤ 4.0V	0
		Vdd > 4.0V	1
1	00	Vdd ≤ 4.5V	0
		Vdd > 4.5V	1
0	××	N/A	1

6.1.8 R7 (MCSR: Miscellaneous Control and Status Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
"0"	"0"	CPUS	IDLE	EIS	TCCSC	TMR1SC	TMR2SC

Bits 7~6: Not used bit. Read as '**0**' all the time.

Bit 5 (CPUS): CPU Oscillator Source Select

0: Sub-oscillator (fs)

1: Main oscillator (fosc)

When CPUS=0, the CPU oscillator selects the sub-oscillator and the main oscillator is stopped.

Bit 4 (IDLE): Idle Mode Enable Bit. This bit will determine as to which mode to proceed to after SLEP instruction.

0: IDLE="0"+SLEP instruction → Sleep mode

1: IDLE="1"+SLEP instruction → Idle mode

■ **CPU Operation Mode**

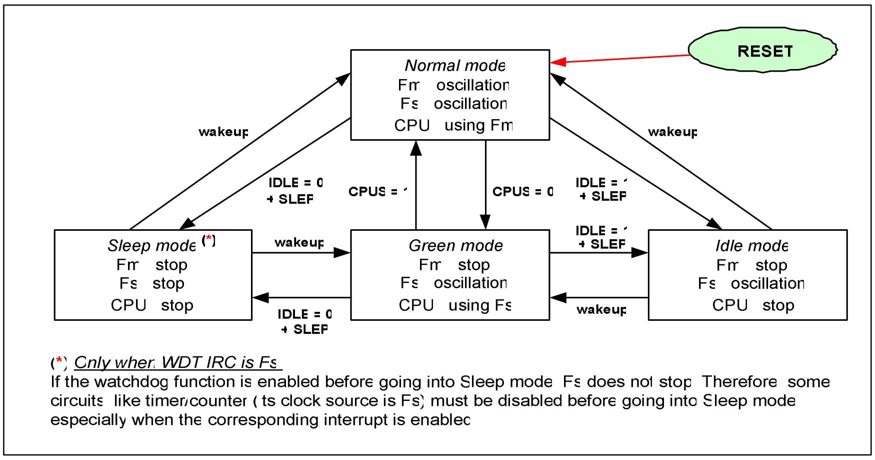


Figure 6-2 CPU Operation Mode

Bit 3 (EIS): Control bit is used to define the P52 (/INT) pin function

0: P52, normal I/O pin

1: /INT, external interrupt pin. In this case, the I/O control bit of P52 (Bit 2 of IOC50) must be set to "**1**".

NOTE

- *When EIS is "**0**," the path of /INT is masked. When EIS is "1", the status of the /INT pin can also be read through reading Port 5 (R5). Refer to Figure 6-4c (I/O Port and I/O Control Register Circuit for P52 (/INT)) in Section 6.4 (I/O Ports).*
- *EIS is both readable and writable.*

Bit 2 (TCCSC): TCC clock source select

0: Fs**:** Sub-frequency for WDT internal RC time base

1: Fm**:** Main-oscillator clock

Bit 1 (TMR1SC): TMR1 clock source select

0: Fs**:** Sub frequency for WDT internal RC time base

1: Fm**:** Main-oscillator clock

Bit 0 (TMR2SC): TMR2 clock source select

0: Fs**:** Sub frequency for WDT internal RC time base

1: Fm**:** Main-oscillator clock

6.1.9 R8 (AISR: ADC Input Select Register)

The AISR register individually defines the Port 5 pins as analog input or as digital I/O.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
”0”	ADE6	ADE5	ADE4	ADE3	ADE2	ADE1	ADE0

Bit 7: Not used bit. Read as ‘**0**’ all the time.

Bit 6 (ADE6): AD converter enable bit of P56 pin

0: Disable AD6, P56 functions as I/O pin

1: Enable AD6 to function as analog input pin

Bit 5 (ADE5): AD converter enable bit of P55 pin

0: Disable AD5, P55 functions as I/O pin

1: Enable AD5 to function as analog input pin

Bit 4 (ADE4): AD converter enable bit of P54 pin

0: Disable AD4, P54 functions as I/O pin

1: Enable AD4 to function as analog input pin

Bit 3 (ADE3): AD converter enable bit of P53 pin

0: Disable AD3, P53 functions as I/O pin

1: Enable AD3 to function as analog input pin

Bit 2 (ADE2): AD converter enable bit of P52 pin

0: Disable AD2, P52 functions as I/O pin

1: Enable AD2 to function as analog input pin

Bit 1 (ADE1): AD converter enable bit of P51 pin

0: Disable AD1, P51 functions as I/O pin

1: Enable AD1 to function as analog input pin

Bit 0 (ADE0): AD converter enable bit of P50 pin

0: Disable AD0, P50 functions as I/O pin

1: Enable AD0 to function as analog input pin

NOTE

- *The TCC, CO and AD5 of the P55/AD5/CO/TCC pins cannot be used at the same time.*
- *The P55/AD5/CO/TCC pin priority is as follows:*

P55/AD5/CO/TCC Priority			
Highest	**High**	**Medium**	**Low**
TCC	**CO**	**AD5**	**P55**

The P50/AD0/OSCI pin cannot be applied to OSCI and AD0 at the same time.
The P50/AD0/OSCI pin priority is as follows:

P50/AD0/OSCI		
High	**Medium**	**Low**
OSCI	**AD0**	**P50**

6.1.10 R9 (ADCON: ADC Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
VREFS	CKR1	CKR0	ADRUN	ADPD	ADIS2	ADIS1	ADIS0

Bit 7 (VREFS): The input source of the VREFS of the ADC

0: The VREFS of the ADC is connected to Vdd (default value), and the P54/VREFS pin carries out the P54 function.

1: The VREFS of the ADC is connected to P54/VREFS.

NOTE

The P54/AD4/CIN-/VERFS pin cannot be applied to VERFS, CIN- and AD4 at the same time.
The P54/AD4/CIN-/VERFS pin priority is as follows:

P54/AD4/CIN-/VREF Pin Priority			
Highest	**High**	**Medium**	**Low**
VREF	**CIN-**	**AD4**	**P54**

Bit 6 and Bit 5 (CKR1 and CKR0): The prescaler of ADC oscillator clock rate

00 = 1**:** 16 (default value)

01 = 1**:** 4

10 = 1**:** 64

11 = 1**:** 8

CKR1: CKR0	Operation Mode	Max. Operation Frequency
00	Fosc/16	4 MHz
01	Fosc/4	1 MHz
10	Fosc/64	16 MHz
11	Fosc/8	2 MHz

Bit 4 (ADRUN): ADC starts to RUN

0: Reset upon completion of the conversion. This bit cannot be reset through software.

1: An AD conversion is started. This bit can be set by software.

Bit 3 (/ADPD): ADC Power-down mode

0: Switch off the resistor reference to save power even if the CPU is operating

1: ADC is operating

> **NOTE**
> *The ADPD bit must be enabled before enabling the ADRUN bit. The program process is shown in Section 6.7.6 (Programming Process/Considerations).*

Bit 2 ~ Bit 0 (ADIS2 ~ADIS0): Analog Input Select

000 = ADIN0/P50

001 = ADIN1/P51

010 = ADIN2/P52

011 = ADIN3/P53

100 = ADIN4/P54

101 = ADIN5/P55

110 = ADIN6/P56

111 = unused

These bits can only be changed when the ADIF bit (see Section 6.1.16) and the ADRUN bit are both Low.

6.1.11 RA (ADOC: ADC Offset Calibration Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CALI	SIGN	VOF[2]	VOF[1]	VOF[0]	"0"	"0"	"0"

Bit 7 (CALI): Calibration enable bit for ADC offset

0: Disable Calibration

1: Enable Calibration

Bit 6 (SIGN): Polarity bit of offset voltage

0: Negative voltage

1: Positive voltage

Bit 5 ~ Bit 3 (VOF[2] ~ VOF[0]): Offset voltage bits

VOF[2]	VOF[1]	VOF[0]	EM78P141
0	0	0	0 LSB
0	0	1	1 LSB
0	1	0	2 LSB
0	1	1	3 LSB
1	0	0	4 LSB
1	0	1	5 LSB
1	1	0	6 LSB
1	1	1	7 LSB

Bit 2 ~ Bit 0: Not used bit. Read as '**0**' all the time.

6.1.12 RB (ADDATAH: Converted Value of ADC)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADD9	ADD8	ADD7	ADD6	ADD5	ADD4	ADD3	ADD2

Bits 7~0 (ADD9~ADD2): AD High 8-Bit Data Buffer for 10-Bit resolution format ADC.

When the AD conversion is completed, the result is loaded into the ADDATAH. The ADRUN bit is cleared, and the ADIF is set (see Section 6.1.16).

RB is read only.

6.1.13 RC (ADDATAL: ADC Converted Value)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
"0"	"0"	"0"	"0"	"0"	"0"	ADD1	ADD0

Bits 1~0 (ADD1~ADD0): AD Low 2-Bit Data Buffer for 10 Bit resolution format ADC.

When the AD conversion is completed, the result is loaded into the ADDATAL. The ADRUN bit is cleared and the ADIF is set (see Section 6.1.16).

RC is read only.

6.1.14 RD (TBLP: LSB of Table Point Register for instruction TBRD)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RBit 7	RBit 6	RBit 5	RBit 4	RBit 3	RBit 2	RBit 1	RBit 0

Bits 7~0: LSB of Table Point Address Bits 7~0

6.1.15 RE (TBHP: MSB of Table Point Register for Instruction TBRD)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MLB	"0"	"0"	"0"	"0"	"0"	RBit 9	RBit 8

Bit 7 (MLB): Take MSB or LSB at machine code.

0: LSB (default)

1: MSB

Bits 6 ~ 2: Not used bit. Read as '**0**' all the time.

Bits 1 ~ 0: MSB of Table Point Address Bits 9~8.

6.1.16 RF (Interrupt Status Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CMPIF	"0"	PWM2IF	PWM1IF	ADIF	EXIF	ICIF	TCIF

NOTE

- *"**1**" means there is an interrupt request. "**0**" means no interrupt occurs.*
- *RF can be cleared by instruction but cannot be set.*
- *IOCF0 is the interrupt mask register.*
- *Reading RF will result to "logic AND" of RF and IOCF0.*

Bit 7 (CMPIF): interrupt flag. Set when a change occurs in the Comparator output. Reset by software.

Bit 6: Not used bit. Read as '**0**' all the time.

Bit 5 (PWM2IF): PWM2 (Pulse Width Modulation) interrupt flag. Set when a selected duration is reached. Reset by software.

Bit 4 (PWM1IF): PWM1 (Pulse Width Modulation) interrupt flag. Set when a selected duration is reached. Reset by software.

Bit 3 (ADIF): Interrupt flag for analog to digital conversion. Set when AD conversion is completed. Reset by software.

Bit 2 (EXIF): External interrupt flag. Set by a falling edge on the /INT pin. Reset by software.

Bit 1 (ICIF): Port 5 input status change interrupt flag. Set when Port 5 input changes. Reset by software.

Bit 0 (TCIF): TCC overflow interrupt flag. Set when TCC overflows. Reset by software.

6.1.17 R10 ~ R3F

These are all 8-bit general-purpose registers.

6.2 Special Purpose Registers

6.2.1 A (Accumulator)

Internal data transfer operation, or instruction operand on hold, usually involves the temporary storage function of the Accumulator, which is not an addressable register.

6.2.2 CONT (Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTE	INT	TS	TE	PSTE	PST2	PST1	PST0

Bit 7 (INTE): INT signal edge

0: Interrupt occurs at a rising edge of the INT pin

1: Interrupt occurs at a falling edge of the INT pin

Bit 6 (INT): Interrupt enable flag

0: Masked by DISI or hardware interrupt

1: Enabled by the ENI/RETI instructions

This bit is readable only

Bit 5 (TS): TCC signal source

0: Internal instruction cycle clock. If P55 is used as I/O pin, TS must be "**0**"

1: Transition on the TCC pin

NOTE

- *The TCC, CO and AD5 of the P55/AD5/CO/TCC pins cannot be used at the same time.*
- *The P55/AD5/CO/TCC pin priority is as follows:*

P55/AD5/CO/TCC Priority			
Highest	**High**	**Medium**	**Low**
TCC	**CO**	**AD5**	**P55**

Bit 4 (TE): TCC signal edge

0: Increment if a transition from **low to high** takes place on TCC pin

1: Increment if a transition from **high to low** takes place on TCC pin

Bit 3 (PSTE): Prescaler enable bit for TCC

0: Prescaler disable bit. TCC rate is 1:1.

1: Prescaler enable bit. TCC rate is set at Bit 2 ~ Bit 0.

Bit 2 ~ Bit 0 (PST2 ~ PST0): TCC prescaler bits

PST2	PST1	PST0	TCC Rate
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

NOTE

Tcc time-out period [1/Fosc x prescaler x (256 - Tcc cnt) x 1 (CLK=2)]
Tcc time-out period [1/Fosc x prescaler x (256 - Tcc cnt) x 1 (CLK=4)]

6.2.3 IOC50 (I/O Port Control Register)

"0" Defines the relative I/O pin as output

"1" Puts the relative I/O pin into high impedance

6.2.4 IOC60 (Pull-high Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
"0"	/PH56	/PH55	/PH54	/PH53	/PH52	/PH51	/PH50

The **IOC60** register is both readable and writable.

Bit 7: Not used bit. Read as '**0**' all the time.

Bit 6 (/PH56): Control bit used to enable pull-high of the P56 pin.

0: Enable internal pull-high

1: Disable internal pull-high

Bit 5 (/PH55): Control bit used to enable internal pull-high of the P55 pin.

Bit 4 (/PH54): Control bit used to enable internal pull-high of the P54 pin.

Bit 3 (/PH53): Control bit used to enable internal pull-high of the P53 pin.

Bit 2 (/PH52): Control bit used to enable internal pull-high of the P52 pin.

Bit 1 (/PH51): Control bit used to enable internal pull-high of the P51 pin.

Bit 0 (/PH50): Control bit used to enable internal pull-high of the P50 pin.

6.2.5 IOC70 (Pull-down Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
"0"	/PD56	/PD55	/PD54	/PD53	/PD52	/PD51	/PD50

IOC70 register is both readable and writable

Bit 7: Not used bit. Read as "**0**" all the time.

Bit 6 (/PD56): Control bit used to enable P56 pin pull-down

0: Enable internal pull-down

1: Disable internal pull-down

Bit 5 (/PD55): Control bit used to enable internal pull-down of P55 pin

Bit 4 (/PD54): Control bit used to enable internal pull-down of P54 pin

Bit 3 (/PD53): Control bit used to enable internal pull-down of P53 pin

Bit 2 (/PD52): Control bit used to enable internal pull-down of P52 pin

Bit 1 (/PD51): Control bit used to enable internal pull-down of P51 pin

Bit 0 (/PD50): Control bit used to enable internal pull-down of P50 pin

6.2.6 IOC80 (Open-Drain Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
"0"	/OD56	/OD55	/OD54	/OD53	/OD52	/OD51	/OD50

IOC80 register is both readable and writable.

Bit 7: Not used bit. Read as "**0**" all the time.

Bit 6 (/OD56): Control bit used to enable the open-drain output of P56 pin

0: Enable open-drain output

1: Disable open-drain output

Bit 5 (/OD55): Control bit used to enable open-drain output of P55 pin

Bit 4 (/OD54): Control bit used to enable open-drain output of P54 pin

Bit 3 (/OD53): Control bit used to enable open-drain output of P53 pin

Bit 2 (/OD52): Control bit used to enable open-drain output of P52 pin

Bit 1 (/OD51): Control bit used to enable open-drain output of P51 pin

Bit 0 (/OD50): Control bit used to enable open-drain output of P50 pin

6.2.7 IOC90 (CMPCON: Comparator Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/IVRE	VRE3	VRE2	VRE1	VRE0	CPOUT	COS1	COS0

Bit 7 (/IVRE): Comparator Internal Voltage Reference Enable bit (“**0**”**:** default).
When the /IVRE bit is set to “**0**”, CIN- pin is set as normal I/O pin.

Bits 6~3: Internal Voltage Reference Ratio Control Bits

VRE3	VRE2	VRE1	VRE0	Voltage Reference Value
0	0	0	0	0
0	0	0	1	VDD × 1/15
0	0	1	0	VDD × 2/15
0	0	1	1	VDD × 3/15
0	1	0	0	VDD × 4/15
0	1	0	1	VDD × 5/15
0	1	1	0	VDD × 6/15
0	1	1	1	VDD × 7/15
1	0	0	0	VDD × 8/15
1	0	0	1	VDD × 9/15
1	0	1	0	VDD × 10/15
1	0	1	1	VDD × 11/15
1	1	0	0	VDD × 12/15
1	1	0	1	VDD × 13/15
1	1	1	0	VDD × 14/15
1	1	1	1	VDD (default)

Bit 2 (CPOUT): Result of the comparator output (register is readable only)

Bit 1 ~ Bit 0 (COS1 ~ COS0): Comparator Select bits

COS1	COS0	Function Description
0	0	Comparator is not used. P55 functions as normal I/O pin.
0	1	Used as Comparator and P55 functions as normal I/O pin.
1	0	Used as Comparator and P55 funcions as Comparator output pin (CO).
1	1	Unused

NOTE

- *The TCC, CO and AD5 of the P55/AD5/CO/TCC pins cannot be used at the same time.*
- *The P55/AD5/CO/TCC pin priority is as follows:*

P55/AD5/CO/TCC Priority			
Highest	**High**	**Medium**	**Low**
TCC	**CO**	**AD5**	**P55**

- *The CIN+ & AD3 of the P53/AD3/CIN+ pins cannot be used at the same time.*
- *The P53/AD3/CIN+ pin priority is as follows:*

P53/AD3/CIN+ Priority		
High	**Medium**	**Low**
CIN+	**AD3**	**P53**

6.2.8 *IOCA0 ~ IOCC0:* Reserved

6.2.9 *IOCD0 (Option Control Bit I)*

Bit	7	6	5	4	3	2	1	0
EM78P141	‘0’	‘0’	‘0’	‘0’	‘0’	‘0’	‘0’	‘0’
ICE143	‘0’	‘0’	‘0’	C4	C3	C2	C1	C0

The **IOCD0** register is both readable and writable.

Bits 7~5: Not used bit. Read as “**0**” all the time.

Bits 4~0 (C4~C0): IRC calibration bits in IRC oscillator mode.

C4	C3	C2	C1	C0	Frequency (MHz)
0	0	0	0	0	F*(1-48%)
0	0	0	0	1	F*(1-45%)
0	0	0	1	0	F*(1-42%)
0	0	0	1	1	F*(1-39%)
0	0	1	0	0	F*(1-36%)
0	0	1	0	1	F*(1-33%)
0	0	1	1	0	F*(1-30%)
0	0	1	1	1	F*(1-27%)
0	1	0	0	0	F*(1-24%)
0	1	0	0	1	F*(1-21%)
0	1	0	1	0	F*(1-18%)
0	1	0	1	1	F*(1-15%)
0	1	1	0	0	F*(1-12%)
0	1	1	0	1	F*(1-9%)
0	1	1	1	0	F*(1-6%)

(Continuation)

C4	C3	C2	C1	C0	Frequency (MHz)
0	1	1	1	1	F*(1-3%)
1	1	1	1	1	F (default)
1	1	1	1	0	F*(1+3%)
1	1	1	0	1	F*(1+6%)
1	1	1	0	0	F*(1+9%)
1	1	0	1	1	F*(1+12%)
1	1	0	1	0	F*(1+15%)
1	1	0	0	1	F*(1+18%)
1	1	0	0	0	F*(1+21%)
1	0	1	1	1	F*(1+24%)
1	0	1	1	0	F*(1+27%)
1	0	1	0	1	F*(1+30%)
1	0	1	0	0	F*(1+33%)
1	0	0	1	1	F*(1+36%)
1	0	0	1	0	F*(1+39%)
1	0	0	0	1	F*(1+42%)
1	0	0	0	0	F*(1+45%)

NOTE

1. *Frequency values shown are theoretical and taken from an instance of a high frequency mode. Hence, they are shown for reference only. Definite values are dependent on the actual process.*
2. *Similar method of calculation is also applicable for low frequency mode.*

6.2.10 IOCE0 (Option Control Bits II)

Bit	7	6	5	4	3	2	1	0
EM78P141	‘0’	‘0’	‘0’	‘0’	‘0’	‘0’	‘0’	‘0’
ICE143	“0”	“0”	LVR1	LVR0	RCM1	RCM0	ADBS	WDTPS

IOCE0 register is both readable and writable.

Bits 7~6: Not used bit. Read as “**0**” all the time.

Bits 5~4 (LVR1 ~ LVR0): Low Voltage Reset enable bits.

LVR1, L VR0	VDD Reset Level	VDD Release Level
11	NA (Power-on Reset)	
10	2.7V	2.9V
01	3.5V	3.7V
00	4.0V	4.2V

Bit 3 and Bit 2 (RCM1 and RCM0): IRC mode select bits

RCM 1	RCM 0	Frequency (MHz)
1	1	4 (default)
1	0	16
0	1	8
0	0	455kHz

Bit 1(ADBS): AD Bit Select Register, fixed at "**0**".

Bit 0 (WDTPS): WDT Time-out Period Select bit

WDT Time	Watchdog Timer
1	18 ms (Default)*
0	4.5 ms*

******Theoretical values, for reference only*

6.2.11 IOCF0 (Interrupt Mask Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CMPIE	"0"	PWM2IE	PWM1IE	ADIE	EXIE	ICIE	TCIE

NOTE

- *The IOCF0 register is both readable and writable.*
- *Individual interrupt is enabled by setting its associated control bit in the IOCF0 to "**1**."*
- *Global interrupt is enabled by the ENI instruction and is disabled by the DISI instruction. Refer to Figure 6-6b (Interrupt Input Circuit) in Section 6.6 (Interrupt).*

Bit 7 (CMPIE): CMPIF interrupt enable bit

0: Disable CMPIF interrupt

1: Enable CMPIF interrupt

When the Comparator output status change is used to enter an interrupt vector or to enter the next instruction, the CMPIE bit must be set to "Enable".

Bit 6: Not used bit. Read as "**0**" all the time

Bit 5 (PWM2IE): PWM2IF interrupt enable bit

0: Disable PWM2 interrupt

1: Enable PWM2 interrupt

Bit 4 (PWM1IE): PWM1IF interrupt enable bit

0: Disable PWM1 interrupt

1: Enable PWM1 interrupt

Bit 3 (ADIE): ADIF interrupt enable bit

0: Disable ADIF interrupt

1: Enable ADIF interrupt

When the ADC Complete status is used to enter an interrupt vector or to enter the next instruction, the ADIE bit must be set to "Enable."

Bit 2 (EXIE): EXIF interrupt enable bit

0: Disable EXIF interrupt

1: Enable EXIF interrupt

Bit 1 (ICIE): ICIF interrupt enable bit

0: Disable ICIF interrupt

1: Enable ICIF interrupt

If Port 5 Input Status Change Interrupt is used to enter an interrupt vector or to enter next instruction, the ICIE bit must be set to "Enable".

Bit 0 (TCIE): TCIF interrupt enable bit

0: Disable TCIF interrupt

1: Enable TCIF interrupt

6.2.12 IOC51 (PWMCON: PWM Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
"0"	"0"	"0"	"0"	"0"	PWMCAS	PWM2E	PWM1E

Bits 7~3: Not used bit. Read as "**0**" all the time

Bit 2 (PWMCAS): PWM Cascade Mode

0: Two Independent 8-bit PWM functions (default value).

1: 16-bit PWM Mode (Cascaded from two 8-bit ones)

Bit 1 (PWM2E): PWM2 enable bit

0: PWM2 is off (default value), and its related pin carries out the P56 function.

1: PWM2 is on, and its related pin is automatically set to output.

Bit 0 (PWM1E): PWM1 enable bit

0: PWM1 is off (default value), and its related pin carries out the P51 function.

1: PWM1 is on, and its related pin is automatically set to output.

NOTE

- *The P56/AD6/PWM2 pin cannot be applied to PWM2 and AD6 at the same time.*
- *The P56/AD6/PWM pin priority is as follows:*

P56/AD6/PWM2		
High	**Medium**	**Low**
PWM2	**AD6**	**P56**

- *The P51/AD1/PWM1/ OSCO pin cannot be applied to AD1, PWM1, and OSCO at the same time.*
- *The P51/AD1 /PWM1/OSCO pin priority is as follows:*

P51/AD1/PWM1/OSCO Priority			
Highest	**High**	**Medium**	**Low**
OSCO	**PWM1**	**AD1**	**P51**

6.2.13 IOC61 (TMRCON: Timer Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
T2EN	T1EN	T2P2	T2P1	T2P0	T1P2	T1P1	T1P0

Bit 7 (T2EN): TMR2 enable bit

0: TMR2 is off (default value)

1: TMR2 is on

Bit 6 (T1EN): TMR1 enable bit

0: TMR1 is off (default value)

1: TMR1 is on

Bit 5 ~ Bit 3 (T2P2 ~ T2P0): TMR2 clock prescaler option bits

T2P2	T2P1	T2P0	Prescale
0	0	0	1:1 (default)
0	0	1	1:2
0	1	0	1:4
0	1	1	1:8
1	0	0	1:16
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

Bit 2 ~ Bit 0 (T1P2 ~ T1P0): TMR1 clock prescale option bits

T1P2	T1P1	T1P0	Prescale
0	0	0	1:1 (default)
0	0	1	1:2
0	1	0	1:4
0	1	1	1:8
1	0	0	1:16
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

6.2.14 IOC71 (PRD1: PWM1 Time Period)

The content of IOC71 is the time period (time base) of PWM1. The frequency of PWM1 is the reverse of the period.

6.2.15 IOC81 (PRD2: PWM2 Time Period)

The content of IOC81 is the time period (time base) of PWM2. The frequency of PWM2 is the reverse of the period.

6.2.16 IOC91 (DT1: PWM1 Duty Cycle)

A specified value keeps the output of PWM1 to remain high until the value matches with TMR1.

6.2.17 IOCA1 (DT2:PWM2 Duty Cycle)

A specified value keeps the output of PWM2 to remain high until the value matches with TMR2.

6.2.18 IOCB1 (TMR1: PWM1 Timer)

The content of IOCB1 is read-only.

6.2.19 IOCC1 (TMR2: PWM2 Timer)

The content of IOCC1 is read-only.

6.2.20 IOCD1 (Wake-up Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
“0”	“0”	“0”	“0”	“0”	ADWE	CMPWE	ICWE

Bits 7~3: Not used bit. Read as “**0**” all the time.

Bit 2 (ADWE): ADC wake-up enable bit

0: Disable ADC wake-up

1: Enable ADC wake-up

When the ADC Complete status is used to enter the interrupt vector or to wake up the EM78P141 from sleep with AD conversion running, the ADWE bit must be set to “Enable“.

Bit 1 (CMPWE): Comparator wake-up enable bit

0: Disable Comparator wake up

1: Enable Comparator wake up

When the Comparator output status change is used to enter the interrupt vector or to wake-up the EM78P141 from Sleep mode, the CMPWE bit must be set to “Enable“.

Bit 0 (ICWE): Port 5 input change to wake-up status enable bit

0: Disable Port 5 input change to wake-up status

1: Enable Port 5 input change wake-up status

When the Port 5 Input Status Change is used to enter an interrupt vector or to wake-up the EM78P141 from sleep, the ICWE bit must be set to “Enable“.

6.2.21 IOCE1 (WDT Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WDTE	”0”	“0”	“0”	PSWE	PSW2	PSW1	PSW0

Bit 7 (WDTE): Control bit is used to enable the Watchdog Timer

0: Disable WDT

1: Enable WDT

The WDTE is both readable and writable

Bits 6~4: Not used bit. Read as “0” all the time.

NOTE

- *The P52/AD2/INT pin cannot be applied to INT and AD2 at the same time.*
- *The P52/AD2/INT pin priority is as follows:*

P52/AD2/INT		
High	**Medium**	**Low**
INT	**AD2**	**P52**

Bit 3 (PSWE): Prescaler enable bit for WDT

0: Prescaler disable bit. WDT rate is 1:1

1: Prescaler enable bit. WDT rate is set at Bit 2~Bit 0

Bit 2 ~ Bit 0 (PSW2 ~ PSW0): WDT prescaler bits

PSW2	PSW1	PSW0	WDT Rate
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

6.2.22 IOCF1: Reserved

6.3 TCC/WDT and Prescaler

■ Registers for the TCC/WDT Circuit

PAGE	Addr.	NAME	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	**CONT**	**INTE**	**INT**	**TS**	**TE**	**PSTE**	**PST2**	**PST1**	**PST0**
R_PAGE	0X0F	**ISR**	CMPIF	"0"	PWM2IF	PWM1IF	ADIF	EXIF	ICIF	**TCIF**
IOCF0	0X0F	**IMR**	CMPIE	"0"	PWM2IE	PWM1IE	ADIE	EXIE	ICIE	**TCIE**
IOCE1	0X0E	**WDTCR**	**WDTE**	"0"	"0"	"0"	**PSWE**	**PSW2**	**PSW1**	**PSW0**

Two 8-bit counters are available as prescalers for the TCC and WDT respectively. The PST0 ~ PST2 bits of the CONT register are used to determine the ratio of the TCC prescaler, and the PSW0 ~ PSW2 bits of the IOCE1 register are used to determine the prescaler of WDT. The prescaler counter is cleared by the instructions each time such instructions are written into TCC. The WDT and prescaler will be cleared by the "WDTC" and "SLEP" instructions. Figure below depicts the block diagram of TCC/WDT.

TCC (R1) is an 8-bit timer/counter. The TCC clock source can be internal clock or external signal input (edge selectable from the TCC pin). If TCC signal source is from internal clock, TCC Will increase by 1 at main oscillator (without prescaler). Referring to Figure 6-3, If TCC signal source is from the external clock input, TCC will increase by 1 at every falling edge or rising edge of the TCC pin. The TCC pin input time length (kept at High or Low level) must be greater than 1CLK.

NOTE

The internal TCC will stop running when Sleep mode occurs. However, during AD conversion, when TCC is set to "SLEP" instruction, with the ADWE bit of IOCD1 register enabled, the TCC will keep on running.

The watchdog timer is a free running on-chip RC oscillator. The WDT will keep on running even when the oscillator driver has been turned off (i.e., in Sleep mode). During normal operation or in Sleep mode, a WDT time-out (if enabled) will cause the device to reset. The WDT can be enabled or disabled at any time during normal mode through software programming. Refer to WDTE bit of IOCE1 register (Section 6.2.23 WDT Control Register). With no prescaler, the WDT time-out duration is approximately 18ms[1] or 4.5ms[2].

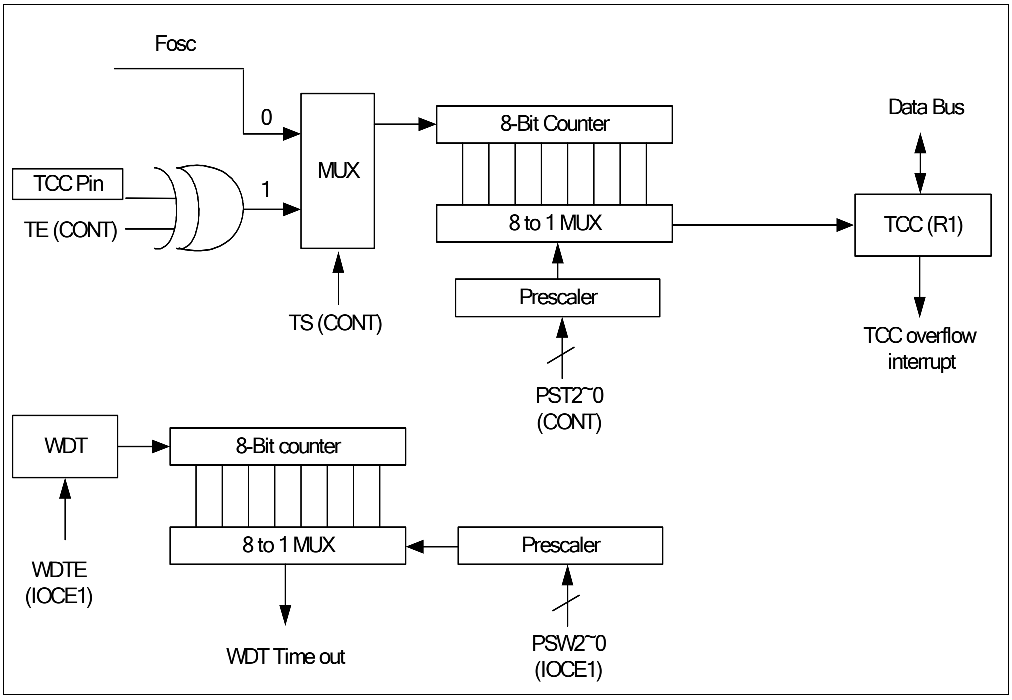


Figure 6-3 TCC and WDT Block Diagram

[1] VDD=5V, Setup time period = 16.5ms ± 30%
VDD=3V, Setup time period = 18ms ± 30%

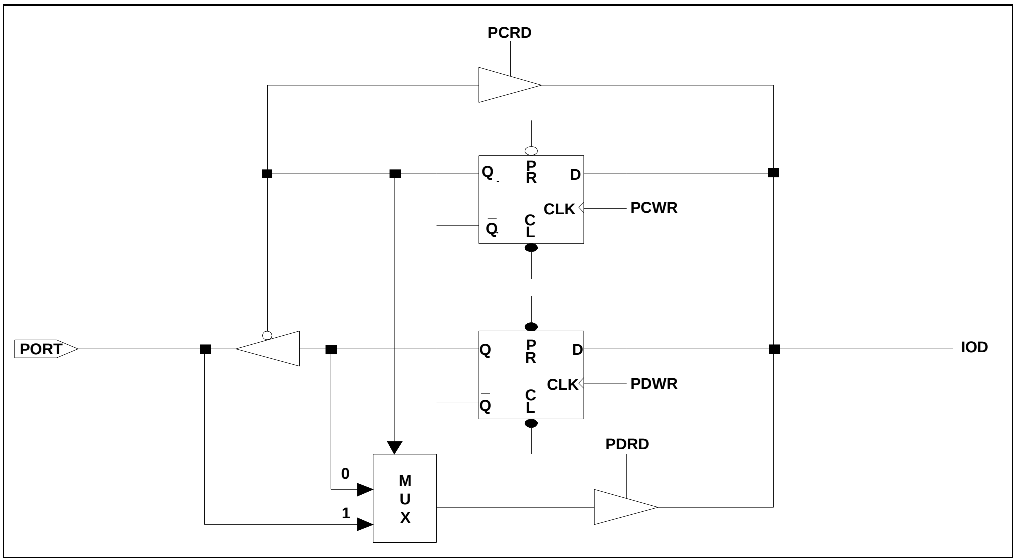
[2] VDD=5V, Setup time period = 4.2ms ± 30%
VDD=3V, Setup time period = 4.5ms ± 30%

6.4 I/O Ports

■ Registers for the I/O Circuit

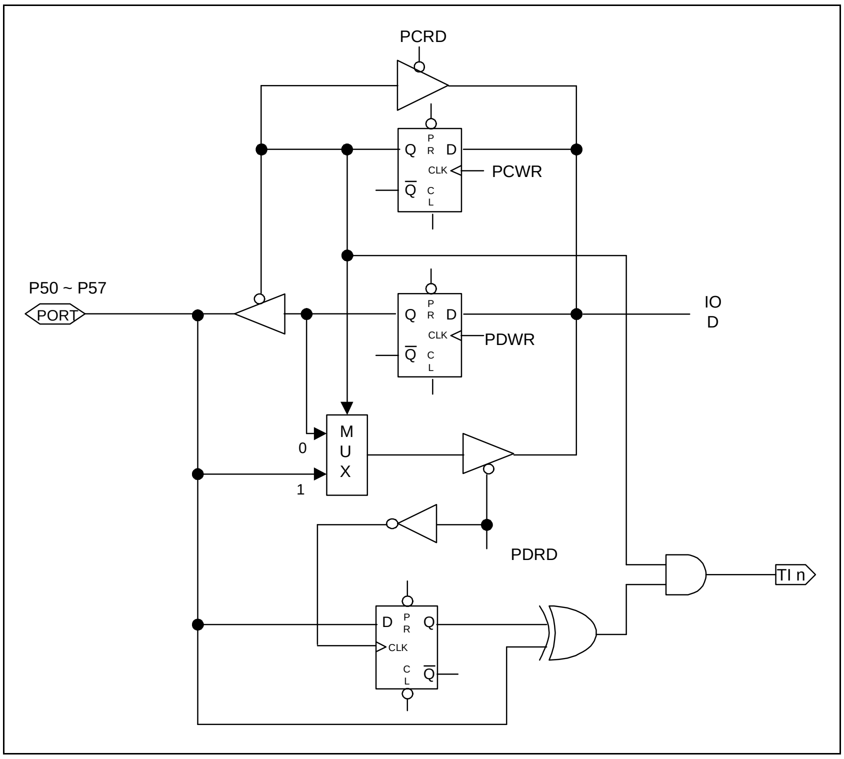
Page	Addr.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IOC50	0×05	**IOCR**	**IOC7**	**ICO6**	**IOC5**	**IOC4**	**IOC3**	**IOC2**	**IOC1**	**IOC0**
IOC60	0×06	**PHCR**	**"0"**	**/PH56**	**/PH55**	**/PH54**	**/PH53**	**/PH52**	**/PH51**	**/PH50**
IOC70	0×07	**PDCR**	**"0"**	**/PD56**	**/PD55**	**/PD54**	**/PD53**	**/PD52**	**/PD51**	**/PD50**
IOC80	0×08	**ODCR**	**"0"**	**/OD56**	**/OD55**	**/OD54**	**/OD53**	**/OD52**	**/OD51**	**/OD50**

The I/O registers (Port 5) are bidirectional tri-state I/O ports. The pull-high, pull-down, and open-drain functions can be set internally by IOC60, IOC70, and IOC80, respectively. Port 5 features an input status change interrupt (or wake-up) function. Each I/O pin can be defined as "input" or "output" pin by the I/O control registers (IOC50). The I/O registers and I/O control registers are both readable and writable. The I/O interface circuits for Port 5 are illustrated in the following Figures 6-4a, 6-4b, and 6-4c respectively. Port 5 with Input Change Interrupt/Wake-up is shown in Figure 6-4d.



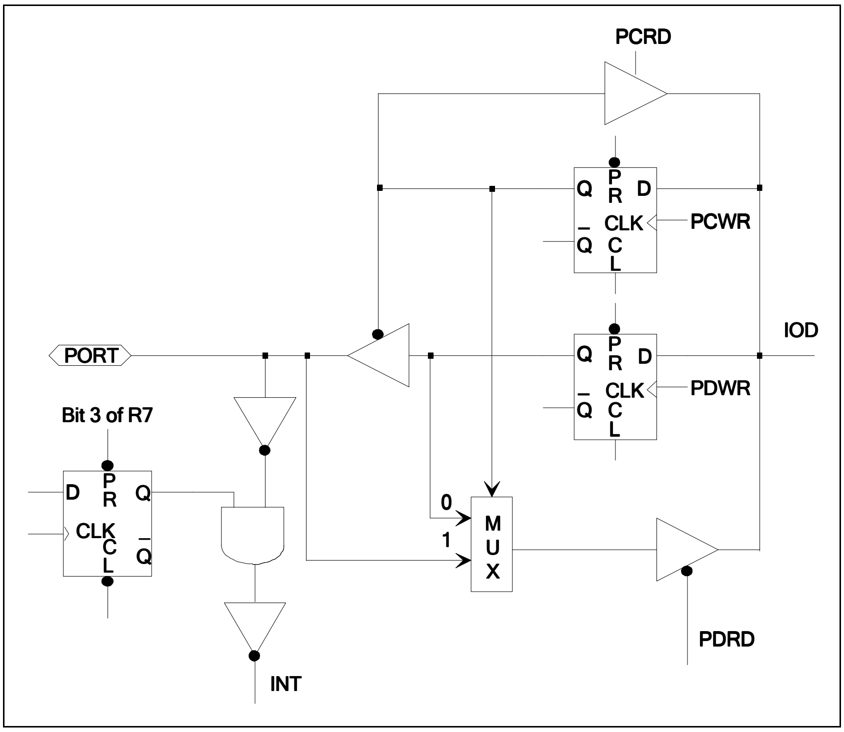
NOTE: *Pull-high and Open-drain are not shown in the figure*

Figure 6-4a I/O Port and I/O Control Register Circuit for Port 5



NOTE: *Pull-high/down and Open-drain are not shown in the figure*

Figure 6-4b I/O Port and I/O Control Register Circuit for Port 5



NOTE: *Pull-high and Open-drain are not shown in the figure*

Figure 6-4c I/O Port and I/O Control Register Circuit for P52 (/INT)

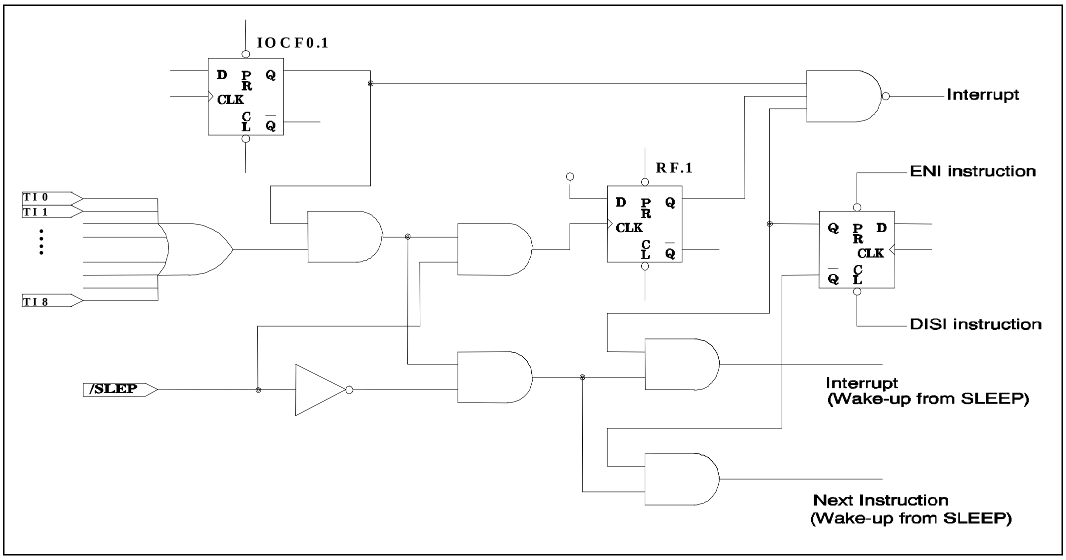


Figure 6-4d Port 5 with Input Change Interrupt/Wake-up

6.4.1 Usage of Port 5 Input Change Wake-up/Interrupt Function

1. Wake-up	2 Wake-up and Interrupt
a) Before Sleep	**a) Before Sleep**
1) Disable WDT	1) Disable WDT
2) Read I/O Port 5 (MOV R5,R5)	2) Read I/O Port 5 (MOV R5,R5)
3) Execute "ENI" or "DISI"	3) Execute "ENI" or "DISI"
4) Enable wake-up bit (Set IOCD1 ICWE =1)	4) Enable wake-up bit (Set IOCD1 ICWE =1)
5) Execute "SLEP" instruction	5) Enable interrupt (Set IOCF0 ICIE =1)
b) After wake-up	6) Execute "SLEP" instruction
→ Next instruction	**b) After Wake-up**
	1) IF "ENI" → Interrupt vector (006H)
	2) IF "DISI" → Next instruction

3. Interrupt
a) Before Port 5 pin change
1) Read I/O Port 5 (MOV R5,R5)
2) Execute "ENI" or "DISI"
3) Enable interrupt (Set IOCF0 ICIE =1)
b) After Port 5 pin changed (interrupt)
1) IF "ENI" → Interrupt vector (006H)
2) IF "DISI" → Next instruction

6.5 Reset and Wake-up

6.5.1 Reset and Wake-up Operation

A reset is initiated by one of the following events**:**

1) Power-on reset
2) /RESET pin input "low"
3) WDT time-out (if enabled)

The device is kept in reset condition for a period of approximately 18ms[3] (except in LXT mode) after the reset is detected. When in LXT2 mode, the reset time is 2~3s. Two choices (18ms[3] or 4.5ms[4]) are available for WDT-time out period. Once a RESET occurs, the following functions are performed (the initial Address is 000h):

- The oscillator continues running, or will be started (if in Sleep mode)
- The Program Counter (R2) is set to all "**0**"
- All I/O port pins are configured as input mode (high-impedance state)
- The Watchdog Timer and prescaler are cleared
- When power is switched on, the upper two bits of R3 and upper two bits of R4 are cleared
- The CONT register bits are set to all "**0**" except for Bit 6 (INT flag)
- The IOC60 register bits are set to all "**1**"
- The IOC70 register bits are set to all "**1**"
- The IOC80 register bits are set to all "**1**"
- RF register and IOCF0 register are cleared

Executing the "SLEP" instruction will assert the Sleep (power down) mode. While going into Sleep mode, the Oscillator, TCC, Timer 1 and Timer 2 are stopped. The WDT (if enabled) is cleared but keeps on running.

The controller can be awakened by any of the following events**:**

1) External reset input on /RESET pin
2) WDT time-out (if enabled)
3) Port 5 input status changes (if ICWE is enabled)
4) Comparator output status changes (if CMPWE is enabled)
5) AD conversion completed (if ADWE is enabled)
6) Low voltage Detector (if LVDWE is enabled)

[3] VDD=5V, WDT Time-out period = 16.5ms ± 30%.
VDD=3V, WDT Time-out period = 18ms ± 30%.

[4] VDD=5V, WDT Time-out period = 4.2ms ± 30%.
VDD=3V, WDT Time-out period = 4.5ms ± 30%.

The first two events (1 and 2) will cause the EM78P141 to reset. The T and P flags of R3 can be used to determine the source of the reset (Wake-up). Events 3, 4, 5, and 6 are considered the continuation of program execution and the global interrupt ("ENI" or "DISI" being executed) determines whether or not the controller branches to the interrupt vector following wake-up. If ENI is executed before SLEP, the instruction will begin to execute from Address 0x06 (Event 3), 0x0F (Event 4), and 0x0C (Event 5) and 0x18 (Event 6) after Wake-up. If DISI is executed before SLEP, the execution will restart from the instruction next to SLEP immediately after waking-up.

Only one of Events 2 to 6 can be enabled before entering into Sleep mode. That is**:**

a) If WDT is enabled before SLEP, the entire IOCD1 bit is disabled. Hence, the EM78P141 can be awakened only under Event 1 or Event 2 condition. Refer to Section 6.6, *Interrupt, f*or further details.

b) If Port 5 Input Status Change is used to wake up the EM78P141 and the ICWE bit of the IOCD1 register is enabled before SLEP, the WDT must be disabled. Hence, the EM78P141 can be awakened only under Event 3 condition. Wake-up time is subject to existing oscillator mode**:**
   - In RC mode, wake-up time is 32 clocks (for stable oscillators).
   - In Crystal mode, wake-up time is 1.5ms (XT, 4 MHz).
   - In low Crystal mode, wake-up time is 2s ~ 3s.

c) If Comparator output status change is used to wake up the EM78P141 and the CMPWE bit of the IOCD1 register is enabled before SLEP, the WDT must be disabled by software. Hence, the EM78P141 can be awakened only under Event 4 condition. Wake-up time is subject to existing oscillator mode**:**
   - In RC mode, wake-up time is 32 clocks (for stable oscillators).
   - In Crystal mode, wake-up time is 1.5ms (XT, 4 MHz).
   - In low Crystal mode, wake-up time is 2s~3s.

d) If AD conversion completed status is used to wake up the EM78P141 and ADWE bit of the IOCD1 register is enabled before SLEP, the WDT must be disabled by software. Hence, the EM78P141 can be awakened only under Event 5 condition. The wake-up time is 15 TAD (ADC clock period).

e) If Low voltage detector is used to wake up the EM78P141 and LVDWE bit of R6 register is enabled before SLEP, the WDT must be disabled by software. Hence, the EM78P141 can be awakened only under Event 6 condition.

If Port 5 Input Status Change Interrupt is used to wake up the EM78P141 (as in Event b above), the following instructions must be executed before SLEP:

```
BS              R3, 6           ; Select Segment 1
MOV             A, @00001110b   ; Select WDT prescaler and Disable WDT
IOW             IOCE1
WDTC                            ; Clear WDT and prescaler
MOV             R5, R5          ; Read Port 5
ENI (or DISI)                   ; Enable (or disable) global interrupt
MOV             A, @00000XX1b   ; Enable Port 5 input change wake-up bit
IOW             IOCD1
BC              R3, 6           ; Select Segment 0
MOV             A, @00000x1xb   ; Enable Port 5 input change interrupt
IOW             IOCF0
SLEP                            ; SLEEP
```

Similarly, if the Comparator Interrupt is used to wake up the EM78P141 (as in Event c above), the following instructions must be executed before SLEP:

```
BC              R3, 6           ; Select Segment 0
MOV             A, @xxxxxx10b   ; Select an comparator and P55 act as CO
                                ; pin
IOW             IOC90
BS              R3, 6           ; Select Segment 1
MOV             A, @00001110b   ; Select WDT prescaler and Disable WDT
IOW             IOCE1
WDTC                            ; Clear WDT and prescaler
ENI (or DISI)                   ; Enable (or disable) global interrupt
MOV             A, @00000X1Xb   ; Enable comparator output status change
                                ; wake-up bit
IOW             IOCD1
BC              R3,6            ; Select Segment 0
MOV             A,@10XXXXXXb    ; Enable comparator output status change
                                ; Interrupt
MOV             IOCF0
SLEP                            ; Sleep
```

6.5.1.1 Wake-up and Interrupt Modes Operation Summary

All categories in Wake-up and Interrupt modes are summarized below.

Wakeup Signal	Sleep Mode	Idle Mode	Green Mode	Normal Mode
External interrupt	×	Wake-up + interrupt (if interrupt enable) + next instruction	Interrupt (if interrupt enable) or next instruction	Interrupt (if interrupt enable) or next instruction
Port 5 pin change	If enable ICWE bit Wake-up + interrupt (if interrupt enable) + next instruction	If enable ICWE bit Wake-up + interrupt (if interrupt enable) + next instruction	Interrupt (if interrupt enable) or next instruction	Interrupt (if interrupt enable) or next instruction
TCC overflow interrupt	×	Wake-up + interrupt (if interrupt enable) + next instruction	Interrupt (if interrupt enable) or next instruction	Interrupt (if interrupt enable) or next instruction
AD conversion complete interrupt	If enable ADWE bit Wake-up + interrupt (if interrupt enable) + next instruction **Fs & Fm don't stop**	If enable ADWE bit Wake-up + interrupt (if interrupt enable) + next instruction **Fs & Fm don't stop**	×	Interrupt (if interrupt enable) or next instruction
Comparator interrupt	If enable CMPWE bit Wake-up + interrupt (if interrupt enable) + next instruction	If enable CMPWE bit Wake-up+ interrupt (if interrupt enable) + next instruction	Interrupt (if interrupt enable) or next instruction	Interrupt (if interrupt enable) or next instruction
PWMX (PWM1 and PWM2) (When TimerX matches PRDX)	×	Wake-up + interrupt (if interrupt enable) + next instruction	Interrupt (if interrupt enable) or next instruction	Interrupt (if interrupt enable) or next instruction
Low Voltage Detector interrupt	If Enable LVDWE bit Wake-up + interrupt (if interrupt enable) + next instruction	If Enable LVDWE bit Wake-up + interrupt (if interrupt enable) + next instruction	Interrupt (if interrupt enable) or next instruction	Interrupt (if interrupt enable) or next instruction
WDT Time out	RESET	RESET	RESET	RESET
Low Voltage Reset	RESET	RESET	RESET	RESET

NOTE

After wake up:

1. *If interrupt enable → interrupt + next instruction*
2. *If interrupt disable → next instruction*

6.5.1.2 Wake-up and Interrupt Modes Operation Summary

Signal	Sleep Mode	Normal Mode
INT Pin	NA	**DISI + IOCF0 (EXIE) Bit 2 = 1**
		Next Instruction+ Set RF (EXIF) = 1
		ENI + IOCF0 (EXIE) Bit 2 = 1
		Interrupt Vector (0x03)+ Set RF (EXIF)=1
Port 5 Input Status Change	IOCD1 (ICWE) Bit1=0, IOCF0 (ICIE) Bit1=0	IOCF0 (ICIE) Bit 1 = 0
	Oscillator, TCC and TIMERX are stopped. Port 5 input status change wake up is invalid.	Port 5 input status change interrupt is invalid
	IOCD1 (ICWE) Bit1=0, IOCF0 (ICIE) Bit1=1	NA
	Set RF (ICIF) = 1, Oscillator, TCC and TIMERX are stopped. Port 5 input status change wake up is invalid.	NA
	IOCD1 (ICWE) Bit 0 = 1, IOCF0 (ICIE) Bit 1 = 0	NA
	Wake-up+ Next Instruction Oscillator, TCC and TIMERX are stopped.	NA
	IOCD1 (ICWE) Bit 0 = 1, DISI + IOCF0 (ICIE) Bit 1 = 1	**DISI + IOCF0 (ICIE) Bit 1 = 1**
	Wake-up+ Next Instruction+ Set RF (ICIF) = 1 Oscillator, TCC and TIMERX are stopped.	Next Instruction+ Set RF (ICIF) = 1
	IOCD1 (ICWE) Bit 0=1, ENI + IOCF0 (ICIE) Bit 1 = 1	**ENI + IOCF0 (ICIE) Bit 1 = 1**
	Wake-up+ Interrupt Vector (0x06)+ Set RF (ICIF) = 1 Oscillator, TCC and TIMERX are stopped.	Interrupt Vector (0x06)+ Set RF (ICIF)=1
TCC Overflow	NA	DISI + IOCF0 (TCIE) Bit 0=1
		Next Instruction + Set RF (TCIF)=1
		ENI + IOCF0 (TCIE) Bit 0=1
		Interrupt Vector (009H) + Set RF (TCIF)=1
AD Conversion	**IOCD1 (ADWE) Bit 2=0, IOCF0 (ADIE) Bit 3 = 0**	IOCF0 (ADIE) Bit 3=0
	Clear R9 (ADRUN) = 0, ADC is stopped, AD conversion wake up is invalid. Oscillator, TCC and TIMERX are stopped.	AD conversion interrupt is invalid
	IOCD1 (ADWE) Bit 2 = 0, IOCF0 (ADIE) Bit 3 = 1	NA
	Set RF (ADIF) = 1, R9 (ADRUN) = 0, ADC is stopped, AD conversion wake up is invalid. Oscillator, TCC and TIMERX are stopped.	NA
	IOCD1 (ADWE) Bit 2 = 1, IOCF0 (ADIE) Bit 3 = 0	NA
	Wake-up+ Next Instruction, Oscillator, TCC and TIMERX keep on running. Wake up when AD conversion is completed.	NA
	IOCD1 (ADWE) Bit 2 = 1, DISI + IOCF0 (ADIE) Bit 3 = 1	DISI + IOCF0 (ADIE) Bit 3=1
	Wake-up+ Next Instruction+ RF (ADIF) = 1, Oscillator, TCC and TIMERX keep on running. Wake up when AD conversion is completed.	Next Instruction + RF (ADIF)=1
	IOCD1 (ADWE) Bit 2 = 1, ENI + IOCF0 (ADIE) Bit 3 = 1	ENI + IOCF0 (ADIE) Bit 3=1
	Wake-up+ Interrupt Vector (0x0C)+ RF (ADIF) = 1, Oscillator, TCC and TIMERX keep on running. Wake up when AD conversion is completed.	Interrupt Vector (00CH) + Set RF (ADIF)=1

(Continuation)

Signal	Sleep Mode	Normal Mode
Comparator (Comparator Output Status Change)	**IOCD1 (CMPWE) Bit 1 = 0, IOCF0 (CMPIE) Bit 7 = 0**	**IOCF0 (CMPIE) Bit 7 = 0**
	Comparator output status change wake-up is invalid. Oscillator, TCC and TIMERX are stopped.	Comparator output status change interrupt is invalid.
	IOCD1 (CMPWE) Bit 1 = 0, IOCF0 (CMPIE) Bit 7 = 1	**NA**
	Set RF (CMPIF) = 1, Comparator output status change wake up is invalid. Oscillator, TCC and TIMERX are stopped.	NA
	IOCD1 (CMPWE) Bit 1 = 1, IOCF0 (CMPIE) Bit 7 = 0	**NA**
	Wake-up+ Next Instruction, Oscillator, TCC and TIMERX are stopped.	NA
	IOCD1 (CMPWE) Bit 1=1, DISI + IOCF0 (CMPIE) Bit 7 = 1	**DISI + IOCF0 (CMPIE) Bit 7 = 1**
	Wake-up+ Next Instruction+ Set RF (CMPIF) = 1, Oscillator, TCC and TIMERX are stopped.	Next Instruction+ Set RF (CMPIF) = 1
	IOCD1 (CMPWE) Bit 1 = 1, ENI + IOCF0 (CMPIE) Bit 7 = 1	**ENI + IOCF0 (CMPIE) Bit 7 = 1**
	Wake-up+ Interrupt Vector (0x0F)+ Set RF (CMPIF) = 1, Oscillator, TCC and TIMERX are stopped.	Interrupt Vector (0x0F)+ Set RF (CMPIF) = 1
Low Voltage Detector	**R6 (LVDWE) Bit 3 = 0, R6 (LVDIE) Bit 4 = 0**	**R6 (LVDIE) Bit 4 = 0**
	Low voltage detector is invalid. Oscillator, TCC and TIMERX are stopped.	Low voltage detector is invalid.
	R6 (LVDWE) Bit 3 = 0, R6 (LVDIE) Bit 4 = 1	**NA**
	Set R6 (LVDIF) Bit 6 =1, Low voltage detector is invalid. Oscillator, TCC and TIMERX are stopped.	NA
	R6 (LVDWE) Bit 3 = 1, R6 (LVDIE) Bit 4 = 0	**NA**
	Wake-up+ Next Instruction, Oscillator, TCC and TIMERX are stopped.	NA
	R6 (LVDWE) Bit 3 = 1, DISI+ R6 (LVDIE) Bit 4 = 1	**DISI + R6 (LVDIE) Bit 4 = 1**
	Wake-up+ Next Instruction+ Set R6 (LVDIF) Bit 3 = 1, Oscillator, TCC and TIMERX are stopped.	Next Instruction+ Set R6 (LVDIF) Bit 3 = 1
	R6 (LVDWE) Bit 3 = 1,ENI+ R6 (LVDIE) Bit 4 = 1	**ENI + R6 (LVDIE) Bit 4 =1**
	Wake-up+ Interrupt Vector (0x18)+ Set R6 (LVDIF) Bit 3 = 1,Oscillator, TCC and TIMERX are stopped.	Interrupt Vector (0x18)+ Set R6 (LVDIF) Bit 3 = 1
WDT Timeout IOCE1 (WDTE) Bit 7 = 1	Wake-up+ Reset (Address 0x00)	Reset (Address 0x00)

6.5.1.3 Register Initial Values after Reset

The following summarizes the initialized values for registers.

Addr.	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
N/A	IOC50	Bit Name	C57	C56	C55	C54	C53	C52	C51	C50
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOC60	Bit Name	-	/PH56	/PH55	/PH55	/PH53	/PH52	/PH51	/PH50
		Power-on	0	1	1	1	1	1	1	1
		/RESET and WDT	0	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOC70	Bit Name	-	/PD56	/PD55	/PD54	/PD53	/PD52	/PD51	/PD50
		Power-on	0	1	1	1	1	1	1	1
		/RESET and WDT	0	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOC80	Bit Name	-	/OD56	/OD55	/OD54	/OD53	/OD52	/OD51	/OD50
		Power-on	0	1	1	1	1	1	1	1
		/RESET and WDT	0	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOC90	Bit Name	/IVRE	VRE3	VRE2	VRE1	VRE0	CPOUT	COS1	COS0
		Power-on	0	1	1	1	1	0	0	0
		/RESET and WDT	0	1	1	1	1	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOCA0	Bit Name	-	-	-	-	-	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOCB0	Bit Name	-	-	-	-	-	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOCC0	Bit Name	-	-	-	-	-	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOCD0	Bit Name	-	-	-	-	-	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOCE0 (Code Option II)	Bit Name	-	-	-	-	-	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P

(Continuation)

Addr.	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
N/A	IOCF0	Bit Name	CMPIE	-	PWM2IE	PWM1IE	ADIE	EXIE	ICIE	TCIE
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOC51 PWMCON	Bit Name	-	-	-	-	-	PWMCAS	PWM2E	PWM1E
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOC61 TMRCON	Bit Name	T2EN	T1EN	T2P2	T2P1	T2P0	T1P2	T1P1	T1P0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOC71 (PRD1)	Bit Name	PRD1 [7]	PRD1 [6]	PRD1 [5]	PRD1 [4]	PRD1 [3]	PRD1 [2]	PRD1 [1]	PRD1 [0]
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOC81 (PRD2)	Bit Name	PRD2 [7]	PRD2 [6]	PRD2 [5]	PRD2 [4]	PRD2 [3]	PRD2 [2]	PRD2 [1]	PRD2 [0]
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOC91 (DT1)	Bit Name	DT1[7]	DT1[6]	DT1[5]	DT1[4]	DT1[3]	DT1[2]	DT1[1]	DT1[0]
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOCA1 (DT2)	Bit Name	DT2[7]	DT2[6]	DT2[5]	DT2[4]	DT2[3]	DT2[2]	DT2[1]	DT2[0]
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOCB1 (TMR1)	Bit Name	TMR1[7]	TMR1[6]	TMR1[5]	TMR1[4]	TMR1[3]	TMR1[2]	TMR1[1]	TMR1[0]
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOCC1 (TMR2)	Bit Name	TMR2[7]	TMR2[6]	TMR2[5]	TMR2[4]	TMR2[3]	TMR2[2]	TMR2[1]	TMR2[0]
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOCD1 (WUCR)	Bit Name	–	–	–	–	–	ADWE	CMPWE	ICWE
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P

(Continuation)

Addr.	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
N/A	IOCE1 (WDTC)	Bit Name	WDTE	–	–	–	PSWE	PSW2	PSW1	PSW0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	CONT	Bit Name	INTE	INT	TS	TE	PSTE	PST2	PST1	PST0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×00	R0 (IAR)	Bit Name	-	-	-	-	-	-	-	-
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×01	R1 (TCC)	Bit Name	-	-	-	-	-	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×02	R2 (PC)	Bit Name	-	-	-	-	-	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	Jump to Address 0×06 or continue to execute next instruction							
0×03	R3 (SR)	Bit Name	RST	IOCS	-	T	P	Z	DC	C
		Power-on	0	0	0	1	1	U	U	U
		/RESET and WDT	0	0	0	t	t	P	P	P
		Wake-up from Pin Change	P	P	P	t	t	P	P	P
0×04	R4 (RSR)	Bit Name	–	–	–	–	–	–	–	–
		Power-on	0	0	U	U	U	U	U	U
		/RESET and WDT	0	0	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×05	R5	Bit Name	P57	P56	P55	P54	P53	P52	P51	P50
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	U	U	U	U	U	U	U	U
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×06	R6 (LVDCR)	Bit Name	–	LVDIF	/LVD	LVDIE	LVDWE	LVDEN	LVD1	LVD0
		Power-on	0	0	1	0	0	0	1	1
		/RESET and WDT	0	0	1	0	0	0	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×07	R7 (MCSR)	Bit Name	–	-	CPUS	IDLE	EIS	TCCSC	TMR1SC	TMR2SC
		Power-on	0	0	1	1	0	0	0	0
		/RESET and WDT	0	0	1	1	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P

(Continuation)

Addr.	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0×08	R8 (AISR)	Bit Name	-	ADE6	ADE5	ADE4	ADE3	ADE2	ADE1	ADE0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×09	R9 (ADCON)	Bit Name	VREFS	CKR1	CKR0	ADRUN	ADPD	ADIS2	ADIS1	ADIS0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0A	RA (ADOC)	Bit Name	CALI	SIGN	VOF[2]	VOF[1]	VOF[0]	–	–	–
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0B	RB ADDATAH	Bit Name	ADD9	ADD8	ADD7	ADD6	ADD5	ADD4	ADD3	ADD2
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	U	U	U	U	U	U	U	U
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0C	RC ADDATAL	Bit Name	–	–	–	–	–	–	ADD1	ADD0
		Power-on	0	0	0	0	0	0	U	U
		/RESET and WDT	0	0	0	0	0	0	U	U
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0D	RD (TBLP)	Bit Name	RBit 7	RBit 6	RBit 5	RBit 4	RBit 3	RBit 2	RBit 1	RBit 0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0E	RE (TBHP)	Bit Name	MLB	-	-	-	-	-	RBit 9	RBit 8
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0F	RF (ISR)	Bit Name	CMPIF	-	PWM2IF	PWM1IF	ADIF	EXIF	ICIF	TCIF
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P

Legend: ×: Not used **U:** Unknown or don't care
P: Previous value before reset **t:** Check table under Section 6.5.2

6.5.1.4 Controller Reset Block Diagram

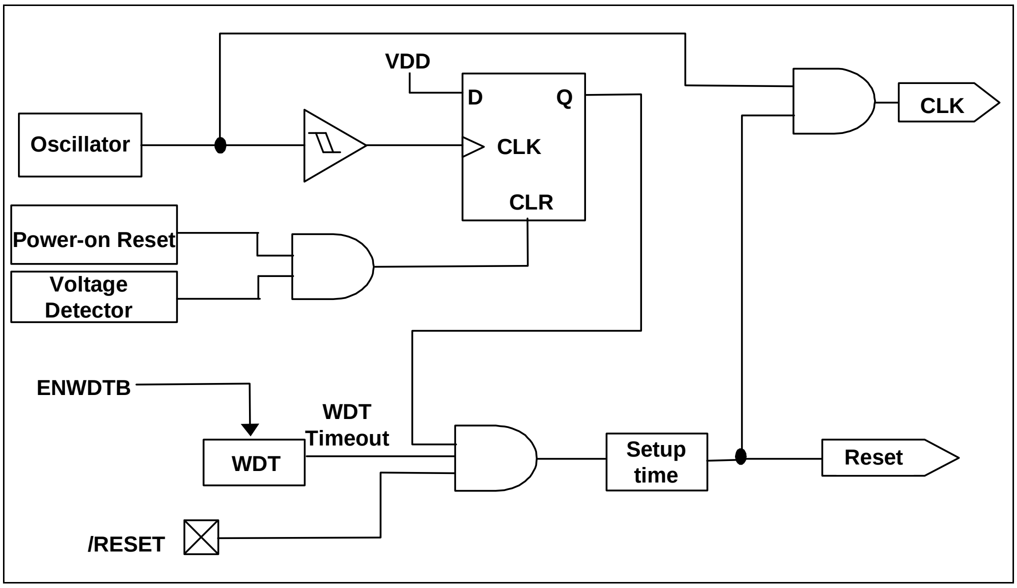


Figure 6-5 Controller Reset Block Diagram

6.5.2 The T and P Status under Status Register

A reset condition is initiated by one of the following events:

1) Power-on reset
2) /RESET pin input "low"
3) WDT time-out (if enabled)

The values of T and P as listed in the table below, are used to check how the processor wakes up.

Reset Type	T	P
Power-on	1	1
/RESET during Operating mode	*P	*P
/RESET wake-up during Sleep mode	1	0
LVR during Operating mode	*P	*P
LVR wake-up during Sleep mode	1	0
WDT during Operating mode	0	1
WDT wake-up during Sleep mode	0	0
Wake-up on pin change during Sleep mode	1	0

****P:** *Previous status before reset*

The following shows the events that may affect the status of T and P.

Event	T	P
Power-on	1	1
WDTC instruction	1	1
WDT time-out	0	*P
SLEP instruction	1	0
Wake-up on pin changed during Sleep mode	1	0

****P:** *Previous value before reset*

6.6 Interrupt

The EM78P141 has seven interrupts as listed below**:**

1) TCC overflow interrupt
2) Port 5 Input Status Change Interrupt
3) External interrupt [(P52, /INT) pin]
4) Analog to Digital conversion completed
5) When TMR1/TMR2 matches with PRD1/PRD2 respectively in PWM
6) When the comparators output changes
7) Low voltage detector interrupt

Before the Port 5 Input Status Change Interrupt is enabled, reading Port 5 (e.g., "MOV R5, R5") is necessary. Each Port 5 pin will have this feature if its status changes. The Port 5 Input Status Change Interrupt will wake up the EM78P141 from Sleep mode if it is enabled prior to going into Sleep mode by executing SLEP instruction. When wake up occurs, the controller will continue to execute the succeeding program if the global interrupt is disabled. If enabled, it will branch out to the Interrupt Vector 006H.

External interrupt equipped with digital noise rejection circuit (input pulse less than system clocks time) is eliminated as noise. However, under Low Crystal oscillator (LXT) mode the noise rejection circuit will be disabled. Edge selection is possible with INTE of CONT. When an interrupt is generated by the External interrupt (when enabled), the next instruction will be fetched from Address 003H. Refer to the Word 0 Bits 4 (Section 6.13.1, *Code Option Register (Word 0)*) for digital noise rejection definition.

RF is the interrupt status register that records the interrupt requests in the relative flags/bits. IOCF0 is an interrupt mask register. The global interrupt is enabled by the ENI instruction and is disabled by the DISI instruction. When one of the interrupts (when enabled) occurs, the next instruction will be fetched from interrupt vector address. Once in the interrupt service routine, the source of an interrupt can be determined by polling the flag bits in RF. The interrupt flag bit must be cleared by instructions before leaving the interrupt service routine to avoid recursive interrupts.

When interrupt mask bits is "Enable", the flag in the Interrupt Status Register (RF) is set regardless of ENI execution. Note that the result of RF will be the logic AND of RF and IOCF0 (refer to figure below). The RETI instruction ends the interrupt routine and enables the global interrupt (the ENI execution).

When an interrupt is generated by the Timer clock/counter (when enabled), the next instruction will be fetched from Address 009, 012, 015 (TCC, Timer 1 and Timer 2, respectively).

When an interrupt is generated by the AD conversion completed status (when enabled), the next instruction will be fetched from Address 00CH.

When an interrupt is generated by the Comparators (when enabled), the next instruction will be fetched from Address 00FH (Comparator interrupt).

When an interrupt is generated during a Low Voltage Detect status (when enabled), the next instruction will be fetched from Address 018H (Low Voltage Detector interrupt).

Before an interrupt subroutine is executed, the contents of ACC and the R3 and R4 registers will be saved by the hardware. If another interrupt occurs, the ACC, R3, and R4 will be replaced by the new interrupt. After the interrupt service routine is completed, the ACC, R3, and R4 registers are restored.

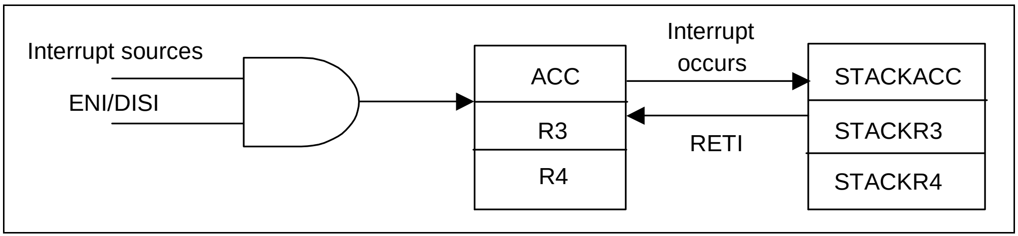


Figure 6-6a Interrupt Backup Diagram

In EM78P141, each individual interrupt source has its own interrupt vector as depicted in the table below.

Interrupt Vector	Interrupt Status	Priority
003H	External interrupt	2*
006H	Port 5 pin change	3*
009H	TCC overflow interrupt	4*
00CH	AD conversion complete interrupt	5*
00FH	Comparator interrupt	6*
012H	Timer 1 (PWM1) overflow interrupt	7*
015H	Timer 2 (PWM2) overflow interrupt	8*
018H	Low Voltage Detector interrupt	1*

** Priority: **1** = highest; **8** = lowest priority*

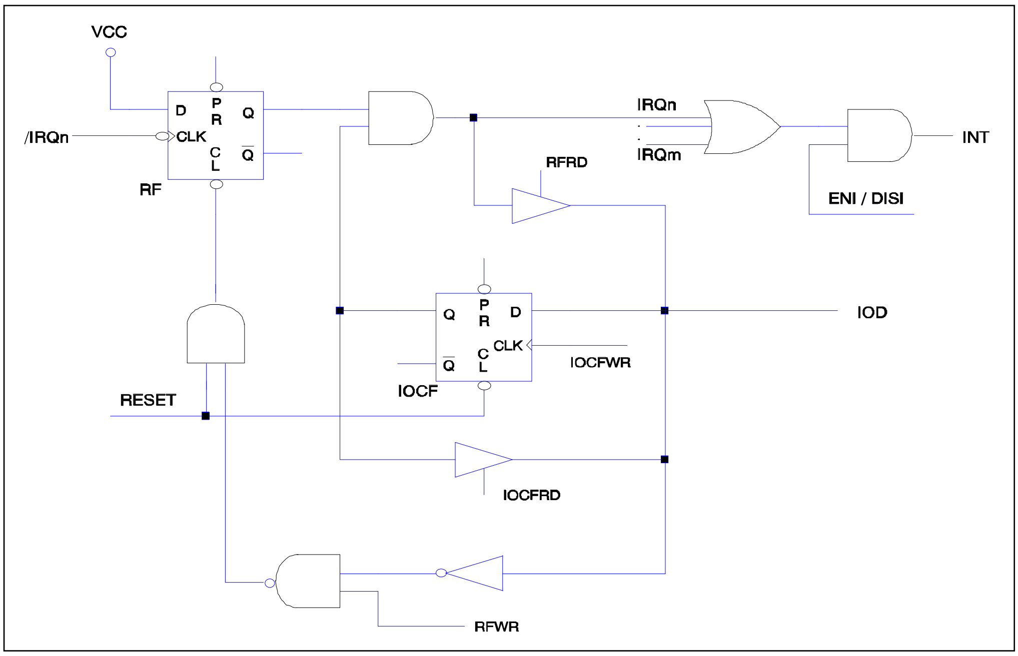


Figure 6-6b Interrupt Input Circuit

6.7 Analog-to-Digital Converter (ADC)

The analog-to-digital circuitry consist of an 8-bit analog multiplexer (7-channels); three control registers (AISR/R8, ADCON/R9, and ADOC/RA), two data registers (ADDATAH/RB, ADDATAL/RC), and an ADC with 10-bit resolution as shown in the functional block diagram below. The analog reference voltage (Vref) and the analog ground are connected via separate input pins. Connecting to the external VREF is more accurate than connecting to the internal VDD.

The ADC module utilizes successive approximation to convert the unknown analog signal into a digital value. The result is fed to the ADDATAH and ADDATAL. Input channels are selected by the analog input multiplexer via the ADCON register Bits ADIS2, ADIS1 and ADIS0.

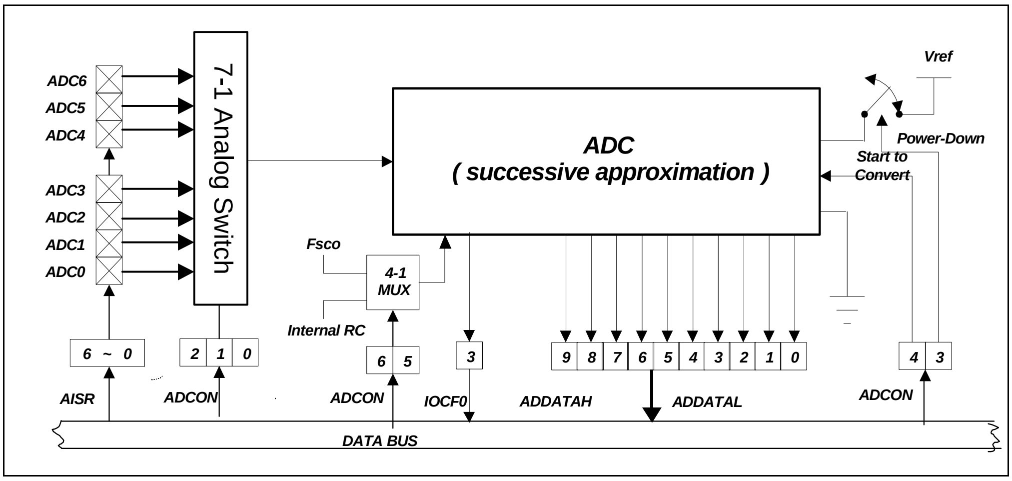


Figure 6-7 Analog-to-Digital Conversion Functional Block Diagram

6.7.1 ADC Control Register (AISR/R8, ADCON/R9, ADOC/RA)

6.7.1.1 R8 (AISR: ADC Input Select Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
–	ADE6	ADE5	ADE4	ADE3	ADE2	ADE1	ADE0

The **AISR** register individually defines the Port 5 pins as analog input or as digital I/O.

Bit 7: Not used bit. Read as "**0**" all the time

Bit 6 (ADE6): AD converter enable bit of P56 pin

0: Disable ADC6, P56 functions as I/O pin

1: Enable ADC6 to function as analog input pin

Bit 5 (ADE5): AD converter enable bit of P55 pin

0: Disable ADC5, P55 functions as I/O pin

1: Enable ADC5 to function as analog input pin

Bit 4 (ADE4): AD converter enable bit of P54 pin

0: Disable ADC4, P54 functions as I/O pin

1: Enable ADC4 to function as analog input pin

Bit 3 (ADE3): AD converter enable bit of P53 pin

0: Disable ADC3, P53 functions as I/O pin

1: Enable ADC3 to function as analog input pin

Bit 2 (ADE2): AD converter enable bit of P52 pin

0: Disable ADC2, P52 acts as I/O pin

1: Enable ADC2 to act as analog input pin

Bit 1 (ADE1): AD converter enable bit of P51 pin

0: Disable ADC1, P51 acts as I/O pin

1: Enable ADC1 to act as analog input pin

Bit 0 (ADE0): AD converter enable bit of P50 pin

0: Disable ADC0, P50 acts as I/O pin

1: Enable ADC0 to act as analog input pin

NOTE

- *The TCC, CO and AD5 of the P55/AD5/CO/TCC pins cannot be used at the same time.*
- *The P55/AD5/CO/TCC pin priority is as follows:*

P55/AD5/CO/TCC Priority			
Highest	High	Medium	Low
TCC	CO	AD5	P55

6.7.1.2 R9 (ADCON: AD Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
VREFS	CKR1	CKR0	ADRUN	ADPD	ADIS2	ADIS1	ADIS0

The **ADCON** register controls the operation of the AD conversion and determines which pin should be currently active.

Bit 7(VREFS): Input source of the ADC Vref

0: The ADC Vref is connected to Vdd (default value), and the P54/AD4/CIN-/VREF pin carries out the P54 function

1: The ADC Vref is connected to P54/VREF

NOTE

The P54/TCC/VREF pin cannot be applied to TCC and VREF at the same time.
The P54/TCC/VREF pin priority is as follows:

P54/TCC/VREF Pin Priority		
High	Medium	Low
VREF	TCC	P54

Bit 6 ~ Bit 5 (CKR1 ~ CKR0): The ADC prescaler oscillator clock rate

00 = 1**:** 16 (default value)

01 = 1**:** 4

10 = 1**:** 64

11 = 1**:** 8

CKR1: CKR0	Operation Mode	Max. Operating Frequency
00	Fosc/16	4 MHz
01	Fosc/4	1 MHz
10	Fosc/64	16 MHz
11	Fosc/8	2 MHz

Bit 4 (ADRUN): ADC starts to RUN.

0: Reset upon completion of the conversion. This bit cannot be reset by software.

1: AD conversion is started. This bit can be set by software.

Bit 3 (ADPD): ADC Power-down mode

0: Switch off the resistor reference to save power even while the CPU is operating.

1: ADC is operating

> **NOTE**
>
> *The ADPD bit must be enabled before enabling the ADRUN bit. The program process is shown in Section 6.7.6 (Programming Process/Considerations).*

Bit 2 ~ Bit 0 (ADIS2 ~ ADIS0): Analog Input Select

111 = unused

110 = ADIN1/P56

101 = ADIN5/P55

100 = ADIN4/P54

011 = ADIN3/P53

010 = ADIN2/P52

001 = ADIN1/P51

000 = ADIN0/P50

These bits can only be changed when the ADIF bit and the ADRUN bit are both Low.

6.7.1.3 RA (ADOC: AD Offset Calibration Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CALI	SIGN	VOF[2]	VOF[1]	VOF[0]	–	–	–

Bit 7 (CALI): Calibration enable bit for ADC offset

0: Calibration disabled

1: Calibration enabled

Bit 6 (SIGN): Polarity bit of offset voltage

0: Negative voltage

1: Positive voltage

Bit 5 ~ Bit 3 (VOF[2] ~ VOF[0]): Offset voltage bits

VOF[2]	VOF[1]	VOF[0]	EM78P141
0	0	0	0 LSB
0	0	1	1 LSB
0	1	0	2 LSB
0	1	1	3 LSB
1	0	0	4 LSB
1	0	1	5 LSB
1	1	0	6 LSB
1	1	1	7 LSB

Bit 2 ~ Bit 0: Not used bit. Read as "**0**" all the time

6.7.2 ADC Data Register (ADDATAH/RB, ADDATAL/RC)

When the AD conversion is completed, the result is loaded to the ADDATAH and ADDATAL registers. The ADRUN bit is cleared, and the ADIF is set.

6.7.3 ADC Sampling Time

The accuracy, linearity, and speed of the successive approximation of AD converter are dependent on the properties of the ADC and the comparator. The source impedance and the internal sampling impedance directly affect the time required to charge the sample holding capacitor. The application program controls the length of the sample time to meet the specified accuracy. Generally speaking, the program should wait for 2 µs for each KΩ of the analog source impedance; and at least 2 µs for the low- impedance source. The maximum recommended impedance for the analog source is 10 KΩ at Vdd=5V. After the analog input channel is selected, this acquisition time must be done before the conversion is started.

6.7.4 AD Conversion Time

CKR1 and CKR0 select the conversion time (Tct), in terms of instruction cycles. This allows the MCU to run at a maximum frequency without sacrificing the AD conversion accuracy. For the EM78P141, the conversion time per bit is about 4 µs. The table below shows the relationship between Tct and the maximum operating frequencies.

CKR1:CKR0	Operation Mode	Max. Operation Frequency	Max. Conversion Rate/Bit	Max. Conversion Rate
00	Fosc/16	4 MHz	250kHz (4 µs)	15×4 µs = 60 µs (16.7kHz)
01	Fosc/4	1 MHz	250kHz (4 µs)	15×4 µs = 60 µs (16.7kHz)
10	Fosc/64	16 MHz	250kHz (4 µs)	15×4 µs = 60 µs (16.7kHz)
11	Fosc/8	2 MHz	250kHz (4 µs)	15×4 µs = 60 µs (16.7kHz)

NOTE

- *Pin that is not used as an analog input pin, can be used as a regular input or output pin.*
- *During conversion, do not perform output instruction. This is to maintain ADC value precision for all the pins.*

6.7.5 ADC Operation during Sleep Mode

In order to obtain a more accurate ADC value and reduce power consumption, the AD conversion remains operational during Sleep mode. As the SLEP instruction is executed, all the MCU operations will stop except for the Oscillators, TCC, Timer 1, Timer 2, and AD conversion.

The AD Conversion is considered completed as determined by following factors**:**

1) ADRUN bit of R9 register is cleared ("**0**" value).
2) ADIF bit of RF register is set to "**1**".
3) ADWE bit of the IOCD1 register is set to "**1**." Wake-up from ADC conversion (where it remains in operation during Sleep mode).
4) Wake-up and executes the next instruction if ADIE bit of IOCF0 is enabled and the "DISI" instruction is executed..
5) Wake-up and enters into Interrupt vector (Address 0x0C) if ADIE bit of IOCF0 is enabled and the "ENI" instruction is executed.
6) Enters into Interrupt vector (Address 0x0C) if ADIE bit of IOCF0 is enabled and "ENI" instruction is executed.

The results are fed into the ADDATAH and ADDATAL registers when the conversion is completed. If the ADIE is enabled, the device will wake up. Otherwise, the AD conversion is shut off, no matter what the status of ADPD bit is.

6.7.6 Programming Process/Considerations

6.7.6.1 Programming Process

Follow these steps to obtain data from the ADC:

1. Write to the seven bits (ADE6:ADE0) on the R8 (AISR) register to define the characteristics of R5 (digital I/O, analog channels, or voltage reference pin).
2. Write to the R9/ADCON register to configure the AD module:
   a) Select the ADC input channel (ADIS2~ADIS0)
   b) Define the AD conversion clock rate (CKR1:CKR0)
   c) Select the VREFS input source of the ADC
   d) Set the ADPD bit to 1 to begin sampling
3. Set the ADWE bit if the wake-up function is employed

4. Set the ADIE bit if the interrupt function is employed
5. Write "ENI" instruction if the interrupt function is employed
6. Set the ADRUN bit to "**1**"
7. Write "SLEP" instruction or Polling
8. Wait for wake-up, ADRUN bit is cleared ("**0**" value)
9. Read the ADDATAH and ADDATAL conversion data registers. If the ADC input channel changes at this time, the ADDATAH and ADDATAL values can be cleared to "**0**".
10. Clear the interrupt flag bit (ADIF)
11. For the next conversion, go to Step 1 or Step 2 as required. At least 2 Tct is required before the next acquisition starts.

> **NOTE**
> *In order to obtain accurate values, it is necessary to avoid any data transition on the I/O pins during AD conversion.*

6.7.6.2 Sample Demo Programs

■ **Define a General Register**

```
R_0 == 0          ; Indirect addressing register
PSW == 3          ; Status register
PORT5 == 5
IOCD1== 0XD       ; Wake-up control register
RF == 0XF         ; Interrupt status register
```

■ **Define a Control Register**

```
IOC50 == 0X5      ; Control Register of Port 5
IOCF0== 0XF       ; Interrupt Control Register
```

■ **ADC Control Register**

```
ADDATAH == 0xB    ; The contents are the results of ADC
ADDATAL == 0XC    ; The contents are the results of ADC
AISR == 0x08      ; ADC input select register
ADCON == 0x9      ;  7     6    5    4     3    2     1     0
                  ; VREFS CKR1 CKR0 ADRUN ADPD ADIS2 ADIS1 ADIS0
```

■ **Define Bits in ADCON**

```
ADRUN == 0x4      ; ADC is executed as the bit is set
ADPD == 0x3       ; Power Mode of ADC
```

■ **Program Starts**

```
ORG 0              ; Initial address
JMP INITIAL

ORG 0x0C           ; Interrupt vector
;
;
;(User program section)
;
;
CLR RF                ; To clear the ADIF bit
BS ADCON, ADRUN       ; To start to execute the next AD conversion
                      ; if necessary

RETI
INITIAL:
MOV A,@0B00000001     ; To define P50 as an analog input
MOV AISR,A
MOV A,@0B00001000     ; To select P50 as an analog input channel, and
                      ; AD power on
MOV ADCON,A           ; To define P50 as an input pin and set
                      ; clock rate at fosc/16
En_ADC:
MOV A, @0BXXXXXXX1 ; To define P50 as an input pin, and the others
IOW PORT5             ; are dependent on applications


BS   R3,6             ; Select Segment 1
MOV A, @0BXXXXX1XX ; Enable the ADWE wake-up function of ADC, "X"
                      ; by application
IOW IOCD1
BC   R3,6             ; Select Segment 0
MOV A, @0BXXXX1XXX  ; Enable the ADIE interrupt function of ADC,
                        ; "X" by application
IOW IOCF0

ENI                   ; Enable the interrupt function

BS ADCON, ADRUN       ; Start to run the ADC
```

```
; If the interrupt function is employed, the following three lines
may be ignored
POLLING:
JBC ADCON, ADRUN    ; To check the ADRUN bit continuously;
JMP POLLING         ; ADRUN bit will be reset as the AD conversion
                    ; is completed
;
;
;(User program section)
;
;
```

6.8 Dual Sets of PWM (Pulse Width Modulation)

■ Register for the PWM Circuit

Page	Addr.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IOC51	0X05	**PWMCON**	**"0"**	**"0"**	**"0"**	**"0"**	**"0"**	**PWMCAS**	**PWM2E**	**PWM1E**
IOC61	0X06	**TMRCON**	**T2EN**	**T1EN**	**T2P2**	**T2P1**	**T2P0**	**T1P2**	**T1P1**	**T1P0**
IOC71	0X07	**PRD1**	**PRD1 [7]**	**PRD1 [6]**	**PRD1 [5]**	**PRD1 [4]**	**PRD1 [3]**	**PRD1 [2]**	**PRD1 [1]**	**PRD1 [0]**
IOC81	0X08	**PRD2**	**PRD2 [7]**	**PRD2 [6]**	**PRD2 [5]**	**PRD2 [4]**	**PRD2 [3]**	**PRD2 [2]**	**PRD2 [1]**	**PRD2 [0]**
IOC91	0X09	**DT1**	**DT1[7]**	**DT1[6]**	**DT1[5]**	**DT1[4]**	**DT1[3]**	**DT1[2]**	**DT1[1]**	**DT1[0]**
IOCA1	0X0A	**DT2**	**DT2[7]**	**DT2[6]**	**DT2[5]**	**DT2[4]**	**DT2[3]**	**DT2[2]**	**DT2[1]**	**DT2[0]**
R PAGE	0X0F	**ISR**	CMPIF	"0"	**PWM2IF**	**PWM1IF**	ADIF	EXIF	ICIF	TCIF
IOCF0	0X0F	**IMR**	CMPIE	"0"	**PWM2IE**	**PWM1IE**	ADIE	EXIE	ICIE	TCIE
-	-	**-**	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

6.8.1 Overview

In PWM mode, PWM1 and PWM2 pins produce up to 8-bit resolution PWM output (see the functional block diagram in Figure 6-8b next page). A PWM output consists of a time period and a duty cycle, and it keeps the output high. The baud rate of the PWM is the inverse of the time period. Figure below depicts the relationships between a time period and a duty cycle.

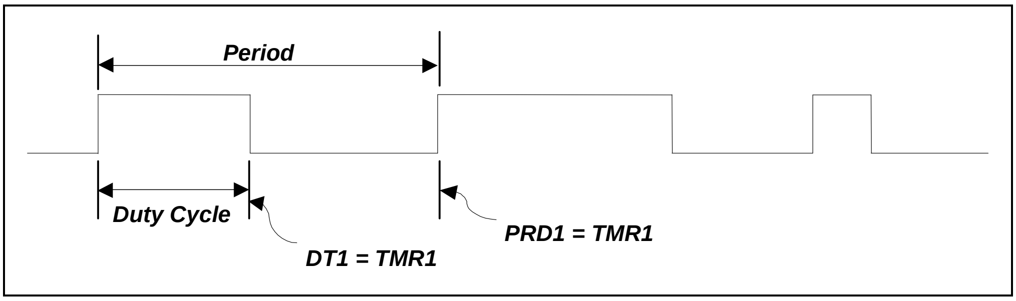


Figure 6-8a PWM Output Timing

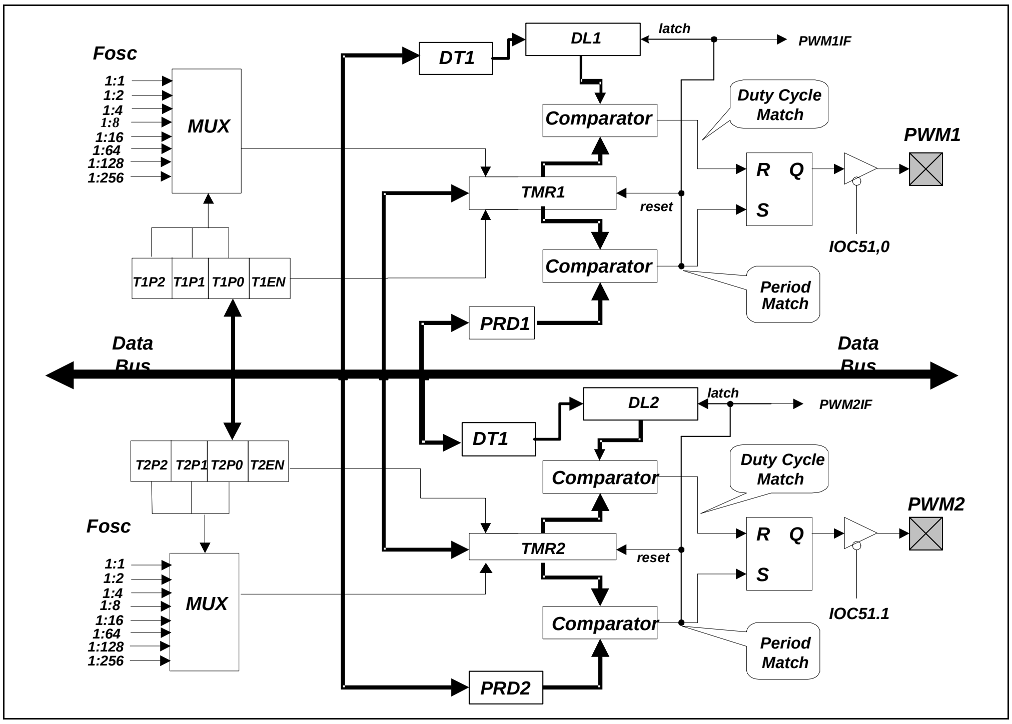


Figure 6-8b Two PWMs Functional Block Diagram

6.8.2 Increment Timer Counter (TMRX: TMR1 or TMR2)

TMRX are 8-bit clock counters with programmable prescalers. They are designed for the PWM module as baud rate clock generators. If employed, they can be turned off for power saving by setting the T1EN bit [IOC61<6>] or T2EN bit [IOC61<7>] to "**0**".

TMR1 and TMR2 are internal designs and cannot be read.

6.8.3 PWM Time Period (PRDX: PRD1 or PRD2)

The PWM time period is defined by writing to the PRDX register. When TMRX is equal to PRDX, the following events occur on the next increment cycle:

1) TMR is cleared
2) The PWMX pin is set to 1
3) The PWM duty cycle is latched from DT1/DT2 to DL1/DL2

NOTE
*The PWM output will not be set, if the duty cycle is "**0**".*

4) The PWMXIF pin is set to 1

The following formula describes how to calculate the PWM time period:

$$Period = (PRDX + 1) \times \left(\frac{1}{FOSC} \right) \times (TMRX \;\; prescale \; value)$$

Example:

PRDX=49; Fosc=4 MHz; TMRX (0, 0, 0) = 1:1,

then $Period = (49+1) \times \left(\frac{1}{4M}\right) \times 1 = 12.5$ **μS**

6.8.4 PWM Duty Cycle (DTX: DT1 or DT2; DLX: DL1 or DL2)

The PWM duty cycle is defined by writing to the DTX register, and is latched from DTX to DLX while TMRX is cleared. When DLX is equal to TMRX, the PWMX pin is cleared. DTX can be loaded anytime. However, it cannot be latched into DLX until the current value of DLX is equal to TMRX.

The following formula describes how to calculate the PWM duty cycle:

$$Duty\ Cycle = (DTX) \times \left(\frac{1}{F_{OSC}}\right) \times (TMRX\ \ prescale\ value)$$

Example:

DTX=10; Fosc=4 MHz; TMRX (0, 0, 0) = 1:1,

then $Duty\ Cycle = 10 \times \left(\frac{1}{4M}\right) \times 1 = 2.5$ **μS**

6.8.5 Comparator X

Changing the output status while a match occurs will simultaneously set the PWMXIF (TMRXIF) flag.

6.8.6 PWM Programming Process/Steps

Load PRDX with the PWM time period.

1. Load DTX with the PWM Duty Cycle.
2. Enable interrupt function by writing IOCF0, if required.
3. Set PWMX pin to be output by writing a desired value to IOC51.
4. Load a desired value to IOC61 with TMRX prescaler value and enable both PWMx and TMRX

6.8.7 PWM Cascade Mode

The PWM Cascade Mode merges two 8-bit PWM function into one 16-bit. In this mode, the necessary parameters are redefined as shown on the table below:

Paramete / 16-bit PWM	DT (Duty)	PRD (Period)	TMR (Timer)
MSB (15~8)	DT2	PRD2	TMR2
LSB (7~0)	DT1	PRD1	TMR1

The prescaler of this 16-bit PWM uses the prescaler of the TMR1. The MSB of TMR is counted when LSB carry and the PWM1IF bit/PWM1 pins are redefined as the PWMIF bit/PWM pin (or PWM1 pin).

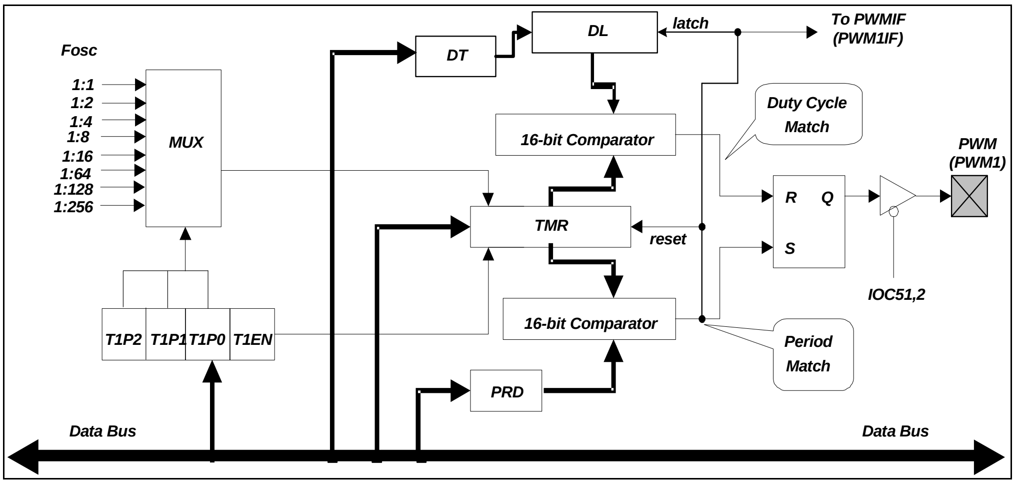


Figure 6-9 16-Bit PWM Functional Block Diagram (Merged from Two 8 Bits)

6.9 Timer

■ Register for the TIMER Circuit

PAGE	Addr.	NAME	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IOCB1	0X0B	**TMR1**	**TMR1[7]**	**TMR1[6]**	**TMR1[5]**	**TMR1[4]**	**TMR1[3]**	**TMR1[2]**	**TMR1[1]**	**TMR1[0]**
IOCC1	0X0C	**TMR2**	**TMR2[7]**	**TMR2[6]**	**TMR2[5]**	**TMR2[4]**	**TMR2[3]**	**TMR2[2]**	**TMR2[1]**	**TMR2[0]**

6.9.1 Overview

Timer 1 (TMR1) and Timer 2 (TMR2) (TMRX) are 8-bit clock counters with programmable prescalers. They are designed for the PWM module as baud rate clock generators. TMRX can be read only. The Timer 1 and Timer 2 will stop running when sleep mode occurs with AD conversion not running. However, if AD conversion is running when sleep mode occurs, the Timer 1 and Timer 2 will keep on running.

6.9.2 Function Description

The following figure shows the TMRX block diagram followed by descriptions of its signals and blocks.

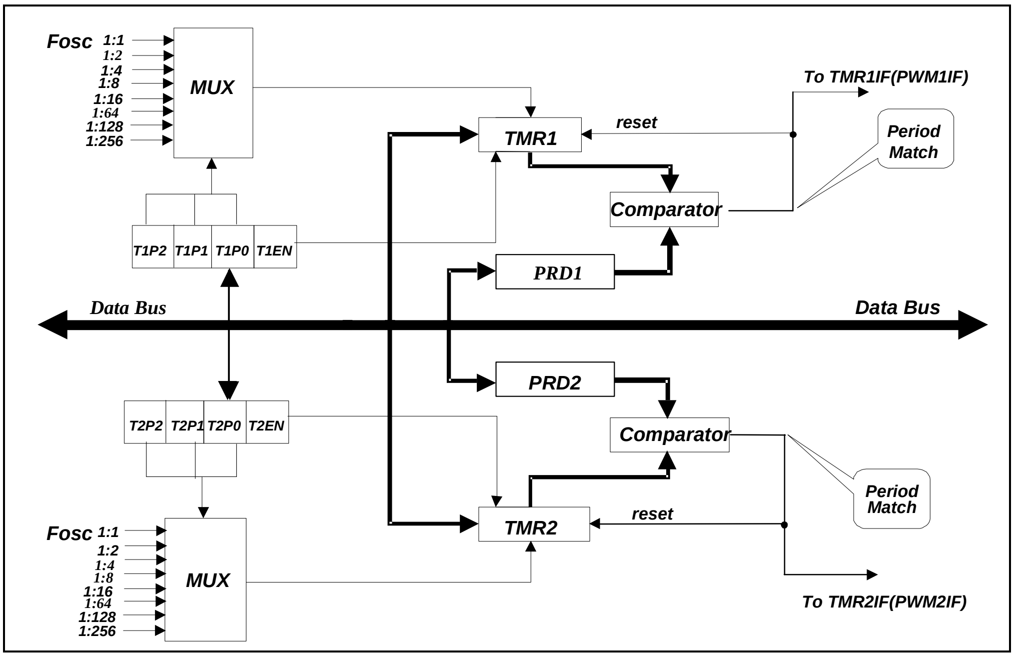


Figure 6-10 TMRX Block Diagram

Where**:**

Fosc: Input clock.

Prescaler (T1P2, T1P1 and T1P0 / T2P2, T2P1 and T2P0): The options 1**:**1, 1**:**2, 1**:**4, 1**:**8, 1**:**16, 1**:**64, 1**:**128, and 1**:**256 are defined by TMRX. It is cleared when any type of reset occurs.

TMR1 and TMR2: Timer X register. TMRX is increased until it matches with PRDX, and then is reset to "**0**" (default value).

PRDX (PRD1, PRD2): PWM time period register

Comparator X (Comparator 1 and Comparator 2): Reset TMRX while a match occurs. The TMRXIF (PWMXIF) flag is set at the same time.

6.9.3 Programming the Related Registers

When defining TMRX, refer to the operation of its related registers as shown in the following table. It must be noted that the PWMX bits must be disabled if their related TMRXs are utilized. That is, Bit 7 ~ Bit 3 of the PWMCON register must be set to "**0**".

■ Related Control Registers of TMR1 and TMR2

Addr.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IOC51	PWMCON/IOC51	"0"	"0"	"0"	"0"	"0"	PWMCAS	PWM2E	PWM1E
IOC61	TMRCON/IOC61	T2EN	T1EN	T2P2	T2P1	T2P0	T1P2	T1P1	T1P0

6.9.4 Timer Programming Process/Steps

1. Load PRDX with the Timer duration
2. Enable interrupt function by writing IOCF0, if required
3. Load a desired value for the TMRX prescaler and enable TMRX and disable PWMX

6.9.5 Timer Cascade Mode

The Timer Cascade Mode merges two 8-bit Timer functions into one 16-bit. In this mode, the necessary parameters are redefined as shown in the table below.

Parameter / 16-bit Timer	PRD (Period)	TMR (Timer)
MSB(15~8)	PD2	TMR2
LSB (7~0)	PD1	TMR1

The prescaler of the 6-bit Timer uses the prescaler of the TMR1. The MSB of TMR is counted when LSB carry and the PWM1IF bit/PWM1 pin are redefined as the PWMIF bit/PWM pin (or PWM1 pin).

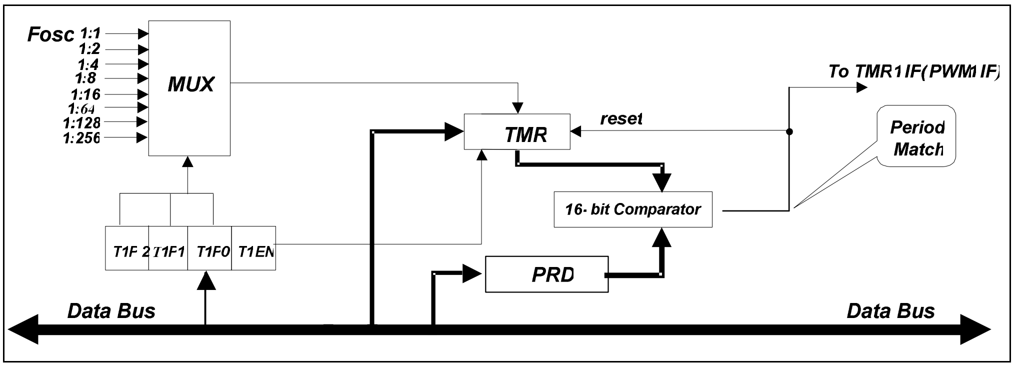


Figure 6-11 16-Bit Timer Functional Block Diagram (Merged from Two 8-Bit Timers)

6.10 Comparator

■ Register for the Comparator Circuit

PAGE	Addr.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IOC90	0X09	**CMPCON**	**/IVRE**	**VRE3**	**VRE2**	**VRE1**	**VRE0**	**CPOUT**	**COS1**	**COS0**
R PAGE	0X0F	**ISR**	**CMPIF**	"0"	PWM2IF	PWM1IF	ADIF	EXIF	ICIF	TCIF
IOCF0	0X0F	**IMR**	**CMPIE**	"0"	PWM2IE	PWM1IE	ADIE	EXIE	ICIE	TCIE
IOCD1	0X0D	**WUCR**	"0"	"0"	"0"	"0"	"0"	ADWE	**CMPWE**	ICWE

The EM78P141 has one comparator which has two analog inputs and one output. The comparator can be employed to wake up the system from Sleep/Idle mode. The comparator circuit diagram is depicted in the following figure.

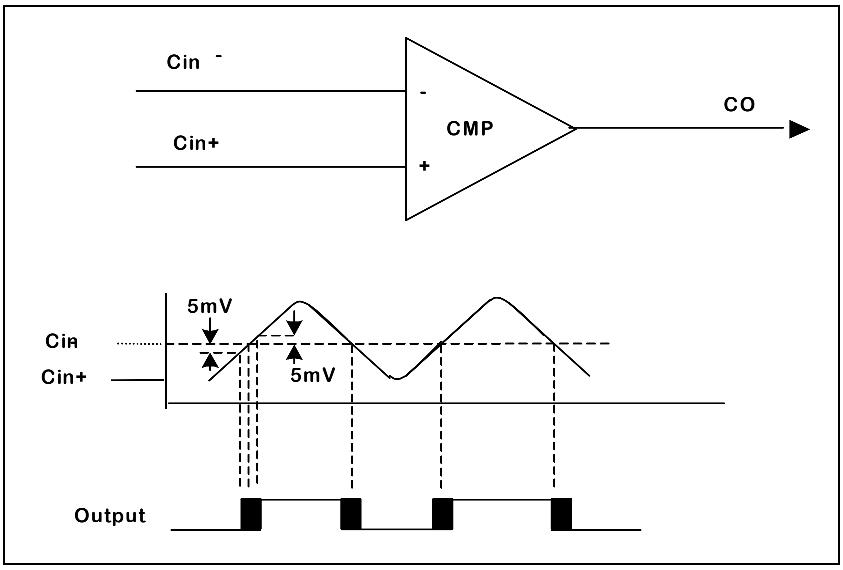


Figure 6-12 Comparator Circuit Diagram and Operating Mode

6.10.1 Comparator Reference Signal

The analog signal that is presented at Cin– is compared to the signal at Cin+, and the digital output (CO) of the comparator is adjusted accordingly by taking the following notes into considerations:

- The reference signal must be located between Vss and Vdd.
- The reference voltage can be applied to either pin of the comparator.

Furthermore, the Cin– signal path can be set using the internal reference voltage through /IVRE bit, and with the VRE3 ~ VRE0 bits as the reference voltage ratio.

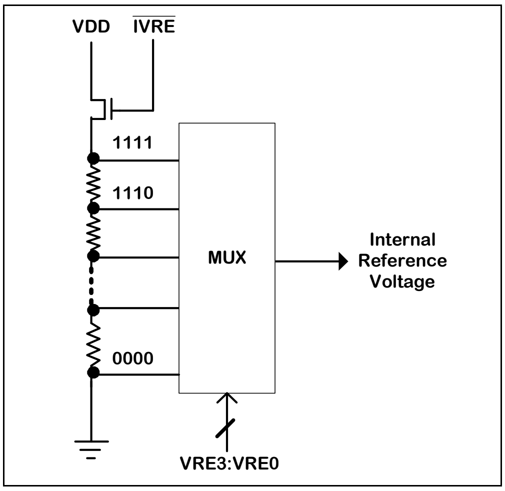


Figure 6-13 Comparator Trim Equivalent Circuit

■ VRE3 ~ VRE0 bits reference voltage ratio:

VRE3	VRE2	VRE1	VRE0	Voltage Reference Value
0	0	0	0	0
0	0	0	1	VDD × 1/15
0	0	1	0	VDD × 2/15
0	0	1	1	VDD × 3/15
0	1	0	0	VDD × 4/15
0	1	0	1	VDD × 5/15
0	1	1	0	VDD × 6/15
0	1	1	1	VDD × 7/15
1	0	0	0	VDD × 8/15
1	0	0	1	VDD × 9/15
1	0	1	0	VDD × 10/15
1	0	1	1	VDD × 11/15
1	1	0	0	VDD × 12/15
1	1	0	1	VDD × 13/15
1	1	1	0	VDD × 14/15
1	1	1	1	VDD (default)

NOTE

- *The P54/AD4/CIN-/VREFS pin cannot be applied to VREFS, CIN- and AD4 at the same time.*
- *The P54/AD4/CIN-/VREFS pin priority is as follows:*

P54/AD4/CIN-/VREF Pin Priority			
Highest	High	Medium	Low
VREF	CIN-	AD4	P54

- *The P53/AD3/CIN+ pin cannot be applied to CIN+ and AD3 at the same time.*
- *The P53/AD3/CIN+ pin priority is as follows:*

P53/AD3/CIN+		
High	Medium	Low
CIN+	AD3	P53

6.10.2 Comparator Outputs

- The compared result is stored in the CMPOUT of IOC90.
- The comparator output are sent to CO (P55) by programming Bit 1, Bit 0<COS1, COS0> of the IOC90 register to <1, 0>. See Section 6.2.7, *IOC90 (CMPCON: Comparator Control Register)* for Comparator select bits function description.

NOTE

- *The TCC, CO and AD5 of the P55/AD5/CO/TCC pins cannot be used at the same time.*
- *The P55/AD5/CO/TCC pin priority is as follows:*

P55/AD5/CO/TCC Priority			
Highest	High	Medium	Low
TCC	CO	AD5	P55

The following figure shows the Comparator Output block diagram.

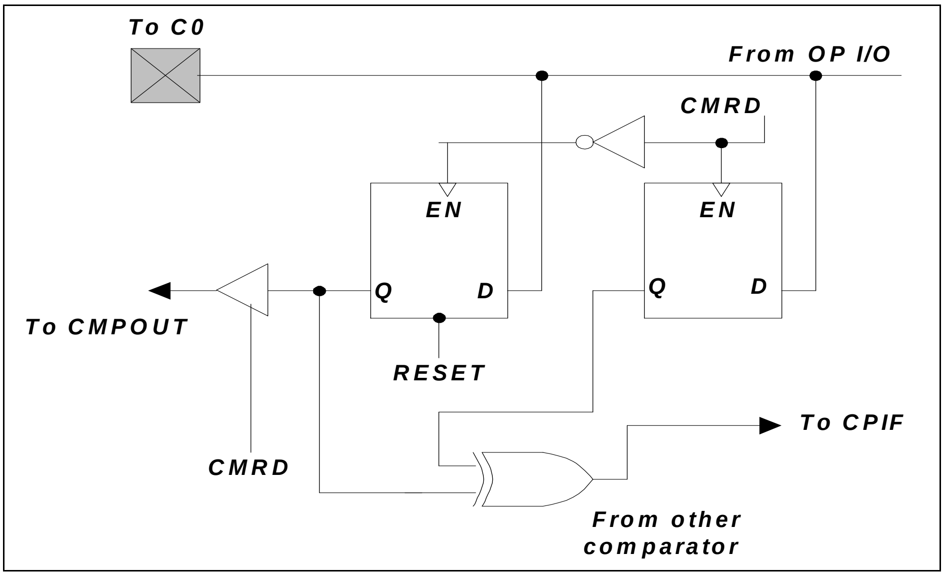


Figure 6-14 Comparator Output Configuration

6.10.3 Comparator Interrupt

- CMPIE (IOCF0.7) must be enabled for the "ENI" instruction to take effect.
- Interrupt is triggered whenever a change occurs on the comparator output pin.
- The actual change on the pin can be determined by reading the Bit CMPOUT, IOC90 <2>.
- CMPIF (RF.7), the comparator interrupt flag, can only be cleared by software.

6.10.4 Wake-up from Sleep Mode

- If enabled, the comparator remains active and the interrupt remains functional even while in Sleep mode.
- If a mismatch occurs, the interrupt will wake up the device from Sleep mode.
- The power consumption should be taken into consideration for the benefit of energy conservation.
- If the function is not employed during Sleep mode, turn off the comparator before going into Sleep mode.

6.11 Oscillator

6.11.1 Oscillator Modes

The EM78P141 can be operated in four different oscillator modes, such as**:**

- High Crystal oscillator mode (HXT),
- Low Crystal oscillator mode (LXT),
- External RC oscillator mode (ERC), and
- RC oscillator mode with Internal RC oscillator mode (IRC)

You can select one of these modes by programming the OSC3, OSC2, OCS1, and OSC0 in the Code Option register as shown below.

Oscillator Mode	OSC3	OSC2	OSC1	OSC0
ERC[1] (External RC oscillator mode); P51/OSCO act P51	0	0	0	0
ERC[1] (External RC oscillator mode); P51/OSCO act OSCO	0	0	0	1
IRC[2] (Internal RC oscillator mode); P51/OSCO act P51	0	0	1	0
IRC[2] (Internal RC oscillator mode); P51/OSCO act OSCO	0	0	1	1
LXT1 (Frequency range of LXT1 mode is 100kHz~1 MHz)	0	1	0	0
HXT1 (Frequency range of HXT1 mode is 12 MHz~16 MHz)	0	1	0	1
LXT2 (Frequency LXT2 mode is 32kHz)	0	1	1	0
HXT2 (Frequency range of HXT2 mode is 6 MHz~12 MHz)	0	1	1	1
XT (Frequency range of XT mode is 1 MHz~6 MHz) (default)	1	1	1	1

[1] In ERC mode, P50 is OSCI pin. P51 is defined by Code Option Word 1 Bit 4~Bit 1.
[2] In IRC mode, P50 is normal I/O pin. P51 is defined by Code Option Word 1 Bit 4~Bit 1.

The maximum operating frequency limit of crystal/resonator at different VDDs, are as follows:

Conditions	VDD	Max. Freq. (MHz)
Two clocks	2.1	4
	4.5	16

6.11.2 Crystal Oscillator/Ceramic Resonators (Crystal)

The EM78P141 can be driven by an external clock signal through the OSCI pin as illustrated at right.

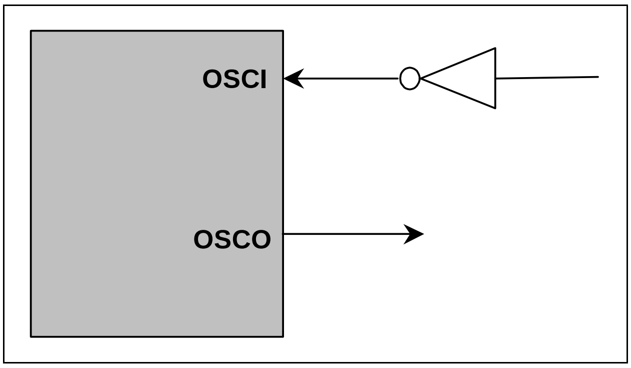


Figure 6-15a External Clock Input Circuit

In most applications, Pin OSCI and Pin OSCO can be connected with a crystal or ceramic resonator to generate oscillation. Figure at right depicts such a circuit. The same applies to the HXT mode and the LXT mode.

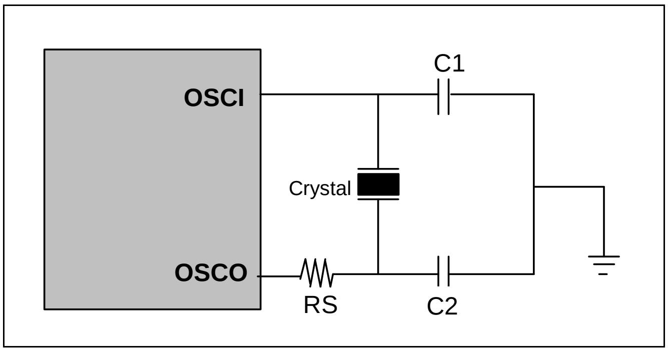


Figure 6-15b Crystal/Resonator Circuit

The following table provides the recommended values for C1 and C2. Since each resonator has its own attribute, you should refer to the resonator specifications for the appropriate values of C1 and C2. RS, a serial resistor, may be required for AT strip cut crystal or low frequency mode.

■ Capacitor selection guide for crystal oscillator or ceramic resonators**:**

Oscillator Type	Frequency Mode	Frequency	C1 (pF)	C2 (pF)
Ceramic Resonators	HXT	455kHz	100~150	100~150
		2.0 MHz	20~40	20~40
		4.0 MHz	10~30	10~30
Crystal Oscillator	LXT	32.768kHz	33~68	33~68
		100kHz	25	25
		200kHz	25	25
	HXT	455kHz	20~40	20~150
		1.0 MHz	15~30	15~30
		2.0 MHz	15	15
		4.0 MHz	15	15

6.11.3 External RC Oscillator Mode

For some applications that do not require precise timing calculation, the RC oscillator (figure at right) could offer you with effective cost savings. Nevertheless, it should be noted that the frequency of the RC oscillator is influenced by the supply voltage, the values of the resistor (Rext), the capacitor (Cext), and even by the operation temperature. Moreover, the frequency also changes slightly from one chip to another due to manufacturing process variation.

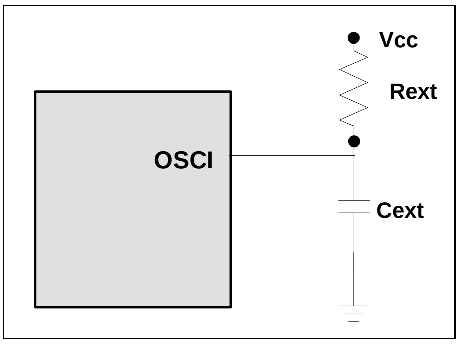


Figure 6-16 External RC Oscillator Mode Circuit

In order to maintain a stable system frequency, the values of the Cext should be no less than 20pF, and that of Rext should be no greater than 1 MΩ. If the frequency cannot be kept within this range, the frequency can be affected easily by noise, humidity, and leakage.

The smaller the Rext in the RC oscillator is, the faster its frequency will be. On the contrary, for very low Rext values, for instance, 1 KΩ, the oscillator will become unstable because the NMOS cannot discharge the capacitance current correctly.

Based on the above logic, it must be kept in mind that all supply voltage, the operation temperature, the components of the RC oscillator, the package types, and the way the PCB is layout, have certain effect on the system frequency.

■ The RC Oscillator frequencies:

Cext	Rext	Average Fosc 5V, 25°C	Average Fosc 3V, 25°C
20 pF	3.3k	3.5 MHz	3.0 MHz
	5.1k	2.4 MHz	2.2 MHz
	10k	1.27 MHz	1.24 MHz
	100k	140 KHz	143 kHz
100 pF	3.3k	1.21 MHz	1.18 MHz
	5.1k	805 kHz	790 kHz
	10k	420 kHz	418 kHz
	100k	45 kHz	46 kHz
300 pF	3.3k	550 kHz	526 kHz
	5.1k	364 kHz	350 kHz
	10k	188 kHz	185 kHz
	100k	20 kHz	20 kHz

NOTE

- *The values are for design reference only.*
- *The frequency drift is ±30%.*

6.11.4 Internal RC Oscillator Mode

The EM78P141 offers a versatile internal RC mode with default frequency value of 4 MHz. Other available frequencies, i.e., 4 MHz, 16 MHz, 8 MHz, and 455kHz; can be set through Code Option (Word 1), RCM1, and RCM0. The next table describes the EM78P141 internal RC drift with voltage, temperature, and process variation.

■ Internal RC Drift Rate (Ta=25°C, VDD=5V ± 5%, VSS=0V)

Internal RC Frequency	Drift Rate			
	Temperature (0°C ~ +70°C)	Voltage (2.3V~5.5V)	Process	Total
4 MHz	± 3%	± 5%	± 3%	± 11%
16 MHz	± 3%	± 5%	± 3%	± 11%
8 MHz	± 3%	± 5%	± 3%	± 11%
455kHz	± 3%	± 5%	± 3%	± 11%

NOTE

These are theoretical values provided for reference only. Actual values may vary depending on the actual process.

6.12 Power-On Considerations

Any microcontroller is not warranted to start operating properly before the power supply stabilizes to a steady state. The EM78P141 has a built-in Power-on Voltage Detector (POVD) with detection level range of 1.7V ~ 1.9V. The circuitry eliminates the extra external reset circuit. It will work well if Vdd rises fast enough (50 ms or less). However, under critical applications, extra devices are still required to assist in solving power-on problems.

6.12.1 Programmable WDT Time-out Period

The Option word (WDTPS) is used to define the WDT time-out period (18 ms[5] or 4.5 ms[6]). Theoretically, the range is from 4.5 ms or 18 ms. For most crystal or ceramic resonators, the lower the operation frequency is, the longer is the required set-up time.

6.12.2 External Power-on Reset Circuit

The circuit shown in the following figure implements an external RC to produce a reset pulse. The pulse width (time constant) should be kept long enough to allow Vdd to achieve the minimum operating voltage. This circuit is applicable when the power supply has a slow power rise time. Since the current leakage from the /RESET pin is about ±5µA, it is recommended that R should not be greater than 40K. This way, the voltage at Pin /RESET is held at below 0.2V. The diode (D) acts as a short circuit at power-down. The “C” capacitor is discharged rapidly and fully. Rin, the current-limited resistor, prevents high current discharge or ESD (electrostatic discharge) from flowing into Pin /RESET.

[5] VDD=5V, WDT time-out period = 16.5 ms ± 30%.
VDD=3V, WDT time-out period = 18 ms ± 30%.

[6] VDD=5V, WDT time-out period = 4.2 ms ± 30%.
VDD=3V, WDT time-out period = 4.5 ms ± 30%.

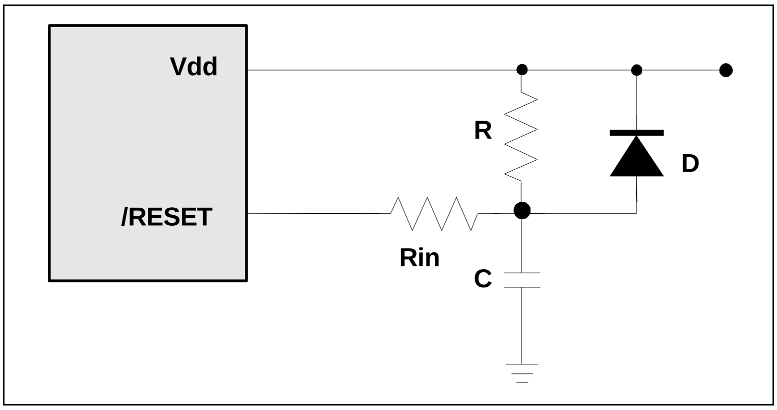


Figure 6-17 External Power-on Reset Circuit

6.12.3 Residual Voltage Protection

When the battery is replaced, device power (Vdd) is removed but the residual voltage remains. The residual voltage may trip below Vdd minimum, but not to zero. This condition may cause a poor power-on reset. The following two figures show how to create a protection circuit against residual voltage.

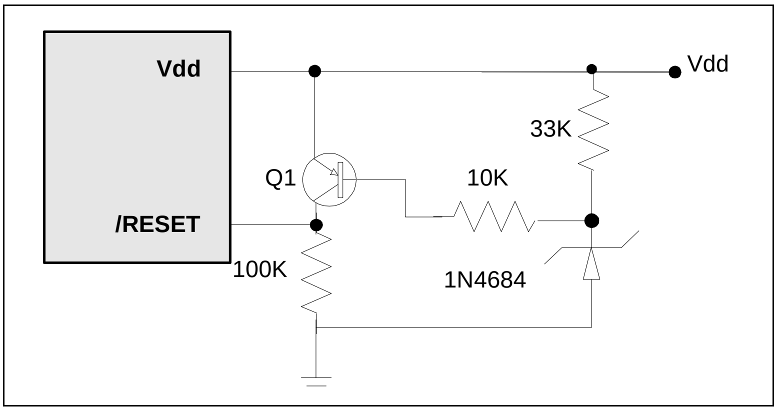


Figure 6-18a Residual Voltage Protection Circuit 1

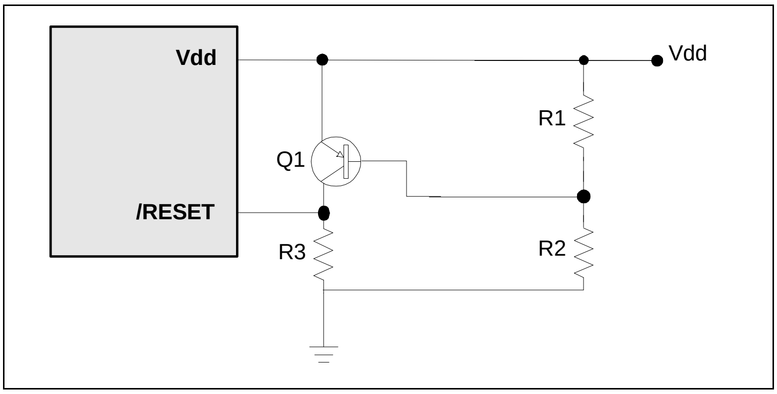


Figure 6-18b Residual Voltage Protection Circuit 2

6.13 Code Option

EM78P141 has two Code Option Words and one Customer ID word that are not part of the normal program memory.

Word 0	Word 1	Word 2
Bit 12 ~ Bit 0	Bit 12 ~ Bit 0	Bit 12 ~ Bit 0

6.13.1 Code Option Register (Word 0)

Word 0													
Bit	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mnemonic	–	–	CLKS	–	LVR1	LVR0	RESETENB	ENWDTB	NRHL	NRE	Protect		
1	–	–	4clocks	–	High	High	P57	Disable	32/fc	Enable	Disable		
0	–	–	2clocks	–	Low	Low	/RESET	Enable	8/fc	Disable	Enable		

Bits 12~11: Not used (reserved). This bit is set to "**1**" all the time.

Bit 10 (CLKS): Instruction period option bit

0: Two oscillator periods

1: Four oscillator periods (default)

Refer to Section 6.15 for Instruction Set

Bit 9: Not used (reserved). This bit is set to "**1**" all the time.

Bits 8~7 (LVR1 ~ LVR0): Low Voltage Reset enable bits

LVR1, LVR0	VDD Reset Level	VDD Release Level
11	NA (Power-on Reset) (Default)	
10	2.7V	2.9V
01	3.5V	3.7V
00	4.0V	4.2V

Bit 6 (RESETENB): RESET/P57 Pin Select Bit

0: P57 set to /RESET pin

1: P57 is general purpose input pin or open-drain for output port (default)

Bit 5 (ENWDTB): Watchdog timer enable bit

0: Enable

1: Disable (default)

Bit 4 (NRHL): Noise rejection high/low pulses defined bit. INT pin is a falling edge or rising edge trigger

0: Pulses equal to 8/fc [s] is regarded as signal

1: Pulses equal to 32/fc [s] is regarded as signal (default)

> **NOTE**
> *The noise rejection function is turned off in LXT2 and Sleep mode.*

Bit 3 (NRE): Noise rejection enable

0: Disable noise rejection

1: Enable noise rejection (default)

However, under Low Crystal oscillator (LXT2) mode, Green mode, and Idle mode, the noise rejection circuit is always disabled.

Bits 2~0 (PR2~PR0): Protect Bit

0: Enable

1: Disable

6.13.2 Code Option Register (Word 1)

Word 1													
Bit	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mnemonic	HLP	C4	C3	C2	C1	C0	RCM1	RCM0	OSC3	OSC2	OSC1	OSC0	RCOUT
1	High	High	High	High	High	High	High	High	High	High	High	High	System_clk
0	Low	Low	Low	Low	Low	Low	Low	Low	Low	Low	Low	Low	Open-drain

Bit 12 (HLP): Power consumption selection.

0: Low power consumption mode, applies to operating frequency at 32kHz or below 32kHz

1: High power consumption mode, applies to operating frequency above 32kHz (default)

Bits 11~7 (C4, C3, C2, C1 and C0): Calibrator of internal RC mode. These bits must be set to "**1**" only (auto calibration)

Bit 6 and Bit 5 (RCM1 and RCM0): RC mode select bits

RCM 1	RCM 0	Frequency (MHz)
1	1	4 (default)
1	0	16
0	1	8
0	0	455kHz

Bits 4~1 (OSC3~OSC0): Oscillator mode select bits

Oscillator Mode	OSC3	OSC2	OSC1	OSC0
ERC[1] (External RC oscillator mode) ; P51/OSCO act P51	0	0	0	0
ERC[1] (External RC oscillator mode) ; P51/OSCO act OSCO	0	0	0	1
IRC[2] (Internal RC oscillator mode) ; P51/OSCO act P51	0	0	1	0
IRC[2] (Internal RC oscillator mode) ; P51/OSCO act OSCO	0	0	1	1
LXT1 (Frequency range of LXT1 mode is 100kHz~1 MHz)	0	1	0	0
HXT1 (Frequency range of HXT1 mode is 12 MHz~16 MHz)	0	1	0	1
LXT2 (Frequency LXT2 mode is 32kHz)	0	1	1	0
HXT2 (Frequency range of HXT2 mode is 6 MHz~12 MHz)	0	1	1	1
XT (Frequency range of XT mode is 1 MHz~6 MHz) (default)	1	1	1	1

[1] *In ERC mode, P50 is OSCI pin, P51 is defined by Code Option Word 1 Bit 4~Bit 1.*
[2] *In IRC mode, P50 is normal I/O pin, P51 is defined by Code Option Word 1 Bit 4~Bit 1.*

Bit 0 (RCOUT): System Clock Output Enable Bit in IRC or ERC mode

0: OSCO pin is open drain

1: OSCO output system clock (default)

6.13.3 Customer ID Register (Word 2)

Word 2													
Bit	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mnemonic	-	-	-	-	WDTPS	-	ID6	ID5	ID4	ID3	ID2	ID1	ID0
1	-	-	-	-	18ms	-	High	High	High	High	High	High	High
0	-	-	-	-	4.5ms	-	Low	Low	Low	Low	Low	Low	Low

Bits 12~ 9: Fixed to "**1**"

Bit 8 (WDTPS): WDT Time-out Period Selection bit

WDT Time	Watchdog Timer
1	18 ms (Default)*
0	4.5 ms*

* *Theoretical values, for reference only*

Bit 7: Fixed to "**1**"

Bits 6 ~ 0: Customer's ID code

6.14 Low Voltage Detector

When an unstable power source condition occurs, such as external power noise interference or EMS test condition, a violent power vibration is generated. At the same time, the Vdd becomes unstable as it could be operating below working voltage. When the system supply voltage (Vdd) is below the operating voltage, the IC kernel will automatically keep all register status.

6.14.1 Low Voltage Reset (LVR)

LVR property is set at Bits 8 and 7 of Code Option Word 0. Detailed operation mode is as follows**:**

Word 0												
Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	CLKS	-	LVR1	LVR0	RESETENB	ENWDTB	NRHL	NRE	Protect		

Bits 8~7 (LVR1 ~ LVR0): Low Voltage Reset enable bits

LVR1, LVR0	VDD Reset Level	VDD Release Level
11	N/A (Power-on Reset)	
10	2.7V	2.9V
01	3.5V	3.7V
00	4.0V	4.2V

6.14.2 Low Voltage Detector (LVD)

LVD property is set at Registers R6. Detailed operation mode is explained below.

6.14.2.1 R6 (LVD Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	LVDIF	/LVD	LVDIE	LVDWE	LVDEN	LVD1	LVD0

NOTE

- *The R6 <4> register is both readable and writable.*
- *Individual interrupt is enabled by setting its associated control bit in the R6<4> to "**1**."*
- *Global interrupt is enabled by the ENI instruction and is disabled by the DISI instruction. Refer to Figure 6-6b (Interrupt Input Circuit) in Section 6.6 (Interrupt).*

Bit 6 (LVDIF): Low Voltage Detector Interrupt Flag

LVDIF is reset to "**0**" by software or hardware

Bit 5 (/LVD): Low voltage Detector state. This is a read only bit. When the VDD pin voltage is lower than the LVD voltage interrupt level (selected by LVD1 and LVD0), this bit will be cleared.

0: Low voltage is detected.

1: Low voltage is not detected or LVD function is disabled.

Bit 4 of R6: **"1" means there's interrupt request, and "0" means no interrupt occurs.**

Bit 4 (LVDIE): Low voltage Detector interrupt enable bit

0: Disable Low Voltage Detector interrupt

1: Enable Low Voltage Detector interrupt

When a detect low level voltage state is used to enter an interrupt vector or enter the next instruction, the LVDIE bit must be set to "Enable."

Bit 3 (LVDWE): Low Voltage Detect wake-up enable bit

0: Disable Low Voltage Detect wake-up

1: Enable Low Voltage Detect wake-up

When the Low Voltage Detect is used to enter interrupt vector or to wake-up IC from Sleep/Idle mode with the Low Voltage Detect running, the LVDWE bit must be set to "Enable."

Bit 2 (LVDEN): Low Voltage Detector enable bit

0: Low voltage detector disable

1: Low voltage detector enable.

Bits 1~0 (LVD1:0): Low Voltage Detector level bits

LVDEN	LVD1, LVD0	LVD Voltage Interrupt Level	/LVD
1	11	Vdd ≤ 2.2V	0
		Vdd > 2.2V	1
1	10	Vdd ≤ 3.3V	0
		Vdd > 3.3V	1
1	01	Vdd ≤ 4.0V	0
		Vdd > 4.0V	1
1	00	Vdd ≤ 4.5V	0
		Vdd > 4.5V	1
0	××	NA	1

6.14.3 Programming Process

Follow these steps to obtain data from the LVD:

1. Write to the two bits (LVD1: LVD0) on the R6 (LVDCR) register to define the LVD level
2. Set the LVDWE bit if the wake-up function is in use.
3. Set the LVDIE bit if the interrupt function is in use.
4. Write "ENI" instruction if the interrupt function is in use.
5. Set LVDEN bit to "**1**"
6. Write "SLEP" instruction or Polling /LVD bit
7. Clear the interrupt flag bit (LVDIF) when Low Voltage Detect occurs.

NOTE

- *The internal LVD module uses the internal circuit, and when the code option is set to enable the LVD module, the current consumption will increase to about 5 µA.*
- *During Sleep mode, the LVD module continues to operate. If the device voltage drops slowly and crosses the detection point, the LVDIF bit will be set and the device will wake up from Sleep mode. The LVD interrupt flag will remain set at priority status.*
- *When the system resets, the LVD flag is cleared.*

The following figure shows the LVD module detection point in an external voltage condition.

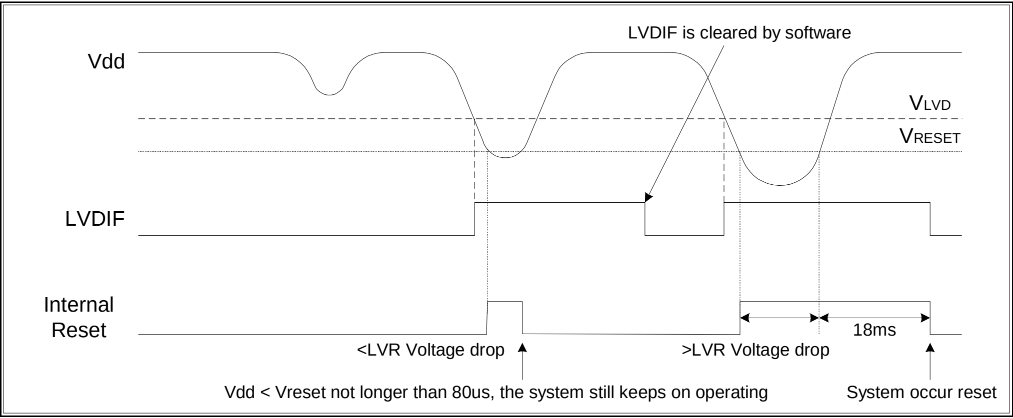


Figure 6-19 LVD/LVR Waveform with the Detection Point in an External Voltage Condition

- When the Vdd drops, but above VLVD, the LVDIF is kept at "**0**".
- When Vdd drops below VLVD, the LVDIF is set to "**1**". If global ENI is enabled, the LVDIF is also set to "**1**" and the next instruction will branch to an interrupt vector. The LVD interrupt flag is cleared to "**0**" by software.
- When Vdds drops below VRESET at less than 80µs, the system will keep all the registers' status and halts it operation, but with the oscillation remaining active.
- When Vdd drops below VRESET at more than 80µs, a system reset will occur. Refer to Section 6.5.1, *Reset and Wake-up Operation*; for the detailed Reset description.

6.15 Instruction Set

Each instruction in the instruction set is a 13-bit word divided into an OP code and one or more operands. Normally, all instructions are executed within one single instruction cycle (one instruction consists of 2 oscillator periods), unless the program counter is changed by instructions "MOV R2,A"; "ADD R2,A"; or by instructions of arithmetic or logic operation on R2 (e.g., "SUB R2,A"; "BS(C) R2,6"; "CLR R2"; etc.).

In addition, the instruction set has the following features**:**

1) Every bit of any register can be set, cleared, or tested directly.
2) The I/O registers can be regarded as general registers. That is, the same instruction can operate on I/O registers.

■ EM78P141 Instruction Set Table

In the following Instruction Set table, the following symbols are used**:**

"**R**" *represents a register designator that specifies which one of the registers (including operational registers and general purpose registers) is to be utilized by the instruction.*

"**b**" *represents a bit field designator that selects the value for the bit which is located in the register "**R**", and affects operation.*

"**k**" *represents an 8 or 10-bit constant or literal value.*

Binary Instruction	HEX	Mnemonic	Operation	Status Affected
0 0000 0000 0000	0000	NOP	No Operation	None
0 0000 0000 0001	0001	DAA	Decimal Adjust A	C
0 0000 0000 0010	0002	CONTW	A → CONT	None
0 0000 0000 0011	0003	SLEP	0 → WDT, Stop oscillator	T, P
0 0000 0000 0100	0004	WDTC	0 → WDT	T, P
0 0000 0000 rrrr	000r	IOW R	A → IOCR	Non[1]
0 0000 0001 0000	0010	ENI	Enable Interrupt	None
0 0000 0001 0001	0011	DISI	Disable Interrupt	None
0 0000 0001 0010	0012	RET	[Top of Stack] → PC	None
0 0000 0001 0011	0013	RETI	[Top of Stack] → PC, Enable Interrupt	None
0 0000 0001 0100	0014	CONTR	CONT → A	None
0 0000 0001 rrrr	001r	IOR R	IOCR → A	None[1]
0 0000 01rr rrrr	00rr	MOV R,A	A → R	None
0 0000 1000 0000	0080	CLRA	0 → A	Z
0 0000 11rr rrrr	00rr	CLR R	0 → R	Z
0 0001 00rr rrrr	01rr	SUB A,R	R-A → A	Z, C, DC
0 0001 01rr rrrr	01rr	SUB R,A	R-A → R	Z, C, DC
0 0001 10rr rrrr	01rr	DECA R	R-1 → A	Z
0 0001 11rr rrrr	01rr	DEC R	R-1 → R	Z
0 0010 00rr rrrr	02rr	OR A,R	A ∨ VR → A	Z
0 0010 01rr rrrr	02rr	OR R,A	A ∨ VR → R	Z
0 0010 10rr rrrr	02rr	AND A,R	A & R → A	Z
0 0010 11rr rrrr	02rr	AND R,A	A & R → R	Z
0 0011 00rr rrrr	03rr	XOR A,R	A ⊕ R → A	Z

[1] *This instruction is applicable to IOC50~IOCF0, IOC51 ~ IOCF1 only.*

Binary Instruction	HEX	Mnemonic	Operation	Status Affected
0 0011 01rr rrrr	03rr	XOR R,A	A ⊕ R → R	Z
0 0011 10rr rrrr	03rr	ADD A,R	A + R → A	Z, C, DC
0 0011 11rr rrrr	03rr	ADD R,A	A + R → R	Z, C, DC
0 0100 00rr rrrr	04rr	MOV A,R	R → A	Z
0 0100 01rr rrrr	04rr	MOV R,R	R → R	Z
0 0100 10rr rrrr	04rr	COMA R	/R → A	Z
0 0100 11rr rrrr	04rr	COM R	/R → R	Z
0 0101 00rr rrrr	05rr	INCA R	R+1 → A	Z
0 0101 01rr rrrr	05rr	INC R	R+1 → R	Z
0 0101 10rr rrrr	05rr	DJZA R	R-1 → A, skip if zero	None
0 0101 11rr rrrr	05rr	DJZ R	R-1 → R, skip if zero	None
0 0110 00rr rrrr	06rr	RRCA R	R(n) → A(n-1), R(0) → C, C → A(7)	C
0 0110 01rr rrrr	06rr	RRC R	R(n) → R(n-1), R(0) → C, C → R(7)	C
0 0110 10rr rrrr	06rr	RLCA R	R(n) → A(n+1), R(7) → C, C → A(0)	C
0 0110 11rr rrrr	06rr	RLC R	R(n) → R(n+1), R(7) → C, C → R(0)	C
0 0111 00rr rrrr	07rr	SWAPA R	R(0-3) → A(4-7), R(4-7) → A(0-3)	None
0 0111 01rr rrrr	07rr	SWAP R	R(0-3) ↔ R(4-7)	None
0 0111 10rr rrrr	07rr	JZA R	R+1 → A, skip if zero	None
0 0111 11rr rrrr	07rr	JZ R	R+1 → R, skip if zero	None
0 100b bbrr rrrr	0xxx	BC R,b	0 → R(b)	None [2]
0 101b bbrr rrrr	0xxx	BS R,b	1 → R(b)	None [3]
0 110b bbrr rrrr	0xxx	JBC R,b	if R(b)=0, skip	None
0 111b bbrr rrrr	0xxx	JBS R,b	if R(b)=1, skip	None
1 00kk kkkk kkkk	1kkk	CALL k	PC+1 → [SP], (Page, k) → PC	None
1 01kk kkkk kkkk	1kkk	JMP k	(Page, k) → PC	None
1 1000 kkkk kkkk	18kk	MOV A,k	k → A	None
1 1001 kkkk kkkk	19kk	OR A,k	A ∨ k → A	Z
1 1010 kkkk kkkk	1Akk	AND A,k	A & k → A	Z
1 1011 kkkk kkkk	1Bkk	XOR A,k	A ⊕ k → A	Z
1 1100 kkkk kkkk	1Ckk	RETL k	k → A, [Top of Stack] → PC	None
1 1101 kkkk kkkk	1Dkk	SUB A,k	k-A → A	Z, C, DC
1 1111 kkkk kkkk	1Fkk	ADD A,k	K+A → A	Z, C, DC
1 1110 11rr rrrr	1Err	TBRD R	See section 6.1.14 and 6.1.15	None

[2] *This instruction is not recommended for RF operation.*

[3] *This instruction cannot operate under RF.*

7 Absolute Maximum Ratings

Items	Rating		
Temperature under bias	0°C	to	70°C
Storage temperature	-65°C	to	150°C
Input voltage	Vss-0.3V	to	Vdd+0.5V
Output voltage	Vss-0.3V	to	Vdd+0.5V
Working Voltage	2.1V	to	5.5V
Working Frequency	DC	to	16 MHz

8 DC Electrical Characteristics

■ **Ta= 25°C, VDD= 5.0V, VSS= 0V**

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
FXT	Crystal: VDD to 5V	Two cycles with two clocks	32.768k	4	16	MHz
ERC	ERC: VDD to 5V	R: 3.3KΩ, C: 100 pF	0.847	1.21	1.573	MHz
VIHRC	Input High Threshold Voltage (Schmitt Trigger)	OSCI in RC mode	3.9	4	4.1	V
IERC1	Sink current	VI from low to high, VI=5V	21	22	23	mA
VILRC	Input Low Threshold Voltage (Schmitt Trigger)	OSCI in RC mode	1.7	1.8	1.9	V
IERC2	Sink current	VI from high to low, VI=2V	16	17	18	mA
IIL	Input Leakage Current for input pins	VIN = VDD, VSS	-1	0	1	μA
VIH1	Input High Voltage (Schmitt Trigger)	Port 5	0.7Vdd	–	Vdd+0.3V	V
VIL1	Input Low Voltage (Schmitt Trigger)	Port 5	-0.3V	–	0.3Vdd	V
VIHT1	Input High Threshold Voltage (Schmitt Trigger)	/RESET	0.7Vdd	–	Vdd+0.3V	V
VILT1	Input Low Threshold Voltage (Schmitt trigger)	/RESET	-0.3v	–	0.3Vdd	V
VIHT2	Input High Threshold Voltage (Schmitt Trigger)	TCC, INT	0.7Vdd	–	Vdd+0.3V	V
VILT2	Input Low Threshold Voltage (Schmitt Trigger)	TCC, INT	-0.3V	–	0.3Vdd	V
VIHX1	Clock Input High Voltage	OSCI in crystal mode	2.9	3.0	3.1	V
VILX1	Clock Input Low Voltage	OSCI in crystal mode	1.7	1.8	1.9	V
IOH1	Output High Voltage (Port 5)	VOH = 0.9VDD	–	-9	–	mA
IOL1	Output Low Voltage (Port 5)	VOL = 0.3VDD	–	70	–	mA
IOL2	Output Low Voltage (Port 5)	VOL = 0.1VDD	–	25	–	mA

(Continuation)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
IPH	Pull-high current	Pull-high active, input pin at VSS	-60	–	-80	µA
IPL	Pull-low current	Pull-low active, input pin at Vdd	40	–	60	µA
ISB1	Power down current	All input and I/O pins at VDD, Output pin floating, WDT disabled LVR disabled, LVD disabled	–	–	2.0	µA
ISB2	Power down current	All input and I/O pins at VDD, Output pin floating, WDT enabled LVR disabled, LVD disabled	–	–	8	µA
ISB3	Power down current	All input and I/O pins at VDD, Output pin floating, WDT disabled LVR enable, LVD disabled	–	–	2.5	µA
ISB4	Power down current	All input and I/O pins at VDD, Output pin floating, WDT enabled LVR enabled, LVD disabled	–	–	10	µA
ICC1	Operating supply current at two clocks	/RESET= 'High', Fosc=32kHz, (Crystal type, CLKS="0"), Output pin floating, WDT disabled LVR disabled, LVD disabled	–	–	35	µA
ICC2	Operating supply current at two clocks	/RESET= 'High', Fosc=32kHz (Crystal type,CLKS="0"), Output pin floating, WDT enabled LVR disabled, LVD disabled	–	–	35	µA
ICC3	Operating supply current at two clocks	/RESET= 'High', Fosc=4 MHz (Crystal type, CLKS="0"), Output pin floating, WDT enabled LVR disabled, LVD disabled	–	–	2.5	mA
ICC4	Operating supply current at two clocks	/RESET= 'High', Fosc=10 MHz (Crystal type, CLKS="0"), Output pin floating, WDT enabled LVR disabled, LVD disabled	–	–	4.5	mA

NOTE

- *These parameters are hypothetical (not tested) and are provided for design reference use only.*
- *Data under Minimum, Typical, and Maximum (Min., Typ., and Max.) columns are based on hypothetical results at 25℃. These data are for design reference only.*

■ **Internal RC Electrical Characteristics (Ta=25°C, VDD=5 V, VSS=0V)**

Internal RC	Drift Rate				
	Temperature	Voltage	Min.	Typ.	Max.
4 MHz	25°C	5V	3.84 MHz	4 MHz	4.16 MHz
16 MHz	25°C	5V	15.36 MHz	16 MHz	16.64 MHz
8 MHz	25°C	5V	7.76 MHz	8 MHz	8.24 MHz
455kHz	25°C	5V	436.8kHz	455kHz	473.2kHz

■ **Internal RC Electrical Characteristics (Ta= 0 ~70°C, VDD=2.2V~5.5V, VSS=0V)**

Internal RC	Drift Rate				
	Temperature	Voltage	Min.	Typ.	Max.
4 MHz	0 ~ 70°C	2.2V~5.5V	3.44 MHz	4 MHz	4.56 MHz
16 MHz	0 ~ 70°C	2.2V~5.5V	13.76 MHz	16MHz	18.24 MHz
8 MHz	0 ~ 70°C	2.2V~5.5V	6.96 MHz	8 MHz	9.04 MHz
455kHz	0 ~ 70°C	2.2V~5.5V	391.3kHz	455kHz	518.7kHz

8.1 AD Converter Characteristics

■ **Vdd=2.5V to 5.5V, Vss=0V, Ta= 0 to 70℃, 10-bit A D**

Symbol		Parameter	Condition	Min.	Typ.	Max.	Unit
V_{AREF}		Analog reference voltage	V_{AREF} - V_{ASS} ≥ 2.5V	2.5	–	Vdd	V
V_{ASS}				Vss	–	Vss	V
VAI		Analog input voltage	–	V_{ASS}	–	V_{AREF}	V
IAI1	Ivdd	Analog supply current	VDD=V_{AREF}=5.0V, V_{ASS} = 0.0V (V reference from Vdd)	1100	1200	1400	μA
	Ivref			-10	0	+10	μA
IAI2	Ivdd	Analog supply current	VDD=V_{AREF}=5.0V, V_{ASS} = 0.0V (V reference from VREF)	500	600	820	μA
	Ivref			550	600	650	μA
RN		Resolution	ADREF=0, Internal VDD VDD=5.0V, VSS = 0.0V	9	10	–	Bits
LN		Linearity error	VDD=V_{AREF}=5.0V, V_{ASS} = 0.0V	0	±1	±2	LSB
DNL		Differential nonlinear error	VDD=V_{AREF}=5.0V, V_{ASS} = 0.0V	0	±0.5	±0.9	LSB
FSE		Full scale error	VDD=V_{AREF}=5.0V, V_{ASS} = 0.0V	±0	±1	±2	LSB
OE		Offset error	VDD=V_{AREF}=5.0V, V_{ASS} = 0.0V	±0	±1	±2	LSB
ZAI		Recommended impedance of analog voltage source	–	0	8	10	KΩ
TAD		ADC clock duration	VDD=V_{AREF}=5.0V, V_{ASS} = 0.0V	4	–	–	μs

(Continuation)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
TCN	AD conversion time	VDD=V_{AREF}=5.0V, V_{ASS} = 0.0V		–	15	TAD
ADIV	ADC OP input voltage range	VDD=V_{AREF}=5.0V, V_{ASS} = 0.0V	0	–	V_{AREF}	V
ADOV	ADC OP output voltage swing	VDD=V_{AREF}=5.0V, V_{ASS} =0.0V, RL=10KΩ	0	0.2	0.3	V
			4.7	4.8	5	
ADSR	ADC OP slew rate	VDD=V_{AREF}=5.0V, V_{ASS} = 0.0V	0.1	0.3	–	V/µs
PSR	Power Supply Rejection	VDD=5.0V±0.5V	± 0	–	±2	LSB

NOTE

- *These parameters are hypothetical (not tested) and are provided for design reference use only.*
- *There is no current consumption when ADC is off other than minor leakage current.*
- *AD conversion result will not decrease when an increase of input voltage and no missing code will result.*
- *These parameters are subject to change without further notice.*

8.2 Comparator Characteristics

- **Vdd = 5.0V, Vss=0V, Ta= 0 to 70℃**

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
SR	Slew rate	–	0.1	0.2	–	V/µs
Vos	Input offset voltage	RL=5.1K, (Note 1)	1	5	10	mV
IVR	Input voltage range	Vdd =5.0V, V_{SS} = 0.0V	0	–	5	V
OVS	Output voltage swing	Vd =5.0V, V_{SS} = 0.0V, RL=10 KΩ	0	0.2	0.3	V
			4.7	4.8	5	
Ico	Supply current of Comparator	–	–	300	–	µA
Vs	Operating range	–	2.5	–	5.5	V

NOTE

- *These parameters are hypothetical (not tested) and are provided for design reference use only.*
- *These parameters are subject to change without further notice.*

9 AC Electrical Characteristics

■ **Ta= 0 to 70°C, VDD=5V ± 5%, VSS=0V**

Symbol	Parameter	Conditions	Min	Typ.	Max	Unit
Dclk	Input CLK duty cycle	–	45	50	55	%
Tins	Instruction cycle time (CLKS="0")	Crystal type	100	–	DC	ns
		RC type	500	–	DC	ns
Ttcc	TCC input time period	–	(Tins+20)/N[1]	–	–	ns
Tdrh	Device reset hold time	Ta = 25°C	11.3	16.2	21.6	ms
Trst	/RESET pulse width	Ta = 25°C	2000	–	–	ns
Twdt1[2]	Watchdog timer period	Ta = 25°C	16.5-30%	16.5	16.5+30%	ms
Twdt2[3]	Watchdog timer period	Ta = 25°C	4.2-30%	4.2	4.2+30%	ms
Tset	Input pin setup time	–	–	0	–	ns
Thold	Input pin hold time	–	15	20	25	ns
Tdelay	Output pin delay time	Cload=20pF	45	50	55	ns
Tdrc	ERC delay time	Ta = 25°C	1	3	5	ns

[1] ***N:*** *Selected prescaler ratio*

[2] ***Twdt1:*** *The Option Word 2 (WDTPS) is used to define the oscillator set-up time. WDT timeout length is the same as the set-up time (18 ms).*

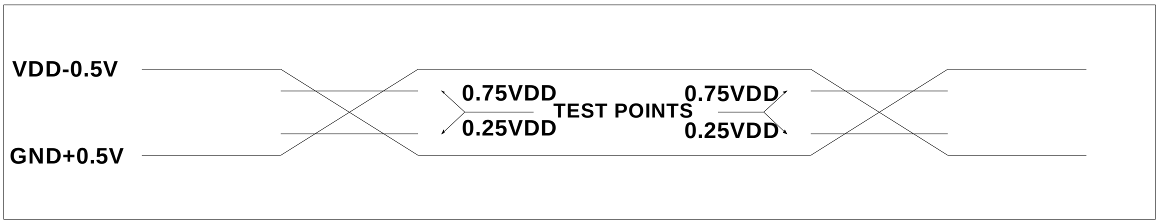
[3] ***Twdt2:*** *The Option Word 2 (WDTPS) is used to define the oscillator set-up time. WDT timeout length is the same as the set-up time (4.5ms).*

NOTE

- *These parameters are hypothetical (not tested) and are provided for design reference use only.*
- *Data under Minimum, Typical, and Maximum (Min., Typ., and Max.) columns are based on hypothetical results at 25°C. These data are for design reference only.*
- *The Watchdog timer duration is determined by Code Option Word 2 (WDTPS).*

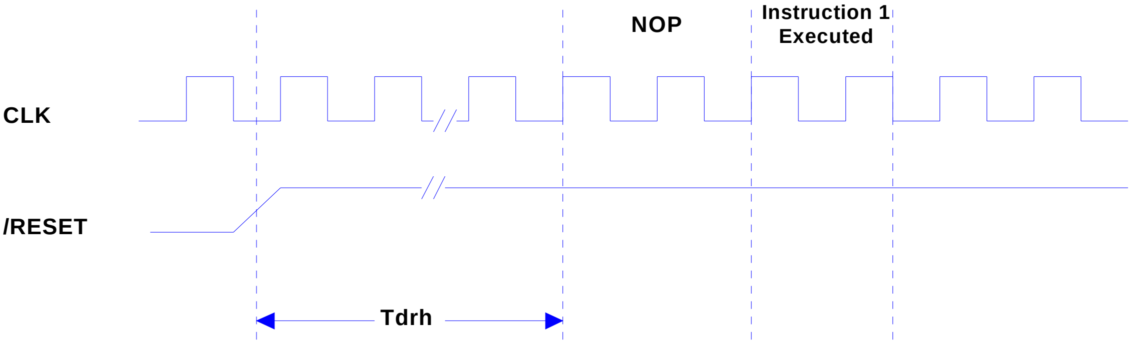
10 Timing Diagrams

AC Test Input/Output Waveform



AC Testing : Input is driven at VDD-0.5V for logic "1",and GND+0.5V for logic "0".Timing measurements are made at 0.75VDD for logic "1",and 0.25VDD for logic "0".

RESET Timing (CLK="0")



TCC Input Timing (CLKS="0")

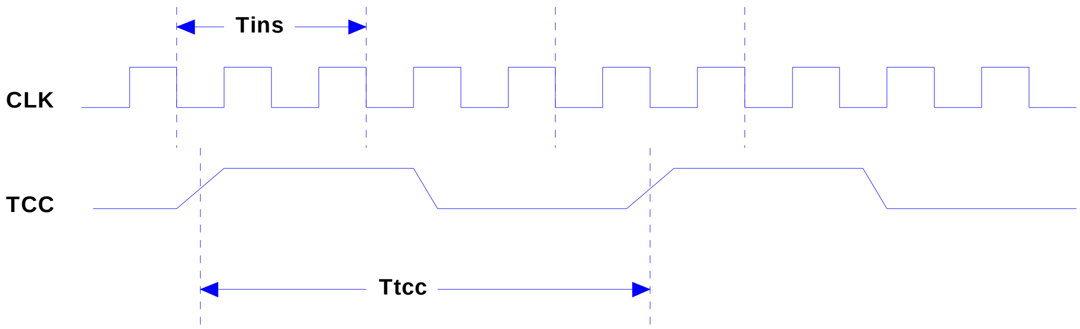


Figure 10-1 EM78P141 Timing Diagrams

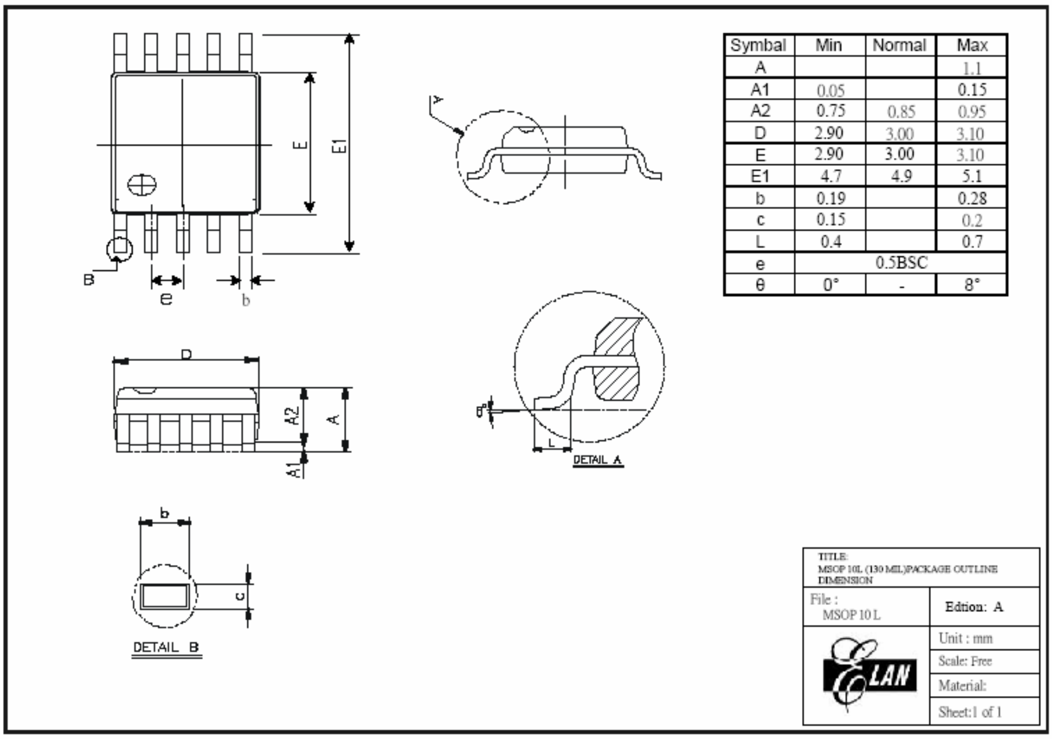
APPENDIX

A Package Type

OTP MCU	Package Type	Pin Count	Package Size
EM78P141MS10J/S	MSOP	10	118 mil

Green products do not contain hazardous substances.

B Packaging Configuration



Symbal	Min	Normal	Max
A			1.1
A1	0.05		0.15
A2	0.75	0.85	0.95
D	2.90	3.00	3.10
E	2.90	3.00	3.10
E1	4.7	4.9	5.1
b	0.19		0.28
c	0.15		0.2
L	0.4		0.7
e		0.5BSC	
θ	0°	-	8°

Figure B-1 EM78P141MS10J/S 10-Pin MSOP Package Type

C How to Use the ICE 143 for EM78P141

C-1 Code Option Pin Selection with JP1 & JP2

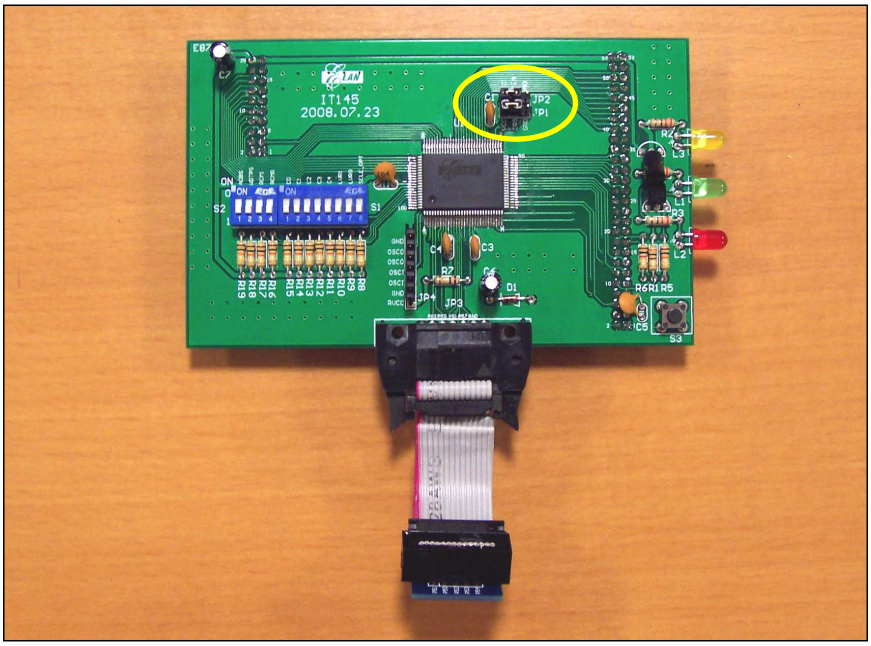


Figure C-1 ICE 143 Indicating JP1 & JP2 Location

W1	Code Option Pin Selection
VCC MCEN GND	JP1 is fixed to VCC (default)
VCC ERS GND	JP2 is fixed to VCC (default)

C-2 DIP Switch (S1 & S2) Setting

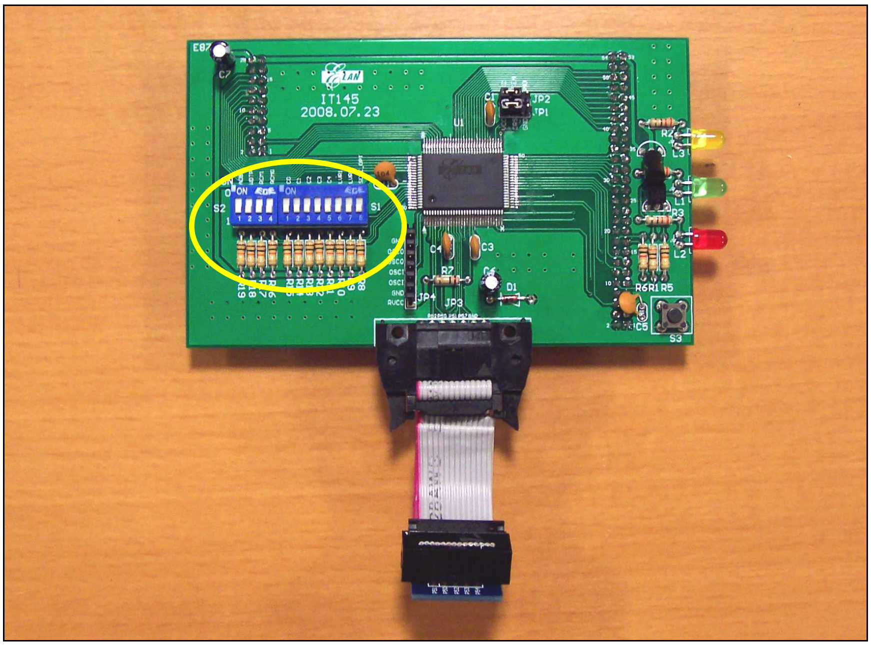


Figure C-2 ICE 143 Indicating DIP Switch Location

Switch	Switch #	Symbol	Pin No.	Type	Function
	8	SELE_ OPT	20	I	**Option bits controlled by pins or registers.** **0: Option bit is controlled by pins.** **1: Option bit is controlled by registers.**
1	7 ~ 6	LVR0, LVR1	93, 94	I	Low Voltage Reset enable bits. These bits are controlled either by pins or registers depending on the SELE_OPT pin. Refer to Section 6.2.10.
	5 ~ 1	C4, C3, C2, C1, C0	26, 25, 24, 23, 22	I	**Calibrator of internal RC mode.** **These bits are controlled either by pins or registers depending on the SELE_OPT pin. Refer to Section 6.2.9.**
	4 ~ 3	RCM0, RCM1	95, 96	I	IRC mode frequency selection bits These bits are controlled either by pins or registers depending on SELE_OPT pin. Refer to Section 6.2.10.
2	2	WDTPS	31	I	Programmable WDT time "**0**" for 4.5ms; "**1**" for 18ms This bit is controlled either by pins or registers depending on SELE_OPT pin. Refer to Section 6.2.10.
	1	ADBS	21	I	**AD Bit Select Register** **This bit is fixed at "0".** This bit is controlled either by pins or registers depending on the SELE_OPT pin.

C-3 ICE 143 ICE Cable Connector (JP3) Pin Assignment

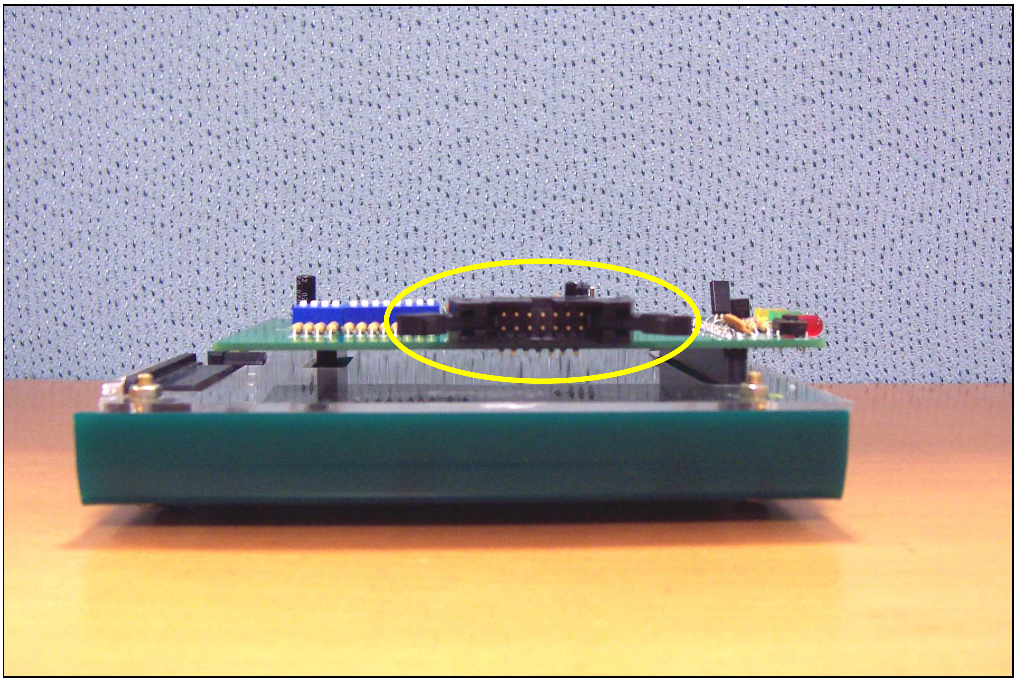


Figure C-3a ICE 143 with its ICE Cable Connector Indicated

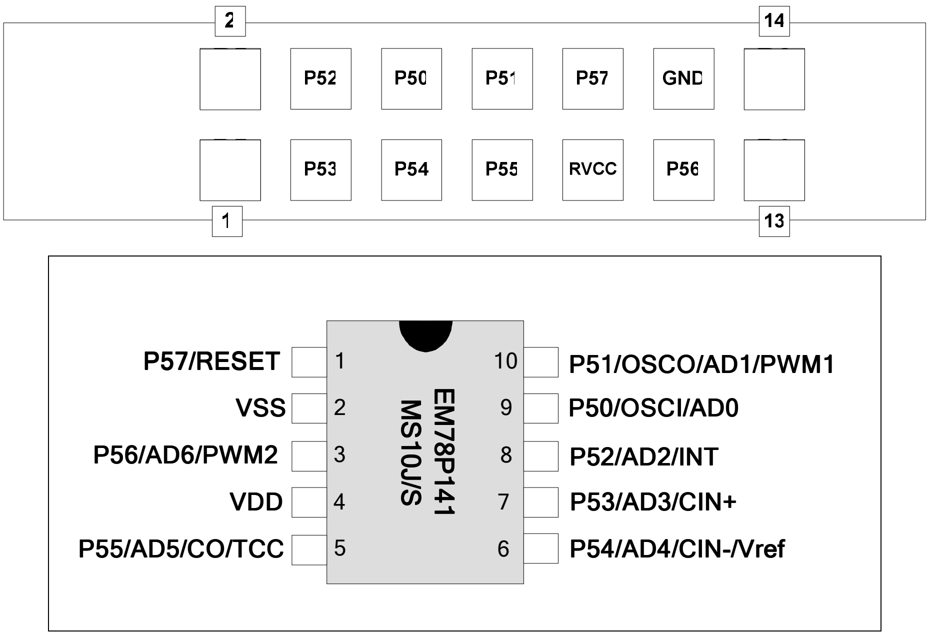


Figure C-3b ICE 143 ICE Cable Connector Pin Assignment

C-4 ICE 143 ICE Cable to Target Pin Assignment

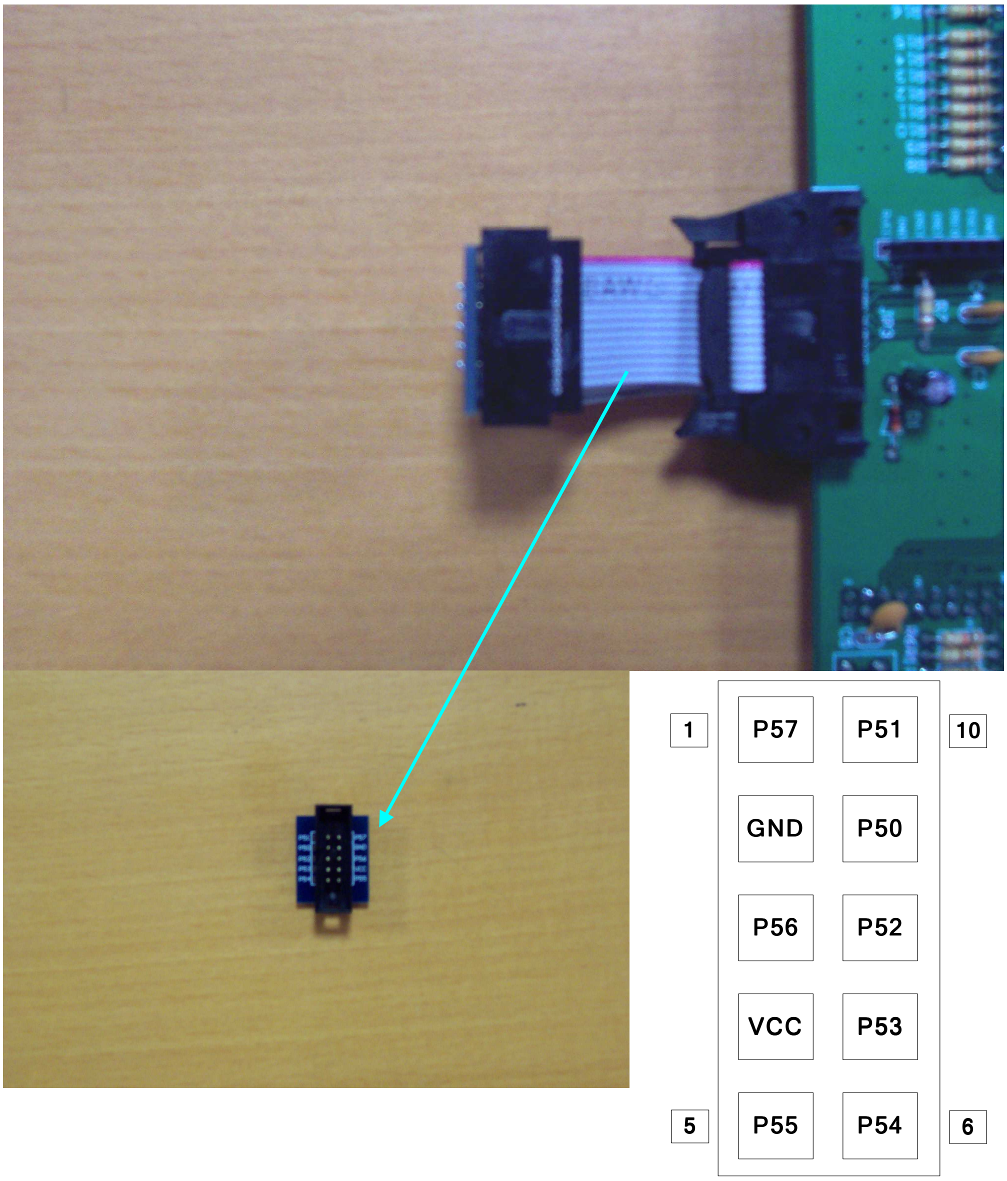


Figure C-4 ICE 143 ICE Cable to Target Pin Assignment