EM78P151

8-Bit Microcontroller

Product Specification

DOC. VERSION 1.0

ELAN MICROELECTRONICS CORP.

December 2014

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Contents

APPENDIX

Specification Revision History

Doc. Version	Revision Description	Date
0.9	Preliminary version	2014/08/06
1.0	1. Modified the IRC 4 MHz and 8 MHz spec. 2. Modified the table of WDT warm-up time.	2014/12/29

1 General Description

The EM78P151 is an 8-bit microprocessor designed and developed with low-power and high-speed CMOS technology. The devices have on-chip 1024×13-bit Electrical One Time Programmable Read Only Memory (OTP-ROM). They provide a protection bit to prevent intrusion of user's OTP memory code. Fifteen Code option bits are also available to meet user's requirements.

With enhanced OTP-ROM features, the EM78P151 provides a convenient way of developing and verifying user's programs. Moreover, this OTP devices offer the advantages of easy and effective program updates, using development and programming tools. You can avail of the ELAN Writer to easily program your development code.

2 Features

- CPU configuration
  - 1K×13 bits on chip ROM
  - 52×8 bits on chip registers (SRAM, general purpose) when KTYPE=1
  - 50×8 bits on chip registers (SRAM, general purpose) when KTYPE=0
  - 5 level stacks for subroutine nesting
  - Less than 1.5 mA at 5V/4MHz
  - Typically 15 μA, at 3V/32kHz
  - Typically 1 μA, during Sleep mode
- I/O port configuration
  - 1 bi-directional I/O port**:** P6
  - 6 I/O pins
  - Wake-up port**:** P6
  - 6 Programmable pull-down I/O pins
  - 5 programmable pull-high I/O pins
  - 5 programmable open-drain I/O pins and 1 open-drain pin (P63)
  - External interrupt : P60
- Operating voltage range
  - 2.0V~5.5V at 0°C~70°C (Commercial)
- Operating frequency range (base on two clocks)
  - Crystal mode:
    DC ~ 20 MHz / 2clks @ 5V; (DC ~ 100ns inst. Cycle)
    DC ~ 16 MHz / 2clks @ 4.5V; (DC ~ 125ns inst. Cycle)
    DC ~ 8 MHz / 2clks @ 3V; (DC ~ 250ns inst. Cycle)
    DC ~ 4 MHz / 2clks @ 2.3V; (DC ~ 500ns inst. Cycle)
    The transient point of system frequency between HXT and LXT is 400 kHz.
  - IRC,ERC mode:
    DC ~ 20 MHz / 2clks @ 5V; (DC ~ 100ns inst. Cycle)
    DC ~ 16 MHz / 2clks @ 4.5V; (DC ~ 125ns inst. Cycle)
    DC ~ 8 MHz / 2clks @ 3V; (DC ~ 250ns inst. Cycle)
    DC ~ 4 MHz / 2clks @ 2.0V; (DC ~ 500ns inst. Cycle)
  - IRC mode:
    Oscillation mode: 4 / 8 / 1 MHz and 455kHz

Internal RC Freq.	Drift Rate			
	Temp. (0°C~70°C)	Voltage (2.0 ~ 5.5V)	Process	Total
4 MHz	± 1.5%	± 1%	± 1%	± 3.5%
8 MHz	± 1.5%	± 1.5%	± 1%	± 4%
1 MHz	± 1.5%	± 1%	± 1%	± 3.5%
455 kHz	± 1.5%	± 1%	± 1%	± 3.5%

- Peripheral Configuration
  - 8-bit real time clock/counter (TCC) with selective signal sources, trigger edges, and overflow interrupt
  - 3 programmable level voltage reset
    LVR : 4.0, 3.5, 2.7V, 1.8V (POR, default)
  - 2 / 4 / 8 clocks per instruction cycle selected by code option
- Three Available Interrupts:
  - TCC overflow interrupt
  - Input-port status changed interrupt (wake-up from sleep mode)
  - External interrupt
- Special Features
  - Programmable free running watchdog timer
  - Power saving Sleep mode
  - Selectable Oscillation mode
  - Programmable prescaler of oscillator set-up time
- Package Type:
  - 8-pin DIP 300mil : EM78P151D8S/J
  - 8-pin SOP 150mil : EM78P151S8S/J
  - 6-pin SOT23 : EM78P151ST6S/J

NOTE
These are Green Products which do not contain hazardous substances.

3 Pin Assignment

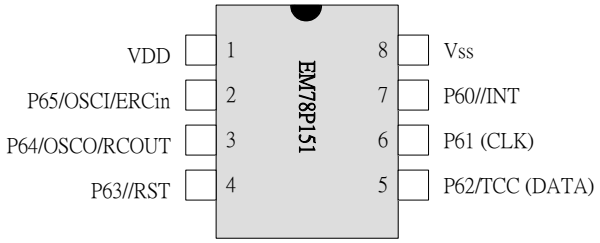


Figure 3-1 ***EM78P151D8/SO8***

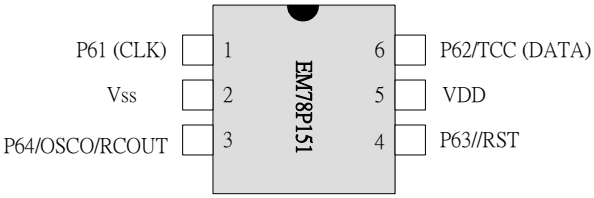


Figure 3-2 ***EM78P151ST6***

4 Pin Description

4.1 EM78P151D8/SO8

Legend: ***ST:*** *Schmitt Trigger input* ***AN:*** *Analog pin*
CMOS: *CMOS output* ***XTAL:*** *Oscillation pin for crystal/ resonator*

Name	Function	Input Type	Output Type	Description
P60//INT	P60	ST	CMOS	Bidirectional I/O pin with programmable pull- high, pull-low, open-drain and wake up pin from sleep mode when the status of the pin changes.
	/INT	ST	-	External interrupt pin triggered by a falling edge
P61/CLK	P61	ST	CMOS	Bidirectional I/O pin with programmable pull- high, pull-low, open-drain and wake up pin from sleep mode when the status of the pin changes.
	CLK	ST	-	Programming clock pin
P62/TCC/DATA	P62	ST	CMOS	Bidirectional I/O pin with programmable pull- high, pull-low, open-drain and wake up pin from sleep mode when the status of the pin changes.
	TCC	ST	-	Real Time Clock/Counter clock input
	DATA	ST	CMOS	Programming data pin
P63//RESET	P63	ST	CMOS	Input pin or open-drain output pin and wake up pin from sleep mode when the status of the pin changes. I/O pin with programmable pull-low.
	/RESET	ST	-	Active low RESET to the device.
P64/OSCO/RCOUT	P64	ST	CMOS	Bidirectional I/O pin with programmable pull- high, pull-low, open-drain and wake up pin from sleep mode when the status of the pin changes.
	OSCO	-	XTAL	Clock output of crystal/ resonator oscillator
	RCOUT	-	CMOS	Clock output of internal RC oscillator and external RC oscillator
P65/OSCI/ERCin	P65	ST	CMOS	Bidirectional I/O pin with programmable pull- high, pull-low, open-drain and wake up pin from sleep mode when the status of the pin changes.
	OSCI	XTAL	-	Clock input of crystal/resonator oscillator
	ERCin	AN	-	External RC input pin
VDD	VDD	Power	-	Power
VSS	VSS	Power	-	Ground

4.2 EM78P151ST6

Legend: ***ST:*** *Schmitt Trigger input* ***AN:*** *Analog pin*
CMOS: *CMOS output* ***XTAL:*** *Oscillation pin for crystal/ resonator*

Name	Function	Input Type	Output Type	Description
P61/CLK	P61	ST	CMOS	Bidirectional I/O pin with programmable pull- high, pull-low, open-drain and wake up pin from sleep mode when the status of the pin changes.
	CLK	ST	-	Programming clock pin
P62/TCC/DATA	P62	ST	CMOS	Bidirectional I/O pin with programmable pull- high, pull-low, open-drain and wake up pin from sleep mode when the status of the pin changes.
	TCC	ST	-	Real Time Clock/Counter clock input
	DATA	ST	CMOS	Programming data pin
P63//RESET	P63	ST	CMOS	Input pin or open-drain output pin and wake up pin from sleep mode when the status of the pin changes. I/O pin with programmable pull-low.
	/RESET	ST	-	Active low RESET to the device.
P64/OSCO/RCOUT	P64	ST	CMOS	Bidirectional I/O pin with programmable pull- high, pull-low, open-drain and wake up pin from sleep mode when the status of the pin changes.
	OSCO	-	XTAL	Clock output of crystal/ resonator oscillator
	RCOUT	-	CMOS	Clock output of internal RC oscillator and external RC oscillator
VDD	VDD	Power	-	Power
VSS	VSS	Power	-	Ground

5 Block Diagram

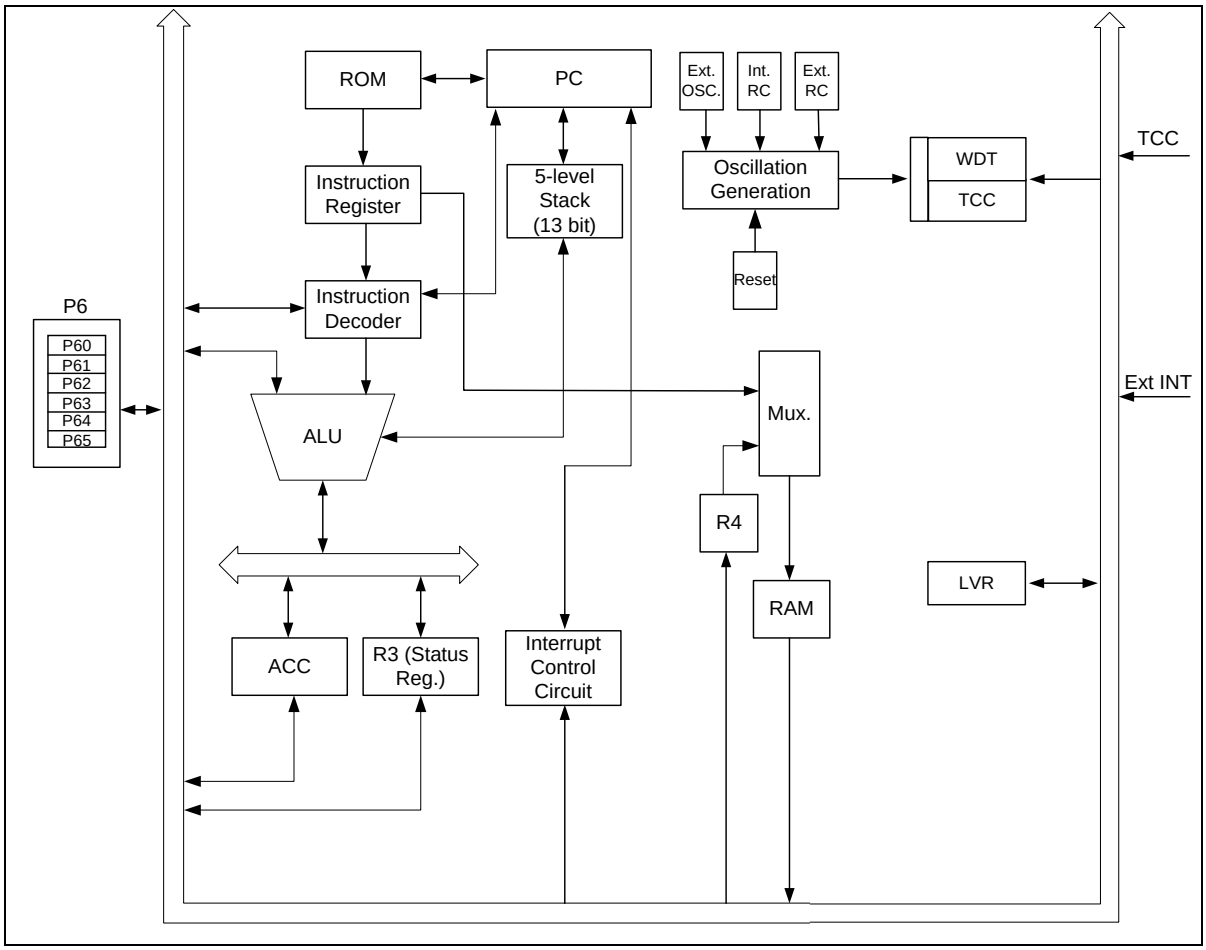


Figure 5-1 Functional Block Diagram of EM78P151

6 Functional Description

KTYPE = 1 (Type A)

6.1 Operational Registers

6.1.1 R0 (Indirect Addressing Register)

R0 is not a physically implemented register. It is used as an indirect addressing pointer. Any instruction using R0 as a pointer actually accesses data pointed by the RAM Select Register (R4).

6.1.2 R1 (Timer Clock/Counter)

- Incremented by an external signal edge, which is defined by TE bit (CONT-4) through the TCC pin, or by the instruction cycle clock.
- Writable and readable as any other registers.
- Defined by resetting PAB (CONT-3).
- The prescaler is assigned to TCC, if the PAB bit (CONT-3) is reset.
- The contents of the prescaler counter will be cleared only when the TCC register is written with a value.

6.1.3 R2 (Program Counter and Stack)

- Depending on the device type, R2 and hardware stack are 10-bit wide. The structure is depicted in the following figure.

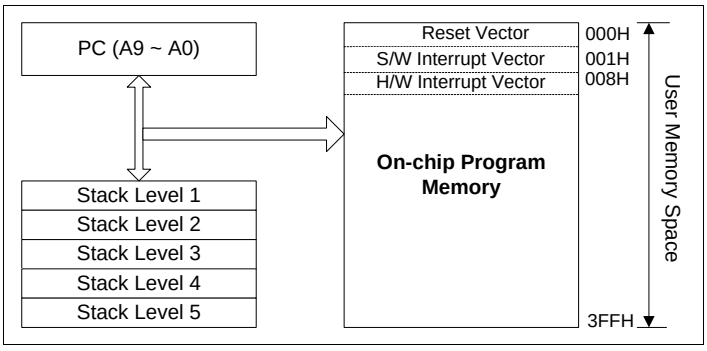
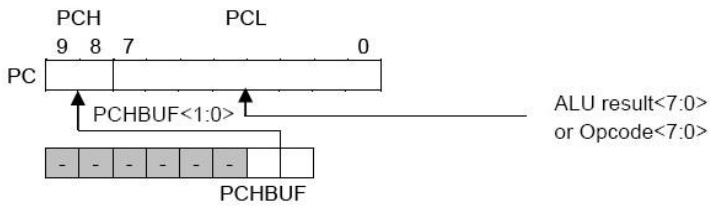


Figure 6-1-1 Program Counter Organization

- The configuration structure generates 1024 × 13 bits on-chip OTP ROM addresses to the relative programming instruction codes. One program page is 1024 words long.
- If KTYPE bit =1 R2 is set as all "0" when under RESET condition.
- If KTYPE bit =0 R2 is set as all "3FF" when under RESET condition.

- "JMP" instruction allows direct loading of the lower 10 program counter bits. Thus, "JMP" allows the PC to go to any location within a page.
- "CALL" instruction loads the lower 10 bits of the PC, and PC+1 are pushed onto the stack. Thus, the subroutine entry address can be located anywhere within a page.
- "RET" ("RETL k", "RETI") instruction loads the program counter with the contents of the top-level stack.



Note: PCHBUF is used only for instruction with PCL as destination for FM8PB53B.

- If KTYPE bit =1, ENHS bit =1 : Any instruction written to R2 (e.g. “ADD R2, A”, "MOV R2, A", "BC R2, 6", etc.·) will cause the ninth bit and the tenth bit (A8 ~ A9) of the PC to be cleared. Hence, the computed jump is limited to the first 256 locations of a page.
- If KTYPE bit =1, ENHS bit =0 : "ADD R2, A" allows a relative address to be added to the current PC, and the ninth and above bits of the PC will increase progressively.
- All instructions are single instruction cycle (F_{CLK} / 2, F_{CLK} / 4 or F_{CLK} / 8) except for instructions that would change the contents of R2. Such instructions will need one more instruction cycle.

■ The Data Memory Configuration is as follows:

Address	R PAGE Registers		IOC PAGE Registers	
00	R0	(IAR)	Reserve	
01	R1	(TCC)	CONT	(Control Register)
02	R2	(PC)	Reserve	
03	R3	(Status)	Reserve	
04	R4	(RSR)	Reserve	
05	R5	(GPR)	Reserve	
06	R6	(Port 6)	IOC6	(I/O Port Control Register)
07	R7	(GPR)	Reserve	
08	R8	(WDTCR)	Reserve	
09	R9	(GPR)	Reserve	
0A	RA	(GPR)	Reserve	
0B	RB	(PDCR)	IOCB	(PDCR)
0C	RC	(ODCR)	IOCC	(ODCR)
0D	RD	(PHCR)	IOCD	(PHCR)
0E	RE	(IMR)	IOCE	(WDTCR)
0F	RF	(ISR)	IOCF	(IMR)
10 : 3F	General Registers			

Figure 6-1-2 Data Memory Configuration

6.1.4 R3 (Status Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RST	GP1	GP0	T	P	Z	DC	C

Bit 7 (RST): Bit for reset type

0: Set to 0 if the device wakes up from other reset type

1: Set to 1 if the device wakes up from sleep mode on a pin change

Bits 6 ~ 5 (GP1 ~ GP0): General-purpose read/write bits

Bit 4 (T): Time-out bit

Set to “1” by the "SLEP" and "WDTC" commands or during power up; and reset to “0” by WDT time-out.

Bit 3 (P): Power down bit

Set to “1” during power on or by a "WDTC" command; and reset to “0” by a "SLEP" command.

Bit 2 (Z): Zero flag

Set to "1" if the result of an arithmetic or logic operation is zero.

Bit 1 (DC): Auxiliary carry flag

Bit 0 (C): Carry flag

6.1.5 R4 (RAM Select Register)

- Bits 7 ~ 6 are not used. (Read only).
- Bits 7 ~ 6 set to “1” at all time.
- Bits 5 ~ 0 are used to select registers (address: 0x00 ~ 0x3F) in the indirect addressing mode.
- See the Data Memory Configuration in Figure 6-1-2.

6.1.6 R5 GPR (General Purpose Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
GP	GP	GP	GP	GP	GP	GP	GP

Bits 7~0 (GP): General purpose register

6.1.7 R6 (Port 6)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
GP	GP	P65	P64	P63	P62	P61	P60

Bits 7~6 (GP): General purpose register

Bit 5 (P65): P65 control bit

Bit 4 (P64): P64 control bit

Bit 3 (P63): P63 control bit

Bit 2 (P62): P62 control bit

Bit 1 (P61): P61 control bit

Bit 0 (P60): P60 control bit

R6 is I/O register.

6.1.8 R7 GPR (General Purpose Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
GP	GP	GP	GP	GP	GP	GP	GP

Bits 7~0 (GP): General purpose register

6.1.9 R9 GPR (General Purpose Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
GP	GP	GP	GP	GP	GP	GP	GP

If KTYPE Bit =1, Port 6 Input Change Interrupt/Wake-up function always enable.

Bits 7~0 (GP): General purpose registers

6.1.10 RA GPR (General Purpose Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
GP	GP	GP	GP	GP	GP	GP	GP

Bits 7~0 (GP): General purpose registers

6.1.11 RF ISR(Interrupt Status Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	EXIF	ICIF	TCIF

***Note: "1"** means with interrupt request **"0"** means no interrupt occurs*

Bits 7 ~ 3: Not used. Set to "0" at all time.

Bit 2 (EXIF): External Interrupt Flag. Set by a falling edge on /INT pin, reset by software.

Bit 1 (ICIF): Port 6 input status changed interrupt flag. Set when Port 6 input changes, reset by software.

Bit 0 (TCIF): TCC Overflow Interrupt Flag. Set when TCC overflows, reset by software.

RF can be cleared by instruction but cannot be set.

IOCF is the interrupt mask register.

NOTE

The result of reading RF is the "logic AND" of RF and IOCF.

6.1.12 R10~R3F

These are all 8-bit general-purpose registers.

6.2 Special Function Registers

6.2.1 A (Accumulator)

Internal data transfer operation, or instruction operand holding usually involves the temporary storage function of the Accumulator, which is not an addressable register.

6.2.2 CONT (Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
GP	/INT	TS	TE	PAB	PSR2	PSR1	PSR0

Bit 7 (GP): General purpose register.

Bit 6 (/INT): Interrupt enable flag.

0: masked by DISI or hardware interrupt

1: enabled by ENI/RETI instructions

Bit 5 (TS): TCC signal source

0: internal instruction cycle clock, P62 is a bidirectional I/O pin

1: transition on TCC pin

Bit 4 (TE): TCC signal edge

0: increment if the transition from low to high takes place on TCC pin

1: increment if the transition from high to low takes place on TCC pin

Bit 3 (PAB): Prescaler Assigned Bit

0: TCC

1: WDT

Bits 2 ~ 0 (PSR2 ~ PSR0): TCC / WDT prescaler bits

PSR2	PSR1	PSR0	TCC Rate	WDT Rate
0	0	0	1:2	1:1
0	0	1	1:4	1:2
0	1	0	1:8	1:4
0	1	1	1:16	1:8
1	0	0	1:32	1:16
1	0	1	1:64	1:32
1	1	0	1:128	1:64
1	1	1	1:256	1:128

The CONT register is both readable and writable.

6.2.3 IOC6 (I/O Port Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	1	C65	C64	C63	C62	C61	C60

Bits 7~6: Not used, set to "1" all the time.

Bit 5 (C65): P65 I/O control register

0: defines the relative I/O pin as output

1: puts the relative I/O pin into high impedance

Bit 4 (C64): P64 I/O control register

Bit 3 (C63): P63 I/O control register

Bit 2 (C62): P62 I/O control register

Bit 1 (C61): P61 I/O control register

Bit 0 (C60): P60 I/O control register

IOC6 registers is both readable and writable.

6.2.4 IOCB/RB PDCR (Pull-down Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
GP	/PD62	/PD61	/PD60	GP	GP	GP	GP

Bit 7 (GP): General purpose register.

Bit 6 (/PD62): Control bit used to enable pull-down of the P62 pin.

0: Enable internal pull-down

1: Disable internal pull-down

Bit 5 (/PD61): Control bit used to enable pull-down of the P61 pin.

Bit 4 (/PD60): Control bit used to enable pull-down of the P60 pin.

Bits 3~0 (GP): General purpose register.

The IOCB Register is both readable and writable.

6.2.5 IOCC/RC ODCR (Open-drain Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
GP	GP	OD65	OD64	GP	OD62	OD61	OD60

Bits 7~6 (GP): General purpose register.

Bit 5 (OD65): Control bit used to enable open-drain of the P65 pin.

0: Disable open-drain output

1: Enable open-drain output

Bit 5 (OD65): Control bit used to enable open-drain of the P65 pin.

Bit 4 (OD64): Control bit used to enable open-drain of the P64 pin.

Bit 3 (GP): General purpose register.

Bit 2 (OD62): Control bit used to enable open-drain of the P62 pin.

Bit 1 (OD61): Control bit used to enable open-drain of the P61 pin.

Bit 0 (OD60): Control bit used to enable open-drain of the P60 pin.

The IOCC Register is both readable and writable.

6.2.6 IOCD/RD PHCR(Pull-high Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
GP	GP	/PH65	/PH64	GP	/PH62	/PH61	/PH60

Bits 7~6 (GP): General purpose register.

Bit 5 (/PH65): Control bit used to enable pull-high of the P65 pin.

0: Enable internal pull-high

1: Disable internal pull-high

Bit 4 (/PH64): Control bit used to enable pull-high of the P64 pin.

Bit 3 (GP): General purpose register.

Bit 2 (/PH62): Control bit used to enable pull-high of the P62 pin.

Bit 1 (/PH61): Control bit used to enable pull-high of the P61 pin.

Bit 0 (/PH60): Control bit used to enable pull-high of the P60 pin.

The IOCD Register is both readable and writable.

6.2.7 IOCE/R8 (WDT Control Register)

ENHS(opt.)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	WDTE	EIS	GP	GP	GP	GP	GP	GP
0	WDTE	EIS	GP	GP	GP	/PD65	/PD64	/PD63

Bit 7 (WDTE): Control bit used to enable the Watchdog timer.

0: Disable WDT

1: Enable WDT

WDTE is both readable and writable.

Bit 6 (EIS): Control bit is used to define the function of P60 (/INT) pin.

0: P60, bidirectional I/O pin.

1: /INT, external interrupt pin. In this case, the I/O control bit of P60 (Bit 0 of IOC6) must be set to "1".

When EIS is "0," the path of /INT is masked. When EIS is "1", the status of the /INT pin can also be read by way of reading Port 6 (R6). See Figure 6-5 under Section 6.6 for reference.

EIS is both readable and writable.

Bits 5~3: Not used. Set to “0” at all time.

If ENHS bit = 1

Bits 2~0: General purpose register.

If ENHS bit = 0

Bit 2 (/PD65): Control bit used to enable pull-down of the P65 pin.

0: Enable internal pull-down

1: Disable internal pull-down

Bit 1 (/PD64): Control bit used to enable pull-down of the P64 pin.

Bit 0 (/PD63): Control bit used to enable pull-down of the P63 pin.

6.2.8 IOCF/RE (Interrupt Mask Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
GP	GP	GP	GP	GP	EXIE	ICIE	TCIE

Bits 7~3 (GP): General purpose registers

Bit 2 (EXIE): EXIF interrupt enable bit

0: disable EXIF interrupt

1: enable EXIF interrupt

Bit 1 (ICIE): ICIF interrupt enable bit

0: disable ICIF interrupt

1: enable ICIF interrupt

Bit 0 (TCIE): TCIF interrupt enable bit

0: disable TCIF interrupt

1: enable TCIF interrupt

The IOCF register is both readable and writable.

KTYPE = 0 (Type B)

6.3 Operational Registers

6.3.1 R0 (Indirect Addressing Register)

R0 is not a physically implemented register. It is used as an indirect addressing pointer. Any instruction using R0 as a pointer actually accesses data pointed by the RAM Select Register (R4).

6.3.2 R1 (Timer Clock/Counter)

- Incremented by an external signal edge, which is defined by TE bit (CONT-4) through the TCC pin, or by the instruction cycle clock.
- Writable and readable as any other registers.
- Defined by resetting PAB (CONT-3).
- The prescaler is assigned to TCC, if the PAB bit (CONT-3) is reset.
- The contents of the prescaler counter will be cleared only when the TCC register is written with a value.

6.3.3 R2 (Program Counter and Stack)

- Depending on the device type, R2 and hardware stack are 10-bit wide. The structure is depicted in the following figure.

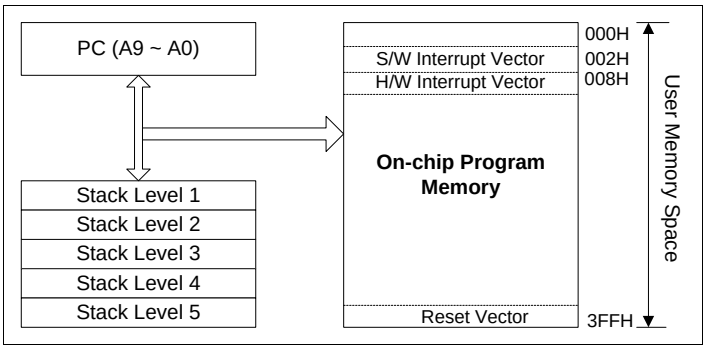
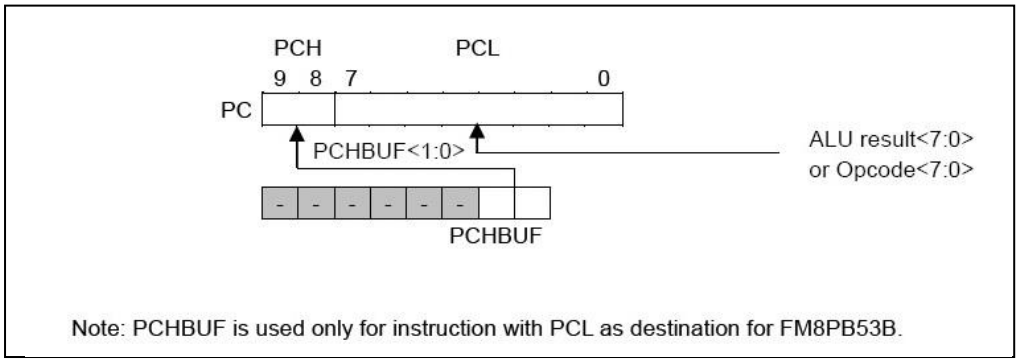


Figure 6-3-1 Program Counter Organization

- The configuration structure generates 1024×13 bits on-chip OTP ROM addresses to the relative programming instruction codes. One program page is 1024 words long.
- If KTYPE bit =1 R2 is set as all "0" when under RESET condition.
- If KTYPE bit =0 R2 is set as all "3FF" when under RESET condition.
- "JMP" instruction allows direct loading of the lower 10 program counter bits. Thus, "JMP" allows PC to go to any location within a page.

- "CALL" instruction loads the lower 10 bits of the PC, and then PC+1 are pushed onto the stack. Thus, the subroutine entry address can be located anywhere within a page.
- "RET" ("RETL k", "RETI") instruction loads the program counter with the contents of the top-level stack.
- If KTYPE bit =0, ENHS bit =x : Any instruction written to R2 (e.g. “ADD R2, A”, "MOV R2, A", "BC R2, 6", etc.) will cause the ninth bit and the tenth bit (A8 ~ A9) from PCHBUF



- All instructions are single instruction cycle (F_{CLK} / 2, F_{CLK} / 4 or F_{CLK} / 8) except for instructions that would change the contents of R2. Such instructions will need one more instruction cycle.
- The Data Memory Configuration is as follows:

Address	R PAGE Registers	IOC PAGE Registers
00	R0 (IAR)	Reserve
01	R1 (TCC)	CONT (Control Register)
02	R2 (PC)	Reserve
03	R3 (Status)	Reserve
04	R4 (RSR)	Reserve
05	R5 (GPR)	Reserve
06	R6 (Port 6)	IOC6 (I/O Port Control Register)
07	R7 (GPR)	Reserve
08	R8 (WDTCR)	Reserve
09	R9 (IIWK)	Reserve
0A	RA (PCHBUF)	Reserve
0B	RB (PDCR)	IOCB (PDCR)
0C	RC (ODCR)	IOCC (ODCR)
0D	RD (PHCR)	IOCD (PHCR)
0E	RE (IMR)	IOCE (WDTCR)
0F	RF (ISR)	IOCF (IMR)

10 : 3F	General Registers

Figure 6-3-2 Data Memory Configuration

6.3.4 R3 (Status Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RST	GP1	GP0	T	P	Z	DC	C

Bit 7 (RST): Bit for reset type

0: Set to 0 if the device wakes up from other reset type

1: Set to 1 if the device wakes up from sleep mode on a pin change

Bits 6 ~ 5 (GP1 ~ GP0): General-purpose read/write bits

Bit 4 (T): Time-out bit

Set to “1” by the "SLEP" and "WDTC" commands, or during power up; and reset to “0” by WDT time-out.

Bit 3 (P): Power down bit

Set to “1” during power on or by a "WDTC" command; and reset to “0” by a "SLEP" command.

Bit 2 (Z): Zero flag

Set to "1" if the result of an arithmetic or logic operation is zero.

Bit 1 (DC): Auxiliary carry flag

Bit 0 (C): Carry flag

6.3.5 R4 (RAM Select Register)

- Bits 7 ~ 6 are not used. (Read only).
- Bits 7 ~ 6 set to “1” at all time.
- Bits 5 ~ 0 are used to select registers (Address: 0x00 ~ 0x3F) in the indirect addressing mode.
- See the Data Memory Configuration in Figure 6-3-2.

6.3.6 R5 GPR (General Purpose Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
GP	GP	GP	GP	GP	GP	GP	GP

Bits 7~0 (GP): General purpose registers

6.3.7 R6 (Port 6)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
GP	GP	P65	P64	P63	P62	P61	P60

Bits 7~6 (GP): General purpose registers

Bit 5 (P65): P65 control bit.

Bit 4 (P64): P64 control bit.

Bit 3 (P63): P63 control bit.

Bit 2 (P62): P62 control bit.

Bit 1 (P61): P61 control bit.

Bit 0 (P60): P60 control bit.

R6 is I/O register.

6.3.8 R7 GPR (General Purpose Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
GP	GP	GP	GP	GP	GP	GP	GP

This is 8-bit general-purpose register.

6.3.9 R9 IIWK (Port6 Input Change Interrupt/Wake-up control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
GP	GP	IIWK65	IIWK64	IIWK63	IIWK62	IIWK61	IIWK60

Bits 7~0 (GP): General purpose registers

Bit 5 (IIWK65): Control bit used to enable Input Change Interrupt/Wake-up of the P65 pin.

0: Disable Input Change Interrupt/Wake-up function

1: Enable Input Change Interrupt/Wake-up function

Bit 4 (IIWK64): Control bit used to enable Input Change Interrupt/Wake-up of the P64 pin.

Bit 3 (IIWK63): Control bit used to enable Input Change Interrupt/Wake-up of the P63 pin.

Bit 2 (IIWK62): Control bit used to enable Input Change Interrupt/Wake-up of the P62 pin.

Bit 1 (IIWK61): Control bit used to enable Input Change Interrupt/Wake-up of the P61 pin.

Bit 0 (IIWK60): Control bit used to enable Input Change Interrupt/Wake-up of the P60 pin.

If KTYPE bit =1, Port6 Input Change Interrupt/Wake-up function always enable.

6.3.10 RA PCH (High byte buffer of Program Counter)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
GP	GP	GP	GP	GP	GP	PC9BUF	PC8BUF

Bits 7~2 (GP): General purpose registers

Bit 1 (PC9BUF): buffer of Program Counter Bit 9

Bit 0 (PC8BUF): buffer of Program Counter Bit 8

6.3.11 RF ISR(Interrupt Status Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	EXIF	ICIF	TCIF

***Note: "1"** means with interrupt request **"0"** means no interrupt occurs*

Bits 7 ~ 3: Not used. Set to "0" at all time.

Bit 2 (EXIF): External Interrupt Flag. Set by a falling edge on /INT pin, reset by software.

Bit 1 (ICIF): Port 6 input status changed interrupt flag. Set when Port 6 input changes, reset by software.

Bit 0 (TCIF): TCC Overflow Interrupt Flag. Set when TCC overflows, reset by software.

RF can be cleared by instruction but cannot be set.

IOCF is the interrupt mask register.

NOTE

The result of reading RF is the "logic AND" of RF and IOCF.

6.3.12 R10~R3F

These are all 8-bit general-purpose registers.

6.4 Special Function Registers

6.4.1 A (Accumulator)

Internal data transfer operation, or instruction operand holding usually involves the temporary storage function of the Accumulator, which is not an addressable register.

6.4.2 CONT (Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
GP	INTEG	TS	TE	PAB	PSR2	PSR1	PSR0

Bit 7 (GP): General purpose register.

Bit 6 (INTEG): Interrupt edge select bit.

0: interrupt on the falling edge of INT pin.

1: interrupt on the rising edge of INT pin.

Bit 5 (TS): TCC signal source

0: internal instruction cycle clock, P62 is a bidirectional I/O pin

1: transition on TCC pin

Bit 4 (TE): TCC signal edge

0: increment if the transition from low to high takes place on TCC pin

1: increment if the transition from high to low takes place on TCC pin

Bit 3 (PAB): Prescaler Assigned Bit

0: TCC

1: WDT

Bits 2 ~ 0 (PSR2 ~ PSR0): TCC / WDT prescaler bits

PSR2	PSR1	PSR0	TCC Rate	WDT Rate
0	0	0	1:2	1:1
0	0	1	1:4	1:2
0	1	0	1:8	1:4
0	1	1	1:16	1:8
1	0	0	1:32	1:16
1	0	1	1:64	1:32
1	1	0	1:128	1:64
1	1	1	1:256	1:128

The CONT register is both readable and writable.

6.4.3 IOC6 (I/O Port Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	1	C65	C64	C63	C62	C61	C60

Bits 7~6: Not used, set to "1" all the time.

Bit 5 (C65): P65 I/O control register

0: defines the relative I/O pin as output

1: puts the relative I/O pin into high impedance

Bit 4 (C64): P64 I/O control register

Bit 3 (C63): P63 I/O control register

Bit 2 (C62): P62 I/O control register

Bit 1 (C61): P61 I/O control register

Bit 0 (C60): P60 I/O control register

IOC6 registers is both readable and writable.

6.4.4 IOCB/RB PDCR (Pull-down Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
GP	/PD62	/PD61	/PD60	GP	GP	GP	GP

Bit 7 (GP): General purpose register.

Bit 6 (/PD62): Control bit used to enable pull-down of the P62 pin.

0: Enable internal pull-down

1: Disable internal pull-down

Bit 5 (/PD61): Control bit used to enable pull-down of the P61 pin.

Bit 4 (/PD60): Control bit used to enable pull-down of the P60 pin.

Bits 3~0 (GP): General purpose register.

The IOCB Register is both readable and writable.

6.4.5 IOCC/RC ODCR (Open-drain Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
GP	GP	OD65	OD64	GP	OD62	OD61	OD60

Bits 7~6 (GP): General purpose registers

Bit 5 (OD65): Control bit used to enable open-drain of the P65 pin.

0: Disable open-drain output

1: Enable open-drain output

Bit 4 (OD64): Control bit used to enable open-drain of the P64 pin.

Bit 3 (GP): General purpose register.

Bit 2 (OD62): Control bit used to enable open-drain of the P62 pin.

Bit 1 (OD61): Control bit used to enable open-drain of the P61 pin.

Bit 0 (OD60): Control bit used to enable open-drain of the P60 pin.

The IOCC Register is both readable and writable.

6.4.6 IOCD/RD PHCR(Pull-high Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
GP	GP	/PH65	/PH64	GP	/PH62	/PH61	/PH60

Bits 7~6 (GP): General purpose registers

Bit 5 (/PH65): Control bit used to enable pull-high of the P65 pin.

0: Enable internal pull-high

1: Disable internal pull-high

Bit 4 (/PH64): Control bit used to enable pull-high of the P64 pin.

Bit 3 (GP): General purpose register.

Bit 2 (/PH62): Control bit used to enable pull-high of the P62 pin.

Bit 1 (/PH61): Control bit used to enable pull-high of the P61 pin.

Bit 0 (/PH60): Control bit used to enable pull-high of the P60 pin.

The IOCD Register is both readable and writable.

6.4.7 IOCE/R8 (WDT Control Register)

ENHS(opt.)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	WDTE	EIS	GP	GP	GP	GP	GP	GP
0	WDTE	EIS	GP	GP	GP	/PD65	/PD64	/PD63

Bit 7 (WDTE): Control bit used to enable the Watchdog timer.

0: Disable WDT

1: Enable WDT

WDTE is both readable and writable.

Bit 6 (EIS): Control bit is used to define the function of P60 (/INT) pin.

0: P60, bidirectional I/O pin.

1: /INT, external interrupt pin. In this case, the I/O control bit of P60 (Bit 0 of IOC6) must be set to "1."

When EIS is "0," the path of /INT is masked. When EIS is "1," the status of the /INT pin can also be read by way of reading Port 6 (R6). For reference, see Figure 6-5 under Section 6.6.

EIS is both readable and writable.

Bits 5~3: Not used. Set to “0” at all time.

If ENHS bit = 1

Bits 2~0: General purpose register.

If ENHS bit = 0

Bit 2 (/PD65): Control bit used to enable pull-down of the P65 pin.

0: Enable internal pull-down

1: Disable internal pull-down

Bit 1 (/PD64): Control bit used to enable pull-down of the P64 pin.

Bit 0 (/PD63): Control bit used to enable pull-down of the P63 pin.

6.4.8 IOCF/RE (Interrupt Mask Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/INT	GP	GP	GP	GP	EXIE	ICIE	TCIE

Bit 7 (/INT): Interrupt Enable flag. If KTYPE Bit = 0

0: BC RE, 7

1: BS RE, 7

Bits 6 ~ 3 (GP): General purpose register.

Bit 2 (EXIE): EXIF interrupt enable bit

0: disable EXIF interrupt

1: enable EXIF interrupt

Bit 1 (ICIE): ICIF interrupt enable bit

0: disable ICIF interrupt

1: enable ICIF interrupt

Bit 0 (TCIE): TCIF interrupt enable bit

0: disable TCIF interrupt

1: enable TCIF interrupt

The IOCF register is both readable and writable.

6.5 TCC/WDT and Prescaler

There is an 8-bit counter available as prescaler for the TCC or WDT. The prescaler is available for the TCC only or the WDT only at the same time and the PAB bit of the CONT register is used to determine the prescaler assignment. The PSR0 ~ PSR2 bits determine the ratio. The prescaler is cleared each time the instruction is written to TCC under TCC mode. The WDT and prescaler, when assigned to WDT mode, are cleared by the “WDTC” or “SLEP” instructions. Figure 6-4 depicts the circuit diagram of TCC / WDT.

- R1 (TCC) is an 8-bit timer / counter. The TCC clock source can be internal or external clock input (edge selectable from TCC pin). If the TCC signal source is from an internal clock, TCC will be incremented by 1 at every instruction cycle (without prescaler). Referring to Figure 6-3, CLK = F_{OSC} / 2, CLK = F_{OSC} / 4 or CLK = F_{OSC} / 8 depends on the Code Option bit CLK[1:0]. CLK = F_{OSC} / 2 is used if CLK[1:0] is set to "10", CLK = F_{OSC} / 4 is used if CLK[1:0] is set to "11", and CLK[1:0] = F_{OSC} / 8 is used if CLK[1:0] is set to "0x". If the TCC signal source is from an external clock input, TCC is incremented by 1 at every falling edge or rising edge of the TCC pin.
- The Watchdog Timer is a free running on-chip RC oscillator. The WDT will keep running even when the oscillator driver has been turned off (i.e. in sleep mode). During normal operation or sleep mode, a WDT time-out (if enabled) will cause the device to reset. The WDT can be enabled or disabled any time during normal mode by software programming. Refer to WDTE bit of the IOCE register. Without prescaler, the WDT time-out period is approximately 18 ms[1] (default).

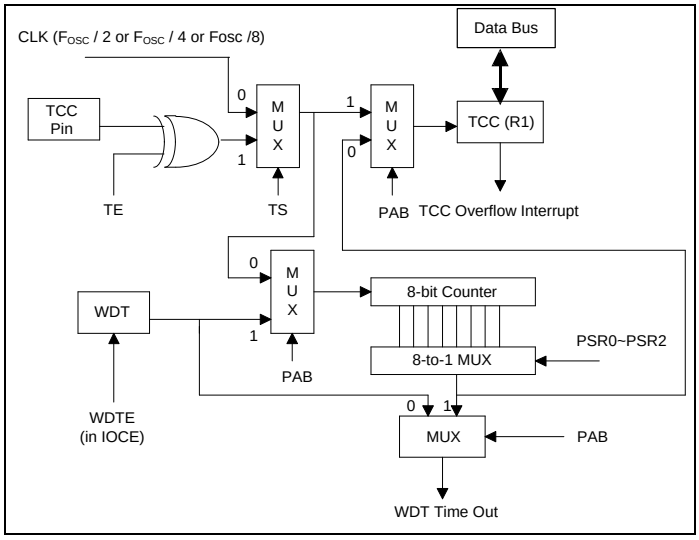
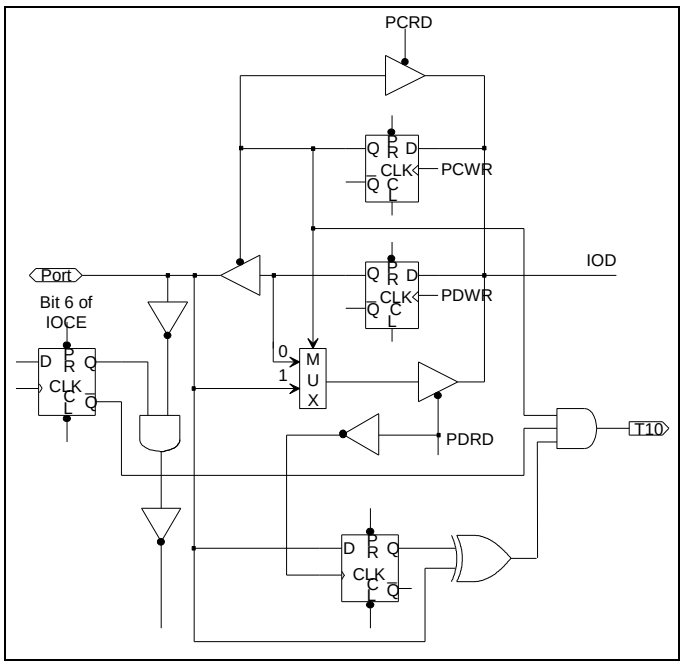


Figure 6-4 TCC and WDT Block Diagram

[1] Vdd = 5V, set up time period = 16.5ms ± 30% at 25°C
Vdd = 3V, set up time period = 18ms ± 30% at 25°C

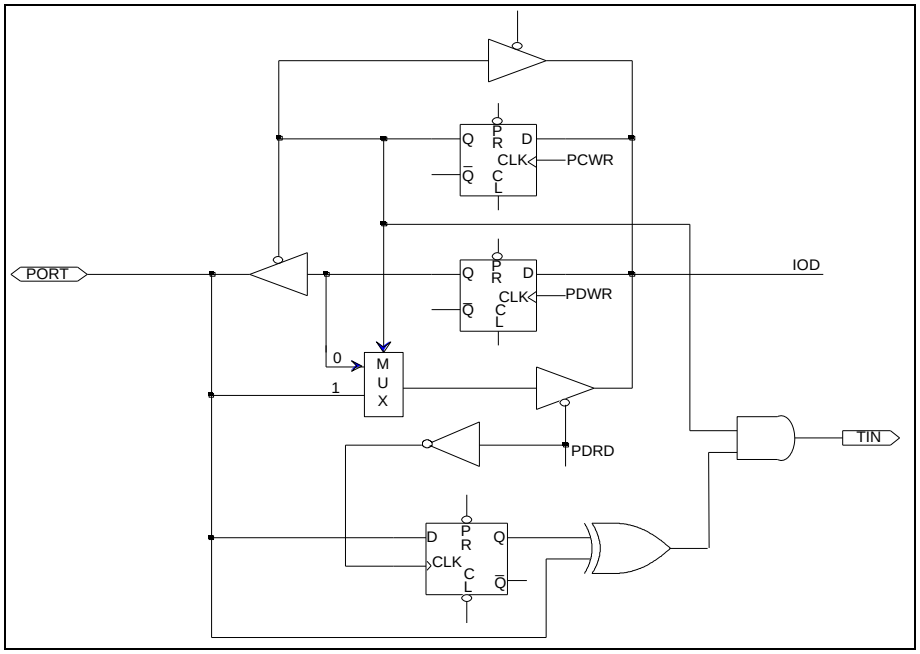
6.6 I/O Ports

The I/O register, port 6, is bidirectional tri-state I/O port. Port 6 can be pulled-high internally by software except P63. In addition, Port 6 can also have open-drain output by software except P63. Input status changed interrupt (or wake-up) function is available from Port 6. P60 ~ P62 pins can be pulled-down by software. Each I/O pin can be defined as "input" or "output" pin by the I/O control register (IOC6) except P63. The I/O registers and I/O control registers are both readable and writable. The I/O interface circuits for Port 6 are shown in Figure 6-5 ~ Figure 6-7 respectively.



Note: Pull-high (down) and open-drain are not shown in the figure.

Figure 6-5 I/O Port and I/O Control Register Circuit for P60 (/INT)



Note: Pull-high (down) and open-drain are not shown in the figure.

Figure 6-6 I/O Port and I/O Control Register Circuit for P61~P62, P64~P65

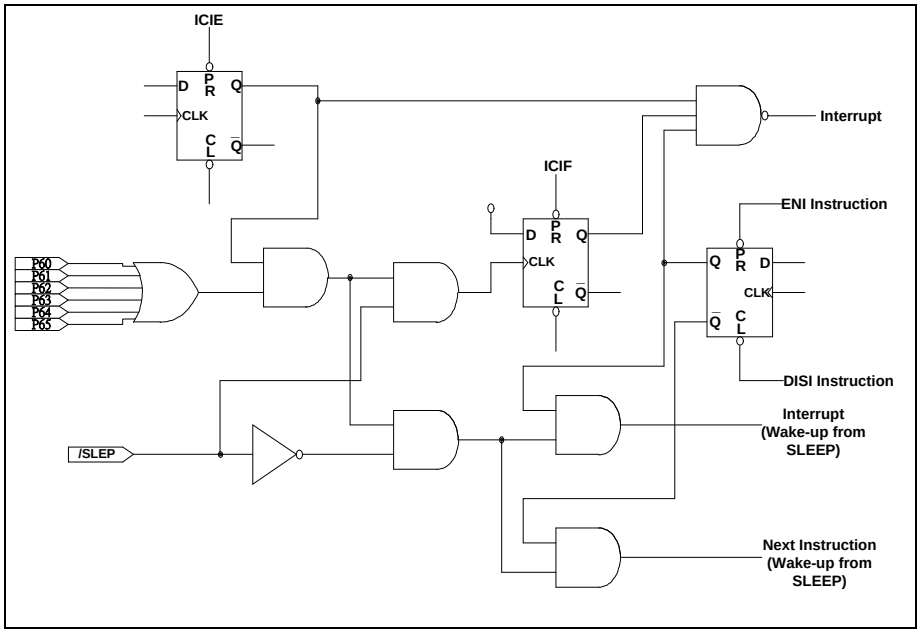


Figure 6-7 Block Diagram of I/O Port 6 with input change interrupt/wake-up

Table 6-1 Usage of Port 6 Input Change Wake-up / Interrupt Function

Usage of Port 6 Input Status Change Wake-up/Interrupt	
(I) Wake-up from Port 6 Input Status Change (a) Before Sleep 1. Disable WDT 2. Read I/O Port 6 (MOV R6,R6) 3. Execute "ENI" or "DISI" 4. Enable interrupt (Set IOCF.1) 5. Execute "SLEP" instruction (b) After Wake-up 1. IF "ENI" → Interrupt vector (008H) 2. IF "DISI" → Next instruction	(II) Port 6 Input Status Change Interrupt 1. Read I/O Port 6 (MOV R6,R6) 2. Execute “ENI” 3. Enable interrupt (Set IOCF.1) 4. IF Port 6 change (interrupt) → Interrupt vector (008H)

6.7 Reset and Wake-up

6.7.1 Reset

A Reset is initiated by one of the following events:

1) Power-on reset

2) /RESET pin input "low"

3) WDT time-out (if enabled)

4) Low Voltage Reset

The device is kept under reset condition for a period of approximately 18ms[2] (one oscillator start-up timer period) after a reset is detected. Once a Reset occurs, the following functions are performed:

- The oscillator is running, or will be started.
- The Program Counter (R2) is set to all "0."
- All I/O port pins are configured as input mode (high-impedance state)
- The Watchdog timer and prescaler are cleared.
- When power is switched on, the upper 3 bits of R3 are cleared.
- The bits of the CONT register are set to all "1" except for Bit 6 (INT flag).
- The bits of the IOCB register are set to all "1."
- The IOCC register is cleared.
- The bits of the IOCD register are set to all "1."
- Bit 7 of the IOCE register is set to "1," and Bits 4 and 6 are cleared.
- Bits 0 ~ 2 of RF and Bits 0 ~ 2 of IOCF registers are cleared.

The Sleep (power down) mode is asserted by executing the “SLEP” instruction. While entering Sleep mode, WDT (if enabled) is cleared but keeps on running.

The controller can be awakened by:

1) External reset input on /RESET pin

2) WDT time-out (If enabled)

3) Port 6 Input Status changed (If enabled)

The first two cases will cause the EM78P151 to reset. The T and P flags of R3 are used to determine the source of the reset (wake-up). The last case is considered the continuation of program execution and the global interrupt ("ENI" or "DISI" being executed) determines whether or not the controller branches to the interrupt vector following a wake-up. If ENI is executed before SLEP, the instruction will begin to execute from Address 008H after wake-up. If DISI is executed before SLEP, the

[2] Vdd = 5V, set up time period = 16.8ms ± 30%
Vdd = 3V, set up time period = 18ms ± 30%

operation will restart from the succeeding instruction right next to SLEP after a wake-up.

Only one of Cases 2 and 3 can be enabled before going into the Sleep mode. That is,

[a] If Port 6 Input Status Change Interrupt is enabled before SLEP, WDT must be disabled by software. Hence, the EM78P151 can be awakened only by Case 1 or Case 3.

[b] If WDT is enabled before SLEP, Port 6 Input Status Change Interrupt must be disabled. Hence, the EM78P151 can be awakened only by Case 1 or Case 2. Refer to Section 7.6, *Interrupt* for further details.

If Port 6 Input Status Change Interrupt is used to wake-up the EM78P151 (Case [a] above), the following instructions must be executed before SLEP:

```
MOV A, @xxxx1110b     ; Select the WDT prescaler, it must be
                      ; set over 1:1
CONTW
WDTC                  ; Clear WDT and prescaler
MOV A, @0xxxxxxxb     ; Disable WDT
IOW RE
MOV R6, R6            ; Read Port 6
MOV A, @00000x1xb     ; Enable Port 6 input change interrupt
IOW RF
ENI (or DISI)         ; Enable (or disable) global interrupt
SLEP                  ; Sleep
```

NOTE

1. After waking up from sleep mode, WDT is automatically enabled. The WDT enable / disable operation after waking up from sleep mode should be appropriately defined in the software.

2. To avoid a reset from occurring when the Port 6 Input Status Changed Interrupt enters into interrupt vector or is used to wake-up the MCU, the WDT prescaler must be set above the 1:1 ratio.

6.7.2 Register Initial Values after Reset

Legend: ***x:*** *Not used* ***P:*** *Previous value before reset*
U: *Unknown or don't care* ***t:*** *Check table on "Reset Type" in Section 6.4.3*

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0×00	R0 IAR	Bit Name	-	-	-	-	-	-	-	-
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×01	R1 TCC	Bit Name	-	-	-	-	-	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×02	R2 PC	Bit Name	-	-	-	-	-	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	Jump to Address 0x08 or continue to execute next instruction							
0×03	R3 SR	Bit Name	RST	GP1	GP0	T	P	Z	DC	C
		Power-on	0	0	0	1	1	U	U	U
		/RESET and WDT	0	0	0	*	*	P	P	P
		Wake-up from Pin Change	1	P	P	*	*	P	P	P
0×04	R4 RSR	Bit Name	GP1	GP0	-	-	-	-	-	-
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×05	R5 GPR	Bit Name	GP	GP	GP	GP	GP	GP	GP	GP
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×06	R6 P6	Bit Name	GP	GP	P65	P64	P63	P62	P61	P60
		Power-on	U	U	1	1	1	1	1	1
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0X07	R7 GPR	Bit Name	GP	GP	GP	GP	GP	GP	GP	GP
		Power-on	U	U	U	U	U	U	U	U
		/RESET and	P	P	P	P	P	P	P	P

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		WDT								
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0E	IOCE (ENHS=1)	Bit Name	WDTE	EIS	GP	GP	GP	GP	GP	GP
		Power-on	1	0	U	U	U	U	U	U
		/RESET and WDT	1	0	P	P	P	P	P	P
		Wake-up from Pin Change	1	P	P	P	P	P	P	P
0X08	R8 WDTCR	Bit Name	WDTE	EIS	GP	GP	GP	/PD65	/PD64	/PD63
		Power-on	1	0	U	U	U	1	1	1
		/RESET and WDT	1	0	P	P	P	1	1	1
		Wake-up from Pin Change	1	P	P	P	P	P	P	P
0X09	R9 IIWK (KTYPE =0)	Bit Name	GP	GP	IIWK65	IIWK64	IIWK63	IIWK62	IIWK61	IIWK60
		Power-on	U	U	0	0	0	0	0	0
		/RESET and WDT	P	P	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0X09	R9 GPR (KTYPE =1)	Bit Name	GP	GP	GP	GP	GP	GP	GP	GP
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0X0A	RA PCHBUF	Bit Name	GP	GP	GP	GP	GP	GP	PC9BUF	PC8BUF
		Power-on	U	U	U	U	U	U	0	0
		/RESET and WDT	P	P	P	P	P	P	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0X0A	RA GPR (KTYPE =1)	Bit Name	GP	GP	GP	GP	GP	GP	GP	GP
		Power-on	U	U	U	U	U	U	U(0)	U(0)
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0X0B	RB PDCR	Bit Name	GP	/PD62	/PD61	/PD60	GP	GP	GP	GP
		Power-on	U	1	1	1	U	U	U	U
		/RESET and WDT	P	1	1	1	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0X0C	RC ODCR	Bit Name	GP	GP	OD65	OD64	GP	OD62	OD61	OD60
		Power-on	U	U	0	0	U	0	0	0
		/RESET and WDT	P	P	0	0	P	0	0	0
		Wake-up from	P	P	P	P	P	P	P	P

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Pin Change								
0X0D	RD PHCR	Bit Name	GP	GP	/PH65	/PH64	GP	/PH62	/PH61	/PH60
		Power-on	U	U	1	1	U	1	1	1
		/RESET and WDT	P	P	1	1	P	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0E	RE IMR (KTYPE=1)	Bit Name	GP	GP	GP	GP	GP	EXIE	ICIE	TCIE
		Power-on	U(0)	U	U	U	U	0	0	0
		/RESET and WDT	P	P	P	P	P	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0X0E	RE IMR (KTYPE=0)	Bit Name	/INT	GP	GP	GP	GP	EXIE	ICIE	TCIE
		Power-on	0	U	U	U	U	0	0	0
		/RESET and WDT	0	P	P	P	P	0	0	0
		Wake-up from Pin Change	0	P	P	P	P	P	P	P
0×0F	RF ISR	Bit Name	×	×	×	×	×	EXIF	ICIF	TCIF
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	0	0	0	0	0	P	N	P
N/A	CONT (KTYPE=1)	Bit Name	GP	/INT	TS	TE	PAB	PSR2	PSR1	PSR0
		Power-on	U	0	1	1	1	1	1	1
		/RESET and WDT	P	0	1	1	1	1	1	1
		Wake-up from Pin Change	P	0	P	P	P	P	P	P
N/A	CONT (KTYPE=0)	Bit Name	GP	INTEG	TS	TE	PAB	PSR2	PSR1	PSR0
		Power-on	U	0	1	1	1	1	1	1
		/RESET and WDT	P	0	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×06	IOC6	Bit Name	-	-	C65	C64	C63	C62	C61	C60
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0X0B	IOCB	Bit Name	GP	/PD62	/PD61	/PD60	GP	GP	GP	GP
		Power-on	U	1	1	1	U	U	U	U
		/RESET and WDT	P	1	1	1	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
		Bit Name	GP	GP	OD65	OD64	GP	OD62	OD61	OD60
		Power-on	U	U	0	0	U	0	0	0

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0×0C	IOCC	/RESET and WDT	P	P	0	0	P	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0D	IOCD	Bit Name	GP	GP	/PH65	/PH64	GP	/PH62	/PH61	/PH60
		Power-on	U	U	1	1	U	1	1	1
		/RESET and WDT	P	P	1	1	P	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0E	IOCE (ENHS=1)	Bit Name	WDTE	EIS	GP	GP	GP	GP	GP	GP
		Power-on	1	0	U	U	U	U	U	U
		/RESET and WDT	1	0	P	P	P	P	P	P
		Wake-up from Pin Change	1	P	P	P	P	P	P	P
0×0E	IOCE (ENHS=0)	Bit Name	WDTE	EIS	GP	GP	GP	/PD65	/PD64	/PD63
		Power-on	1	0	U	U	U	1	1	1
		/RESET and WDT	1	0	P	P	P	1	1	1
		Wake-up from Pin Change	1	P	P	P	P	P	P	P
0×0F	IOCF (KTYPE=1)	Bit Name	GP	GP	GP	GP	GP	EXIE	ICIE	TCIE
		Power-on	U(0)	U	U	U	U	0	0	0
		/RESET and WDT	P	P	P	P	P	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0F	IOCF (KTYPE=0)	Bit Name	/INT	GP	GP	GP	GP	EXIE	ICIE	TCIE
		Power-on	0	U	U	U	U	0	0	0
		/RESET and WDT	0	P	P	P	P	0	0	0
		Wake-up from Pin Change	0	P	P	P	P	P	P	P
0×10 ~ 0×3F	R10~R3F	Bit Name	-	-	-	-	-	-	-	-
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P

6.7.3 Status of T and P of the Status Register

A Reset condition is initiated by the following events

1) A power-on condition

2) A high-low-high pulse on /RESET pin

3) Watchdog timer time-out

The values of T and P listed in the table below are used to check how the processor wakes up.

Table 6-2 Values of RST, T, and P after a Reset

Reset Type	RST	T	P
Power on	0	1	1
/RESET during Operating mode	0	*P	*P
/RESET wake-up during Sleep mode	0	1	0
WDT during Operating mode	0	0	*P
WDT wake-up during Sleep mode	0	0	0
Wake-up on pin change during Sleep mode	1	1	0

* *P: Previous status before reset*

The following table shows the events that may affect the status of T and P.

Table 6-3 Status of T and P Being Affected by Events

Event	RST	T	P
Power on	0	1	1
WDTC instruction	*P	1	1
WDT time-out	0	0	*P
SLEP instruction	*P	1	0
Wake-up on pin change during Sleep mode	1	1	0

* ***P:*** *Previous status before reset*

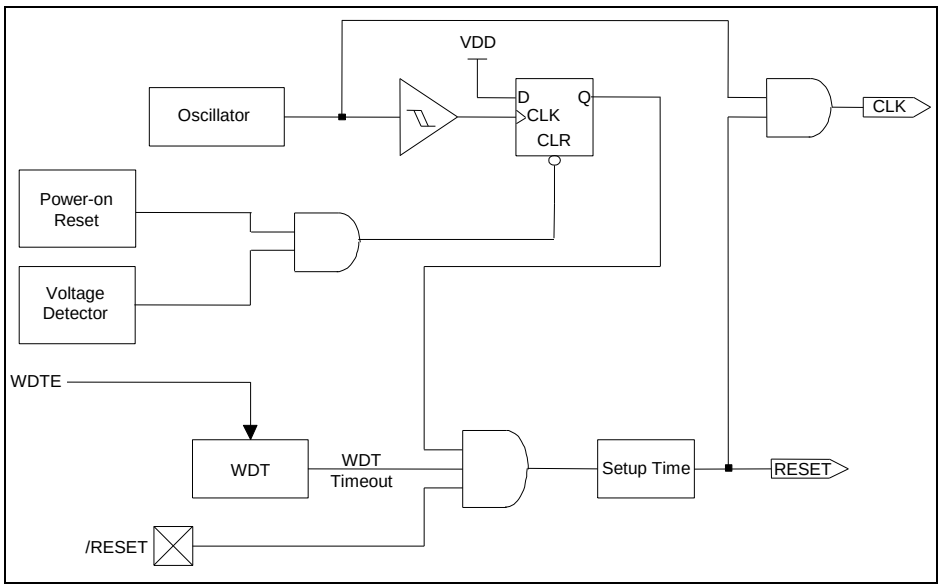


Figure 6-8 Controller Reset Block Diagram

6.8 Interrupt

The EM78P151 has three falling-edge interrupts as listed herewith:

1) TCC overflow interrupt

2) Port 6 Input Status Change Interrupt

3) External interrupt [(P60, /INT) pin]

Before the Port 6 Input Status Changed Interrupt is enabled, reading Port 6 (e.g. "MOV R6, R6") is necessary. Each pin of Port 6 will have this feature if its status changes. Any pin configured as output or P60 pin configured as /INT is excluded from this function. The Port 6 Input Status Changed Interrupt can wake up the EM78P151 from Sleep mode if Port 6 is enabled prior to going into Sleep mode by executing SLEP instruction. When the chip wakes-up, the controller will continue to execute the program in-line if the global interrupt is disabled. If the global interrupt is enabled, it will branch to the interrupt Vector 008H.

RF is the interrupt status register that records the interrupt requests in the relative flags / bits. IOCF is an interrupt mask register. The global interrupt is enabled by the ENI instruction and is disabled by the DISI instruction. When one of the interrupts (enabled) occurs, the next instruction will be fetched from Address 008H. Once in the interrupt service routine, the source of an interrupt can be determined by polling the flag bits in RF. The interrupt flag bit must be cleared by instructions before leaving the interrupt service routine before interrupts are enabled to avoid recursive interrupts.

The flag (except ICIF bit) in the Interrupt Status Register (RF) is set regardless of the status of its mask bit or the execution of ENI. Note that the outcome of RF will be the logic AND of RF and IOCF (refer to Figure 6-9). The RETI instruction ends the interrupt routine and enables the global interrupt (the execution of ENI).

When an interrupt is generated by the INT instruction (enabled), the next instruction will be fetched from Address 001H.

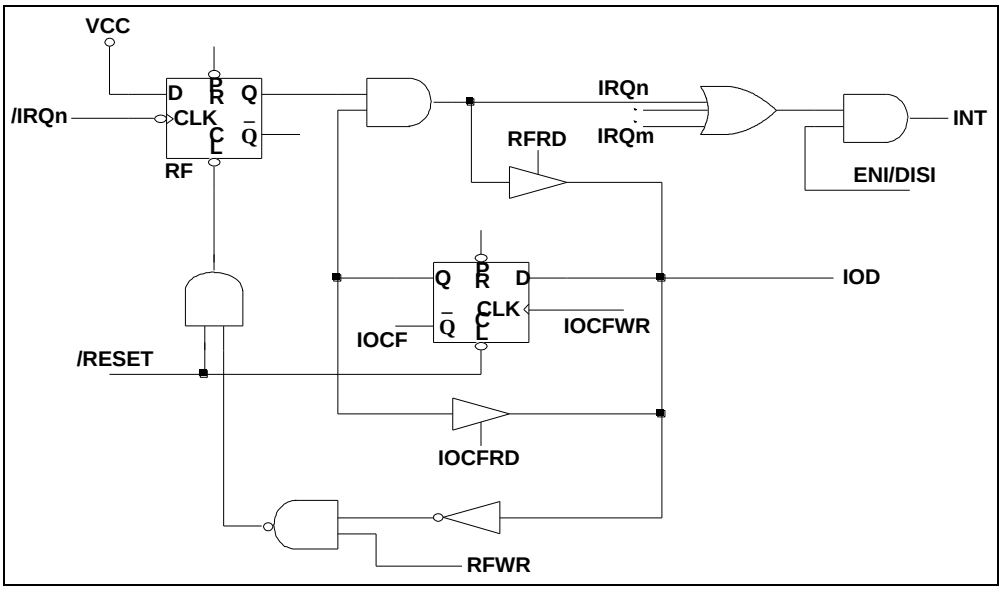


Figure 6-9 Interrupt Input Circuit

6.9 Oscillator

6.9.1 Oscillator Modes

The EM78P151 can be operated in four different oscillator modes, such as External RC oscillator mode (ERC), Internal RC oscillator mode (IRC), High Crystal oscillator mode (HXT), and Low Crystal oscillator mode (LXT). The desired mode can be selected by programming OSC2 ~ OSC0 in the Code Option register. Table 6-4 describes how these oscillator modes are defined.

Table 6-4 Oscillator Modes Defined by OSC

Oscillator Modes	RCOUT	OSC1	OSC0
LXT (Low crystal oscillator mode, Freq. range is over 400 kHz)	x	0	0
HXT (High crystal oscillator mode, Freq. range is above 400 kHz)	x	0	1
ERC[1] (External RC oscillator mode); P64/RCOUT act as P64	0	1	0
ERC[1] (External RC oscillator mode); P64/RCOUT act as RCOUT	1	1	0
IRC[2] (Internal RC oscillator mode); P64/RCOUT act as P64	0	1	1
IRC[2] (Internal RC oscillator mode); P64/RCOUT act as RCOUT	1	1	1

[1] In ERC mode, ERCin is used as oscillator pin. RCOUT/P64 is defined by code option Word 1 Bits 3 ~ 1.
[2] In IRC mode, P64 is normal I/O pin. RCOUT/P64 is defined by code option Word 1 Bits 3 ~ 1.

The maximum operational frequency of the crystal/resonator under different V_{DD} is listed below.

Table 6-5 Summary of Maximum Operating Speeds

Conditions	V_{DD}	Max Freq. (MHz)
Two cycles with two clocks	2.3	4.0
	3.0	8.0
	5.0	20.0

6.9.2 Crystal Oscillator/Ceramic Resonators (Crystal)

The EM78P151 can be driven by an external clock signal through the OSCI pin as shown in the following figure.

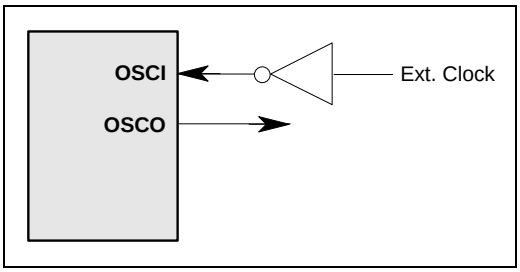


Figure 6-10 Circuit for External Clock Input

In most applications, pin OSCI and pin OSCO can be connected with a crystal or ceramic resonator to generate oscillation. Figure 6-11 depicts such a circuit. The same thing applies whether it is in the HXT mode or in the LXT mode.

In Figure 6-11-1, when the connected resonator in OSCI and OSCO is used in applications, the 1 MΩ R1 needs to be shunted with resonator.

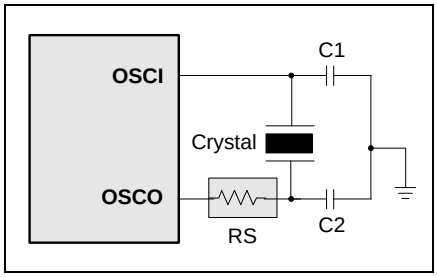


Figure 6-11 Circuit for Crystal/Resonator

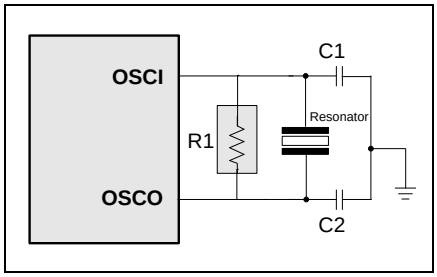


Figure 6-11-1 Circuit for Crystal/Resonator

The following table provides the recommended values of C1 and C2. Since each resonator has its own attribute, refer to its specification for appropriate values of C1 and C2. RS, a serial resistor, may be necessary for the AT strip cut crystal or low frequency mode.

Table 6-6 Capacitor Selection Guide for Crystal Oscillator or Ceramic Resonator

Oscillator Type	Frequency Mode	Frequency	C1 (pF)	C2 (pF)
Ceramic Resonators	HXT	455 kHz	100 ~ 150	100 ~ 150
		2.0 MHz	20 ~ 40	20 ~ 40
		4.0 MHz	10 ~ 30	10 ~ 30
Crystal Oscillator	LXT	32.768 kHz	25	15
		100 kHz	25	25
		200 kHz	25	25
	HXT	455 kHz	20 ~ 40	20 ~ 150
		1.0 MHz	15 ~ 30	15 ~ 30
		2.0 MHz	15	15
		4.0 MHz	15	15

Note: The values of capacitors C1 and C2 are for reference only

6.9.3 External RC Oscillator Mode

For some applications that do not require a very precise timing calculation, the RC oscillator (Figure 6-12) offers a cost-effective oscillator configuration. Nevertheless, it should be noted that the frequency of the RC oscillator is influenced by the supply voltage, the values of the resistor (R_{EXT}), the capacitor (C_{EXT}), and even by the operation temperature. Moreover, the frequency also changes slightly from one chip to another due to manufacturing process variations.

In order to maintain a stable system frequency, the values of the C_{EXT} should not be lesser than 20pF, and that the value of R_{EXT} should not be greater than 1 MΩ. If they cannot be kept in this range, the frequency can be easily affected by noise, humidity, and leakage.

The smaller the R_{EXT} in the RC oscillator is, the faster its frequency will be. On the contrary, for very low R_{EXT} values, for instance, 1 kΩ, the oscillator becomes unstable because the NMOS cannot discharge the current of the capacitance correctly.

Based on the above reasons, it must be kept in mind that all of the supply voltage, the operation temperature, the components of the RC oscillator, the package types, the way the PCB is layout, will affect the system frequency.

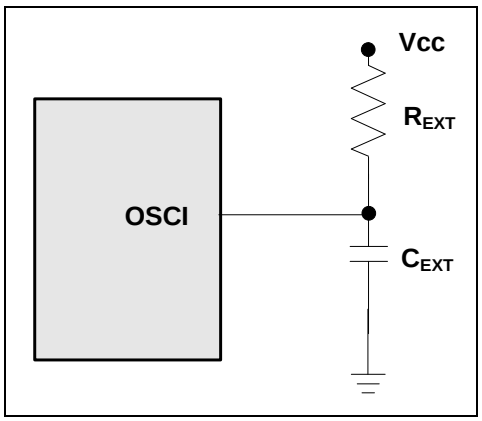


Figure 6-12 External RC Oscillator Mode Circuit

Table 6-7 RC Oscillator Frequencies

C_{EXT}	R_{EXT}	Average F_{OSC} 5V, 25°C	Average F_{OSC} 3V, 25°C
20 pF	3.3 kΩ	3.92 MHz	3.65 MHz
	5.1 kΩ	2.67 MHz	2.60 MHz
	10 kΩ	1.4 MHz	1.40 MHz
	100 kΩ	150 kHz	156 kHz
100 pF	3.3 kΩ	1.4 MHz	1.33 MHz
	5.1 kΩ	940 kHz	917 kHz
	10 kΩ	476 kHz	480 kHz
	100 kΩ	50 kHz	52 kHz
300 pF	3.3 kΩ	595 kHz	570 kHz

C_{EXT}	R_{EXT}	Average F_{OSC} 5V, 25°C	Average F_{OSC} 3V, 25°C
	5.1 kΩ	400 kHz	384 kHz
	10 kΩ	200 kHz	203 kHz
	100 kΩ	20.9 kHz	20 kHz

Note: [1]*: These are measured in DIP packages*

[2]*. The values are for design reference only*

[3]*. The frequency drift is ±30%*

6.9.4 Internal RC Oscillator Mode

EM78P151 offers a versatile internal RC mode with default frequency value of 4 MHz. The Internal RC oscillator mode has other frequencies (1 MHz, 8 MHz and 455 kHz) that can be set by Code Option (Word 1), RCM1, and RCM0. All these four main frequencies can be calibrated by programming the Option Bits CT0 ~ CT3, RT0 ~ RT3. The table below describes the EM78P151 internal RC drift with variation of voltage, temperature, and process.

Table 6-8 Internal RC Drift Rate (T_A = 25°C, V_{DD} = 5V, V_{SS} = 0V)

Internal RC Freq.	Drift Rate			
	Temp. (0°C ~ 70°C)	Voltage	Process	Total
4 MHz	± 1.5%	± 1% @ 2.0V ~ 5.5V	± 1%	± 3.5%
8 MHz	± 1.5%	± 1.5% @ 2.0V ~ 5.5V	± 1%	± 4%
1 MHz	± 1.5%	± 1% @ 2.0V ~ 5.5V	± 1%	± 3.5%
455 kHz	± 1.5%	± 1% @ 2.0V ~ 5.5V	± 1%	± 3.5%

Note: *These are theoretical values provided for reference only. Actual values may vary depending on the actual process.*

6.10 Power-on Considerations

Any microcontroller is not guaranteed to start to operate properly before the power supply stabilizes at its steady state. Under customer application, when power is OFF, V_{DD} must drop to below 1.8V and remains OFF for 10 µs before power can be switched ON again. This way, the EM78P151 will reset and operate normally. The extra external reset circuit will work well if V_{DD} can rise at very fast speed (50ms or less). However, under most cases where critical applications are involved, extra devices are required to assist in solving the power-up problems.

6.10.1 Programmable Oscillator Set-up Time

The Option word contains SUT0 and SUT1 which can be used to define the oscillator set-up time. Theoretically, the range is from 4.5ms to 72ms. For most of crystal or ceramic resonators, the lower the operation frequency, the longer the Set-up time may be required. Table 12 describes the values of the Oscillator Set-up Time.

6.10.2 External Power-on Reset Circuits

The circuitry in the figure implements an external RC to produce the reset pulse. The pulse width (time constant) should be kept long enough for V_{DD} to reach minimum operation voltage. This circuit is used when the power supply has a slow rise time.

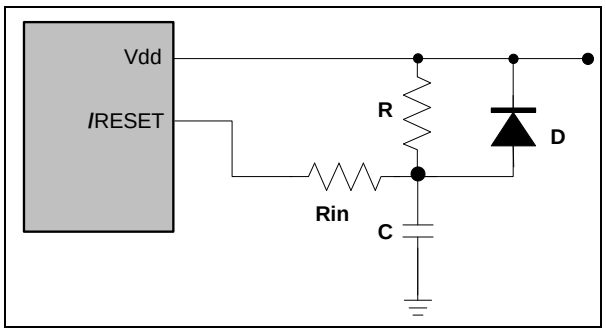


Figure 6-13 External Power-up Reset Circuit

Since the current leakage from the /RESET pin is ± 5 µA, it is recommended that R should not be greater than 40k. In this way, the /RESET pin voltage is held below 0.2V. The diode (D) acts as a short circuit at the moment of power down. The capacitor C will discharge rapidly and fully. R_{IN}, the current-limited resistor, will prevent high current or ESD (electrostatic discharge) from flowing to pin /RESET.

6.10.3 Residue-Voltage Protection

When the battery is replaced, the device power (V_{DD}) is cut off but residue-voltage remains. The residue-voltage may trip below the minimum V_{DD}, but not to zero. This condition may cause a poor power-on reset. The following figures illustrate two recommended methods on how to build a residue-voltage protection circuit for the EM78P151.

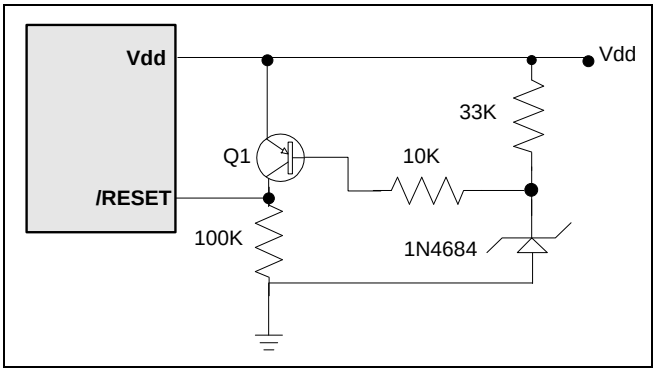


Figure 6-14 Residue Voltage Protection Circuit 1

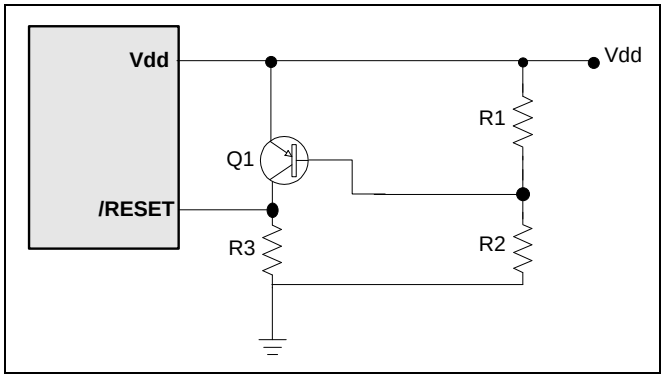


Figure 6-15 Residue Voltage Protection Circuit 2

Note

Figure 6-14 and Figure 6-15 should be designed to ensure that the voltage of the /RESET pin is larger than VIH (min).

6.11 Code Option

The EM78P151 has three Code option words and one Customer ID word that are not part of the normal program memory.

Word 0	Word1	Word 2	Word 3
Bit 12 ~ Bit 0	Bit 12 ~ Bit 0	Bit 12 ~ Bit 0	Bit 12 ~ Bit 0

6.11.1 Code Option Register (Word 0)

Word 0											
Bit	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2 ~ 0**
Mnemonic	RESETEN	ENWDT	CLKS0	LVR1	LVR0	-	WDTPS1	WDTPS0	WDTPS	CLKS1	Protect
1	Disable	Disable	High	High	High	-	High	High	High	High	Disable
0	Enable	Enable	Low	Low	Low	-	Low	Low	Low	Low	Enable

Bit 12 (RESETEN): Define Pin 63 as a reset pin

0: /RESET enable (only Schmitt trigger)

1: /RESET disable

Bit 11 (ENWDT): Watchdog timer enable bit

0: Enable

1: Disable

Bit 10 (CLKS0): Instruction period option bit.

Refer to the Instruction Set section.

CLKS1	CLKS0	Instruction Period
1	1	Fosc/4
1	0	Fosc/2
0	1	Fosc/8
0	0	Fosc/8

Bits 9 ~ 8 (LVR1 ~ LVR0): Low Voltage Reset control bits

LVR1, LVR0	VDD Reset Level	VDD Release Level
11	NA (Power-on Reset) (default)	
10	2.7V	2.9V
01	3.5V	3.7V
00	4.0V	4.2V

Refer to the Instruction Set section.

Bit 7: Not used, set it to “1” all the time.

Bits 6 ~ 4 (WDTPS1, WDTPS0, WDTPS): WDT Time-out Period of device bits.

WDTPS1	WDTPS0	WDTPS	Warm up time from POR, LVR Condition: IRC, ERC	Warm up time from /RESET, WDTO Condition: IRC, ERC	Warm up time from /RESET, WDTO Condition: XT	*WDT Time-out Period or Warm up time from POR, LVR Condition: XT
1	1	1	18 ms	IRC or ERC *8 clocks	HXT * 510 LXT * 254	18 ms
1	0	1	4.5 ms	IRC or ERC *8 clocks	HXT * 510 LXT * 254	4.5 ms
0	1	1	288 ms	IRC or ERC *8 clocks	HXT * 510 LXT * 254	288 ms
0	0	1	72 ms	IRC or ERC *8 clocks	HXT * 510 LXT * 254	72 ms

Note: These are theoretical values, provided for reference only

Bit 3 (CLKS1): Instruction period option bit ii.

Refer to the Instruction Set section.

CLKS1	CLKS0	Instruction period
1	1	Fosc/4
1	0	Fosc/2
0	1	Fosc/8
0	0	Fosc/8

Bits 2 ~ 0 (Protect): Protect Bits. Each protect status is as follows:

Protect Bits	Protect
0	Enable
1	Disable (Default)

6.11.2 Code Option Register (Word 1)

Word 1													
Bit	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Mnemonic	-	KTYPE	DisSMT	EnSMT	ENHS	-	RCM1	RCM0	-	RCOUT	OSC1	OSC0	-
1	-	Type A	Schmitt	Inverter	Normal	-	High	High	-	High	High	High	-
0	-	Type B	Inverter	Schmitt	Enhance	-	Low	Low	-	Low	Low	Low	-

Bit 12: Not used, set to “0” all the time.

Bit 11 (KTYPE): Kernel type selection

0: Type B

1: Type A (default)

	KTYPE = 0	KTYPE = 1
Reset Address	0X3FF	0X000
S/W Interrupt Vector	0x002	0x001
PC: A8, A9 **Any instruction written to R2**	A8, A9 from PCHBUF bit1,0	ENHS=1, A8,A9 =0 ENHS=0, "ADD R2, A" allows a relative address to be added to the current PC, and the ninth and above bits of the PC will increase progressively.
CONT BIT6	INTEG	/INT
IOCF/RE BIT7	/INT	General purpose register
R9 BIT5~0	IIWK65~IIWK60 (Input Change Interrupt/Wake-up)	General purpose register
RA BIT1~0	PC9BUF~PC8BUF (buffer of Program Counter Bits 9,8)	General purpose register

Bit 10 (DISSMT): P60~P62, P63 Schmitt trigger disable

0: Inverter

1: Schmitt trigger

Bit 9 (ENSMT): P64 and P65 Schmitt trigger enable

0: Schmitt trigger

1: Inverter

Bit 8 (ENHS): Function Enhance selection

0: Enhance mode.

A. 6 pin Pull-low function (/PD60 ~ /PD65)

B. "ADD R2, A" allows a relative address to be added to the current PC, and the ninth and above bits of the PC will increase progressively.

1: Normal mode.

A. 3 pin Pull-low function (/PD60 ~ /PD62).

B. Any instruction written to R2 (e.g. “ADD R2, A”, "MOV R2, A", "BC R2, 6",···) will cause the ninth bit and the tenth bit (A8 ~ A9) of the PC to be cleared. Hence, the computed jump is limited to the first 256 locations of a page

	ENHS = 0	ENHS = 1
PC A9, A8	"ADD R2, A" allows a relative address to be added to the current PC, and the ninth and above bits of the PC will increase progressively.	Any instruction written to R2 will cause the ninth and the tenth bit (A8 ~ A9) of the PC to be cleared.
R8/IOCE Bits 2~0	/PD65~PD63: Enable Pull-down function.	General purpose register
RB/IOCB Bits 6~4	/PD62~PD60: Enable Pull-down function	

Bit 7: Not used, set to “1” all the time.

Bits 6 ~ 5 (RCM1, RCM0): RC mode selection bits

RCM 1	RCM 0	*Frequency (MHz)
1	1	4
1	0	8
0	1	1
0	0	455 kHz

* Theoretical values, for reference only

Bit 4: Not used, set to “1” all the time.

Bit 3 (RCOUT): Selection bit of Oscillator output or I/O port

0: P64

1: OSCO

Bits 2 ~ 1 (OSC1 and OSC0): Oscillator Mode Select bits

Mode	OSC1	OSC0
LXT (Low crystal oscillator mode, Freq. range is below 400 kHz)	0	0
HXT (High crystal oscillator mode, Freq. range is above 400 kHz)	0	1
ERC (External RC oscillator mode)	1	0
IRC (Internal RC oscillator mode)	1	1

Oscillator Modes	RCOUT	OSC1	OSC0
LXT (Low crystal oscillator mode, Freq. range is over 400 kHz)	x	0	0
HXT (High crystal oscillator mode, Freq. range is above 400 kHz)	x	0	1
ERC[1] (External RC oscillator mode); P64/RCOUT act as P64	0	1	0
ERC[1] (External RC oscillator mode); P64/RCOUT act as RCOUT	1	1	0
IRC[2] (Internal RC oscillator mode); P64/RCOUT act as P64	0	1	1
IRC[2] (Internal RC oscillator mode); P64/RCOUT act as RCOUT	1	1	1

[1] In ERC mode, ERCin is used as oscillator pin. RCOUT/P64 is defined by code option Word 1 Bits 3 ~ Bit 1.

[2] In IRC mode, P64 is normal I/O pin. RCOUT/P64 is defined by code option Word 1 Bits 3 ~ 1.

Bit 0: Not used, set it to "1" all the time.

6.11.3 Customer ID Register (Word 2)

Word 2												
Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
×	×	×	×	×	×	×	×	×	×	×	×	×

Bits 12 ~ 0: Customer's ID code

6.11.4 Code Option Register (Word 3)

Word 3													
Bit	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mnemonic	-	HLP	PSS	-	-	CT3	CT2	CT1	CT0	RT3	RT2	RT1	RT0
1	-	High	Int. Vref	-	-	High	High	High	High	High	High	High	High
0	-	Low	VDD	-	-	Low	Low	Low	Low	Low	Low	Low	Low

Bit 12: Not used, set to "1" all the time.

Bit 11 (HLP): Power Consumption Selection

0: Low power consumption, apply to working frequency at 4 MHz or below 4 MHz

1: High power consumption, apply to working frequency above 4 MHz

Bit 10 (PSS): Power Source Selection

0: VDD

1: Internal voltage reference

Bits 9 ~ 8: Not used, set to “1” all the time.

Bits 7 ~ 4 (CT3 ~ CT0): Internal RC mode Capacitance Trim bits (Coarse Calibration). These bits must always be set to “1” only (auto calibration).

Trimming Code				CLK Period	Frequency
CT[3]	CT[2]	CT[1]	CT[0]		
0	0	0	0	Period*(1+40%)	F*(1-28.57%)
0	0	0	1	Period*(1+35%)	F*(1-25.93%)
0	0	1	0	Period*(1+30%)	F*(1-23.08%)
0	0	1	1	Period*(1+25%)	F*(1-20.00%)
0	1	0	0	Period*(1+20%)	F*(1-16.67%)
0	1	0	1	Period*(1+15%)	F*(1-13.04%)
0	1	1	0	Period*(1+10%)	F*(1-9.09%)
0	1	1	1	Period*(1+5%)	F*(1-4.76%)
1	1	1	1	Period (default)	F (default)
1	1	1	0	Period*(1-5%)	F*(1+5.26%)
1	1	0	1	Period*(1-10%)	F*(1+11.11%)
1	1	0	0	Period*(1-15%)	F*(1+17.65%)
1	0	1	1	Period*(1-20%)	F*(1+25.00%)
1	0	1	0	Period*(1-25%)	F*(1+33.33%)
1	0	0	1	Period*(1-30%)	F*(1+42.86%)
1	0	0	0	Period*(1-35%)	F*(1+53.85%)

Bits 3 ~ 0 (RT3 ~ RT0): Internal RC mode Resistance Trim bits (Fine Calibration). These bits must always be set to “1” only (auto calibration).

Trimming Code				CLK Period	Frequency
RT[3]	RT[2]	RT[1]	RT[0]		
0	0	0	0	Period*(1+8%)	F*(1-7.41%)
0	0	0	1	Period*(1+7%)	F*(1-6.54%)
0	0	1	0	Period*(1+6%)	F*(1-5.66%)
0	0	1	1	Period*(1+5%)	F*(1-4.76%)
0	1	0	0	Period*(1+4%)	F*(1-3.85%)
0	1	0	1	Period*(1+3%)	F*(1-2.91%)
0	1	1	0	Period*(1+2%)	F*(1-1.96%)
0	1	1	1	Period*(1+1%)	F*(1-0.99%)
1	1	1	1	Period (default)	F (default)
1	1	1	0	Period*(1-1%)	F*(1+1.01%)
1	1	0	1	Period*(1-2%)	F*(1+2.04%)
1	1	0	0	Period*(1-3%)	F*(1+3.09%)
1	0	1	1	Period*(1-4%)	F*(1+4.17%)
1	0	1	0	Period*(1-5%)	F*(1+5.26%)
1	0	0	1	Period*(1-6%)	F*(1+6.38%)
1	0	0	0	Period*(1-7%)	F*(1+7.53%)

6.12 Instruction Set

Each instruction in the instruction set is a 13-bit word divided into an OP code and one or more operands. Normally, all instructions are executed within one single instruction cycle (one instruction consists of 2 oscillator time periods), unless the program counter is changed by instructions "MOV R2,A," "ADD R2,A," or by instructions of arithmetic or logic operation on R2 (e.g., "SUB R2,A," "BS(C) R2,6," "CLR R2," etc.).

In addition, the instruction set has the following features:

1. Every bit of any register can be set, cleared, or tested directly.
2. The I/O registers can be regarded as general registers. That is, the same instruction can operate on I/O registers.

■ EM78P151 Instruction Set Table:

The following symbols are used in the table**:**

"**R**" *Register designator that specifies which one of the registers (including operation and general purpose registers) is to be utilized by the instruction.*

"**B**" *Bit field designator that selects the value for the bit located in the register R and which affects the operation.*

"**k**" *8 or 10-bit constant or literal value*

Mnemonic	Operation	Status Affected
NOP	No Operation	None
DAA	Decimal Adjust A	C
CONTW	A → CONT	None
SLEP	0 → WDT, Stop oscillator	T, P
WDTC	0 → WDT	T, P
IOW R	A → IOCR	None [1]
ENI	Enable Interrupt	None
DISI	Disable Interrupt	None
RET	[Top of Stack] → PC	None
RETI	[Top of Stack] → PC, Enable Interrupt	None
CONTR	CONT → A	None
IOR R	IOCR → A	None [1]
MOV R,A	A → R	None
CLRA	0 → A	Z
CLR R	0 → R	Z
SUB A,R	R-A → A	Z, C, DC
SUB R,A	R-A → R	Z, C, DC
DECA R	R-1 → A	Z
DEC R	R-1 → R	Z
OR A,R	A ∨ VR → A	Z
OR R,A	A ∨ VR → R	Z
AND A,R	A & R → A	Z
AND R,A	A & R → R	Z
XOR A,R	A ⊕ R → A	Z
XOR R,A	A ⊕ R → R	Z
ADD A,R	A + R → A	Z, C, DC
ADD R,A	A + R → R	Z, C, DC
MOV A,R	R → A	Z
MOV R,R	R → R	Z
COMA R	/R → A	Z
COM R	/R → R	Z
INCA R	R+1 → A	Z

(Continuation)

Mnemonic	Operation	Status Affected
INC R	R+1 → R	Z
DJZA R	R-1 → A, skip if zero	None
DJZ R	R-1 → R, skip if zero	None
RRCA R	R(n) → A(n-1), R(0) → C, C → A(7)	C
RRC R	R(n) → R(n-1), R(0) → C, C → R(7)	C
RLCA R	R(n) → A(n+1), R(7) → C, C → A(0)	C
RLC R	R(n) → R(n+1), R(7) → C, C → R(0)	C
SWAPA R	R(0-3) → A(4-7), R(4-7) → A(0-3)	None
SWAP R	R(0-3) ↔ R(4-7)	None
JZA R	R+1 → A, skip if zero	None
JZ R	R+1 → R, skip if zero	None
BC R,b	0 → R(b)	None [2]
BS R,b	1 → R(b)	None [3]
JBC R,b	if R(b)=0, skip	None
JBS R,b	if R(b)=1, skip	None
CALL k	PC+1 → SP, k → PC	None
JMP k	k → PC	None
MOV A,k	k → A	None
OR A,k	A ∨ k → A	Z
AND A,k	A & k → A	Z
XOR A,k	A ⊕ k → A	Z
RETL k	k → A, [Top of Stack] → PC	None
SUB A,k	k-A → A	Z, C, DC
INT	PC + 1 → [SP], 001H → PC	None
DAS	Decimal Adjust A after either subtraction operation	C
ADC A,R	R + A + C → A r = 0x00~0x1F	Z, C, DC
ADC A,R	R + A + C → A r = 0x20~0x3F	Z, C, DC
ADC R,A	R + A + C → R	Z, C, DC
SBC A,R	R + $\overline{A}$ + C → A	Z, C, DC
SBC R,A	R + $\overline{A}$ + C → R	Z, C, DC
ADD A,k	k+A → A	Z, C, DC

Note: *[1]This instruction is applicable to IOC5 ~ IOC6, IOCB ~ IOCF only.*
[2]This instruction is not recommended for RF operation.
[3]This instruction cannot operate under RF.

7 Absolute Maximum Ratings

Items	Rating		
Temperature under bias	-40°C	to	85°C
Storage temperature	-65°C	to	150°C
Input voltage	Vss-0.3V	to	Vdd+0.5V
Output voltage	Vss-0.3V	to	Vdd+0.5V
Working Voltage	2.0V	to	5.5V
Working Frequency	DC	to	20 MHz

8 DC Electrical Characteristics

■ **Ta = 25°C, VDD = 5.0V, VSS = 0V**

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
FXT	Crystal: V_{DD} to 2.3V	Two cycles with two clocks	DC	–	4.0	MHz
	Crystal: V_{DD} to 3V	Two cycles with two clocks	DC	–	8.0	MHz
	Crystal: V_{DD} to 5V	Two cycles with two clocks	DC	–	20.0	MHz
ERC	ERC: V_{DD} to 5V	R: 5 kΩ, C: 39 pF	F±30%	1500	F±30%	kHz
IIL	Input Leakage Current for Input Pins	VIN = V_{DD}, V_{SS}	–	–	±1	μA
VIH0	Input High Voltage (V_{DD} = 5V) (P60 ~P62,P64~P65 are Schmitt trigger)	Port 6	1.52	–	V_{DD}+0.3	V
VIL0	Input Low Voltage (V_{DD} = 5V) (P60 ~P62,P64~P65 are Schmitt trigger)	Port 6	V_{SS} - 0.3	–	1.12	V
VIH1	Input High Voltage (V_{DD} = 5V) (P60 ~P65 are inverter trigger)	Port 6	1.52	–	V_{DD}+0.3	V
VIL1	Input Low Voltage (V_{DD} = 5V) (P60 ~P65 are inverter trigger)	Port 6	V_{SS} - 0.3	–	1.52	V
VIHT1	Input High Threshold Voltage (V_{DD} = 5V)	/RESET, TCC (Schmitt trigger)	1.8	–	V_{DD}+0.3	V
VILT1	Input Low Threshold Voltage (V_{DD} = 5V)	/RESET, TCC (Schmitt trigger)	V_{SS} - 0.3	–	1.1	V
VIH2	Input High Voltage (V_{DD} = 3V) (P60 ~P62, P64~P65 are Schmitt trigger)	Port 6	1.35	–	V_{DD}+0.3	V
VIL2	Input Low Voltage (VDD = 3V) (P60 ~P62,P64~P65 are Schmitt trigger)	Port 6	V_{SS} - 0.3	–	0.55	V
VIH3	Input High Voltage (V_{DD} = 3V) (P60 ~P65 are inverter trigger)	Port 6	1.35	–	V_{DD}+0.3	V
VIL3	Input Low Voltage (V_{DD} = 3V) (P60 ~P65 are inverter trigger)	Port 6	V_{SS} - 0.3	–	1.35	V
VIHX2	Clock Input High Voltage (V_{DD} = 3V)	OSCI	1.52	–	V_{DD}+0.3	V
VILX2	Clock Input Low Voltage (V_{DD} = 3V)	OSCI	V_{SS} - 0.3	–	1.12	V
VOH1	Output High Voltage	IOH = -13 mA	2.4	–	–	V
VOH2	Output High Voltage	IOH = -6 mA	3.6	–	–	V
VOL1	Output Low Voltage	IOL = 14.5 mA	–	–	0.4	V
VOL2	Output Low Voltage	IOL = 20 mA	–	–	0.6	V
IPH	Pull-High Current	Pull-high active, input pin at V_{SS}	-45	-60	-75	μA
IPD	Pull-Down Current	Pull-down active, input pin at V_{DD}	15	30	45	μA

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
ISB1	Power Down Current	All input and I/O pins at V_{DD}, Output pin floating, WDT disabled	-	-	1	μA
ISB2	Power Down Current	All input and I/O pins at V_{DD}, Output pin floating, WDT enabled	-	**5**	10	μA
ICC1	Operating Supply Current at Two Clocks (V_{DD} = 3V)	/RESET = 'High', F_{OSC} = 32kHz (XTAL type, CLKS[1:0] = "10"), Output pin floating, WDT disabled	-	15	30	μA
ICC2	Operating Supply Current at Two Clocks (V_{DD} = 3V)	/RESET = 'High', F_{OSC} = 32kHz (XTAL type, CLKS[1:0] = "10"), Output pin floating, WDT enabled	-	19	35	μA
ICC3	Operating Supply Current at Two Clocks (V_{DD} = 5.0V)	/RESET = 'High', F_{OSC} = 4 MHz (Crystal type, CLKS[1:0) = "10"), Output pin floating	-	-	2.0	mA
ICC4	Operating Supply Current at Two Clocks (V_{DD} = 5.0V)	/RESET = 'High', F_{OSC} = 10 MHz (XTAL type, CLKS[1:0] = "10"), Output pin floating	-	-	4.0	mA

■ Internal RC Electrical Characteristics

(Ta = 25°C, VDD = 5.0V, VSS = 0V)

Internal RC	Drift Rate				
	Temperature	Voltage	Min.	Typ.	Max.
4 MHz	25°C	5V	3.96 MHZ	4 MHz	4.04 MHz
8 MHz	25°C	5V	7.88 MHz	8 MHz	8.12 MHz
1 MHz	25°C	5V	0.9 MHz	1 MHz	1.1 MHz
455kHz	25°C	5V	450.45 kHz	455 kHz	459.55 kHz

■ Internal RC Electrical Characteristics

(Ta = 0 ~ 70°C, VDD = 2 ~ 5.5V, VSS = 0V)

Internal RC	Drift Rate				
	Temperature	Voltage	Min.	Typ.	Max.
4 MHz	0 ~ 70°C	2 ~ 5.5V	3.86 MHz	4 MHz	4.14 MHz
8 MHz	0 ~ 70°C	2 ~ 5.5V	7.68 MHz	8 MHz	8.32 MHz
1 MHz	0 ~ 70°C	2 ~ 5.5V	0.65 MHz	1 MHz	1.35 MHz
455 kHz	0 ~ 70°C	2 ~ 5.5V	439.075 kHz	455 KHz	470.925 kHz

9 AC Electrical Characteristics

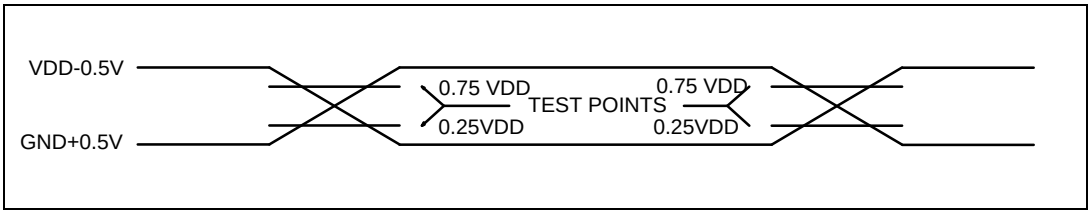
■ **Ta=25℃, VDD=5V ± 5%, VSS=0V**

Symbol	Parameter	Conditions	Min.	Type	Max.	Unit
Dclk	Input CLK duty cycle	–	45	50	55	%
Tins	Instruction cycle time (CLKS="0")	Crystal type	100	–	DC	ns
		RC type	500	–	DC	ns
Ttcc	TCC input time period	–	(Tins+20) × N*	–	–	ns
Tdrh	Device reset hold time	Ta = 25℃	11.3	16.2	21.6	ms
Trst	/RESET pulse width	Ta = 25℃	2000	–	–	ns
Twdt	Watchdog timer duration	Ta = 25℃	11.3	16.2	21.6	ms
Tset	Input pin setup time	–	–	0	–	ns
Thold	Input pin hold time	–	15	20	25	ns
Tdelay	Output pin delay time	Cload = 20 pF	45	50	55	ns
Tdrc	ERC delay time	Ta = 25℃	1	3	5	ns

*__N__ = *Selected prescaler ratio*

10 Timing Diagrams

■ AC Test Input / Output Waveform



Note: *AC Testing: Input is driven at VDD-0.5V for logic "**1**", and GND+0.5V for logic "**0**"*
*Timing measurements are made at 0.75VDD for logic "**1**", and 0.25VDD for logic "**0**"*

Figure 10-1a AC Test Input / Output Waveform Timing Diagram

■ Reset Timing (CLK = 0)

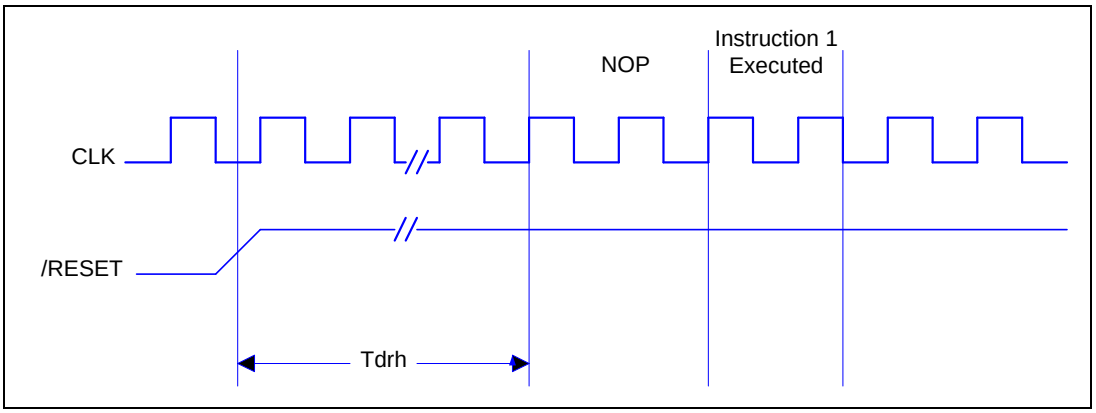


Figure 10-1b Reset Timing Diagram

■ TCC Input Timing (CLKS = 0)

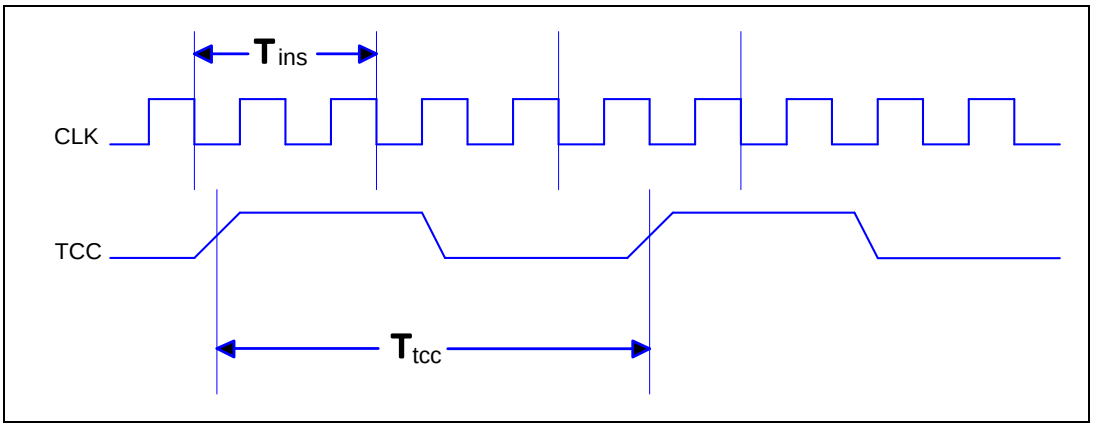
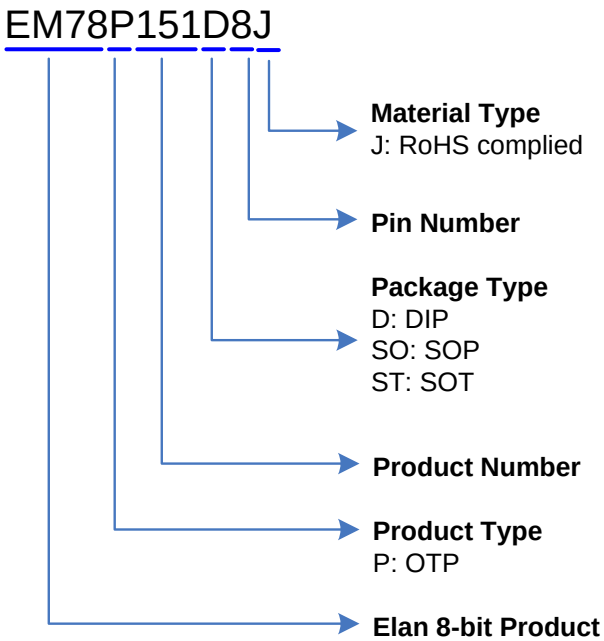
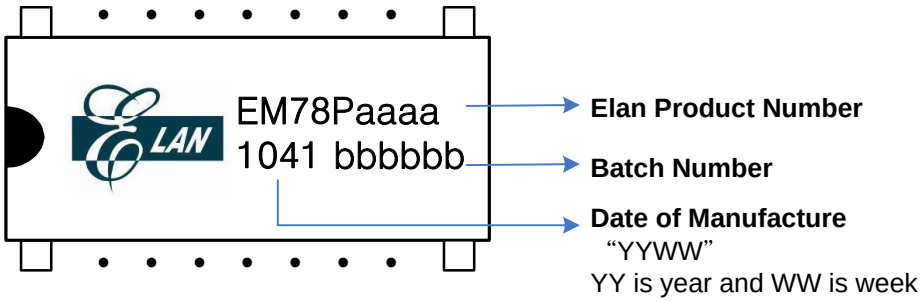


Figure 10-1c TCC Input Timing Diagram

APPENDIX

A Ordering and Manufacturing Information





B Package Type

OTP MCU	Package Type	Pin Count	Package Size
EM78P151D8J	DIP	8	300 mil
EM78P151SO8J	SOP	8	150 mil
EM78P151ST6J	SOT23-6	6	-

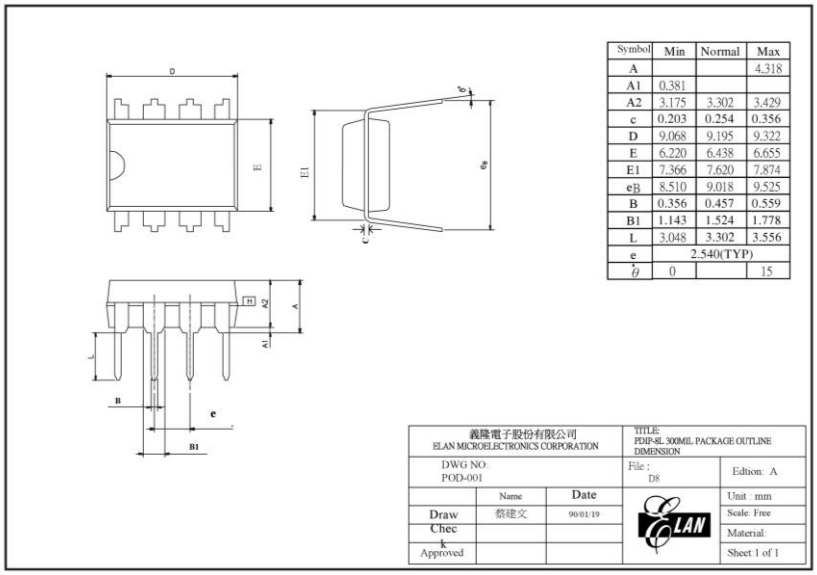
(For product code “J”)

These are Green products that comply with RoHS specifications.

Part No.	EM78P151D8J EM78P151SO8J EM78P151ST6J
Electroplate type	Pure Tin
Ingredient (%)	Sn: 100%
Melting point (°C)	232°C
Electrical resistivity (μΩ-cm)	11.4
Hardness (hv)	8~10
Elongation (%)	>50%

C Packaging Configurations

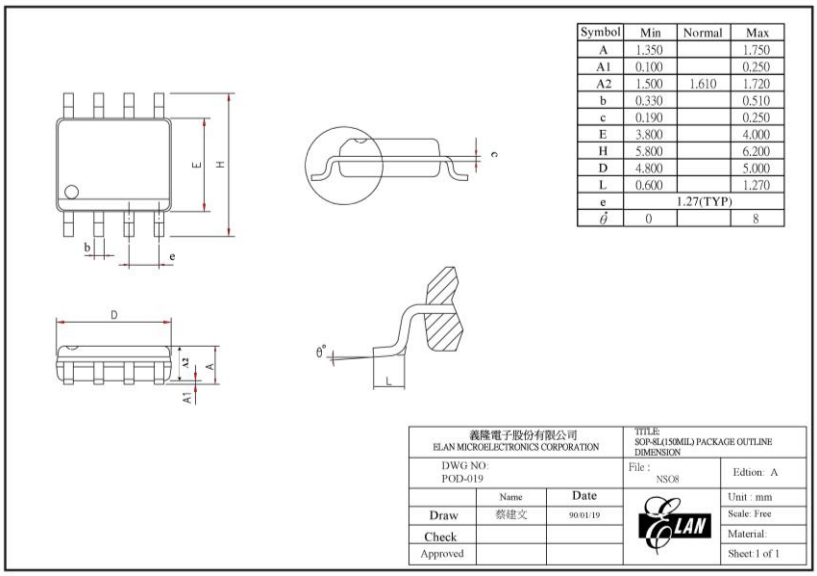
C.1 8-Lead Plastic Dual in-line (DIP) – 300 mil



Symbol	Min	Normal	Max
A			4.318
A1	0.381		
A2	3.175	3.302	3.429
c	0.203	0.254	0.356
D	9.068	9.195	9.322
E	6.220	6.438	6.655
E1	7.366	7.620	7.874
eB	8.510	9.018	9.525
B	0.356	0.457	0.559
B1	1.143	1.524	1.778
L	3.048	3.302	3.556
e	2.540(TYP)		
θ	0		15

Figure C-1 EM78P151 8-Pin DIP (300 mil) Package Type

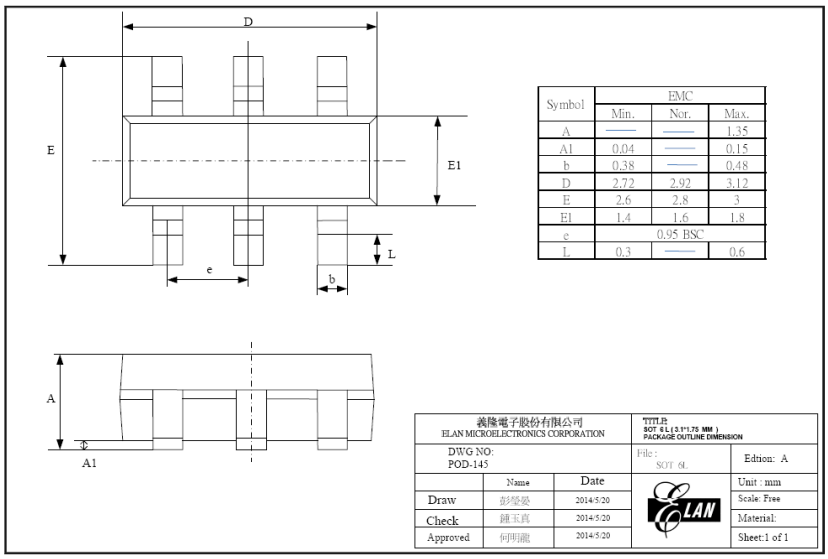
C.2 8-Lead Small Outline Package (SOP) – 150 mil



Symbol	Min	Normal	Max
A	1.350		1.750
A1	0.100		0.250
A2	1.500	1.610	1.720
b	0.330		0.510
c	0.190		0.250
E	3.800		4.000
H	5.800		6.200
D	4.800		5.000
L	0.600		1.270
e	1.27(TYP)		
θ	0		8

Figure C-2 EM78P151 8-Pin SOP (150 mil) Package Type

C.3 6-Lead Small Outline Transistor Plastic Package (SOT)



Symbol	EMC		
	Min.	Nor.	Max.
A	——	——	1.35
A1	0.04	——	0.15
b	0.38	——	0.48
D	2.72	2.92	3.12
E	2.6	2.8	3
E1	1.4	1.6	1.8
e	0.95 BSC		
L	0.3	——	0.6

Figure C-3 EM78P151 8-Pin SOT23-6 Package Type