EM78P224N

8-Bit Microcontroller

Product Specification

DOC. VERSION 1.4

ELAN MICROELECTRONICS CORP.

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Contents

APPENDIX

Specification Revision History

Doc. Version	Revision Description	Date
1.0	Initial version	2010/11/22
1.1	1. Modified the Pin Assignment. 2. Added the pin status with enabled functions. 3. Modified the operating voltage on the IRC drift rate table. 4. Modified the measured value of ESD and Latch up. 5. Modified Figure 6-3 and the Note. 6. Modified the Stack status after reset occured. 7. Modified the table of AC electrical characteristic.	2010/12/03
1.2	1. Modified description of P67 at pin description. 2. Modified description of R3 Bit 7. 3. Modified description of Bank 0 R12, Bits 7~4. 4. Modified decscription of Chapter 6.8.2. 5. Deleted HLP at Code Option Word 0 Bit 9. 6. Added Code Option Word 3 for Customer ID 7. Deleted Code Option Word 2 Bit 14. 8. Added Ordering and Manufacturing Information. 9. Added diagram on Frequency to Voltage Curve. 10. Modified descriptions on POR and LVR in the feature spec.	2012/06/08
1.3	1. Added device characteristic curve.	2012/11/27
1.4	1. Added LVR characteristics in the DC Electrical Characteristics. 2. Added P53 remark at the Pin Description section. 3. Modified Apendix A for Ordering and Manufacturing Information 4. Added User Application Note	2016/05/12

User Application Note

(Before using this IC, take a look at the following description note, it includes important messages.)

1. We strongly recommend that users have to place an external pull-down or pull-high resistor on P53 no matter what the pin function is. The purpose of this is to prevent P53 from floating.

1 General Description

EM78P224N is an 8-bit microprocessor with low-power, high-speed CMOS technology, and high noise immunity. It has a built-in 4K×15-bit in system programmable SRAM, and 176×8 bits in OTP-ROM (Electrical One Time Programmable Read Only Memory). It provides three protection bits to prevent intrusion of user's OTP memory code. Seven option bits are also available to meet user's unique requirements.

With its enhanced OTP-ROM features, the EM78P224N can provide a convenient way of developing and verifying user's programs. Moreover, this OTP device offers the advantages of effective program updates with the use of development and programming tools, such as the ELAN Writer to easily program your development codes.

2 Features

- CPU Configuration:
  - Support 4K×15 bits program ROM
  - 176×8 bits on-chip registers (SRAM)
  - 8-level stacks for subroutine nesting
  - Dual clock operation mode
  - Power on reset level Voltage: 1.8V(Reset)~1.9V (Release)
  - Less than 1.0mA at 5V/4 MHz
  - Typically 15μA, at 3V/16kHz
  - Typically 2μA, during Sleep mode
  - Four operation modes:

Mode	CPU	Main Clock	Sub Clock
Sleep mode	Turn off	Turn off	Turn off
Idle Mode	Turn off	Turn off	Turn on
Green mode	Turn on	Turn off	Turn on
Normal mode	Turn on	Turn on	Turn on

- I/O Port Configuration:
  - 4 bidirectional I/O ports: P5, P6, P7, P8
  - 30 I/O pins
  - 8 Programmable open-drain I/O pins
  - 24 programmable pull-high I/O pins
  - 8 programmable pull-low I/O pins
  - 16 programmable high sink I/O pins
  - 16 programmable high drive I/O pins
  - External interrupt : INT
- Operating voltage range:
  - 2.1V~5.5V at 0~70°C (commercial)
  - 2.3V~5.5V at -40~85°C (industrial)
- Operating frequency range:
  - Crystal/IRC oscillation circuit selected by code option for system clock
  - IRC oscillation circuit selected by code option for sub clock

  Main Clock
  - Crystal mode:
    DC ~ 20 MHz at 5V
    DC ~ 8 MHz at 3V
    DC ~ 4 MHz at 2.1V
  - IRC mode:
    DC ~ 16 MHz/2clks at 4.5V
    DC ~ 8 MHz/2clks at 3V
    DC ~ 4 MHz/2clks at 2.1V
  - IRC Drift Rate (Ta=25°C, VDD=5V ± 5%, VSS=0V)

Internal RC Frequency	Drift Rate			
	Temprature (-40°C+85°C)	Voltage (2.3V~5.5V)	Process	Total
1 MHz	±2%	±3%	±2%	±7%
4 MHz	±2%	±3%	±2%	±7%
8 MHz	±2%	±3%	±2%	±7%
16 MHz	±2%	±3%	±2%	±7%

  Sub Clock
  - IRC mode: 32kHz/16kHz
- Peripheral Configuration:
  - 8-bit real time clock/counter (TCC) with selective signal sources and trigger edges
  - 8-bit Timer/Counter
    TC1: Timer/Counter/capture/window/buzzer/PWM /PDO (Programmable Divider Output) Mode
  - External interrupt wake-up
    Function: Rising or falling edges interrupt
  - Four Ports input status change wake-up
  - Four programmable Level Voltage Detectors (LVD): 4.5V, 4V, 3.3V, & 2.2V.
  - Four programmable Level Voltage Resets (LVR): 4.0V, 3.5V, 2.7V, & 1.8V(POR)
- 5 available interrupts

- Special Features:
  - Programmable free running watchdog timer
  - High ESD immunity
  - Power saving Sleep mode
  - Selectable Oscillation mode
- Package Types:
  - 28-pin DIP 600 mil: EM78P224ND28
  - 28-pin Skinny DIP 400 mil: EM78P224NK28A
  - 28-pin SOP 300 mil: EM78P224NSO28
  - 28-pin SSOP 209 mil: EM78P224SS28
  - 32-pin DIP 600 mil: EM78P224ND32
  - 32-pin SOP 450 mil: EM78P224NSO32
  - 32-pin SOP 300 mil: EM78P224NSO32A

NOTE
These are all Green products which do not contain hazardous substances.

3 Pin Assignment

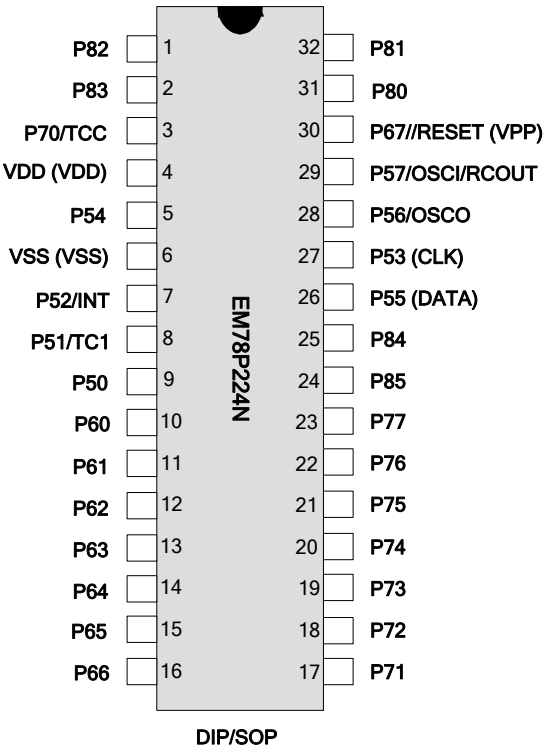


Figure 3-1a EM78P224ND32/SO32

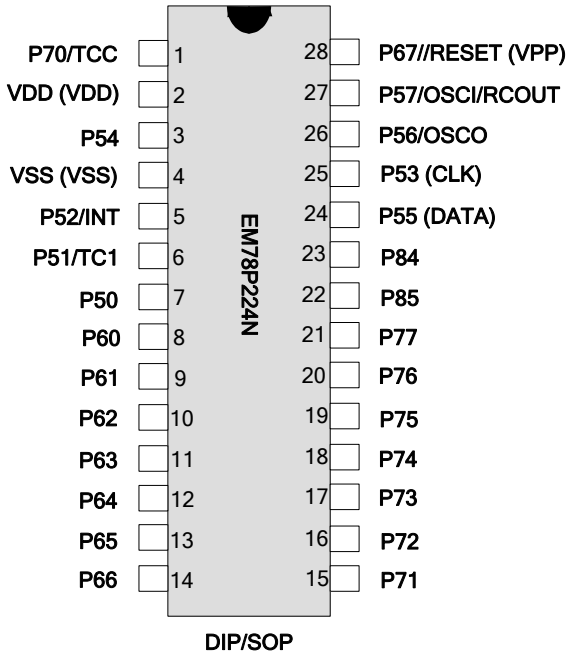


Figure 3-1b EM78P224ND28/SO28/K28A/SS28

4 Pin Description

4.1 EM78P224N

Legend: ***ST:*** *Schmitt Trigger input* ***AN:*** *analog pin*
CMOS: *CMOS output* ***XTAL:*** *Oscillation pin for crystal / resonator*

Name	Function	Input Type	Output Type	Description
P50	P50	ST	CMOS	Bidirectional I/O pin with programmable pull-high and pin change wake-up.
P51/TC1	P51	ST	CMOS	Bidirectional I/O pin with programmable pull-high and pin change wake-up.
	TC1	ST	CMOS	Timer 1 (Counter1/CAP1/Window/PDO1/PWM1/BUZ1)
P52/INT	P52	ST	CMOS	Bidirectional I/O pin with programmable pull-high and pin change wake-up.
	INT	ST	–	External interrupt pin
P53 (CLK)	P53	ST	CMOS	Bidirectional I/O pin with pin change wake-up. **Remark: Off-chip pull-down or pull-high**
	(CLK)	ST	–	Clock pin for Writer programming **Remark: Off-chip pull-down or pull-high**
P54	P54	ST	CMOS	Bidirectional I/O pin with pin change wake-up.
P55 (DATA)	P55	ST	CMOS	Bidirectional I/O pin with pin change wake-up.
	(DATA)	ST	CMOS	Data pin for Writer programming
P56	P56	ST	CMOS	Bidirectional I/O pin with pin change wake-up.
	OSCO	–	XTAL	Clock output of crystal / resonator oscillator
P57	P57	ST	CMOS	Bidirectional I/O pin with pin change wake-up.
	OSCI	XTAL	–	Clock input of crystal / resonator oscillator
	RCOUT	–	COMS	Clock output of internal RC oscillator
P60	P60	ST	CMOS	Bidirectional I/O pin with programmable pull-high, open-drain, high-sink and pin change wake-up.
P61	P61	ST	CMOS	Bidirectional I/O pin with programmable pull-high, open-drain, high-sink and pin change wake-up.
P62	P62	ST	CMOS	Bidirectional I/O pin with programmable pull-high, open-drain, and pin change wake-up.
P63	P63	ST	CMOS	Bidirectional I/O pin with programmable pull-high, open-drain, and pin change wake-up.
P64	P64	ST	CMOS	Bidirectional I/O pin with programmable pull-high, open-drain, and pin change wake-up.
P65	P65	ST	CMOS	Bidirectional I/O pin with programmable pull-high, open-drain, and pin change wake-up.
P66	P66	ST	CMOS	Bidirectional I/O pin with programmable pull-high, open-drain, and pin change wake-up.
P67//RESET (VPP)	P67	ST	CMOS	Bidirectional I/O pin with pin change wake-up.This pin is always open-drain.
	/RESET	ST	–	Reset pin
	(VPP)	power	–	VPP pin for Writer programming

(*Continuation*)

Name	Function	Input Type	Output Type	Description
P70/TCC	P70	ST	CMOS	Bidirectional I/O pin with programmable pull-low, pull-high, high-sink/drive and pin change wake-up.
	TCC	ST	–	Real Time Clock/Counter clock input
P72	P72	ST	CMOS	Bidirectional I/O pin with programmable pull-low, pull-high, high-sink/drive and pin change wake-up.
P73	P73	ST	CMOS	Bidirectional I/O pin with programmable pull-low, pull-high, high-sink/drive and pin change wake-up.
P74	P74	ST	CMOS	Bidirectional I/O pin with programmable pull-low, pull-high, high-sink/drive and pin change wake-up.
P75	P75	ST	CMOS	Bidirectional I/O pin with programmable pull-low, pull-high, high-sink/drive and pin change wake-up.
P76	P76	ST	CMOS	Bidirectional I/O pin with programmable pull-low, pull-high, high-sink/drive and pin change wake-up.
P77	P77	ST	CMOS	Bidirectional I/O pin with programmable pull-low, pull-high, high-sink/drive and pin change wake-up.
P80	P80	ST	COMS	Bidirectional I/O pin with programmable pull-high, high-sink/drive and pin change wake-up.
P81	P81	ST	COMS	Bidirectional I/O pin with programmable pull-high, high-sink/drive and pin change wake-up.
P82	P82	ST	COMS	Bidirectional I/O pin with programmable pull-high, high-sink/drive and pin change wake-up.
P83	P83	ST	CMOS	Bidirectional I/O pin with programmable pull-high, high-sink/drive and pin change wake-up.
P84	P84	ST	CMOS	Bidirectional I/O pin with programmable pull-high, high-sink/drive and pin change wake-up.
P85	P85	ST	CMOS	Bidirectional I/O pin with programmable pull-high, high-sink/drive and pin change wake-up.
VDD	VDD	Power	–	Power
(VDD)	(VDD)	Power		VDD pin for Writer programming
VSS	VSS	Power	–	Ground
(VSS)	(VSS)	Power		Ground pin for Writer programming

NOTE

It is strongly recommended that user has to place external pull-down or pull-high resistor on P53 no matter what the pin function is.

The purpose of this is to prevent P53 from floating.

4.1.1 Pin Status under Enabled Function

Pin Function	I/O Status		Pin Control		
	I/O Direction	Pin Change Wake-up/Interrupt	Pull High	Pull Low	O.D.
General Input	Input	S/W	S/W	S/W	S/W
General Output	Output	Disable	S/W	S/W	S/W
TCC	Input	Disable	S/W	S/W	S/W
TC-IN	Input	Disable	S/W	S/W	S/W
TC-OUT	Output	Disable	S/W	S/W	S/W
Reset	Input	Disable	Init: ENABLE	S/W	S/W
EX_INT	Input	Disable	S/W	S/W	S/W
OSCI	Input	Disable	Disable	Disable	S/W
OSCO	Input	Disable	Disable	Disable	S/W

NOTE

Disable: *→ It is always disabled*

Enable: *→ It is always enabled*

S/W: *→ It can be controlled by register. The initial status is disabled.*

1. If the pin is not working as general I/O, the Pin Change Wake-up/Interrupt function must be at disable status.

2. Priority: Digital function output > digital function input > general I/O

5 Block Diagram

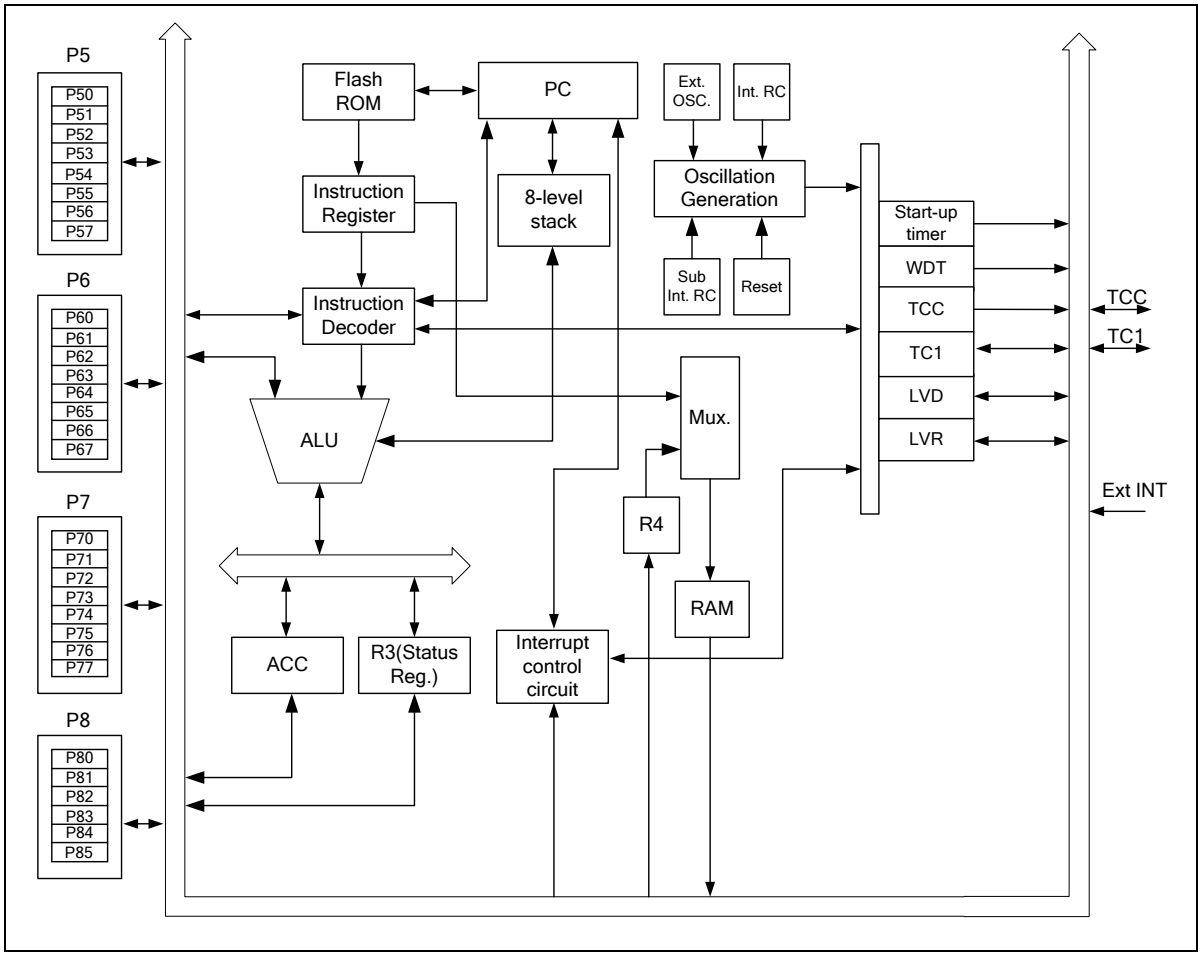


Figure 5-1 EM78P224N Functional Block Diagram

6 Functional Description

6.1 Operational Registers

6.1.1 R0 (Indirect Addressing Register)

R0 is not a physically implemented register. Its major function is to perform as an indirect addressing pointer. Any instruction using R0 as a pointer actually accesses data pointed by the RAM Select Register (R4).

6.1.2 R1 (Bank Select Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
–	–	–	SBS0	–	–	–	–
–	–	–	R/W	–	–	–	–

Bits 7 ~ 5: Not used. Set to "**0**" all the time.

Bit 4 (SBS0): Special register bank select bit. It is used to select Bank 0 or Bank 1 of the special Registers R5~R4F.

0: Bank 0

1: Bank 1

Bits 3 ~ 0: Not used. Set to "**0**" all the time.

6.1.3 R2 (Program Counter Low and Stack)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7 ~ 0 (PC7 ~ PC0): The low byte of the program counter.

- Depending on the device type, R2 and hardware stack are **12**-bit wide. The structure is depicted in the following Figure 6-1; *EM78P224N Program Counter Configuration*.
- The configuration structure generates **4K×15** bits on-chip OTP ROM addresses to the relative programming instruction codes. One program page is **4096** words long.
- R2 is set as all "**0**"s when under Reset condition.
- "JMP" instruction allows direct loading of the lower **12** program counter bits. Thus, "JMP" allows the PC to go to any location within a page.

- "CALL" instruction loads the lower 12 bits of the PC, and the present PC value will add 1 and is pushed onto the stack. Thus, the subroutine entry address can be located anywhere within a page.
- "LJMP" instruction allows direct loading of the lower 15 program counter bits. Therefore, "LJMP" allows PC to jump to any location within 16K (2^{14}).
- "LCALL" instruction loads the lower 15 bits of the PC, and then PC+1 is pushed onto the stack. Thus, the subroutine entry address can be located anywhere within 16K (2^{14}).
- "RET" ("RETL k", "RETI") instruction loads the program counter with the contents of the top-level stack.
- "ADD R2, A" allows a relative address to be added to the current PC, and the ninth and above bits of the PC will increase progressively.
- "MOV R2, A" allows to load an address from the "A" register to the lower 8 bits of the PC, and the ninth and above bits of the PC will not change.
- Any instruction except “ADD R2,A” that is written to R2 (e.g., "MOV R2, A", "BC R2, 6", etc.) will cause the ninth bit and the above bits (A8~A11) of the PC to remain unchanged.
- All instructions are single instruction cycle (Fsys/2) except “LCALL” and “LJMP” instructions. The “LCALL” and “LJMP” instructions need two instructions cycle.

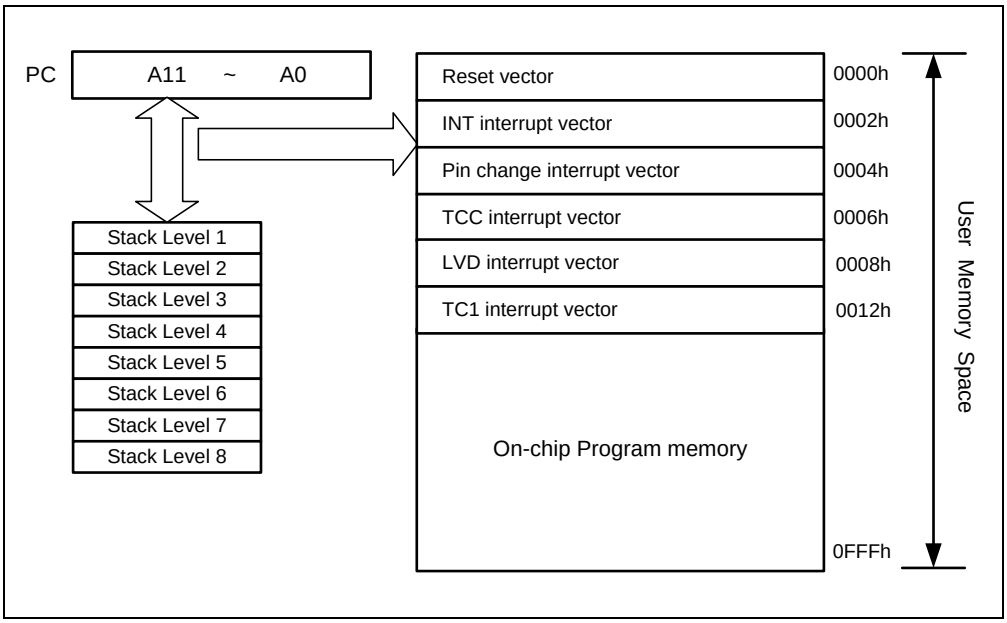


Figure 6-1 EM78P224N Program Counter Organization

■ Data Memory Configuration

Address	Bank 0	Bank 1
0X00	IAR (Indirect Addressing Register)	
0X01	BSR (Bank Select Control Register)	
0X02	PC (Program Counter)	
0X03	SR (Status Register)	
0X04	RSR (RAM Selection Register)	
0X05	Port 5	IOCR8
0X06	Port 6	–
0X07	Port 7	–
0X08	Port 8	P5PHCR
0X09	–	P6PHCR
0X0A	–	P78PHCR
0x0B	IOC5	–
0X0C	IOC6	–
0X0D	IOC7	P7PLCR
0X0E	OMCR (Operating Mode Control Register)	–
0X0F	EIESCR (External Interrupt Edge Selection Control Register)	P6HDSCR
0X10	WUCR1	P78HDSCR
0X11	–	–
0X12	WUCR3	P6ODCR
0X13	–	–
0X14	SFR1 (Status Flag Register 1)	–
0X15	SFR2 (Status Flag Register 2)	–
0X16	–	–
0X17	SFR4 (Status Flag Register 4)	–
0X18	–	–
0X19	–	–
0X1A	–	–
0X1B	IMR1 (Interrupt Mask Register 1)	–
0X1C	IMR2 (Interrupt Mask Register 2)	–
0X1D	–	–
0X1E	IMR4 (Interrupt Mask Register 4)	–
0X1F	–	–
0X20	–	–

(*Continuation)*

Address	Bank 0	Bank 1
0x21	WDTCR	–
0X22	TCCCR	–
0X23	TCCD	–
0X24	TC1CR1	–
0X25	TC1CR2	–
0X26	TC1DA	–
0X27	TC1DB	–
0X28	–	–
0X29	–	–
0X2A	–	–
0x2B	–	–
0X2C	–	–
0X2D	–	–
0X2E	–	–
0X2F	–	–
0X30	–	–
0X31	–	–
0X32	–	–
0X33	–	–
0X34	–	–
0X35	–	–
0X36	–	–
0X37	–	–
0X38	–	–
0X39	–	–
0X3A	–	–
0x3B	–	–
0X3C	–	–
0X3D	–	–
0X3E	–	–
0X3F	–	–
0X40	–	–
0X41	–	–
0X42	–	–

(*Continuation)*

Address	Bank 0	Bank 1
0X43	–	–
0X44	–	–
0X45	–	TBPTL
0X46	–	TBPTH
0X47	–	STKMON
0X48	–	PCH
0X49	–	LVDCR
0X4A	–	–
0x4B	–	–
0X4C	–	–
0X4D	–	–
0X4E	–	–
0X4F	–	–
0X50	General Purpose Register	
0X51		
.		
.		
0X7F		
0X80	Bank 0 General Registers (128×8 bits)	
0X81		
.		
.		
.		
0XFE		
0XFF		

6.1.4 R3 (Status Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INT	–	–	T	P	Z	DC	C
F	–	–	R/W	R/W	R/W	R/W	R/W

Bit 7 (INT): Interrupt Enable flag

0: Interrupt masked by DISI or hardware interrupt

1: Interrupt enabled by ENI/RETI instructions

Bits 6 ~ 5: Not used. Set to "**0**" all the time.

Bit 4 (T): Time-out bit

Set to "**1**" with the "SLEP" and "WDTC" commands, or during power up and reset to "**0**" by WDT time-out.

Bit 3 (P): Power down bit

Set to "1" during power on or by a "WDTC" command and reset to "0" by a "SLEP" command.

Bit 2 (Z): Zero flag

Set to "1" if the result of an arithmetic or logic operation is zero.

Bit 1 (DC): Auxiliary carry flag

Bit 0 (C): Carry flag

6.1.5 R4 (RAM Select Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RSR7	RSR6	RSR5	RSR4	RSR3	RSR2	RSR1	RSR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7 ~ 0 (RSR7 ~ RSR0): These bits are used to select registers (Address: 00~FF) in indirect addressing mode. You can refer to the table on Data Memory Configuration for more details under Section 6.1.3; *R2: PCL* (*Program Counter Low and Stack)***.**

6.1.6 Bank 0 R5 ~ R8 (Port 5 ~ Port 8)

R5, R6, R7, and R8 are I/O data registers.

6.1.7 Bank 0 RB~RD (IOCR5 ~ IOCR7)

These registers are used to control the I/O port direction. They are both readable and writable.

0: Put the relative I/O pin as output

1: Put the relative I/O pin into high impedance

6.1.8 Bank 0 RE OMCR (Operating Mode Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CPUS	IDLE	–	–	–	–	RCM1	RCM0
R/W	R/W	–	–	–	–	R/W	R/W

Bit 7 (CPUS): CPU Oscillator Source Select.

0: Fs: sub-oscillator

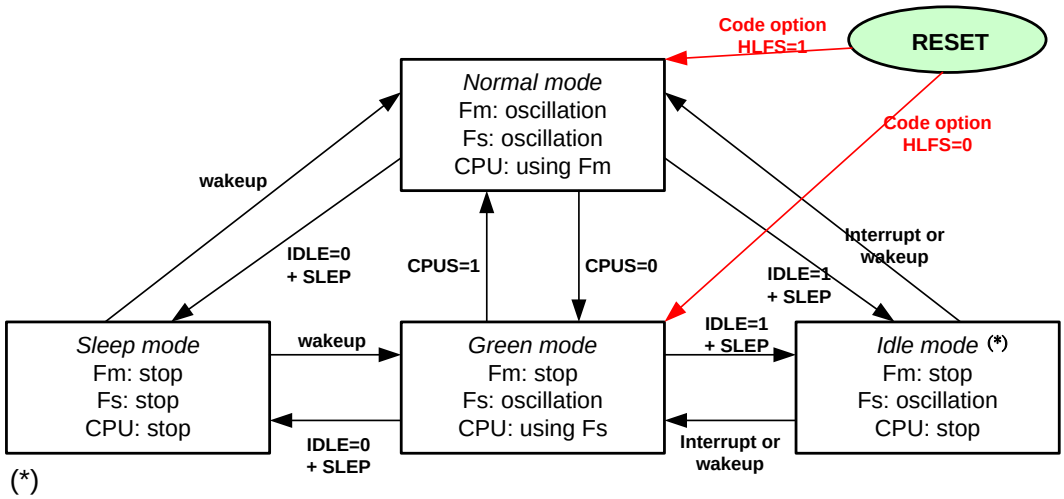
1: Fm: main-oscillator

When CPUS=0, the CPU oscillator selects the sub-oscillator and the main oscillator is stopped.

Bit 6 (IDLE): Idle Mode Enable Bit. This bit determines which mode (see figure below) to use with SLEP instruction.

0: "IDLE=0"+SLEP instruction → Sleep mode

1: "IDLE=1"+SLEP instruction → Idle mode



(*)

switching operation mode at idle>normal, idle->green:

If the clock source of timer is Fs, timer/counter must continue to count in idle mode.When the matching condition of the timer/counter happens in idle mode, the interrupt flag of timer/counter would be active. However, the MCU will jump to interrupt vector when corresponding interrupt is enabled.

Figure 6-2 CPU Operation Mode

■ **Oscillation Characteristics**

Oscillation Mode	CPU Mode Switch	Waiting Time before CPU Starts to Work
Crystal mode	Sleep → Normal	WSTO + 510 clocks (main frequency)
	Idle → Normal	WSTO + 510 clocks (main frequency)
	Green → Normal	WSTO + 510 clocks (main frequency)
	Sleep → Green	WSTO + 8 clocks (sub frequency)
	Idle → Green	WSTO + 8 clocks (sub frequency)
IRC mode	Sleep → Normal	WSTO + 8 clocks (main frequency)
	Idle → Normal	WSTO + 8 clocks (main frequency)
	Green → Normal	WSTO + 8 clocks (main frequency)
	Sleep → Green	WSTO + 8 clocks (sub frequency)
	Idle → Green	WSTO + 8 clocks (sub frequency)

WSTO: *Waiting Time from Start-to-Oscillation*

Bits 5 ~ 2: Not used. Set to "**0**" all the time.

Bits 1 ~ 0 (RCM1 ~ RCM0): Internal RC mode select bits

RCM1	RCM0	Frequency (MHz)
0	0	1
0	1	8
1	0	16
1	1	4

NOTE

The initial value of RCM1~0 is the same with settings in Code Option Word 0.

6.1.9 Bank 0 RF EIESCR (External Interrupt Edge Select Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
–	–	–	–	EIES	–	–	–
–	–	–	–	R/W	–	–	–

Bits 7 ~ 4: Not used. Set to "**0**" all the time.

Bit 3 (EIES): External interrupt edge select bit

0: Falling edge interrupt

1: Rising edge interrupt

Bits 2 ~ 0: Not used. Set to "**0**" all the time.

6.1.10 Bank 0 R10 WUCR1 (Wake-up Control Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
–	–	LVDWK	–	INTWK	–	–	–
–	–	R/W	–	R/W	–	–	–

Bits 7 ~ 6: Not used. Set to "**0**" all the time.

Bit 5 (LVDWK): Low Voltage Detect Wake-up Enable Bit

0: Disable Low Voltage Detect wake-up.

1: Enable Low Voltage Detect wake-up.

Bit 4: Not used. Set to "**0**" all the time.

Bit 3 (INTWK): External Interrupt (INT pin) Wake-up Function Enable Bit

0: Disable external interrupt wake-up

1: Enable external interrupt wake-up

Bits 2 ~ 0: Not used. Set to "**0**" all the time.

6.1.11 Bank 0 R12 WUCR3 (Wake-up Control Register 3)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ICWKP8	ICWKP7	ICWKP6	ICWKP5	–	–	–	–
R/W	R/W	R/W	R/W	–	–	–	–

Bits 7 ~ 4 (ICWKP8 ~ 5): (Ports 8~5) Pin-change Wake-up Function Enable Bit

0: Disable Pin-change wake-up

1: Enable Pin-change wake-up

Bits 3 ~ 0: Not used. Set to "**0**" all the time.

6.1.12 Bank 0 R14 SFR1 (Status Flag Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
–	–	LVDSF	–	EXSF	–	–	TCSF
–	–	F	–	F	–	–	F

Each corresponding status flag is set to "1" when the interrupt condition is triggered.

Bits 7 ~ 6: Not used. Set to "**0**" all the time.

Bit 5 (LVDSF): Low Voltage Detector status flag

LVDEN	LVDS1, LVDS0	LVD Voltage Interrupt Level	LVDSF
1	11	2.2V	1*
1	10	3.3V	1*
1	01	4.0V	1*
1	00	4.5V	1*
0	XX	NA	0

* *If Vdd crossovers at the LVD voltage interrupt level as Vdd varies, LVDSF =1.*

Bit 4: Not used. Set to "**0**" all the time.

Bit 3 (EXSF): External interrupt status flag

Bits 2 ~ 1: Not used. Set to "**0**" all the time.

Bit 0 (TCSF): TCC overflow status flag. Set when TCC overflows. Reset by software.

NOTE

If a function is enabled, the corresponding status flag will be active regardless whether the interrupt mask is enabled or not.

6.1.13 Bank 0 R15 SFR2 (Status Flag Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
–	–	–	–	–	–	–	TC1SF
–	–	–	–	–	–	–	F

Each corresponding status flag is set to "**1**" when the interrupt condition is triggered.

Bits 7~1: Not used. Set to "**0**" all the time.

Bit 0 (TC1SF): 8-bit timer/Counter 1 status flag, cleared by software.

NOTE

If a function is enabled, the corresponding status flag will be active regardless whether the interrupt mask is enabled or not.

6.1.14 Bank 0 R17 SFR4 (Status Flag Register 4)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P8ICSF	P7ICSF	P6ICSF	P5ICSF	–	–	–	–
F	F	F	F	–	–	–	–

Bit 7 (P8ICSF): Port 8 status flag. The flag is cleared by software.

Bit 6 (P7ICSF): Port 7 status flag. The flag is cleared by software.

Bit 5 (P6ICSF): Port 6 status flag. The flag is cleared by software.

Bit 4 (P5ICSF): Port 5 status flag. The flag is cleared by software.

Bits 3 ~ 0: Not used. Set to "**0**" all the time.

6.1.15 Bank 0 R1B IMR1 (Interrupt Mask Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
–	–	LVDIE	–	EXIE	–	–	TCIE
–	–	R/W	–	R/W	–	–	R/W

Bits 7 ~ 6: Not used. Set to "**0**" all the time.

Bit 5 (LVDIE): LVDSF interrupt enable bit.

0: Disable LVDSF interrupt

1: Enable LVDSF interrupt

Bit 4: Not used. Set to "**0**" all the time.

Bit 3 (EXIE): EXSF interrupt enable bit.

0: Disable EXSF interrupt

1: Enable EXSF interrupt

Bits 2 ~ 1: Not used. Set to "**0**" all the time.

Bit 0 (TCIE): TCSF interrupt enable bit.

0: Disable TCSF interrupt

1: Enable TCSF interrupt

NOTE

If the interrupt mask is enabled, the program counter will jump to the corresponding interrupt vector when the corresponding status flag is set.

6.1.16 Bank 0 R1C IMR2 (Interrupt Mask Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
–	–	–	–	–	–	–	TC1IE
–	–	–	–	–	–	–	R/W

Bits 7 ~ 1: Not used. Set to "**0**" all the time.

Bit 0 (TC1IE): Interrupt enable bit.

0: Disable TC1SF interrupt

1: Enable TC1SF interrupt

NOTE

If the interrupt mask is enabled, the program counter will jump to the corresponding interrupt vector when the corresponding status flag is set.

6.1.17 Bank 0 R1E IMR4 (Interrupt Mask Register 4)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P8ICIE	P7ICIE	P6ICIE	P5ICIE	–	–	–	–
R/W	R/W	R/W	R/W	–	–	–	–

Bit 7 (P8ICIE): Interrupt enable bit.

0: Disable P8ICSF interrupt

1: Enable P8ICSF interrupt

Bit 6 (P7ICIE): Interrupt enable bit.

0: Disable P7ICSF interrupt

1: Enable P7ICSF interrupt

Bit 5 (P6ICIE): Interrupt enable bit.

0: Disable P6ICSF interrupt

1: Enable P6ICSF interrupt

Bit 4 (P5ICIE): Interrupt enable bit.

0: Disable P5ICSF interrupt

1: Enable P5ICSF interrupt

Bits 3 ~ 0: Not used. Set to "**0**" all the time.

NOTE

If the interrupt mask is enabled, the program counter will jump to the corresponding interrupt vector when the corresponding status flag is set.

6.1.18 Bank 0 R21 WDTCR (Watchdog Timer Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WDTE	–	–	–	PSWE	WPSR2	WPSR1	WPSR0
R/W	–	–	–	R/W	R/W	R/W	R/W

Bit 7 (WDTE): Watchdog Timer Enable Bit. WDTE is both readable and writable.

0: Disable WDT

1: Enable WDT

Bits 6 ~ 4: Not used. Set to "**0**" all the time.

Bit 3 (PSWE): Prescaler enable bit for WDT

0: Prescaler disable bit. WDT Rate is 1:1.

1: Prescaler enable bit. WDT rate is set at Bits 2~0.

Bit 2 ~ 0 (WPSR2 ~ WPSR0): WDT Prescale Bits

WPSR2	WPSR1	WPSR0	WDT Rate
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

6.1.19 Bank 0 R22 TCCCR (TCC Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
–	TCCS	TS	TE	PSTE	TPSR2	TPSR1	TPSR0
–	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7: Not used. Set to "**0**" all the time.

Bit 6 (TCCS): TCC Clock Source Select Bit

0: Fs (sub clock)

1: Fm (main clock)

Bit 5 (TS): TCC signal source

0: Internal instruction cycle clock

1: Transition on the TCC pin. The TCC period must be larger than the internal instruction clock period.

Bit 4 (TE): TCC Signal Edge

0: Increment if a transition from low to high takes place on the TCC pin

1: Increment if a transition from high to low takes place on the TCC pin

Bit 3 (PSTE): Prescaler enable bit for TCC

0: Prescaler disable bit. The TCC rate is 1:1.

1: Prescaler enable bit. The TCC rate is set at Bit 2 ~ Bit 0.

Bits 2 ~ 0 (TPSR2 ~ TPSR0): TCC Prescaler Bits

TPSR2	TPSR1	TPSR0	TCC Rate
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

6.1.20 Bank 0 R23 TCCD (TCC Data Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TCC7	TCC6	TCC5	TCC4	TCC3	TCC2	TCC1	TCC0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7 ~ 0 (TCC7 ~ TCC0): TCC data

The counter is increased by an external signal edge through the TCC pin, or by the instruction cycle clock. The external signal of the TCC trigger pulse width must be greater than one instruction. The signals to increase the counter are determined by
Bit 4 and Bit 5 of the TCCCR register. Writable and readable as any other registers. If there is an overflow, the value previously written to TCCD will be auto-reloaded to the TCC circuit.

6.1.21 Bank 0 R24 TC1CR1 (Timer/Counter 1 Control Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TC1S	TC1RC	TC1SS1	–	TC1FF	TC1OMS	TC1IS1	TC1IS0
R/W	R/W	R/W	–	R/W	R/W	R/W	R/W

Bit 7 (TC1S): Timer/Counter 1 start control (the total of all mode switches)

0: Stop and clear the counter (default)

1: Start

Bit 6 (TC1RC): Timer 1 Read Control Bit

0: When this bit is set to 0, cannot read data from TC1DB (default).

1: When this bit is set to 1, data read from TC1DB is a number of counting.

Bit 5 (TC1SS1): Timer/Counter 1 clock source select bit1

0: Internal clock as counting source (Fc), Fs/Fm (default)

1: External TC1 pin as counting source (Fc). It is used only for timer/counter mode.

Bit 4: Not used. Set to "**0**" all the time.

Bits 3 (TC1FF): Inversion for Timer/Counter 1 as PWM

0: Duty is Logic 1 (default)

1: Duty is Logic 0

Bit 2 (TC1OMS): Timer Output Mode Select Bit

0: Repeating mode (default)

1: One-shot mode

NOTE

One-shot mode means the timer only counts a cycle.

Bits 1 ~ 0 (TC1IS1 ~ TC1IS0): Timer 1 Interrupt Type Select Bits. These two bits are used when the Timer operates in PWM mode.

TC1IS1	TC1IS0	Timer 1 Interrupt Type Select
0	0	TC1DA (period) matching
0	1	TC1DB (duty) matching
1	×	TC1DA and TC1DB matching

6.1.22 Bank 0 R25 TC1CR2 (Timer/Counter 1 Control Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TC1M2	TC1M1	TC1M0	TC1SS0	TC1CK3	TC1CK2	TC1CK1	TC1CK0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7 ~ 5 (TC1M2 ~ TC1M0): Timer/Counter 1 Operation Mode Select.

TC1M2	TC1M1	TC1M0	Operating Mode Select
0	0	0	Timer/Counter Rising Edge
0	0	1	Timer/Counter Falling Edge
0	1	0	Capture Mode Rising Edge
0	1	1	Capture Mode Falling Edge
1	0	0	Window mode
1	0	1	Programmable Divider output
1	1	0	Pulse Width Modulation output
1	1	1	Buzzer (output timer timer/counter clock source. The duty cycle of the clock source must be 50/50)

Bit 4 (TC1SS0): Timer/Counter 1 clock source select bit

0: Fs is used as counting source (Fc) (default)

1: Fm is used as counting source (Fc)

Bits 3 ~ 0 (TC1CK3 ~ TC1CK0): Timer/Counter 1 clock source prescaler select

TC1CK3	TC1CK2	TC1CK1	TC1CK0	Clock Source	Resolution 8 MHz	Max. Time 8 MHz	Resolution 16kHz	Max. Time 16kHz
				Normal	FC=8M	FC=8M	FC=16K	FC=16K
0	0	0	0	FC	125ns	32 μs	62.5 μs	16 ms
0	0	0	1	FC/2	250ns	64 μs	125 μs	32 ms
0	0	1	0	FC/22	500ns	128 μs	250 μs	64 ms
0	0	1	1	FC/23	1 μs	256 μs	500 μs	128 ms
0	1	0	0	FC/24	2 μs	512 μs	1 ms	256 ms
0	1	0	1	FC/25	4 μs	1024 μs	2 ms	512 ms
0	1	1	0	FC/26	8 μs	2048 μs	4 ms	1024 ms
0	1	1	1	FC/27	16 μs	4096 μs	8 ms	2048 ms
1	0	0	0	FC/28	32 μs	8192 μs	16 ms	4096 ms
1	0	0	1	FC/29	64 μs	16384 μs	32 ms	8192 ms
1	0	1	0	FC/210	128 μs	32768 μs	64 ms	16384 ms
1	0	1	1	FC/211	256 μs	65536 μs	128 ms	32768 ms
1	1	0	0	FC/212	512 μs	131072 μs	256 ms	65536 ms
1	1	0	1	FC/213	1.024 ms	262144 μs	512 ms	131072 ms
1	1	1	0	FC/214	2.048 ms	524.288 ms	1.024 s	262144 ms
1	1	1	1	FC/215	4.096 ms	1.048 s	2.048 s	524288 ms

6.1.23 Bank 0 R26 TC1DA (Timer/Counter 1 Data Buffer A)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TC1DA7	TC1DA6	TC1DA5	TC1DA4	TC1DA3	TC1DA2	TC1DA1	TC1DA0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7 ~ 0 (TC1DA7 ~ TC1DA0): Data buffer A of 8 bit timer/counter

6.1.24 Bank 0 R27 TC1DB (Timer/Counter 1 Data Buffer B)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TC1DB7	TC1DB6	TC1DB5	TC1DB4	TC1DB3	TC1DB2	TC1DB1	TC1DB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7 ~ 0 (TC1DB7 ~ TC1DB0): Data buffer B of 8-bit Timer/Counter 1

NOTE

1. *When Timer / Counter x is used in PWM mode, the duty value stored at Register TCxDB must be smaller than or equal to the period value stored at Register TCxDA.,i.e;. duty ≤period. Then the PWM waveform is generated. If the duty is greater than the period, the PWM output waveform is kept at **high** voltage level.*
2. *The period value set by user is automatically added by 1 within the inner circuit.*
   For example:
   When the period value is set as 0x4F, the circuit processes 0x50 as actual period length.
   When the period value is set as 0xFF, the circuit processes 0x100 as actual period length.

6.1.25 Bank 1 R5 IOCR8

These registers are used to control the I/O port direction. They are both readable and writable.

0: Put the relative I/O pin as output

1: Put the relative I/O pin into high impedance

6.1.26 Bank 1 R8: P5PHCR (Port 5 Pull-high Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
–	–	–	–	–	PH52	PH51	PH50
–	–	–	–	–	R/W	R/W	R/W

Bits 7 ~ 3: Not used. Set to "**1**" all the time.

Bit 2 (PH52): Control bit used to enable pull-high of P52 pin

0: Enable internal pull-high

1: Disable internal pull-high

Bit 1 (PH51): Control bit used to enable pull-high of the P51 pin

Bit 0 (PH50): Control bit used to enable pull-high of the P50 pin

6.1.27 Bank 1 R9 P6PHCR (Port 6 Pull-high Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
–	PH66	PH65	PH64	PH63	PH62	PH61	PH60
–	R/W	R/W	R/W	R/W	R/W	R/W	R/W

All of these bits are low active

Bit 7: Not used. Set to "**1**" all the time.

Bit 6 (PH66): Control bit used to enable pull-high of the P66 pin

Bit 5 (PH65): Control bit used to enable pull-high of the P65 pin

Bit 4 (PH64): Control bit used to enable pull-high of the P64 pin

Bit 3 (PH63): Control bit used to enable pull-high of the P63 pin

Bit 2 (PH62): Control bit used to enable pull-high of the P62 pin

Bit 1 (PH61): Control bit used to enable pull-high of the P61 pin

Bit 0 (PH60): Control bit used to enable pull-high of the P60 pin

6.1.28 Bank 1 RA P78PHCR (Ports 7~8 Pull-high Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
–	–	–	–	P8HPH	P8LPH	P7HPH	P7NPH
–	–	–	–	R/W	R/W	R/W	R/W

All of these bits are low active.

Bits 7 ~ 4: Not used. Set to "**1**" all the time.

Bit 3 (P8HPH): Control bit used to enable pull-high of the Port 8 high nibble pin

Bit 2 (P8LPH): Control bit used to enable pull-high of the Port 8 low nibble pin

Bit 1 (P7HPH): Control bit used to enable pull-high of the Port 7 high nibble pin

Bit 0 (P7LPH): Control bit used to enable pull-high of the Port 7 low nibble pin

6.1.29 Bank 1 RD P7PLCR (Port 7 Pull-low Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
–	–	–	–	–	–	P7HPL	P7LPL
–	–	–	–	–	–	R/W	R/W

All of these bits are low active.

Bits 7 ~ 2: Not used. Set to "**1**" all the time.

Bit 1 (P7HPH): Control bit used to enable pull low of the Port 7 high nibble pin

Bit 0 (P7LPH): Control bit used to enable pull low of the Port 7 low nibble pin

6.1.30 Bank 1 RF P6HDSCR (Port 6 High Drive/Sink Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
–	–	–	–	–	–	H61	H60
–	–	–	–	–	–	R/W	R/W

Bits 7 ~ 2: Not used. Set to "**1**" all the time.

Bits 1 ~ 0 (H61 ~ H60): P61~P60 high sink current control bits

0: Enable high drive/sink

1: Disable high drive/sink

6.1.31 Bank 1 R10 P78HDSCR (Ports 7 ~ 8 High Drive/Sink Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
–	–	–	–	P8HHDS	P8LHDS	P7HHDS	P7LHDS
–	–	–	–	R/W	R/W	R/W	R/W

All of these bits are low active.

Bits 7 ~ 4: Not used. Set to "**1**" all the time.

Bit 3 (P8HHDS): Control bit used to enable high drive/sink of Port 8 high nibble pin

Bit 2 (P8LHDS): Control bit used to enable high drive/sink of Port 8 low nibble pin

Bit 1 (P7HHDS): Control bit used to enable high drive/sink of Port 7 high nibble pin

Bit 0 (P7LHDS): Control bit used to enable high drive/sink of Port 7 low nibble pin

6.1.32 Bank 1 R12 P6ODCR (Port 6 Open-Drain Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OD67	OD66	OD65	OD64	OD63	OD62	OD61	OD60
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7 (OD67): Open-Drain control bit. This bit is set to "**0**" all the time as P67 is always enabled as Open-Drain.

Bits 6 ~ 0 (OD66 ~ OD60): Open-Drain control bits

0: Disable open-drain function

1: Enable open-drain function

6.1.33 Bank 1 R45 TBPTL (Table Point Low Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TB7	TB6	TB5	TB4	TB3	TB2	TB1	TB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7 ~ 0 (TB7 ~ TB0): Table Point Address Bits 7 ~ 0.

6.1.34 Bank 1 R46 TBPTH (Table Point High Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
HLB	GP0	–	–	TB11	TB10	TB9	TB8
R/W	R/W	–	–	R/W	R/W	R/W	R/W

Bit 7 (HLB): Take MLB or LSB at machine code

Bit 6 (GP0): General purpose read/write bits

Bits 5 ~ 4: Not used. Set to "**0**" all the time.

Bits 3 ~ 0 (TB11 ~ TB8): Table Point Address Bits 11 ~ 8.

6.1.35 Bank 1 R47 Stack Pointer

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
STOV	–	–	–	–	STL2	STL1	STL0
R	–	–	–	–	R	R	R

Bit 7 (STOV): Stack pointer overflow indication bit. Read only.

Bits 2 ~ 0 (STL2 ~ 0): Stack pointer number. Read only.

6.1.36 Bank 1 R48 PCH (Program Counter High)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
–	–	–	–	PC11	PC10	PC9	PC8
–	–	–	–	R/W	R/W	R/W	R/W

Bits 7 ~ 4: Not used. Set to "**0**" all the time.

Bits 3 ~ 0 (PC11 ~ PC8): High byte of the program counter.

6.1.37 Bank 1 R49 LVDCR (Low Voltage Detect Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LVDEN	–	LVDS1	LVDS0	LVDB	–	–	–
R/W	–	R/W	R/W	R	–	–	–

Bit 7 (LVDEN): Low Voltage Detector Enable Bit

0: Disable low voltage detector

1: Enable low voltage detector

Bit 6: Not used. Set to "**0**" all the time.

Bits 5 ~ 4 (LVDS1 ~ LVDS0): Low Voltage Detector Level Bits.

LVDEN	LVDS1, LVDS0	LVD Voltage Interrupt Level	LVDB
1	11	VDD < 2.2V	0
		VDD > 2.2V	1
1	10	VDD < 3.3V	0
		VDD > 3.3V	1
1	01	VDD < 4.0V	0
		VDD > 4.0V	1
1	00	VDD < 4.5V	0
		VDD > 4.5V	1
0	XX	NA	1

Bit 3 (LVDB): Low Voltage Detector State Bit. This is a read only bit. When the VDD pin voltage is lower than the LVD voltage interrupt level (selected by LVDS2 ~ LVDS0), this bit will be cleared.

0: Low voltage is detected

1: Low voltage is not detected or LVD function is disabled.

Bits 2 ~ 0: Not used. Set to "**0**" all the time.

6.2 TCC/WDT and Prescaler

Two 8-bit counters are available as prescalers for the TCC and WDT respectively. The TPSR0~ TPSR2 bits of the TCCCR register (Bank 0 R22) are used to determine the ratio of the TCC prescaler. Likewise, the WPSR0~WPSR2 bits of the WDTCR register (Bank 0 R21) are used to determine the WDT prescaler. The prescaler counter is cleared by the instructions each time they are written into TCC. The WDT and prescaler counter are cleared by the "WDTC" and "SLEP" instructions. Figure 6-3 below depicts the block diagram of TCC/WDT.

TCCD (Bank 0 R23) is an 8-bit timer/counter. The clock source of TCC can be either internal clock or external signal input (edge selectable from the TCC pin). As illustrated in Figure 6-3, if the TCC signal source is from an internal clock, TCC will increase by 1 at every instruction cycle (without prescaler). If the TCC signal source is from an external clock input, TCC will increase by 1 at every falling edge or rising edge of the TCC pin. The TCC pin input time length (keep in High or Low level) must be greater than 1CLK. **The TCC will stop running when Sleep mode occurs.**

The Watchdog Timer is a free running on-chip RC oscillator. The WDT will keep on running even after the oscillator driver has been turned off (i.e., in Sleep mode). During normal operation or the Sleep mode, a WDT time-out (if enabled) will cause the device to reset. The WDT can be enabled or disabled at any time during the Normal mode by software programming (refer to WDTE bit of WDTCR (Bank 0 R21) register in Section. 6.1.8). With no prescaler, the WDT time-out period is approximately 16 ms[1] (one oscillator start-up timer period).

[1] *VDD=5V, WDT time-out period = 16ms ± 10%.*
VDD=3V, WDT time-out period = 16ms ± 10%.

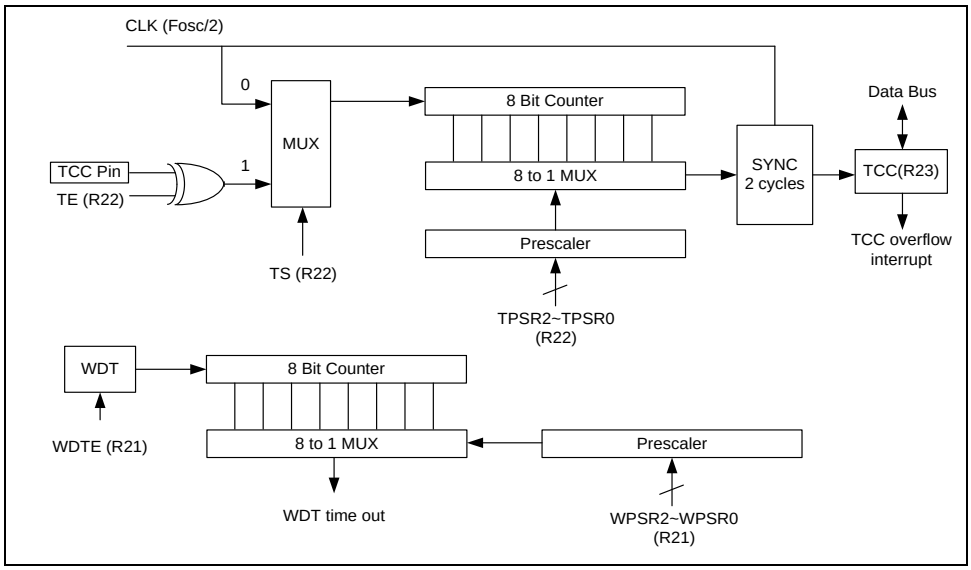


Figure 6-3 TCC and WDT Block Diagram

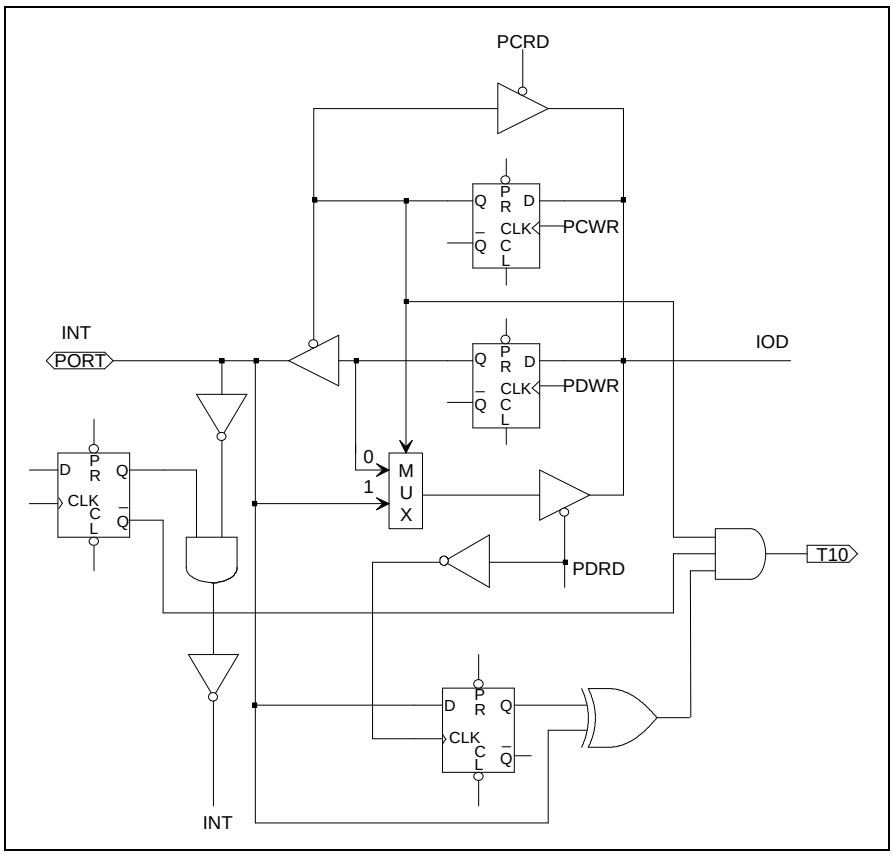
6.3 I/O Ports

The I/O registers, Port 5~Port 8 are bi-directional tri-state I/O ports. They can be pulled high and pulled low internally by software. They can also be set as open-drain output and high sink/drive setting by software. Ports 5~8 feature Wake-up and interrupt functions as well as input status change interrupt function. Each I/O pin can be defined as "input" or "output" pin by the I/O control registers (IOC5 ~ IOC8).

The I/O registers and I/O control registers are both readable and writable. The I/O interface circuits for Port 5 ~ Port 8 are shown in the following Figures 6-4a to 6-4c.

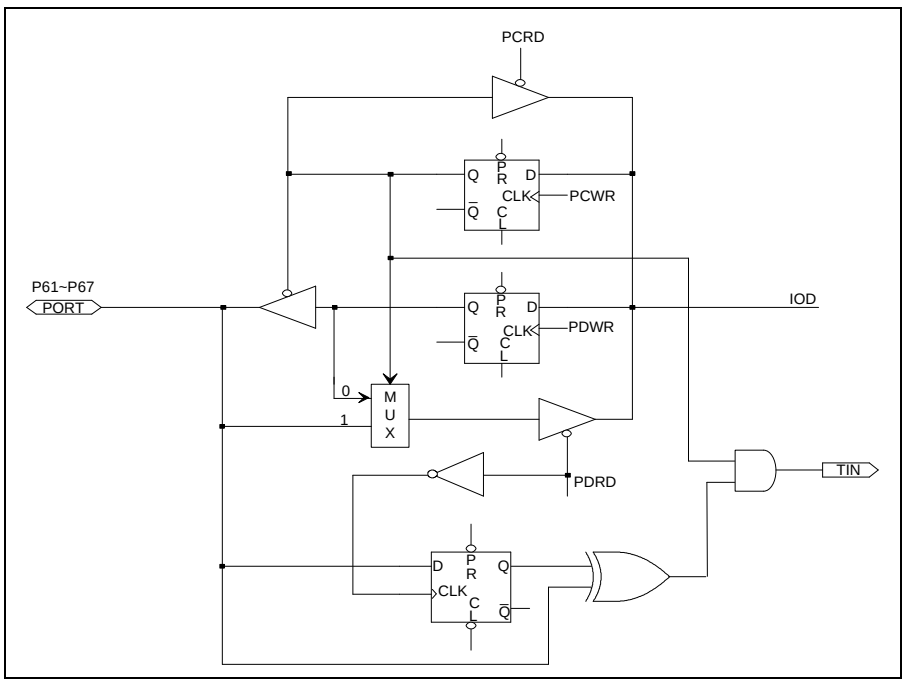
The EM78P224N has two different types of packaging with different number of pins. To achieve maximum power consumption, it is highly recommended to program P80, P81, P82, and P83 on the 32 and 28-packagings as “not used” under the following conditions**:**

1. When the “not-used” pins need to be defined as output ports, the pins should be set as output high or pull low relative to its pull high/low status.
2. When the “not-used” pins need to be defined as input ports, the pins should be set as input pull high or pull low.



Note: *Pull-high (down) and Open-drain are not shown in the figure.*

Figure 6-4a I/O Port and I/O Control Register Circuit for /INT



Note: *Pull-high (down) and Open-drain are not shown in the figure.*

Figure 6-4b I/O Port and I/O Control Register Circuit for Port 5~8

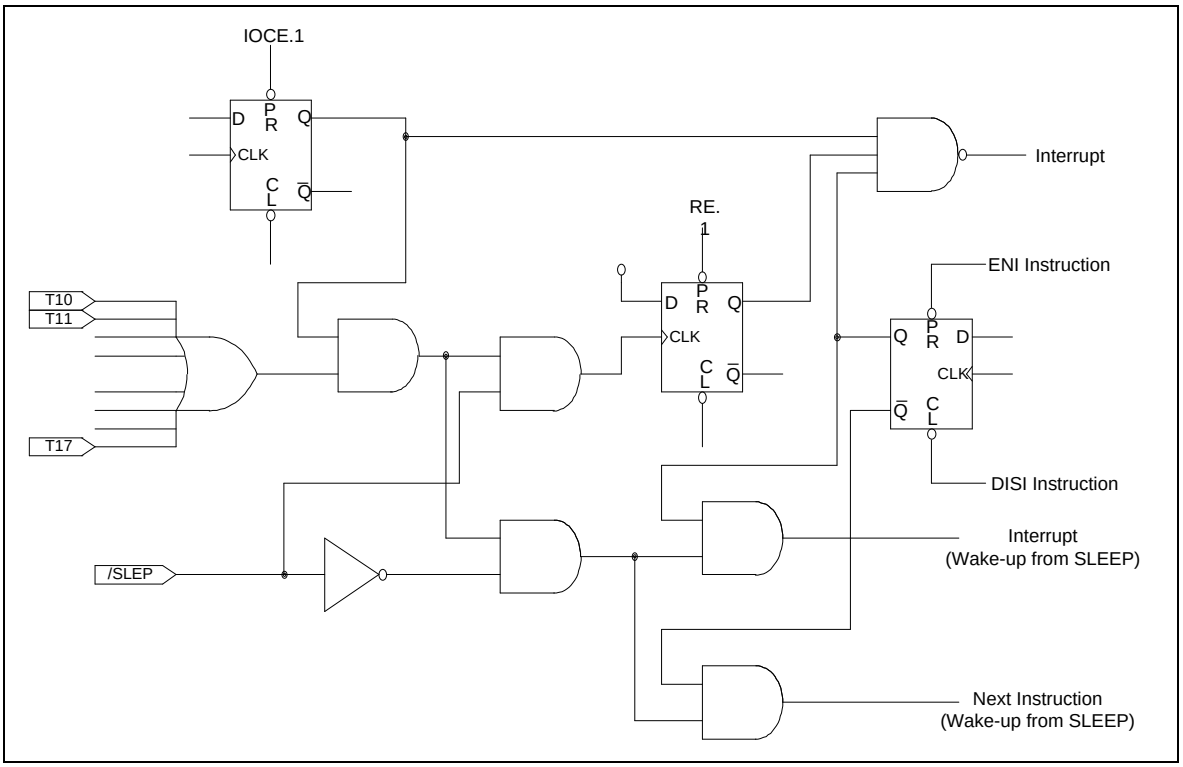


Figure 6-4c I/O Port 5~8 with Input Change Interrupt/Wake-up Block Diagram

6.3.1 Usage of Ports 5~8 Input Changed Wake-up/Interrupt Function

1. Wake-up
a) Before SLEEP:
1) Disable WDT
2) Read I/O Port (MOV R6,R6)
3) Execute "ENI" or "DISI"
4) Enable wake-up bit (Set ICWK6 =1)
5) Execute "SLEP" instruction
b) After Wake-up:
→ Next instruction

2. Wake-up and Interrupt
a) Before SLEEP
1) Disable WDT
2) Read I/O Port (MOV R6, R6)
3) Execute "ENI" or "DISI"
4) Enable wake-up bit (Set ICWK6 =1)
5) Enable interrupt (Set P6ICIE =1)
6 Execute "SLEP" instruction
b) After Wake-up
1) IF "ENI" → Interrupt vector (0006H)
2) IF "DISI" → Next instruction

6.4 Reset and Wake-up Operations

6.4.1 Reset

A reset is initiated by one of the following events**:**

1) Power-on reset

2) /RESET pin input "low", or

3) WDT time-out (if enabled)

4) LVR (if enabled)

The device is kept in a reset condition for a period of approximately 18 ms (one oscillator start-up timer period) after the Power-on reset is detected. If the /Reset pin goes “low” or WDT time-out is active, a reset is generated. In RC mode the reset time is 8 clocks, in XTAL mode, the reset time is 510 clocks. Once a RESET occurs, the following functions are performed.

- The oscillator continues running, or will be started.
- The Program Counter (R2) is set to all "**0**".
- The contents of the stack are cleared to all “**0**”.
- All I/O port pins are configured as input mode (high-impedance state).
- The Watchdog Timer and prescaler are cleared.
- When power is switched on, R1 is cleared.
- The control register bits are set according to the table shown in Section 6.4.4, *Summary of Register Initial Values after Reset*.

Executing the “SLEP” instruction will assert the Sleep (power down) mode. While entering Sleep mode, the Oscillator, TCC and Timer1 are stopped. The WDT (if enabled) is cleared but keeps on running. Wake-up time is then generated (in RC mode, the wake-up time is 8 clocks, in High XTAL mode, the wake-up time is 2 ms and 510 clocks, in Low XTAL mode, the wake-up time is 255 clocks). The controller can be awakened by any of the following events**:**

1) External reset input on /RESET pin

2) WDT time-out (if enabled)

3) Port input status change (if ICWKx is enabled)

4) External Interrupt status change (if INTWK is enabled)

5) Low Voltage Detector (if LVDWE is enabled)

The first two events will cause the MCU to reset. The T and P flags of R3 can be used to determine the source of the reset (Wake-up). Cases 3~5 are considered the continuation of program execution and the global interrupt ("ENI" or "DISI" being executed) determines whether or not the controller branches to the interrupt vector following a Wake-up. If ENI is executed before SLEP, the instruction will begin to execute from the Address 0x03~0x22 by each interrupt vector after Wake-up. If DISI is executed before SLEP, the execution will restart from the instruction right next to SLEP after Wake-up. From Sleep to Normal mode, the Wake-up time is 510 clocks + warm-up time with Crystal oscillator and 8 clocks (Fm) + warm-up time with IRC oscillator. From Idle to Green mode, only warm-up time is needed. From Sleep to Green mode the wake-up time is 8 clocks (Fs) + warm-up time.

One or more of the Events 3 to 5 can be enabled before entering into Sleep mode. That is**:**

a) If WDT is enabled before SLEP, all Wake-up bits are disabled. Hence, the MCU can be waked up only under Events 1 or 2 conditions. Refer to the Section 6.5, *Interrupt*; for further details.

b) If Port Input Status Change is used to wake-up the MCU and Bank 0-R11 register is enabled before SLEP, the WDT must be disabled. Hence, the MCU can be waked up only under Event 3 condition.

c) If External Interrupt Status Change is used to wake-up MCU and INTWK bit is enabled before SLEP, WDT must be disabled by software. Hence, the MCU can be waked up only under Event 4 condition.

d) If Low voltage detector is used to wake-up the MCU and LVDWK bit of Bank 0-RF register is enabled before SLEP, WDT must be disabled by software. Hence, the MCU can be waked up only under Event 5 condition.

If input Status Change Interrupt is used to Wake-up the MCU (as in the Event b above), the subsequent instructions must be executed before SLEP:

6.4.2 Wake-up

Summary of Wake-up and Interrupt modes

Event (Corresponding Wake-up Bit is Enabled)	Sleep Mode		Idle Mode		Green Mode	Normal Mode
	Interrupt Disable	Interrupt Enable	Interrupt Disable	Interrupt Enable		
TCC	X	Wake-up only for external clock source	X	Wake-up + interrupt + next instruction	Interrupt (if interrupt is enabled)	Interrupt (if interrupt is enabled)
INT pin	Wake-up + next instruction	Wake-up + interrupt + next instruction	Wake-up + next instruction	Wake-up + interrupt + next instruction	Interrupt (if interrupt is enabled)	Interrupt (if interrupt is enabled)
Timer 1	X	Wake-up only for external clock source	X	Wake-up + interrupt + next instruction	Interrupt (if interrupt is enabled)	Interrupt (if interrupt is enabled)
Pin change	Wake-up + next instruction	Wake-up + interrupt + next instruction	Wake-up + next instruction	Wake-up + interrupt + next instruction	Interrupt (if interrupt is enabled)	Interrupt (if interrupt is enabled)
LVD	Wake-up + next instruction	Wake-up + interrupt + next instruction	Wake-up + next instruction	Wake-up + interrupt + next instruction	Interrupt (if interrupt is enabled)	Interrupt (if interrupt is enabled)
Low Voltage Reset	RESET	RESET	RESET	RESET	RESET	RESET
WDT Time-out	RESET	RESET	RESET	RESET	RESET	RESET

NOTE

After Wake-up:

1. If interrupt is enabled → interrupt+ next instruction

2. If interrupt is disabled → next instruction

6.4.3 Status of RST, T, and P of the Status Register

A reset condition is initiated by one of the following events:

1) A power-on condition

2. A high-low-high pulse on /RESET pin, and

3. Watchdog timer time-out.

The values of T and P as listed in the following table are used to check how the processor wakes up. The second table shows the events that may affect the status of T and P.

■ Values of RST, T and P after RESET

Reset Type	T	P
Power on	1	1
/RESET during Operating mode	*P	*P
/RESET wake-up during Sleep mode	1	0
WDT during Operating mode	0	*P
WDT wake-up during Sleep mode	0	0
Wake-up on pin change during Sleep mode	1	0

***P:** Previous status before reset*

■ Status of T and P Being Affected by Events

Event	T	P
Power on	1	1
WDTC instruction	1	1
WDT time-out	0	*P
SLEP instruction	1	0
Wake-up on pin change during Sleep mode	1	0

***P:** Previous value before reset*

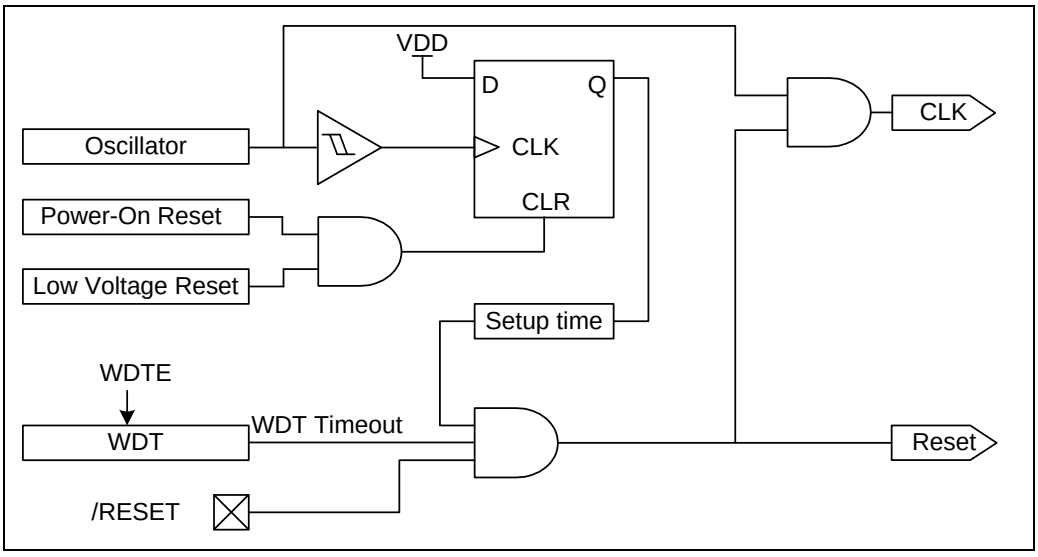


Figure 6-5 Block Diagram of Controller Reset

6.4.4 Summary of Register Initial Values after Reset

Legend: ***U:*** *Unknown or don't care* ***P:*** *Previous value before reset*
C: *Same with Code option* ***t:*** *Check tables under Section 6.4.2*

Address	Bank, Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x00	R0 (IAR)	Bit Name	-	-	-	-	-	-	-	-
		Power-On	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0x01	R1 (BSR)	Bit Name	0	0	0	SBS0	0	0	0	0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	0	0	0	P	0	0	0	0
0x02	R2 (PC)	Bit Name	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0x03	R3 (SR)	Bit Name	INT	0	0	T	P	Z	DC	C
		Power-on	0	0	0	1	1	U	U	U
		/RESET and WDT	0	0	0	t	t	P	P	P
		Wake-up from Sleep/Idle	P	0	0	t	t	P	P	P
0x04	R4 (RSR)	Bit Name	RSR7	RSR6	RSR5	RSR4	RSR3	RSR2	RSR1	RSR0
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X05	Bank 0, R5 (Port 5)	Bit Name	P57	P56	P55	P54	P53	P52	P51	P50
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0x06	Bank 0, R6 (Port 6)	Bit Name	P67	P66	P65	P64	P63	P62	P61	P60
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P

(Continuation)

Address	Bank, Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x07	Bank 0, R7 (Port 7)	Bit Name	P77	P76	P75	P74	P73	P72	P71	P70
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0x08	Bank 0, R8 (Port 8)	Bit Name	0	0	P85	P84	P83	P82	P81	P80
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	0	0	P	P	P	P	P	P
0X0B	Bank 0, RB (IOCR5)	Bit Name	IOC57	IOC56	IOC55	IOC54	IOC53	IOC52	IOC51	IOC50
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0x0C	Bank 0, RC (IOCR6)	Bit Name	IOC67	IOC66	IOC65	IOC64	IOC63	IOC62	IOC61	IOC60
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	P	P
0X0D	Bank 0, RD (IOCR7)	Bit Name	IOC77	IOC76	IOC75	IOC74	IOC73	IOC72	IOC71	IOC70
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0x0E	Bank 0, RE (OMCR)	Bit Name	CPUS	IDLE	0	0	0	0	RCM1	RCM0
		Power-on	1	1	0	0	0	0	0	0
		/RESET and WDT	1	1	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	0	0	0	0	P	P
0X0F	Bank 0, RF (EIESCR)	Bit Name	0	0	0	0	EIES	0	0	0
		Power-on	0	0	0	0	1	0	0	0
		/RESET and WDT	0	0	0	0	1	0	0	0
		Wake-up from Sleep/Idle	0	0	0	0	P	0	0	0

(Continuation)

Address	Bank, Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x10	Bank 0, R10 (WUCR1)	Bit Name	0	0	LVDWK	0	INTWK	0	0	0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	0	0	P	0	P	0	0	0
0X12	Bank 0, R12 (WUCR3)	Bit Name	ICWKP8	ICWKP7	ICWKP6	ICWKP5	0	0	0	0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	0	0	0	0
0X14	Bank 0, R14 SFR1	Bit Name	0	0	LVDSF	0	EXSF	0	0	TCSF
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	0	0	P	0	P	0	0	P
0X15	Bank 0, R15 SFR2	Bit Name	0	0	0	0	0	0	0	TC1SF
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	0	0	0	0	0	0	0	P
0X17	Bank 0, R17 SFR4	Bit Name	P8ICSF	P7ICSF	P6ICSF	P5ICSF	0	0	0	0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	0	0	0	0
0X1B	Bank 0, R1B IMR1	Bit Name	0	0	LVDIE	0	EXIE	0	0	TCIE
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	0	0	P	0	P	0	0	P
0X1C	Bank 0, R1C IMR2	Bit Name	0	0	0	0	0	0	0	TC1IE
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	0	0	0	0	0	0	0	P

(Continuation)

Address	Bank, Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0X1E	Bank 0, R1E IMR4	Bit Name	P8ICIE	P7ICIE	P6ICIE	P5ICIE	0	0	0	0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	0	0	0	0
0X21	BANK 0, R21 WDTCR	Bit Name	WDTE	0	0	0	PSWE	WPSR2	WPSR1	WPSR0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	0	0	0	P	P	P	P
0X22	Bank 0, R22 TCCR	Bit Name	0	TCCS	TS	TE	PSTE	TPSR2	TPSR1	TPSR0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	0	P	P	P	P	P	P	P
0X23	Bank 0, R23 TCCD	Bit Name	TCC7	TCC6	TCC5	TCC4	TCC3	TCC2	TCC1	TCC0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X24	Bank 0, R24 TC1CR1	Bit Name	TC1S	TC1RC	TC1SS1	0	TC1FF	TC1OMS	TC1IS1	TC1IS0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	0	P	P	P	P
0X25	Bank 0, R25 TC1CR2	Bit Name	TC1M2	TC1M1	TC1M0	TC1SS0	TC1CK3	TC1CK2	TC1CK1	TC1CK0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X26	Bank 0, R26 TC1DA	Bit Name	TC1DA7	TC1DA6	TC1DA5	TC1DA4	TC1DA3	TC1DA2	TC1DA1	TC1DA0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P

(Continuation)

Address	Bank, Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0X27	Bank 0, R27 TC1DB	Bit Name	TC1DB7	TC1DB6	TC1DB5	TC1DB4	TC1DB3	TC1DB2	TC1DB1	TC1DB0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X05	Bank 1, R5 IOCR8	Bit Name	0	0	IOC85	IOC84	IOC83	IOC82	IOC81	IOC80
		Power-on	0	0	1	1	1	1	1	1
		/RESET and WDT	0	0	1	1	1	1	1	1
		Wake-up from Sleep/Idle	0	0	P	P	P	P	P	P
0X08	Bank 1, R8 P5PHCR	Bit Name	1	1	1	1	1	PH52	PH51	PH50
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Sleep/Idle	1	1	1	1	1	P	P	P
0X09	Bank 1, R9 P6PHCR	Bit Name	1	PH66	PH65	PH64	PH63	PH62	PH61	PH60
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Sleep/Idle	1	P	P	P	P	P	P	P
0X0A	Bank 1, RA P78PHCR	Bit Name	1	1	1	1	P8HPH	P8LPH	P7HPH	P7LPH
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Sleep/Idle	1	1	1	1	P	P	P	P
0X0D	Bank 1, RD P7PLCR	Bit Name	1	1	1	1	1	1	P7HPL	P7LPL
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Sleep/Idle	1	1	1	1	1	1	P	P
0X0F	Bank 1, RF P6HDSCR	Bit Name	1	1	1	1	1	1	H61	H60
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Sleep/Idle	1	1	1	1	1	1	P	P

(Continuation)

Address	Bank, Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0X10	Bank 1, R10 P78HDSCR	Bit Name	1	1	1	1	P8HHDS	P8LHDS	P7HHDS	P7LHDS
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Sleep/Idle	1	1	1	1	P	P	P	P
0X12	Bank 1, R12 P6ODCR	Bit Name	OD67	OD66	OD65	OD64	OD63	OD62	OD61	OD60
		Power-on	1	0	0	0	0	0	0	0
		/RESET and WDT	1	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	1	P	P	P	P	P	P	P
0X45	Bank 1, R45 TBPTL	Bit Name	TB7	TB6	TB5	TB4	TB3	TB2	TB1	TB0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X46	Bank 1, R46 TBPTH	Bit Name	HLB	GP0	0	0	TB11	TB10	TB9	TB8
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	0	0	P	P	P	P
0X47	Bank 1, R47 STKMON	Bit Name	STOV	0	0	0	0	STL2	STL1	STL0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	0	0	0	0	P	P	P
0X48	Bank 1, R48 PCH	Bit Name	0	0	0	0	PC11	PC10	PC9	PC8
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	0	0	0	0	P	P	P	P
0X49	Bank 1, R49 LVDCR	Bit Name	LVDEN	0	LVDS1	LVDS0	LVDB	0	0	0
		Power-on	0	0	0	0	1	0	0	0
		/RESET and WDT	0	0	0	0	1	0	0	0
		Wake-up from Sleep/Idle	P	0	P	P	P	0	0	0

6.5 Interrupt

The EM78P224N has five interrupts as listed below:

Interrupt Source		Enable Condition	Int. Flag	Int. Vector	Priority
Internal / External	Reset	-	-	0	High 0
External	INT	ENI + EXIE=1	EXSF	2	1
External	Pin change	ENI +ICIE=1	ICSF	4	2
Internal	TCC	ENI + TCIE=1	TCSF	6	3
Internal	LVD	ENI+LVDEN & LVDIE=1	LVDSF	8	4
Internal	TC1(TCXDA)	ENI + TC1IE=1	TC1SF	12	5

Bank 0 R14~R17 are the interrupt status registers that record the interrupt requests in the relative flags/bits. Bank 0 R1B~R1E is the interrupt mask register. The global interrupt is enabled by the ENI instruction and is disabled by the DISI instruction. When one of the interrupts (if enabled) occurs, the next instruction will be fetched from an individual address. The interrupt flag bit must be cleared by instructions before leaving the interrupt service routine and before interrupts are enabled to avoid recursive interrupts.

The flag (except when PxICSF bit is deleted) in the Interrupt Status Register is set regardless of the status of its mask bit or the execution of ENI. The RETI instruction ends the interrupt routine and enables the global interrupt (the execution of ENI).

External interrupt is equipped with digital noise rejection circuit (input pulse of less than **4 system clocks time** is eliminated as noise if code option NRHL=0), **but in Low XTAL oscillator (LXT) mode the noise rejection circuit is disabled**. When an interrupt (falling edge) is generated by the External interrupt (when enabled), the next instruction will be fetched from Address 003H.

Before the interrupt subroutine is executed, the contents of ACC, R3, and R4 registers are saved by hardware. If another interrupt occurs, the ACC, R3, and R4 will be replaced by the new interrupt. After the interrupt service routine is finished, ACC, R3, and R4 are restored.

When the RESET (POR, LVR, WDT, and /RESET) occurs, the contents of stack would be cleared to all "**0**".

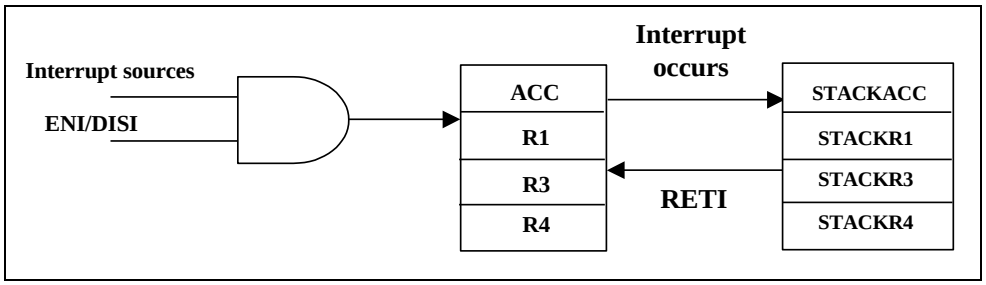


Figure 6-6a Interrupt Back-up Diagram

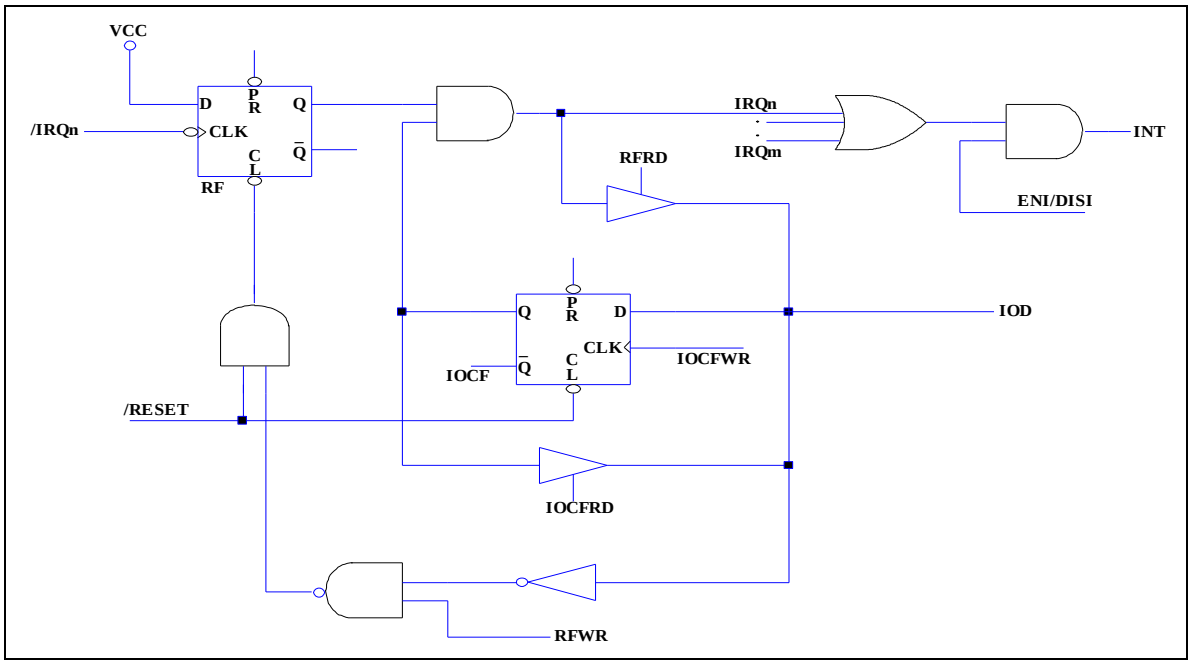


Figure 6-6b Interrupt Input Circuit

6.6 Timer

The EM78P224N has a timer, Timer 1 which can be an 8-bit up-counter.

R_BANK	Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bank 0	0x24	TC1CR1	TC1S	TC1RC	TC1SS1	TC1MOD	TC1FF	TC1OMS	TC1IS1	TC1IS0
			R/W	R/W	R/W	R/W	R	R/W	R/W	R/W
Bank 0	0x25	TC1CR2	TC1M2	TC1M1	TC1M0	TC1SS0	TC1CK3	TC1CK2	TC1CK1	TC1CK0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 0	0x26	TC1DA	TC1DA7	TC1DA6	TC1DA5	TC1DA4	TC1DA3	TC1DA2	TC1DA1	TC1DA0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 0	0x27	TC1DB	TC1DB7	TC1DB6	TC1DB5	TC1DB4	TC1DB3	TC1DB2	TC1DB1	TC1DB0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 0	0x16	ISR2								TC1SF
										F
Bank 0	0x1C	IMR2								TC1IE
										R/W

6.6.1 Timer/Counter Mode

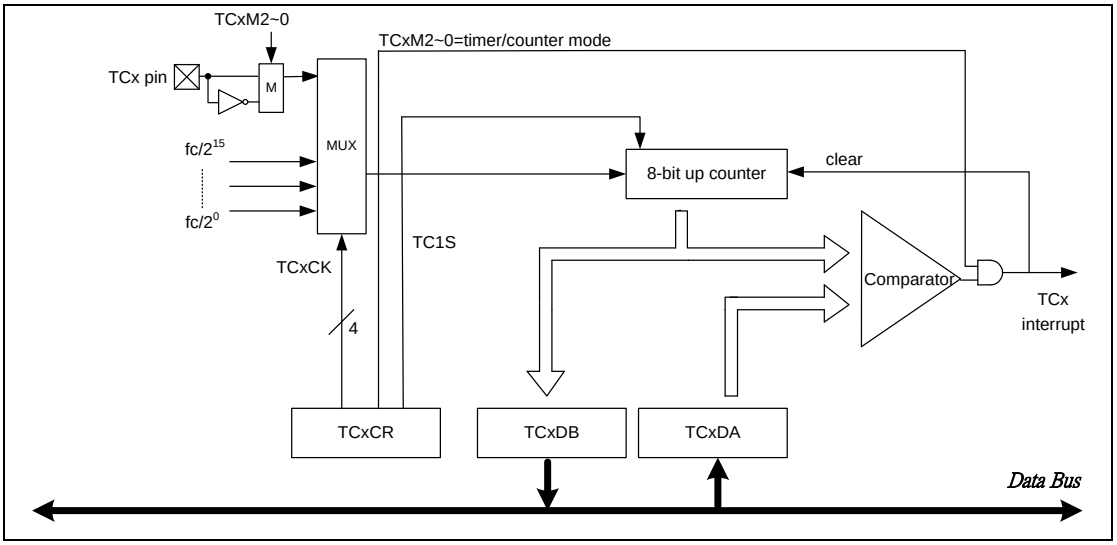


Figure 6-7a Timer/Counter Mode Diagram

In Timer/Counter mode, counting up is performed using internal clock or TCx pin. When the contents of the up-counter match the TCxDA, the interrupt is generated and the counter is cleared. Counting up resumes after the counter is cleared. The current contents of the up-counter are loaded into TCxDB by setting TCxRC to "**1**".

When in Counter mode with the MCU operating in Sleep mode, the counting edge of the timer TCx Pin is selected to rising edge. When the contents of the up-counter match the TCxDA, the MCU will wake-up and enters into interrupt by generating a falling edge from TCx pin and vice versa.

The Timer/Counter mode waveforms are illustrated in the following figures.

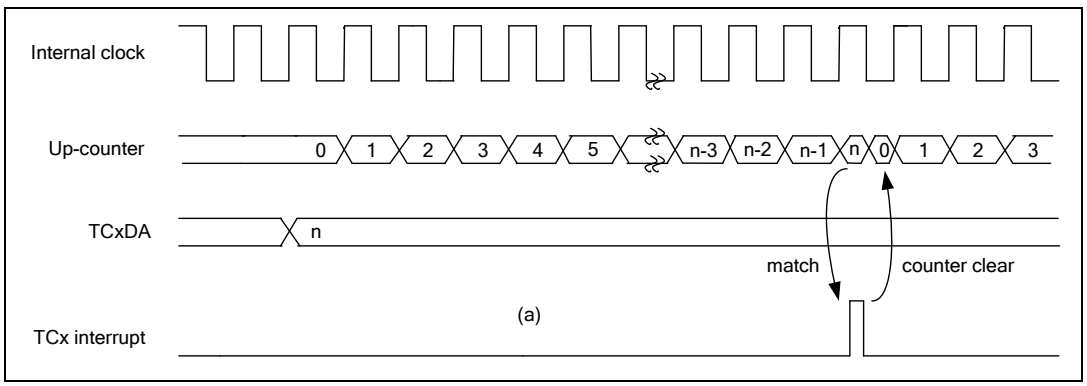


Figure 6-7b Timer/Counter Mode Waveform Using Internal Clock

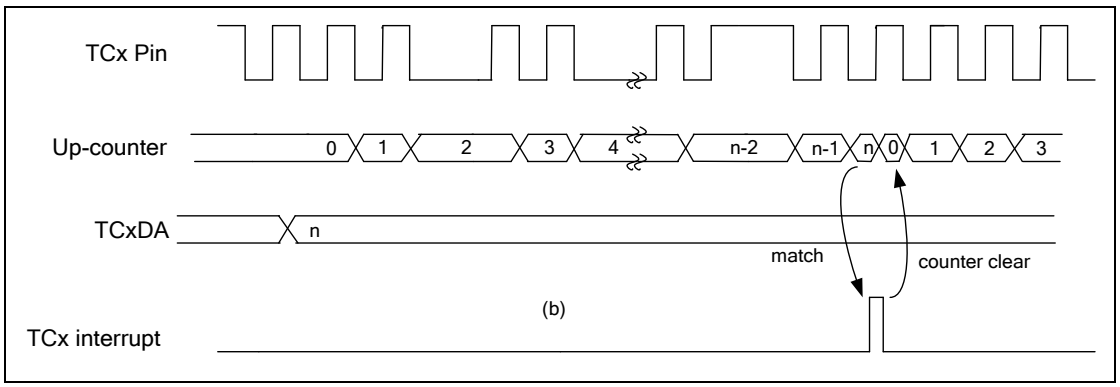


Figure 6-7c Timer/Counter Mode Waveform using External Clock

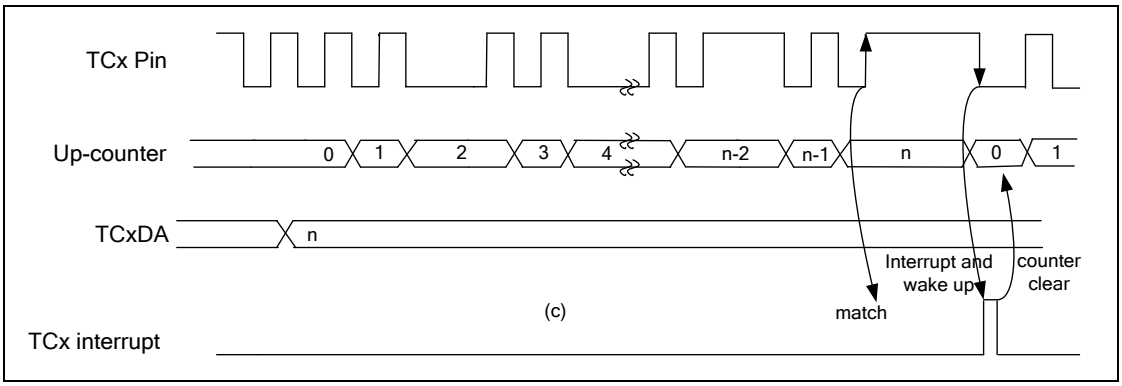


Figure 6-7d Timer/Counter Mode Waveform using External Clock under Sleep Mode

6.6.2 Window Mode

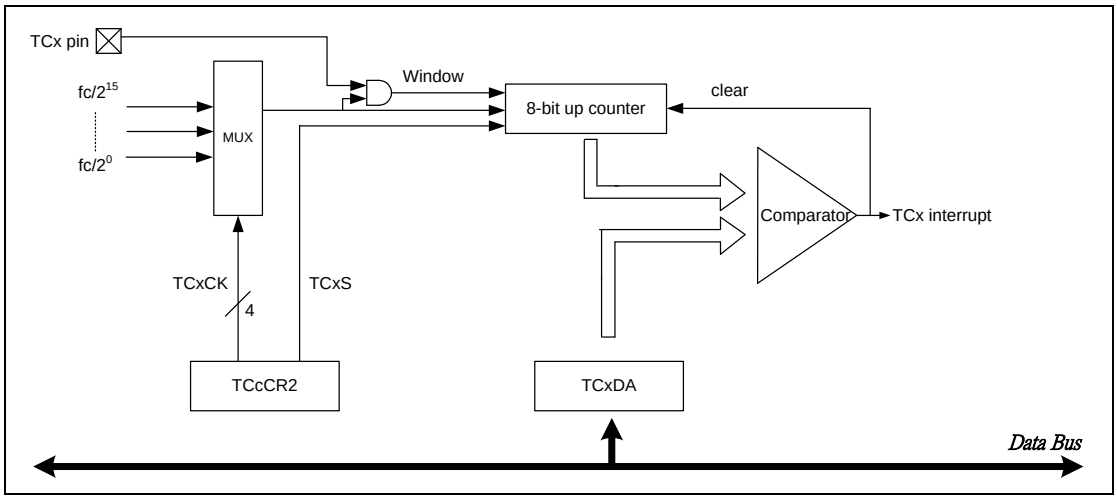


Figure 6-8a Window Mode

In Window mode, counting up is performed on a rising edge of the pulse that is logical AND of an internal clock and the TCx pin (window pulse). When the contents of the up-counter match the TCxDA, interrupt is generated and the counter is cleared. The frequency (window pulse) must be slower than the selected internal clock.

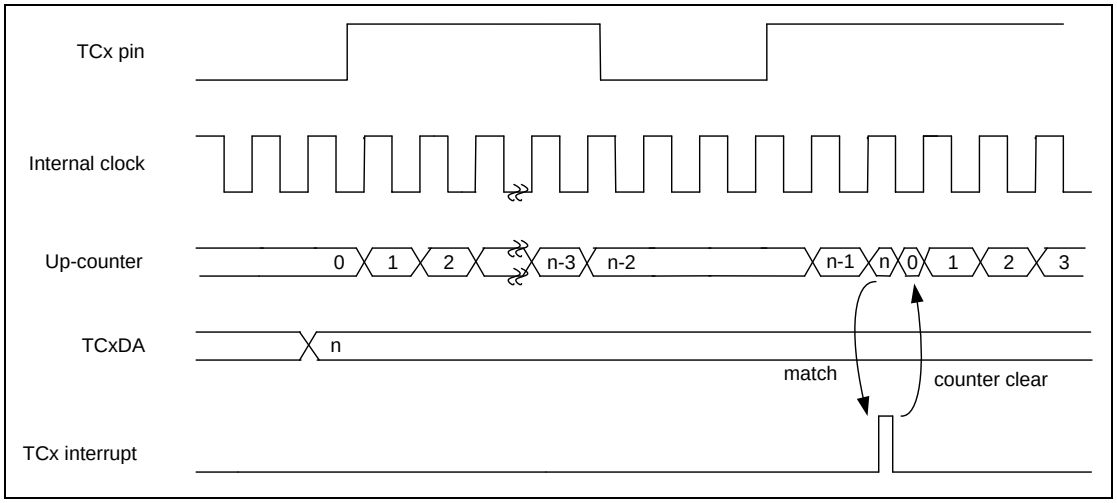


Figure 6-8b Window Mode Waveform

6.6.3 Capture Mode

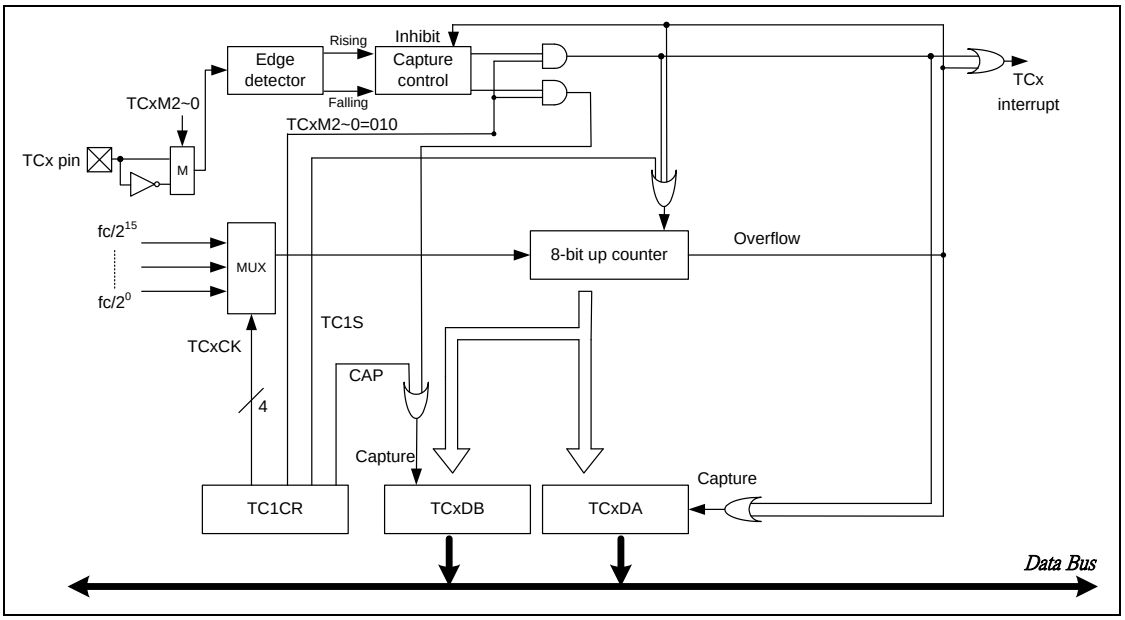


Figure 6-9a Capture Mode

In Capture mode, the pulse width, period, and duty of the TCx input pin are measured in this mode and are used to decode the remote control signal. The counter is free running by the internal clock. On the rising (falling) edge of the TCx pin, the contents of counter is loaded into TCxDA, then the counter is cleared and interrupt is generated. On the falling (rising) edge of the TC1 pin, the contents of counter are loaded into TCxDB while the counter is still counting.

Once the next rising edge of TCx pin is triggered, the contents of the counter are loaded into TCxDA and the counter is cleared. Then interrupt is generated again. If overflow before the edge is detected, the FFH is loaded into TCxDA and the overflow interrupt is generated. During interrupt processing, it can be determined whether or not the TCxDA value is FFH. After an interrupt (capture to TCxDA or overflow detection) is generated, capture and overflow detection are halted until TCxDA is read out.

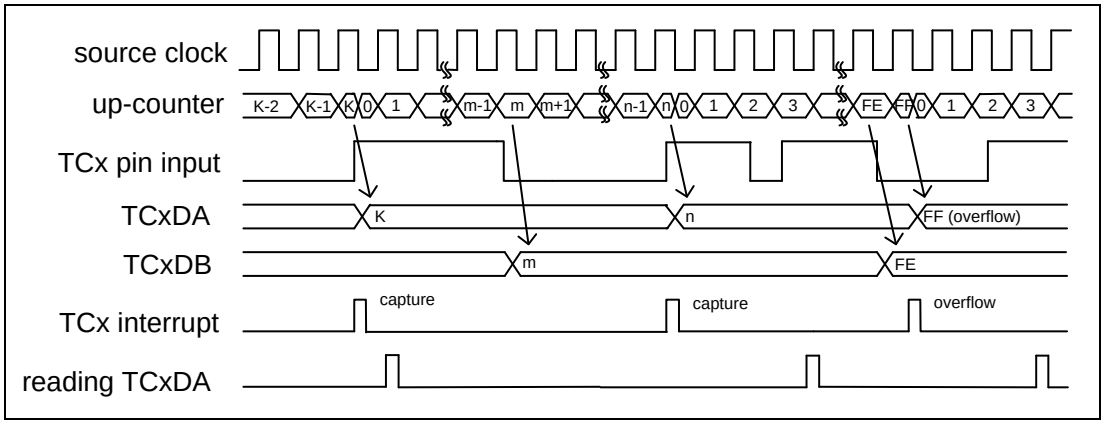


Figure 6-9b Capture Mode Waveform

6.6.4 Programmable Divider Output (PDO) Mode and Pulse Width Modulation (PWM) Mode

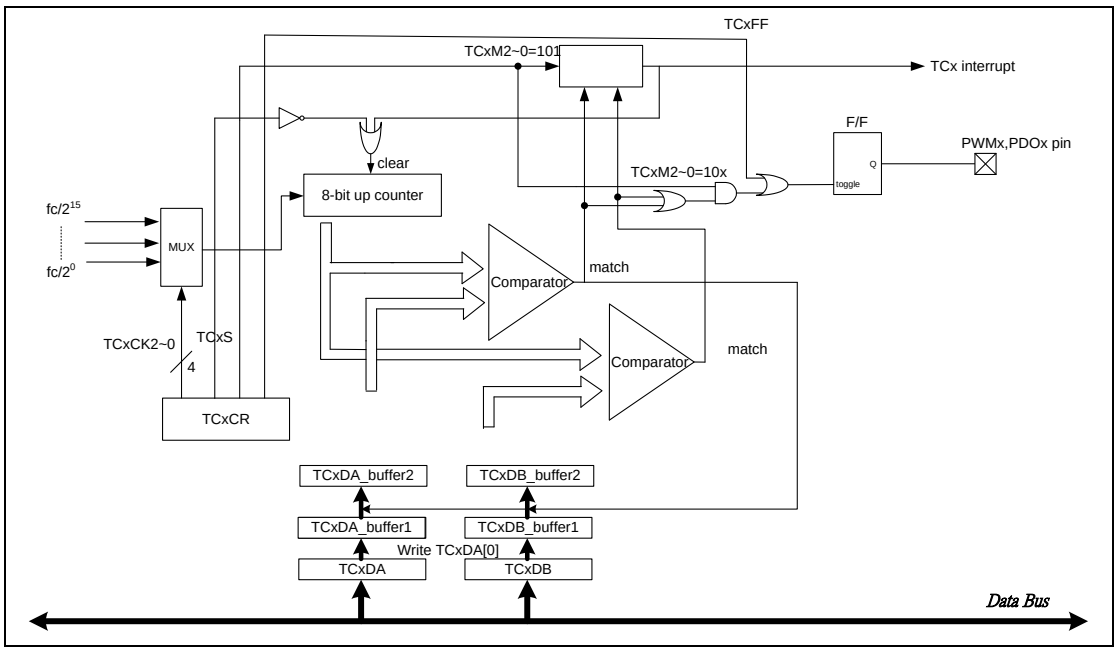


Figure 6-10a PWM/PDO Mode

■ Programmable Divider Output (PDO) Mode

In Programmable Divider Output (PDO) mode, counting up is performed by using the internal clock. The contents of TCxDA are compared with the contents of up-counter. The F/F output is toggled and the counter is cleared each time a match is found. The F/F output is inverted and output to PDO pin. This mode can generate 50% duty pulse output. The PDO pin is initialized to "**0**" during reset. A TCx interrupt is generated each time the PDO output is toggled.

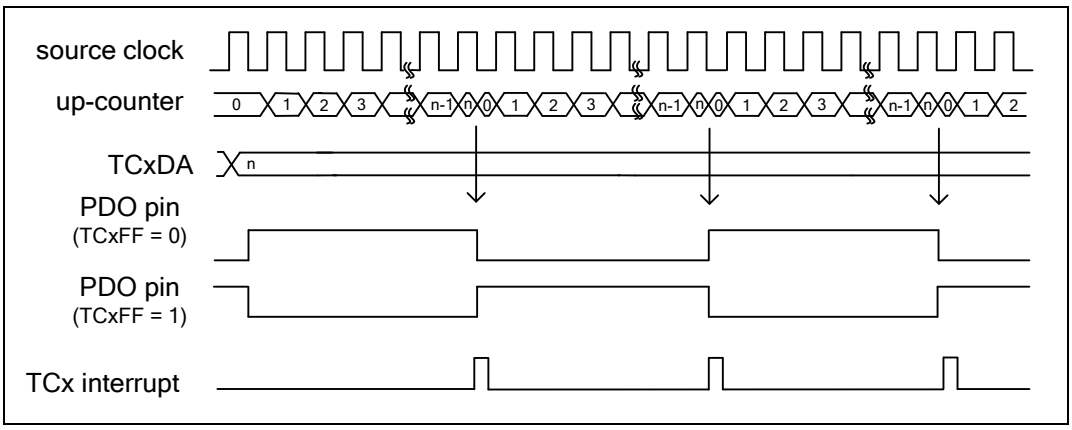


Figure 6-10b PDO Mode Waveform

■ Pulse Width Modulation (PWM) Mode PWM

In Pulse Width Modulation (PWM) Output mode, counting up is performed using the internal clock with prescaler. The Duty of PWMx is controlled by TCxDB, and the Period of PWM1 is controlled by TCxDA. The pulse at the PWMx pin is held to a high level as long as TCxS=1 or Timerx matches TCxDA, while the pulse is held to a low level as long as Timerx matches TCxDB. Once TCxFF is set to "**1**", the signal of PWMx is inverted. A TCx interrupt is generated and defined by TCxS. On the other hand, the TCxDA and TCxDB can be written anytime, but the data of TCxDA and TCxDB are latched only at writing TCxDA[0]. Therefore, the new Duty and new Period of PWM appear at the PMW pin at the last period–match.

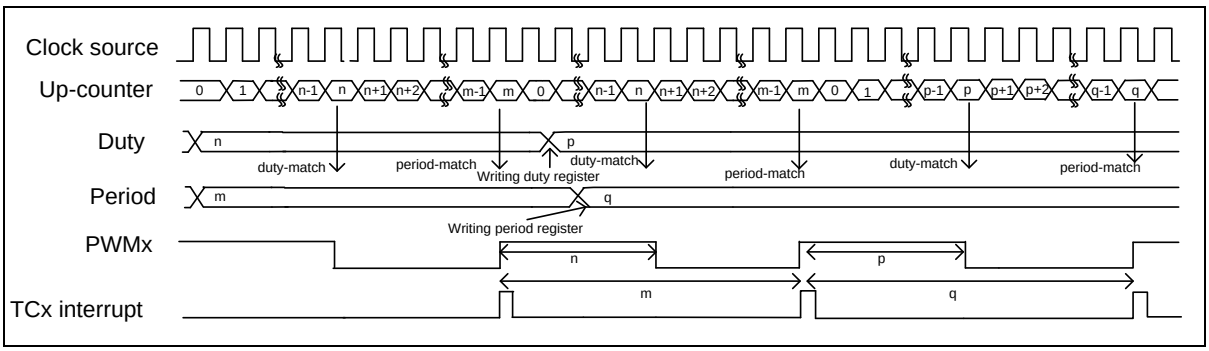


Figure 6-10c PWM Mode Waveform

6.6.5 Buzzer Mode

TCx pin outputs the clock after dividing the frequency.

6.7 LVD (Low Voltage Detector)

Under unstable power source condition, such as external power noise interference or EMS test condition, a violent power vibration could occur. At the same time, the VDD could become unstable as it could be operating below the working voltage. When the system supply voltage (VDD) is below the operating voltage, the IC kernel will automatically keep all register status.

6.7.1 Low Voltage Reset

The detailed LVR operation mode is as follows:

LVR1	LVR0	VDD Reset Level	VDD Release Level
0	0	4.0V*	4.2V
0	1	3.5V**	3.7V
1	0	2.7V***	2.9V
1	1	NA (Power-on Reset)	

* *If VDD < 4.0V and is kept for about 5μs, the IC will be reset.*
** *If VDD < 3.5V and is kept for about 5μs, the IC will be reset.*
*** *If VDD < 2.7V and is kept for about 5μs, the IC will be reset.*

6.7.2 Low Voltage Detect

■ **Registers for LVD Circuit**

R_BANK	Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2 ~ Bit 0
Bank 1	0X49	LVDCR	LVDEN	–	LVDS1	LVDS0	LVDB	–
Bank 0	0X10	WUCR2	–	–	LVDWK	–	–	–
Bank 0	0x1B	IMR1	–	–	LVDIE	–	–	–
Bank 0	0x15	ISR1	–	–	LVDSF	–	–	–

■ **Corresponding Bits for LVD**

LVDEN	LVDS1,LVDS0	LVD Voltage Interrupt Level	LVDB
1	11	VDD < 2.2V	0
		VDD > 2.2V	1
1	10	VDD < 3.3V	0
		VDD > 3.3V	1
1	01	VDD < 4.0V	0
		VDD > 4.0V	1
1	00	VDD < 4.5V	0
		VDD > 4.5V	1
0	XX	NA	1

Follow the steps below to obtain data from the LVD:

1) Write to the two bits (LVDS1 ~ LVDS0) on the Bank1-R49 register to define the LVD level (See Section 6.1.37 for details).
2) Set the LVDWK bit if the wake-up function is implemented.
3) Set the LVDIE bit if the interrupt function is implemented.
4) Write "ENI" instruction if the interrupt function is implemented.
5) Set LVDEN bit to "**1**".
6) Write "SLEP" instruction or poll /LVDB bit.
7) Clear the interrupt flag bit (LVDSF) when Low Voltage is detected.

NOTE

- *When the LVDEN bit is set to enable the LVD module, the current consumption will increase to 10μA.*
- *During the Sleep mode, the LVD module continues to operate. If the device voltage drop slowly and crosses the detect point, the LVDSF bit will be set and the device will wake-up from Sleep mode.*
- *When the system resets, the LVD flag will be cleared.*

Figure below shows the LVD module detection point in an external voltage condition.

- When VDD drops but remains above V_{LVD}, the LVDSF remains at "**0**".
- When VDD drops, but above V_{LVD}, LVDSF remains at "**0**". When VDD drops below V_{LVD}, LVDSF is set to "**1**." If global ENI is enabled, the LVDSF is also set to "**1**", and the next instruction will branch to interrupt vector.
  After the VDD rises above V_{LVD} again, the LVDSF will set to "**1**" again. When the global ENI is enabled, the next instruction will be executed in the interrupt vector. Then the LVD interrupt flag is cleared to "**0**" by software.
- When VDD drops below V_{RESET} in less than 80μs, the system will keep all the registers status, and the system halts but with the oscillation remaining active. When VDD drops below V_{RESET} but in more than 80μs, a system reset occurs (refer to Section 6.1.12 for more details).

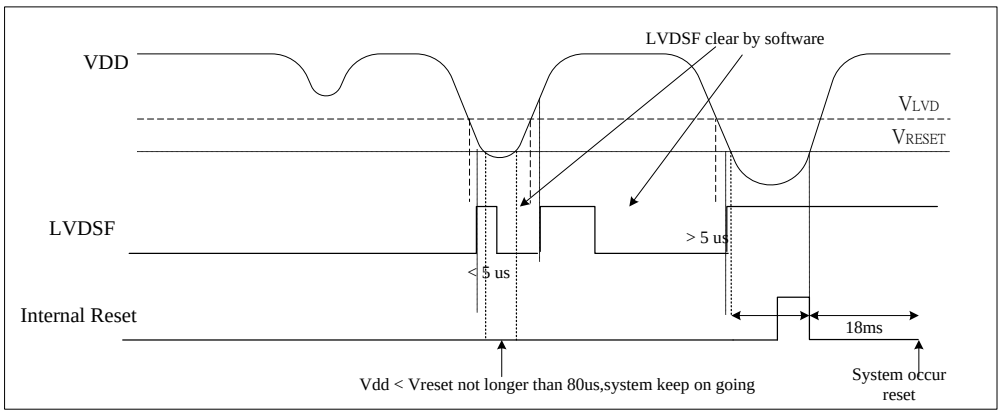


Figure 6-11 LVD Waveform

6.8 Oscillator

6.8.1 Oscillator Modes

The MCU can be operated in five different oscillator modes (Fm), such as**:**

- High XTAL Oscillator Mode 2 (HXT2)
- High XTAL oscillator mode1 (HXT1)
- XTAL oscillator mode (XT)
- Low XTAL oscillator mode (LXT)
- Internal RC oscillator mode (IRC)

You can select one of the above modes by programming the Option pin. There are two types of clock source which is used for Fs. Fs is determined by Fss1 and Fss0 options. The maximum operating frequency of crystal/resonator on the different VDD is listed in the following table.

- **Summary of Maximum Operating Speeds**

Conditions	VDD	Fxt max. (MHz)
Two clocks	1.8	4
	3.0	8
	5.0	20

6.8.2 Crystal Oscillator/Ceramic Resonators (XTAL)

The EM78P224N can be driven by an external clock signal through the OSCI pin as shown in the figure at right.

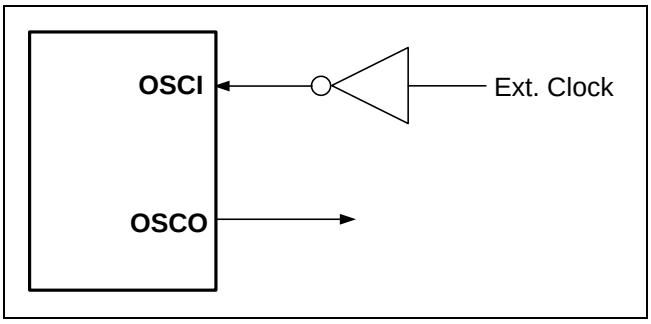


Figure 6-12a External Clock Input Circuit

In most applications, Pin OSCI and Pin OSCO can be connected with a crystal or ceramic resonator to generate oscillation as depicted in the following circuit diagram. The same thing applies to HXT mode or LXT mode.

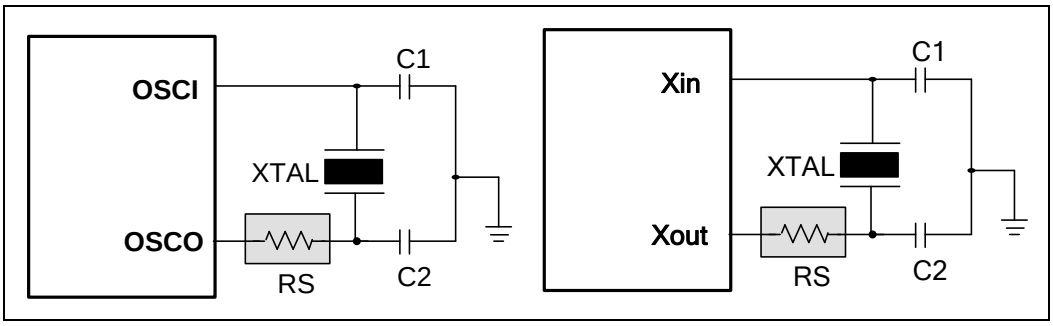


Figure 6-12b Crystal/Resonator Circuits

The table below provides the recommended values of C1 and C2. Since each resonator has its own attributes, user should refer to its specification for appropriate values of C1 and C2. The serial resistor, RS; may be required for AT strip cut crystal or low frequency mode.

■ **Capacitor Selection Guide for Crystal Oscillator or Ceramic Resonator**

Oscillator Source	Oscillator Type		Frequency	C1 (pF)	C2 (pF)
Main Oscillator	Ceramic Resonators		455kHz	30	30
			2.0 MHz	30	30
			4.0 MHz	30	30
	Crystal Oscillator	100K~1 MHz	100kHz	68	68
			200kHz	30	30
			455kHz	30	30
		1M~6 MHz	1.0 MHz	30	30
			2.0 MHz	30	30
			4.0 MHz	30	30
		6M~12 MHz	6.0 MHz	30	30
			8.0 MHz	30	30
			10.0 MHz	30	30
		12M~20 MHz	12.0 MHz	30	30
			16.0 MHz	20	20
			20.0 MHz	15	15

6.8.3 Internal RC Oscillator Mode

The EM78P224N offers a versatile internal RC mode with default frequency value of 4 MHz. Internal RC oscillator mode has other frequencies (16 MHz, 8 MHz, and 1 MHz) that can be set by Code Option: RCM1 and RCM0. All these four main frequencies can be calibrated by programming the Code Option Word 1 Bits C5~C0. Table below shows a typical drift rate of the calibration.

■ **Internal RC Drift Rate (Ta=25°C, VDD=5V ± 5%, VSS=0V)**

Internal RC Frequency	Drift Rate			
	Temperature (-40℃~+85℃)	Voltage (2.3V~5.5V)	Process	Total
1 MHz	±2%	±3%	±2%	±7%
4 MHz	±2%	±3%	±2%	±7%
8 MHz	±2%	±3%	±2%	±7%
16 MHz	±2%	±3%	±2%	±7%

NOTE

These are theoretical values provided for reference only. Actual values may vary depending on the actual process.

6.9 Power-on Considerations

Any microcontroller is not guaranteed to start to operate properly before the power supply stabilizes to a steady state. The EM78P224N is equipped with a built-in Power-on Voltage Detector (POVD) with a detecting level of 2.0V. It will work well if Vdd rises fast enough (50 ms or less). However, under critical applications, extra devices may still be required to assist in solving power-up problems.

6.10 External Power-on Reset Circuit

The circuits shown at the right figure implements an external RC to generate the reset pulse. The pulse width (time constant) should be kept long enough for Vdd to achieve minimum operating voltage. Apply this circuit when the power supply has a slow rising time. Since the current leakage from the /RESET pin is about ±5μA, it is recommended that R should not be greater than 40KΩ in order for the /RESET pin voltage to remain at below 0.2V. The diode (D) acts as a short circuit at the moment of power down. The capacitor (C) will discharge rapidly and fully. The current-limited resistor (Rin), will prevent high current or ESD (electrostatic discharge) from flowing to Pin /RESET.

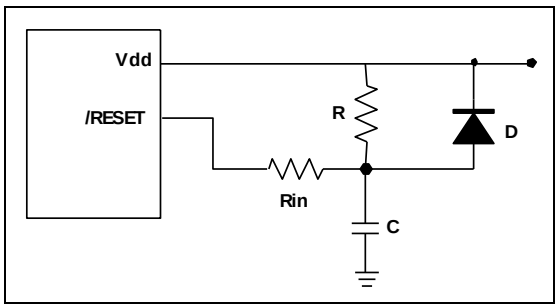


Figure 6-13 External Power-up Reset Circuit

6.11 Residue-Voltage Protection

When battery is replaced, device power (Vdd) is taken off but residue-voltage remains. The residue-voltage may trip below Vdd minimum, but not to zero. This condition may cause a poor power-on reset. Figure 6-14a and Figure 6-14b show how to build a residue-voltage protection circuit.

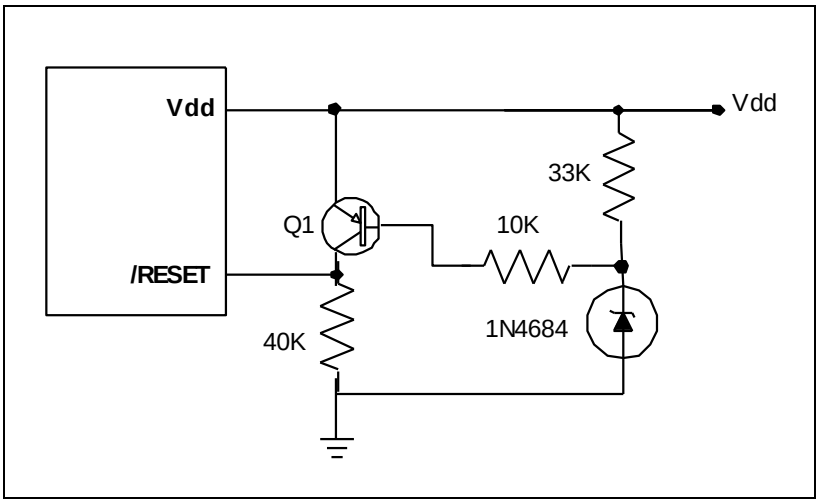


Figure 6-14a Residue Voltage Protection Circuit 1

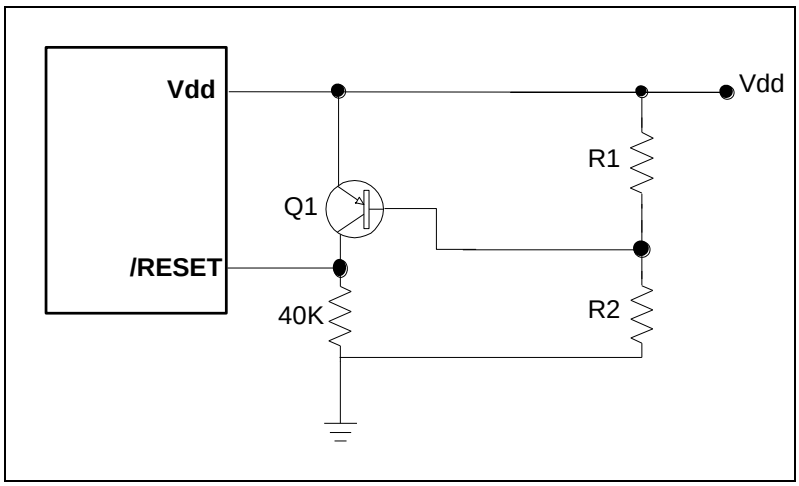


Figure 6-14b Residue Voltage Protection Circuit 2

6.12 Code Option Register

The EM78P224N has a code option Word that is not part of the normal program memory. The option bits cannot be accessed during normal program execution.

Code Option Register and Customer ID Register arrangement distribution:

Word 0	Word 1	Word 2
Bit 12~Bit 0	Bit 12~Bit 0	Bit 12~Bit 0

6.12.1 Code Option Register (Word 0)

Word 0															
Bit	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Mnemonic	**-**	**-**	**-**	**-**	**HLFS**	**-**	**LVR1**	**LVR0**	**RESETEN**	**ENWDT**	**NRHL**	**NRE**	**PR2**	**PR1**	**PR0**
1	-	-	-	-	Normal	-	High	High	P67	Disable	32/fc	Enable	Enable		
0	-	-	-	-	Green	-	Low	Low	/RST	Enable	8/fc	Disable	Disable		
Default	0	1	0	0	1	0	1	1	1	1	1	1	1	1	1

Bit 14: Not used. Set to "**0**" all the time.

Bit 13: Not used. Set to "**1**" all the time.

Bits 12 ~ 11: Not used. Set to "**0**" all the time.

Bit 10 (HLFS): Reset to Normal or Green Mode select bit

0: CPU is selected as Green mode when a reset occurs.

1: CPU is selected as Normal mode when a reset occurs (default).

Bit 9: Not used. Set to "**0**" all the time.

Bits 8 ~ 7 (LVR1 ~ LVR0): LVR Low Voltage Reset Enable bits

LVR1	LVR0	VDD Reset Level	VDD Release Level
0	0	4.0V*	4.2V
0	1	3.5V**	3.7V
1	0	2.7V***	2.9V
1	1	NA (Power-on Reset)	

** If VDD < 4.0V and is kept for about 5μs, the IC will be reset.*
*** If VDD < 3.5V and is kept for about 5μs, the IC will be reset.*
**** If VDD < 2.7V and is kept for about 5μs, the IC will be reset.*

Bit 6 (RESETEN): P67//RST pin selection bit

0: Enable, /RST pin

1: Disable, P67 pin (default)

Bit 5 (ENWDT): WDT enable bit

0: Enable

1: Disable (default)

Bit 4 (NRHL): Noise rejection high/low pulse define bit.

0: pulses equal to 8/fc [s] are regarded as signal

1: pulses equal to 32/fc [s] are regarded as signal (default)

NOTE

Under Low XTAL oscillator (LXT) mode, the noise rejection high/low pulses are always 8/Fm.

Bit 3 (NRE): Noise Rejection Enable bit

0: Disable

1: Enable (default)

> **NOTE**
> *Under Green, Idle, and Sleep modes, the noise rejection circuit is always disabled.*

Bits 2 ~ 0 (Protect): Protect Bit

Protect Bits	Protect
0	Enable
1	Disable (default)

6.12.2 Code Option Register (Word 1)

Word 1															
Bit	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Mnemonic	**-**	**FSS0**	**C5**	**C4**	**C3**	**C2**	**C1**	**C0**	**RCM1**	**RCM0**	**-**	**OSC2**	**OSC1**	**OSC0**	**RCOUT**
1	-	16kHz	-	High	High	High	High	High	High	High	-	High	High	High	High
0	-	32kHz	-	Low	Low	Low	Low	Low	Low	Low	-	Low	Low	Low	Low
Default	1	1	1	1	1	1	1	1	1	1	0	0	1	1	1

Bit 14: Not used. Set to "**0**" all the time.

Bit 13 (FSS0): Sub Frequency Selection

FSS0	
0	Fs is 32kHz, Xin/Xout pin act as I/O
1 (default)	Fs is 16kHz, Xin/Xout pin act as I/O

Bit 12: Not used. Set to "**0**" all the time.

Bits 11 ~ 7 (C4 ~ C0): IRC trim bits

Trimming Code					CLK Period	Frequency
CA[4]	CA[3]	CA[2]	CA[1]	CA[0]		
0	0	0	0	0	Period*(1+32%)	F*(1-24.2%)
0	0	0	0	1	Period*(1+30%)	F*(1-23.1%)
0	0	0	1	0	Period*(1+28%)	F*(1-21.9%)
0	0	0	1	1	Period*(1+26%)	F*(1-20.6%)
0	0	1	0	0	Period*(1+24%)	F*(1-19.4%)
0	0	1	0	1	Period*(1+22%)	F*(1-18%)
0	0	1	1	0	Period*(1+20%)	F*(1-16.7%)
0	0	1	1	1	Period*(1+18%)	F*(1-15.3%)

(Continuation)

Trimming Code					CLK Period	Frequency
CA[4]	CA[3]	CA[2]	CA[1]	CA[0]		
0	1	0	0	0	Period*(1+16%)	F*(1-13.8%)
0	1	0	0	1	Period*(1+14%)	F*(1-12.3%)
0	1	0	1	0	Period*(1+12%)	F*(1-10.7%)
0	1	0	1	1	Period*(1+10%)	F*(1-9.1%)
0	1	1	0	0	Period*(1+8%)	F*(1-7.4%)
0	1	1	0	1	Period*(1+6%)	F*(1-5.7%)
0	1	1	1	0	Period*(1+4%)	F*(1-3.8%)
0	1	1	1	1	Period*(1+2%)	F*(1-2%)
1	1	1	1	1	Period (default)	F (default)
1	1	1	1	0	Period*(1-2%)	F*(1+2%)
1	1	1	0	1	Period*(1-4%)	F*(1+4.2%)
1	1	1	0	0	Period*(1-6%)	F*(1+6.4%)
1	1	0	1	1	Period*(1-8%)	F*(1+8.7%)
1	1	0	1	0	Period*(1-10%)	F*(1+11.1%)
1	1	0	0	1	Period*(1-12%)	F*(1+13.6%)
1	1	0	0	0	Period*(1-14%)	F*(1+16.3%)
1	0	1	1	1	Period*(1-16%)	F*(1+19%)
1	0	1	1	0	Period*(1-18%)	F*(1+22%)
1	0	1	0	1	Period*(1-20%)	F*(1+25%)
1	0	1	0	0	Period*(1-22%)	F*(1+28.2%)
1	0	0	1	1	Period*(1-24%)	F*(1+31.6%)
1	0	0	1	0	Period*(1-26%)	F*(1+35.1%)
1	0	0	0	1	Period*(1-28%)	F*(1+38.9%)
1	0	0	0	0	Period*(1-30%)	F*(1+42.9%)

Bits 6 ~ 5 (RCM1 ~ RCM0): IRC frequency selection bits

RCM1	RCM0	Frequency (MHz)
0	0	1
0	1	8
1	0	16
1	1	4 (default)

Bit 4: Not used. Set to "**0**" all the time.

Bits 3 ~ 1 (OSC2 ~ OSC0): Oscillator modes selection bits

Mode	OSC2	OSC1	OSC0
HXT1(High XTAL1 oscillator mode) Frequency range: 12 ~ 20 MHz	1	1	1
HXT2 (High XTAL2 oscillator mode) Frequency range: 6 ~ 12 MHz	1	1	0
XT (XTAL oscillator mode) Frequency range: 1 ~ 6 MHz	1	0	1
LXT1 (Low XTAL1 oscillator mode) Frequency range: 100kHz ~ 1MHz	1	0	0
IRC(Internal RC oscillator mode); OSCI pin act as I/O(default)	0	1	1
IRC(Internal RC oscillator mode); OSCI pin act RCOUT	0	1	0

Bit 0 (RCOUT): System Clock Output Enable Bit in IRC mode

0: OSCI pin output instruction cycle time with open drain

1: OSCI output instruction cycle time (default)

6.12.3 Code Option Register (Word 2)

Word 2															
Bit	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mnemonic	–	–	–	SC3	SC2	SC1	SC0	–	–	–	–	–	–	–	–
1	–	–	–	High	High	High	High	–	–	–	–	–	–	–	–
0	–	–	–	Low	Low	Low	Low	–	–	–	–	–	–	–	–
Default	0	0	0	1	1	1	1	0	0	1	0	0	0	0	0

Bits 14~12: Not used. Set to "**0**" all the time.

Bits 11 ~ 8 (SC3 ~ SC0): Trim bits of sub-frequency IRC

Trimming Code				Clock Period	Frequency
SC[3]	SC[2]	SC[1]	SC[0]		
0	0	0	0	Period*(1+32%)	F*(1-24.24%)
0	0	0	1	Period*(1+28%)	F*(1-21.88%)
0	0	1	0	Period*(1+24%)	F*(1-19.35%)
0	0	1	1	Period*(1+20%)	F*(1-16.67%)
0	1	0	0	Period*(1+16%)	F*(1-13.79%)
0	1	0	1	Period*(1+12%)	F*(1-10.71%)
0	1	1	0	Period*(1+8%)	F*(1-7.41%)
0	1	1	1	Period*(1+4%)	F*(1-3.85%)

(Continuation)

Trimming Code				Clock Period	Frequency
SC[3]	SC[2]	SC[1]	SC[0]		
1	1	1	1	Period (default)	F (default)
1	1	1	0	Period*(1-4%)	F*(1+4.17%)
1	1	0	1	Period*(1-8%)	F*(1+8.70%)
1	1	0	0	Period*(1-12%)	F*(1+13.64%)
1	0	1	1	Period*(1-16%)	F*(1+19.05%)
1	0	1	0	Period*(1-20%)	F*(1+25.00%)
1	0	0	1	Period*(1-24%)	F*(1+31.58%)
1	0	0	0	Period*(1-28%)	F*(1+38.89%)

Bits 7 ~ 6: Not used. Set to "**0**" all the time.

Bit 5: Not used. Set to "1" all the time.

Bits 4 ~ 0: Not used. Set to "**0**" all the time.

6.12.4 Code Option Register (Word 3)

Word 3															
	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mnemonic	–	–	–	–	–	–	–	–	–	ID5	ID4	ID3	ID2	ID1	ID0
1	–	–	–	–	–	–	–	–	–	Customer ID					
0	–	–	–	–	–	–	–	–	–						
Default	1	1	1	1	1	1	1	1	1						

Bits 14 ~ 6: Not used. Set to "1" all the time.

Bits 5 ~ 0: Customer ID

6.13 Instruction Set

Each instruction in the Instruction Set is a 15-bit word divided into an OP code and one or more operands. Normally, all instructions are executed within one single instruction cycle (one instruction consists of 2 oscillator periods), unless the program counter is changed by instruction "MOV R2,A", "ADD R2,A", or by instructions of arithmetic or logic operation on R2 (e.g., "SUB R2,A", "BS(C) R2,6", "CLR R2", etc.). In this case, the execution takes two instruction cycles.

If for some reasons, the specification of the instruction cycle is not suitable for certain applications, try modifying the conditional skip ("JBS", "JBC", "JZ", "JZA", "DJZ", "DJZA") commands which were tested to be true, to be executed within two instruction cycles. The instructions that are written to the program counter also take two instruction cycles.

Moreover, the Instruction Set also offers the following features**:**

a) Every bit of any register can be set, cleared, or tested directly.

b) The I/O register can be regarded as general register. That is, the same instruction can operate on I/O register.

■ Instruction Set Convention:

R = *Register designator that specifies which one of the registers (including operation and general purpose registers) is to be utilized by the instruction.*

b = *Bit field designator that selects the value for the bit located in the Register R and which affects the operation.*

k = *An 8 or 12-bit constant or literal value*

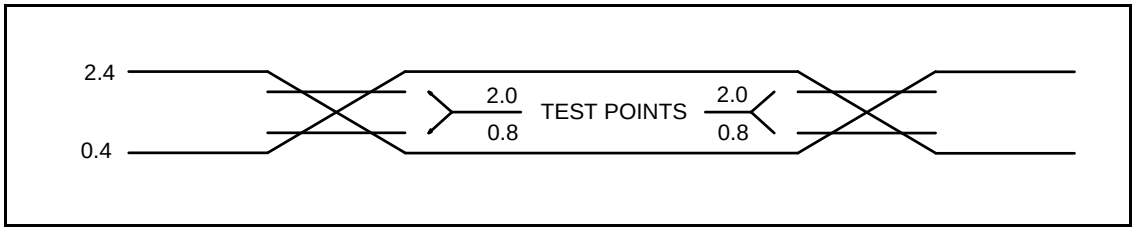
Mnemonic	Operation	Status Affected
NOP	No Operation	None
DAA	Decimal Adjust A	C
SLEP	0 → WDT, Stop oscillator	T, P
WDTC	0 → WDT	T, P
ENI	Enable Interrupt	None
DISI	Disable Interrupt	None
RET	[Top of Stack] → PC	None
RETI	[Top of Stack] → PC, Enable Interrupt	None
MOV R,A	A → R	None
CLRA	0 → A	Z
CLR R	0 → R	Z
SUB A,R	R-A → A	Z, C, DC
SUB R,A	R-A → R	Z, C, DC
DECA R	R-1 → A	Z
DEC R	R-1 → R	Z
OR A,R	A ∨ R → A	Z
OR R,A	A ∨ R → R	Z
AND A,R	A & R → A	Z
AND R,A	A & R → R	Z
XOR A,R	A ⊕ R → A	Z
XOR R,A	A ⊕ R → R	Z
ADD A,R	A + R → A	Z, C, DC
ADD R,A	A + R → R	Z, C, DC
MOV A,R	R → A	Z

(Continuation)

Mnemonic	Operation	Status Affected
MOV R,R	R → R	Z
COMA R	/R → A	Z
COM R	/R → R	Z
INCA R	R+1 → A	Z
INC R	R+1 → R	Z
DJZA R	R-1 → A, skip if zero	None
DJZ R	R-1 → R, skip if zero	None
RRCA R	R(n) → A(n-1), R(0) → C, C → A(7)	C
RRC R	R(n) → R(n-1), R(0) → C, C → R(7)	C
RLCA R	R(n) → A(n+1), R(7) → C, C → A(0)	C
RLC R	R(n) → R(n+1), R(7) → C, C → R(0)	C
SWAPA R	R(0-3) → A(4-7), R(4-7) → A(0-3)	None
SWAP R	R(0-3) ↔ R(4-7)	None
JZA R	R+1 → A, skip if zero	None
JZ R	R+1 → R, skip if zero	None
BC R,b	0 → R(b)	None
BS R,b	1 → R(b)	None
JBC R,b	if R(b)=0, skip	None
JBS R,b	if R(b)=1, skip	None
CALL k	PC+1 → [SP], (Page, k) → PC	None
JMP k	(Page, k) → PC	None
MOV A,k	k → A	None
OR A,k	A ∨ k → A	Z
AND A,k	A & k → A	Z
XOR A,k	A ⊕ k → A	Z
RETL k	k → A, [Top of Stack] → PC	None
SUB A,k	k-A → A	Z,C,DC
ADD A,k	k+A → A	Z,C,DC
SBANK k	K->R1(4)	None
GBANK k	K->R1(0)	None
LCALL k	Next instruction: k kkkk kkkk kkkk PC+1→[SP], k→PC	None
LJMP k	Next instruction: k kkkk kkkk kkkk K→PC	None
TBRD R	ROM[(TABPTR)] → R	None

7 Timing Diagrams

AC Test Input/Output Waveform



Note: *AC Testing: Input are driven at 2.4V for logic "**1**," and 0.4V for logic "**0**"*
*Timing measurements are made at 2.0V for logic "**1**," and 0.8V for logic "**0**"*

Figure 7-1 AC Test Input/Output Waveform Timing Diagram

Reset Timing (CLK = "0")

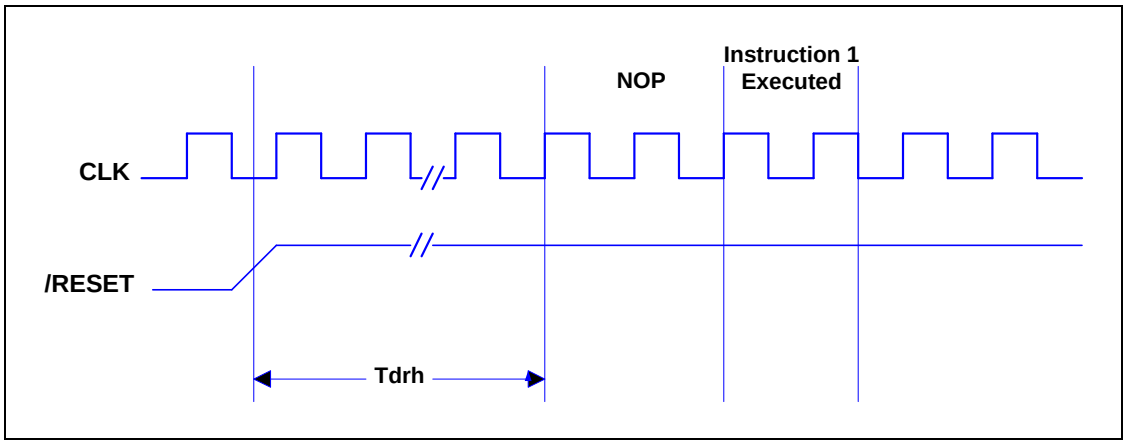


Figure 7-2 Reset Timing Diagram

TCC Input Timing (CLKS = "0")

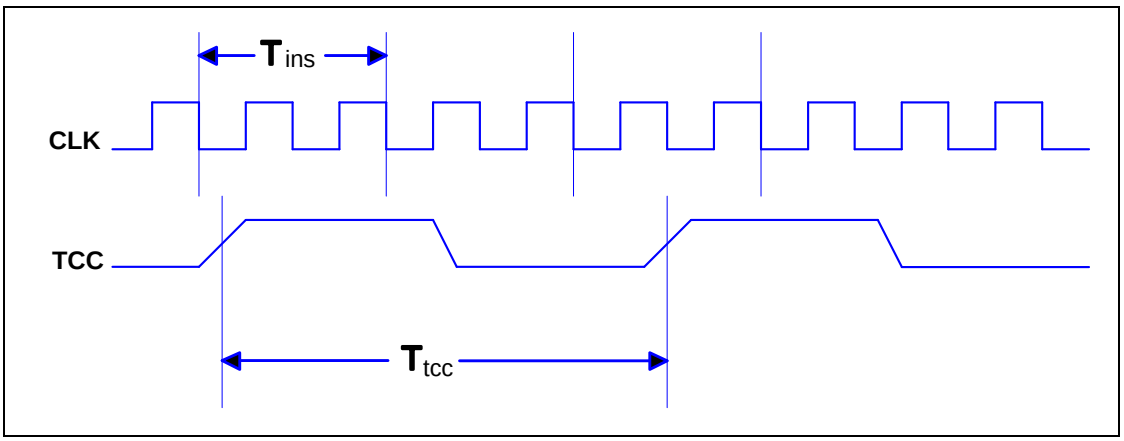


Figure 7-3 TCC Input Timing Diagram

8 Absolute Maximum Ratings

Items	Rating		
Temperature under bias	-40°C	to	85°C
Storage temperature	-65°C	to	150°C
Input voltage	Vss-0.3V	to	Vdd+0.5V
Output voltage	Vss-0.3V	to	Vdd+0.5V
Working Voltage	2.3V	to	5.5V
Working Frequency	DC	to	20 MHz

Note: *These parameters are theoretical values only and have not been tested nor verified.*

9 DC Electrical Characteristics

■ **Ta=25°C, VDD = 5.0V ± 5%, VSS = 0V**

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Fxt	XTAL: VDD to 3V	Two cycles with two clocks	DC	10(-)	14(8)	MHz
	XTAL: VDD to 5V		DC	20(-)	24(20)	MHz
	IRC: VDD to 5V	4 MHz, 1 MHz, 8kHz, 16 MHz	–	F	–	Hz
IIL	Input Leakage Current for input pins	VIN = VDD, VSS	-1	0	1	μA
IRCE	Internal RC oscillator error per stage	–	–	±1	–	%
IRC1	IRC: VDD to 5V	RCM0:RCM1=1:1	–	4	–	MHz
IRC2	IRC: VDD to 5V	RCM0:RCM1=1:0	–	8	–	MHz
IRC3	IRC: VDD to 5V	RCM0:RCM1=0:1	–	16	–	MHz
IRC4	IRC: VDD to 5V	RCM0:RCM1=0:0	–	1	–	MHz
IIL	Input Leakage Current for input pins	VIN = VDD, VSS	-1	0	1	μA
VIH1	Input High Voltage (Schmitt trigger)	Ports 5, 6, 7, 8	0.7Vdd	–	Vdd+0.3V	V
VIL1	Input Low Voltage (Schmitt trigger)	Ports 5, 6, 7, 8	-0.3V	–	0.3Vdd	V
VIHT1	Input High Threshold Voltage (Schmitt trigger)	/RESET	0.7Vdd	–	Vdd+0.3V	V
VILT1	Input Low Threshold Voltage (Schmitt trigger)	/RESET	-0.3V	–	0.3Vdd	V
VIHT2	Input High Threshold Voltage (Schmitt trigger)	TCC, INT	0.7Vdd	–	Vdd+0.3V	V
VILT2	Input Low Threshold Voltage (Schmitt trigger)	TCC, INT	-0.3V	–	0.3Vdd	V
VIHX1	Clock Input High Voltage	OSCI in crystal mode	2.9	3.0	3.1	V
VILX1	Clock Input Low Voltage	OSCI in crystal mode	1.7	1.8	1.9	V
IOH1	Output High Voltage (Ports 5, 6, 7, 8)	VOH = VDD-0.1VDD	–	-4	–	mA
IOH2	Output High Voltage (high drvie) (Ports 6, 7, 8)	VOH = VDD-0.1VDD	–	-7.5	–	mA

(Continuation)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
IOL1	Output Low Voltage (Ports 5, 6, 7, 8)	VOL = GND+0.1VDD	–	14	–	mA
IOL2	Output Low Voltage (high sink) (Ports 6, 7, 8)	VOL = GND+0.1VDD	–	30	–	mA
LVR1	Low voltage reset level	Ta= 25°C	2.41	2.7	2.99	V
		Ta= -40~85°C	2.14	2.7	3.25	V
LVR2	Low voltage reset level	Ta= 25°C	3.1	3.5	3.92	V
		Ta= -40~85°C	2.73	3.5	4.25	V
LVR3	Low voltage reset level	Ta= 25°C	3.56	4.0	4.43	V
		Ta= -40~85°C	3.16	4.0	4.81	V
IPH	Pull-high current	Pull-high active, input pin at VSS	–	-75	–	µA
IPL	Pull-low current	Pull-low active, input pin at Vdd	–	40	–	µA
ISB1	Power down current (Sleep mode)	/RESET= 'High', Fm and Fs off All input and I/O pins at VDD, Output pin floating, WDT disabled	–	1.0	–	µA
ISB2	Power down current (Sleep mode)	/RESET= 'High', Fm and Fs off All input and I/O pins at VDD, Output pin floating, WDT enabled	–	9	–	µA
ISB3	Power down current (Idle mode)	/RESET= 'High', Fm off, Fs=32kHz (IRC type), output pin floating, WDT enabled,	–	9	–	µA
ICC1	Operating supply current (Green mode)	/RESET= 'High', Fm off, Fs=16kHz (IRC type), output pin floating, WDT enabled	–	19	–	µA
ICC2	Operating supply current (Green mode)	/RESET= 'High', Fm off, Fs=32KHz (IRC type), output pin floating, WDT enabled	–	25	–	µA
ICC3	Operating supply current (Normal mode)	/RESET= 'High', Fm = 4 MHz (Crystal type), Fs on, output pin floating, WDT enabled	–	1.2	–	mA
ICC4	Operating supply current (Normal mode)	/RESET= 'High', Fm= 4 MHz (IRC type), Fs on, output pin floating, WDT enabled	–	1.1	–	mA
ICC5	Operating supply current (Normal mode)	/RESET= 'High', Fm=10 MHz (Crystal type), Fs on, Output pin floating, WDT enabled	–	2.2	–	mA
ICC6	Operating supply current (Normal mode)	/RESET= 'High', Fm=16 MHz (IRC type), Fs on, output pin floating, WDT enabled	–	3.2	–	mA
ICC7	Operating supply current (Normal mode)	/RESET= 'High', Fm=16 MHz (Crystal type), Fs on, Output pin floating, WDT enabled	–	3.5	–	mA

NOTE

- *The above parameters are theoretical values only and have not been tested nor verified.*
- *Data under the "Min.", "Typ.", and "Max." columns are based on theoretical results at 25°C. These data are for design reference only and were not tested or verified.*

■ **Internal RC Electrical Characteristics (T_A = 25°C, V_{DD} = 5V, V_{SS} = 0V)**

Internal RC Selected Band	Drift Rate				
	Temperature	Operating Voltage	Min.	Typ.	Max.
4 MHz	25°C	5V	3.92 MHz	4 MHz	4.08 MHz
16 MHz	25°C	5V	15.68 MHz	16 MHz	16.32 MHz
8 MHz	25°C	5V	7.84 MHz	8 MHz	8.16 MHz
1 MHz	25°C	5V	0.98 MHz	1 MHz	1.02 MHz

■ **Internal RC Electrical Characteristics (Process, Voltage, and Temperature Deviation)**

Internal RC Selected Band	Drift Rate (Process & Operating Voltage and Temperature Variation)				
	Temperature	Operating Voltage	Min.	Typ.	Max.
4 MHz	-40 ~ 85°C	2.1V ~ 5.5V	3.76 MHz	4 MHz	4.24 MHz
16 MHz	-40 ~ 85°C	4.0V ~ 5.5V	15.36 MHz	16 MHz	16.64 MHz
8 MHz	-40 ~ 85°C	3.0V ~ 5.5V	7.60 MHz	8 MHz	8.40 MHz
1 MHz	-40 ~ 85°C	2.1V ~ 5.5V	0.94 MHz	1 MHz	1.06 MHz

10 AC Electrical Characteristics

■ **Ta =25°C, VDD=5V, VSS=0V**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Dclk	Input CLK duty cycle	–	45	50	55	%
Tins	Instruction cycle time	Crystal type	100	–	DC	ns
		IRC type	125	–	DC	ns
Tpor	Delay time after Power-On-Reset release	FSS0=1 (16kHz)	–	16+/-3% *	–	ms
Trstrl	Delay time after /Reset,WDT,and LVR release	Crystal type, HLFS=1	–	WSTO**+510/ Fm	–	μs
		IRC type HLFS=1	–	WSTO+8/Fm	–	μs
		HLFS=0	–	WSTO+8/Fs	–	μs
Trsth1	Hold time after /RESET pin reset	–	–	1	–	μs
Trsth2	Hold time after LVR occurred	–	–	1	–	μs
Twdt	Watchdog timer time-out	FSS0=1 (16kHz)	–	16+/-3% *	–	ms
		FSS0=0 (32kHz)	–	8+/-3%	–	ms
Tset	Input pin setup time	–	–	0	–	ns
Thold	Input pin hold time	–	15	20	25	ns
Tdelay	Output pin delay time	Cload=20pF Rload=1MΩ	–	20	–	ns

* ***Tpor and Twdt:*** *are16± 10% ms at FSS0=1(16kHz), Ta=-40°~85°C, and VDD=2.1~5.5V*

** **WSTO:** *Waiting time of Start-to-Oscillation*

NOTE

- *The above parameters are theoretical values only and have not been tested or verified.*
- *Data under the "Min.", "Typ.", and "Max." columns are based on theoretical results at 25°C. These data are for design reference only and were not tested or verified.*

11 Device Characteristics

The graphs provided in the following pages were derived based on a limited number of samples and are shown here for reference only. The device characteristics illustrated herein are not guaranteed for its accuracy. In some graphs, the data maybe out of the warranted operating range.

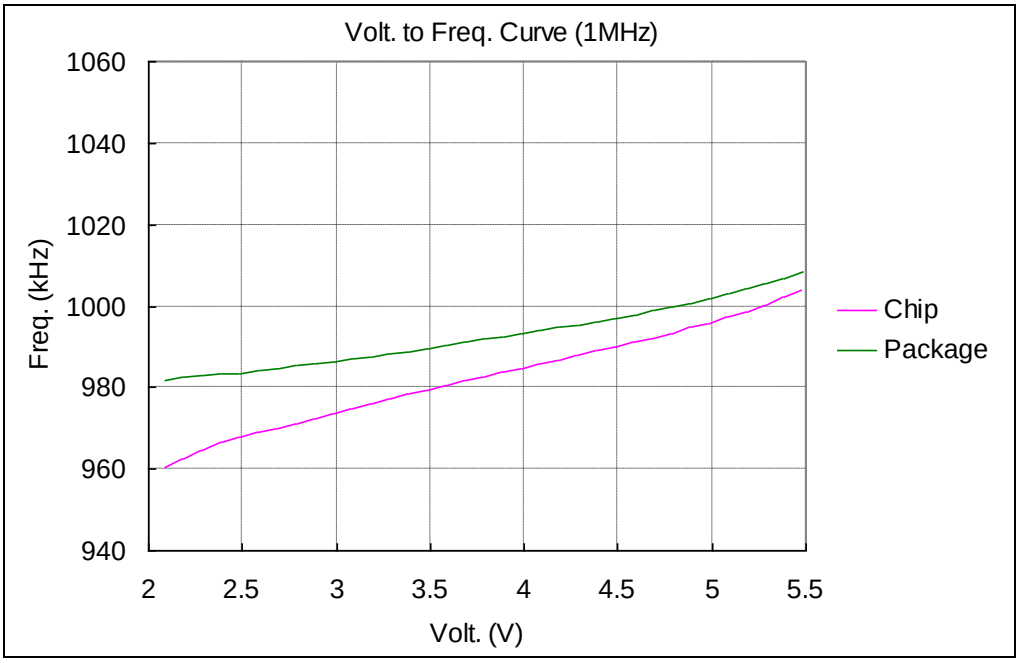


Figure 11-1a Voltage vs. Frequency Curve (1MHz)

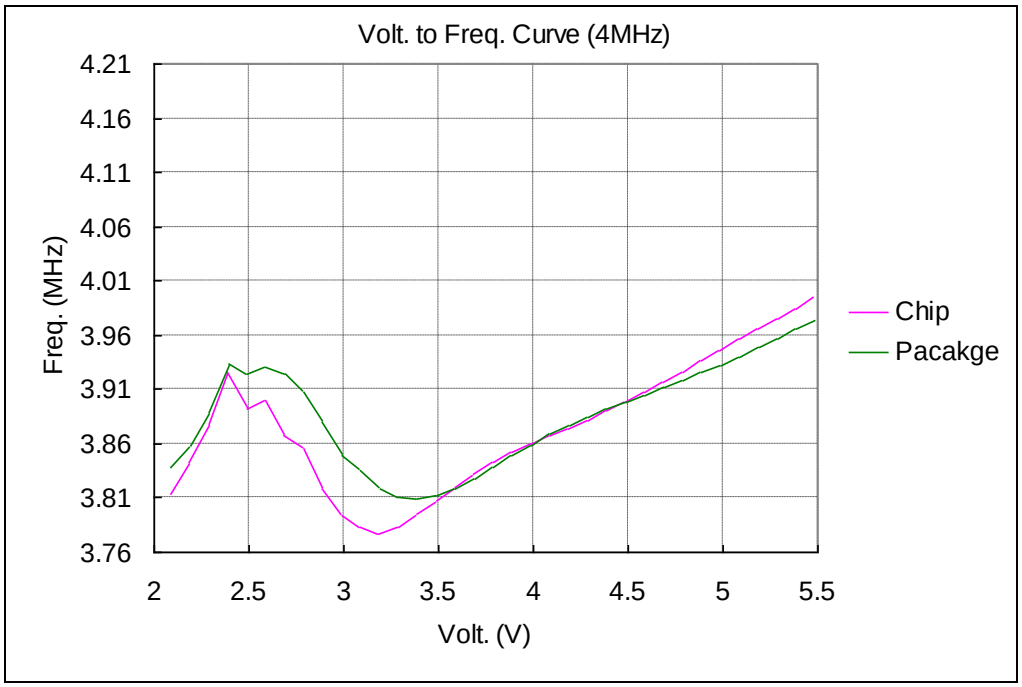


Figure 11-1b Voltage vs. Frequency Curve (4MHz)

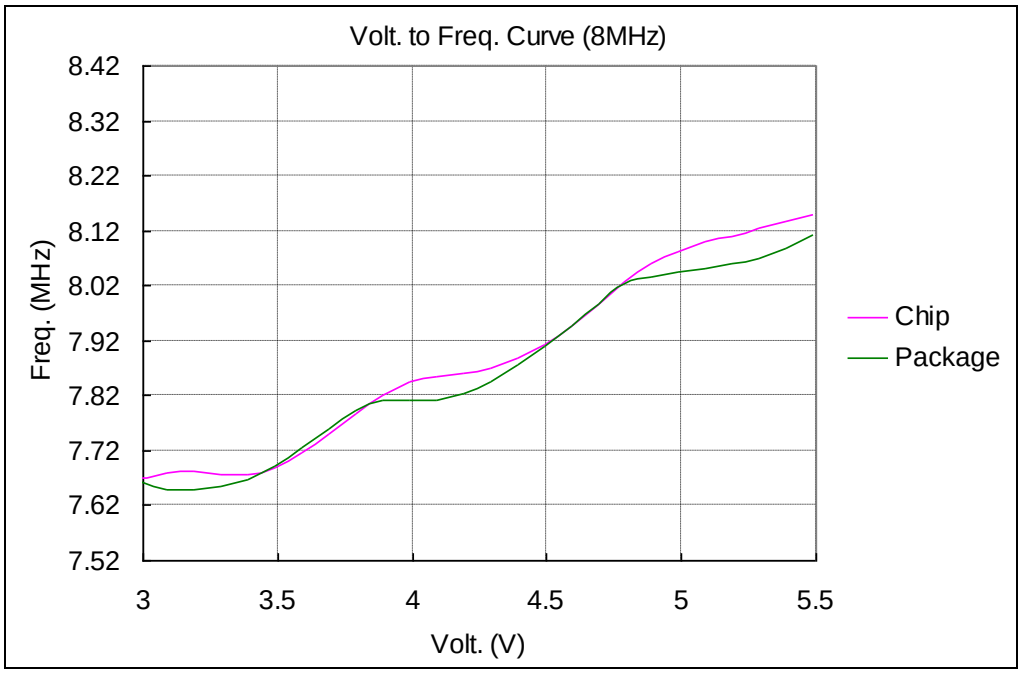


Figure 11-1c Voltage vs. Frequency Curve (8 MHz)

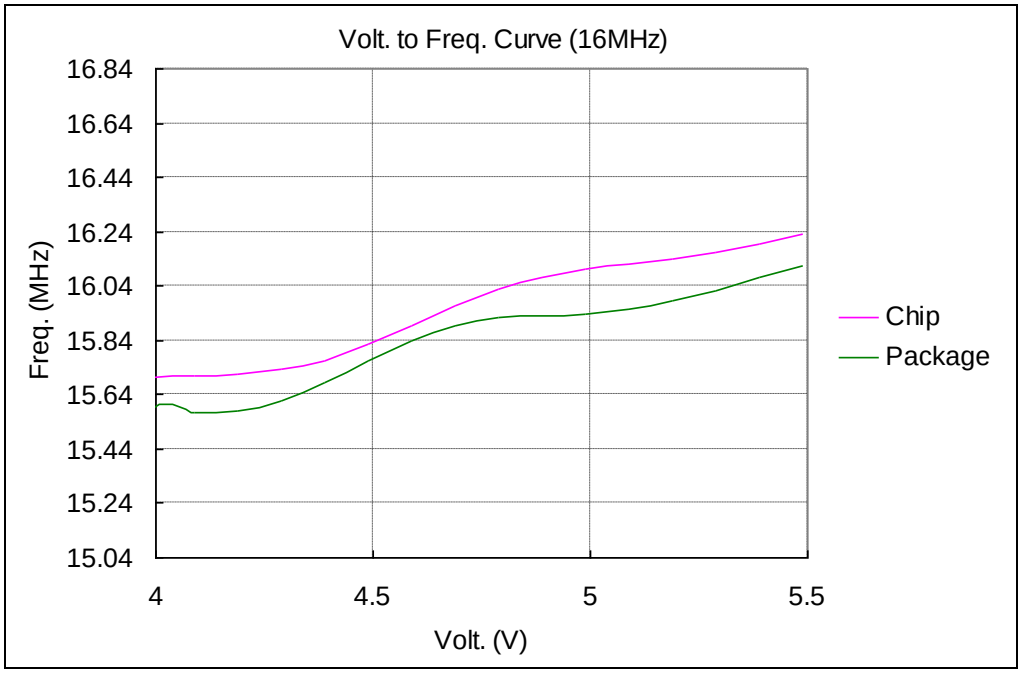


Figure 11-1d Voltage vs. Frequency Curve (16 MHz)

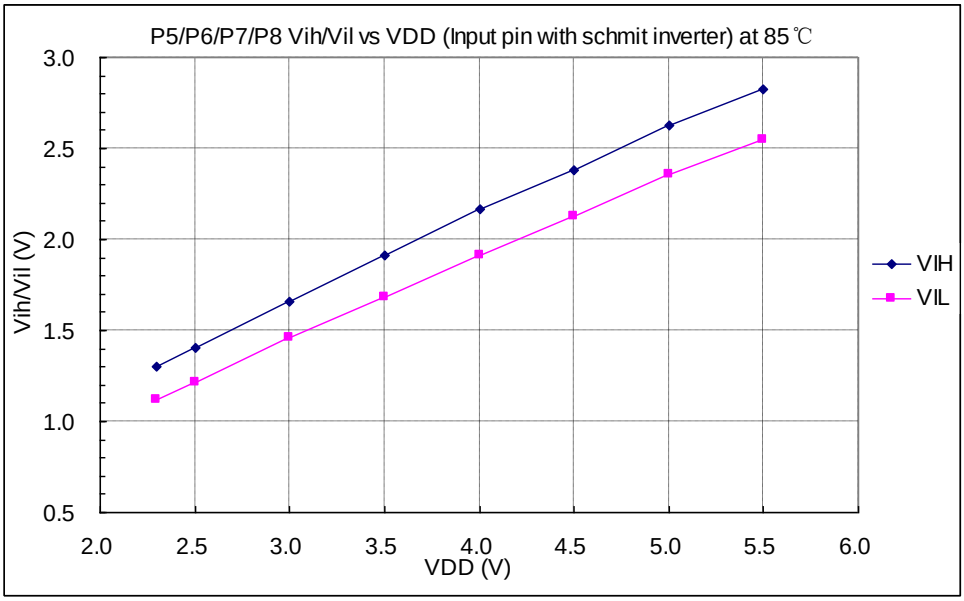


Figure 11-2 VIH/VIL vs. VDD (85°C)

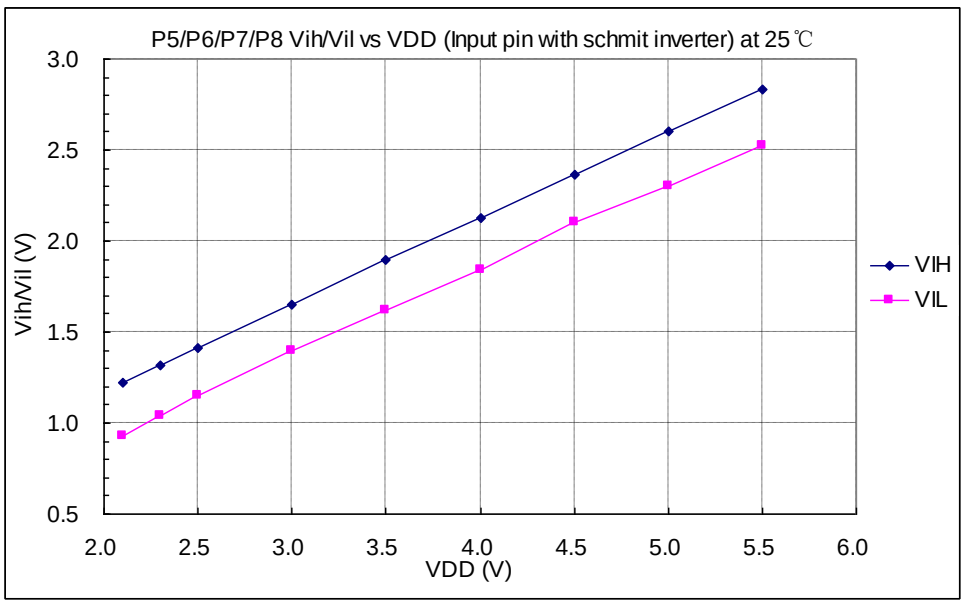


Figure 11-3 VIH/VIL vs. VDD (25°C)

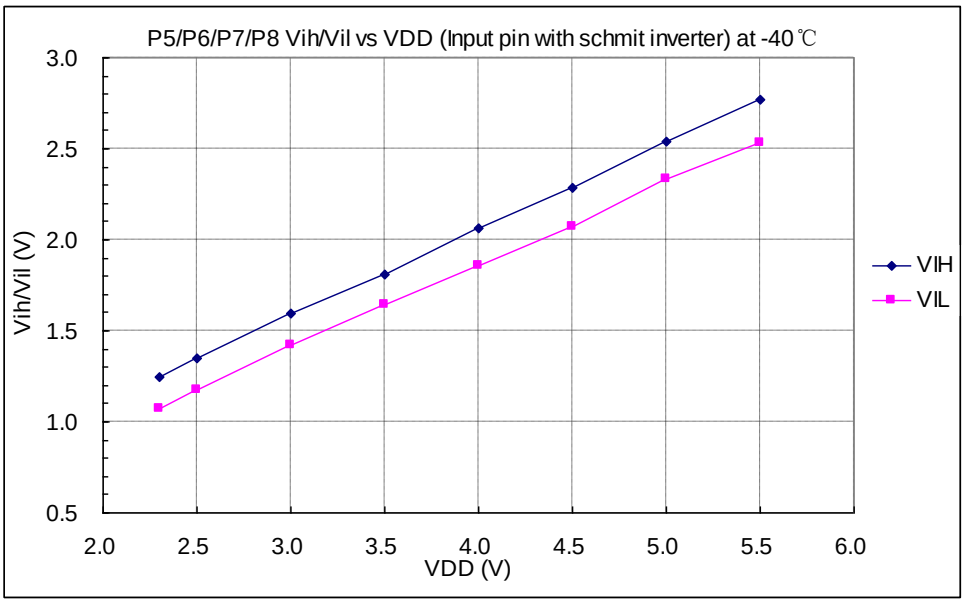


Figure 11-4 VIH/VIL vs. VDD (-40°C)

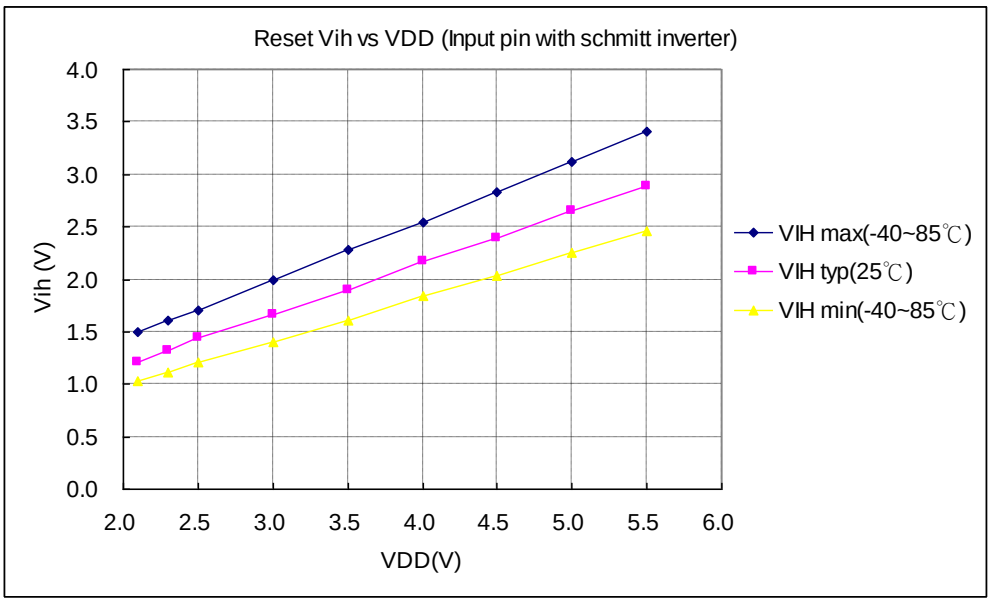


Figure 11-5 VIH of RESET Pin vs. VDD

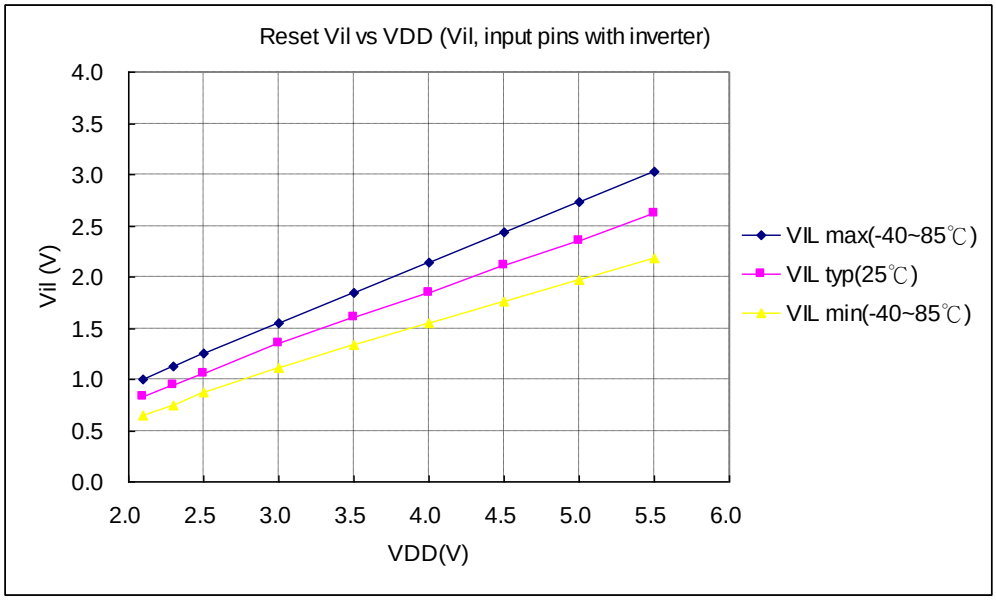


Figure 11-6 VIL of RESET Pin vs. VDD

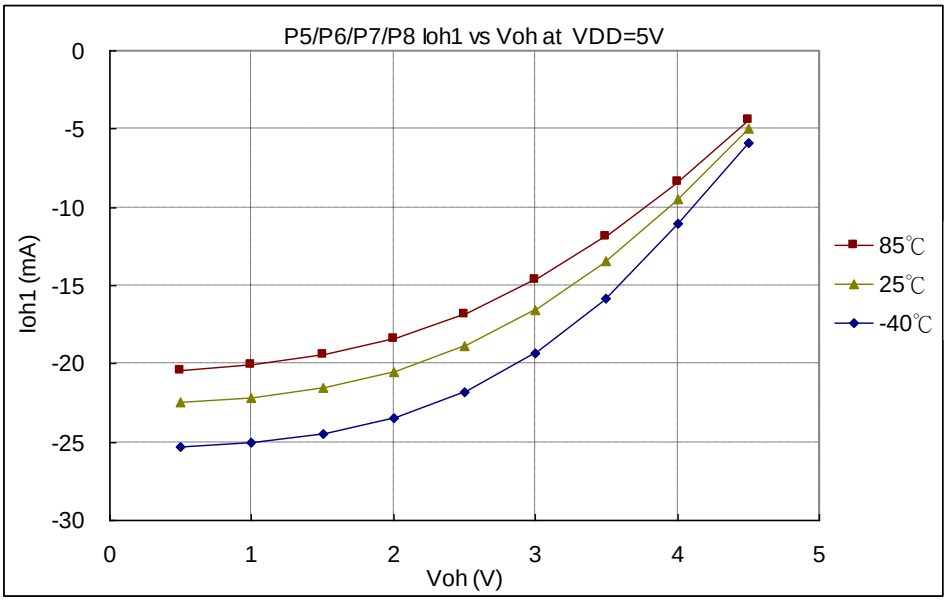


Figure 11-7 VOH vs. IOH1, VDD=5V

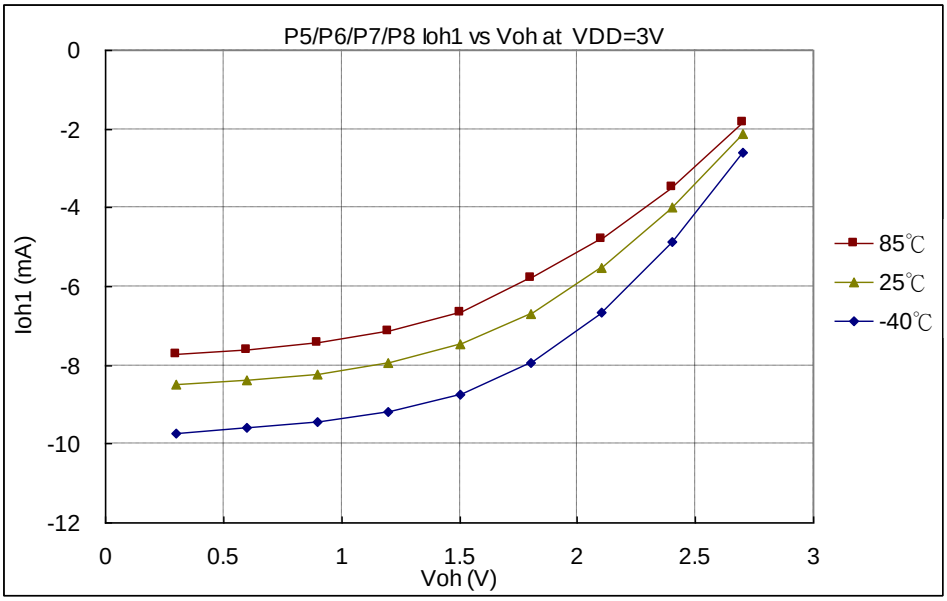


Figure 11-8 VOH vs. IOH1, VDD=3V

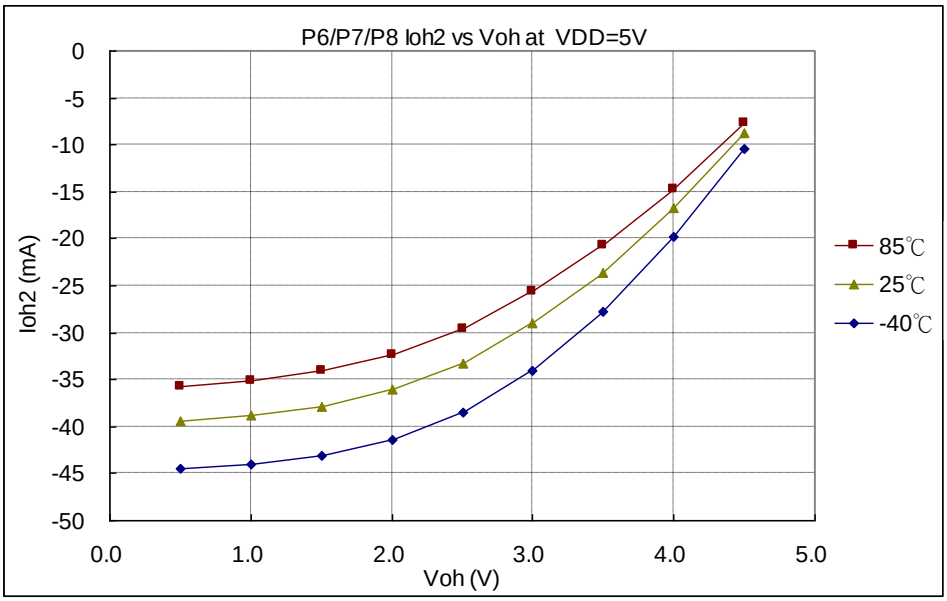


Figure 11-9 VOH vs. IOH2, VDD=5V

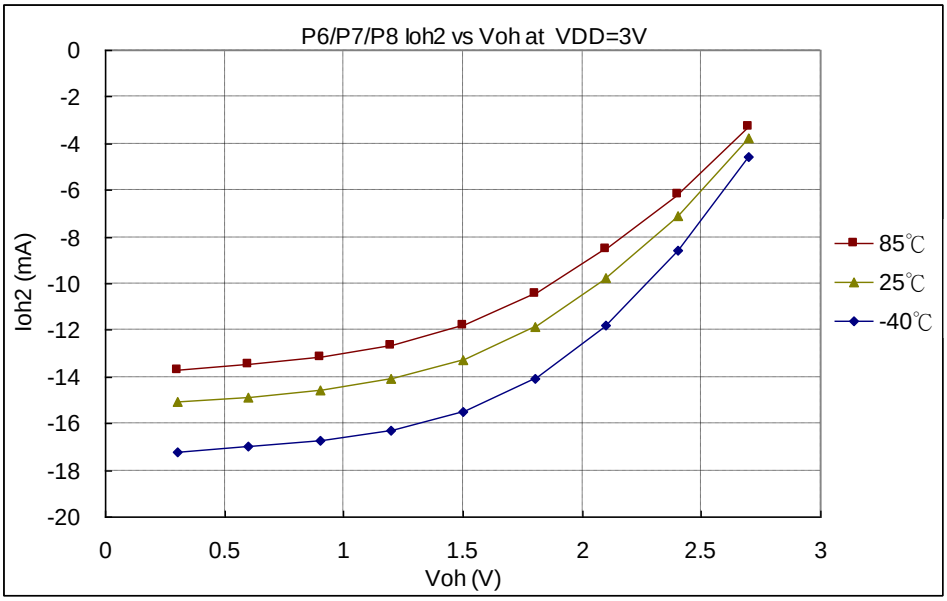


Figure 11-10 VOH vs. IOH2, VDD=3V

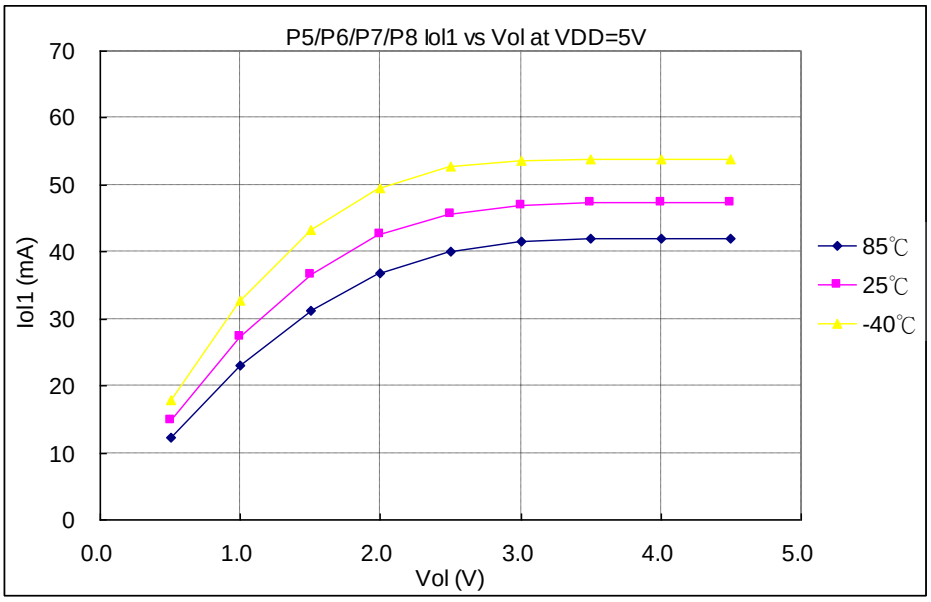


Figure 11-11 VOL vs. IOL1, VDD=5V

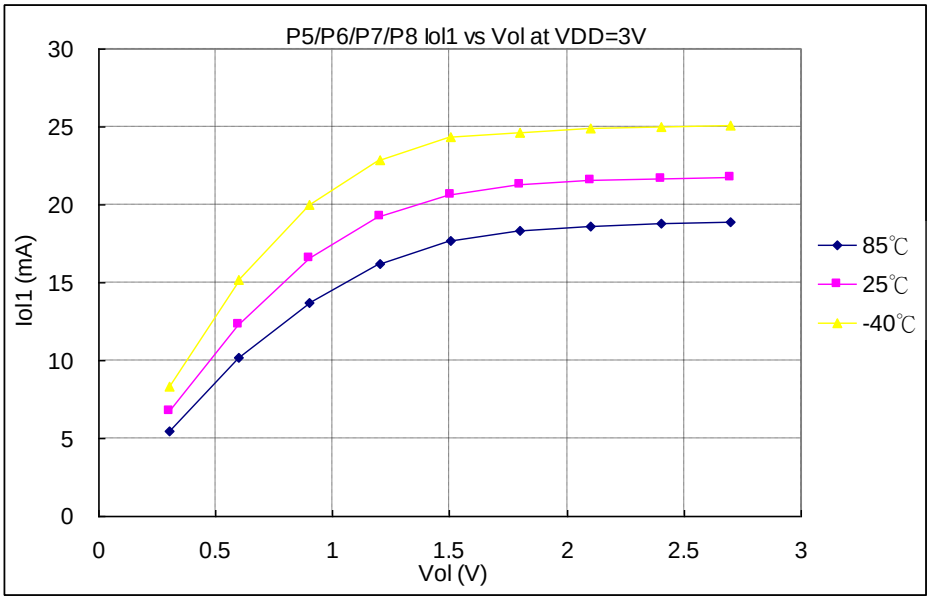


Figure 11-12 VOL vs. IOL1, VDD=3V

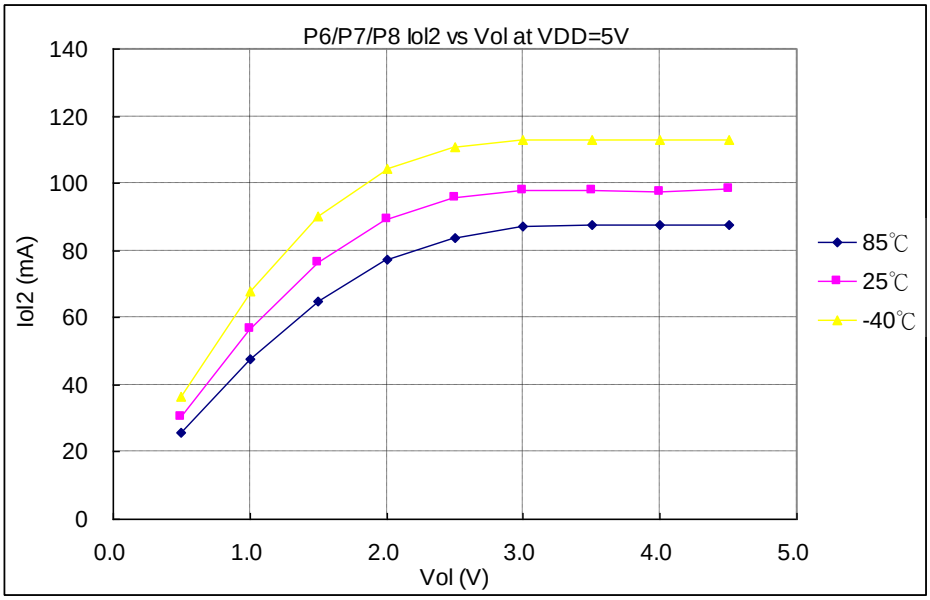


Figure 11-13 VOL vs. IOL2, VDD=5V

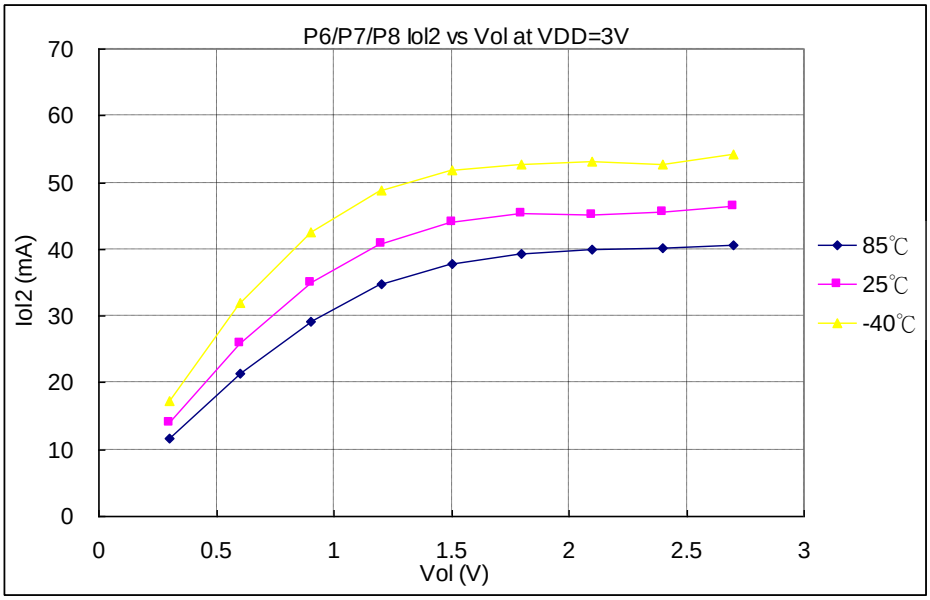


Figure 11-13 VOL vs. IOL, VDD=3V

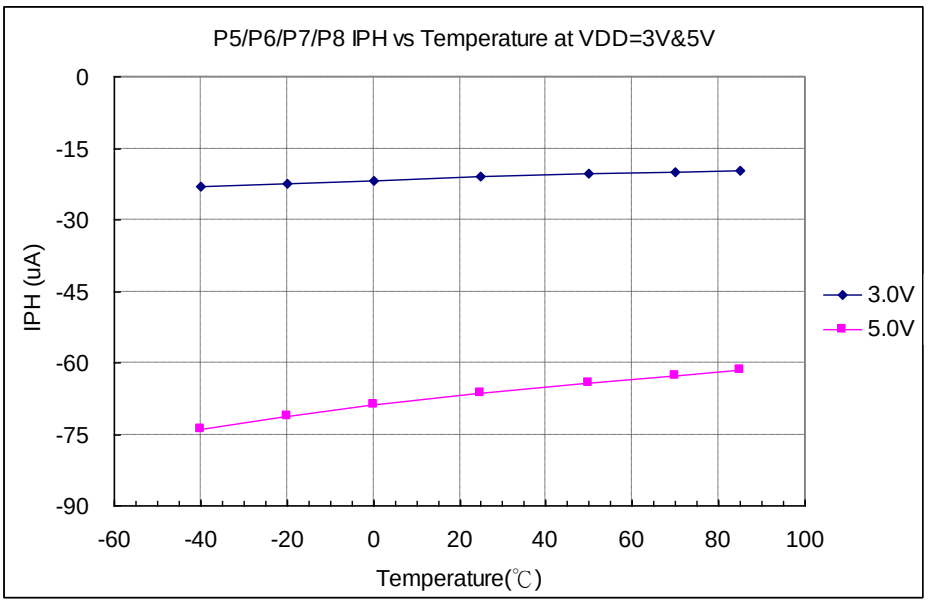


Figure 11-14 IPH vs. Temperature, VDD=3V and 5V

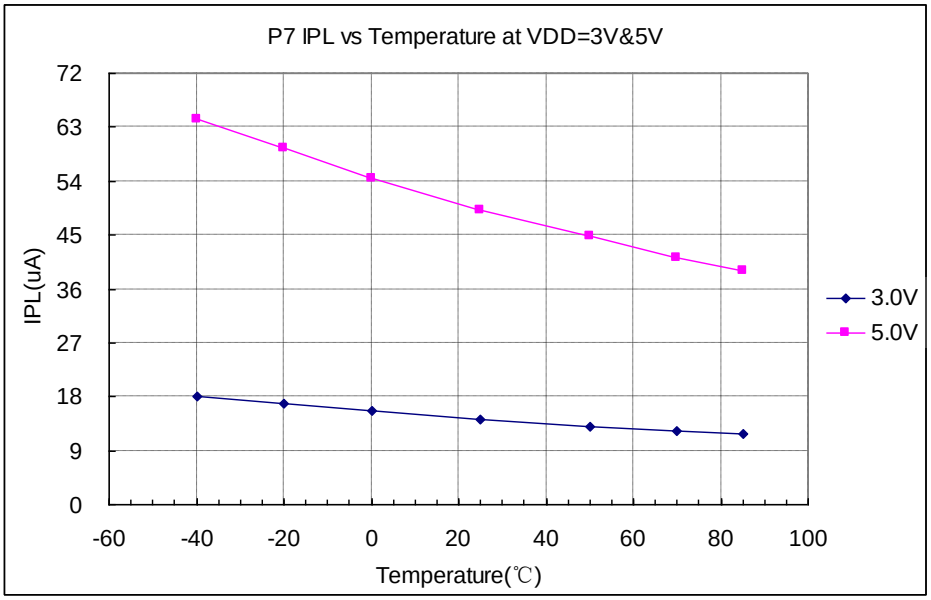


Figure 11-15 IPL of Ports 7 vs. Temperature, VDD=3V and 5V

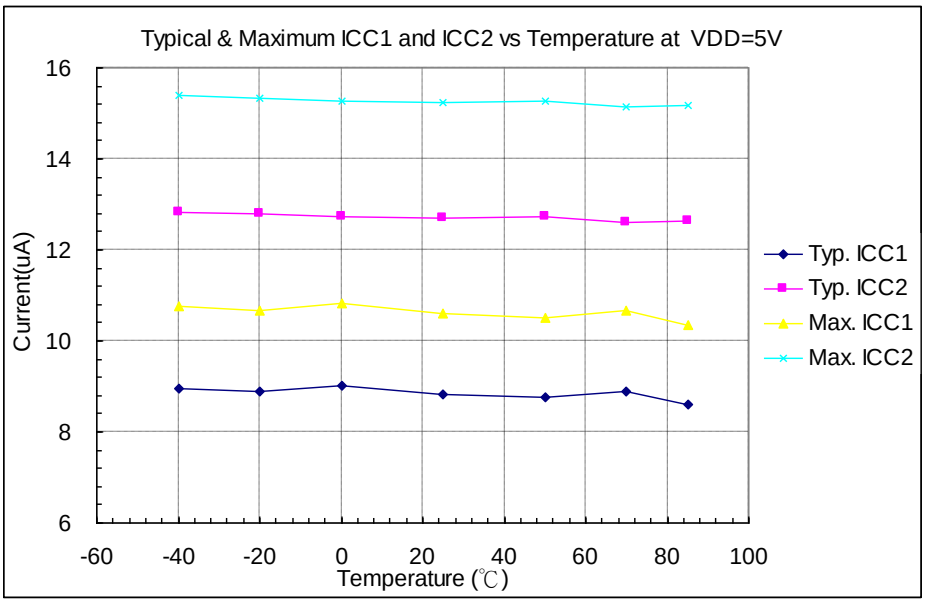


Figure 11-16 ICC1 and ICC2 vs. Temperature, VDD=5V

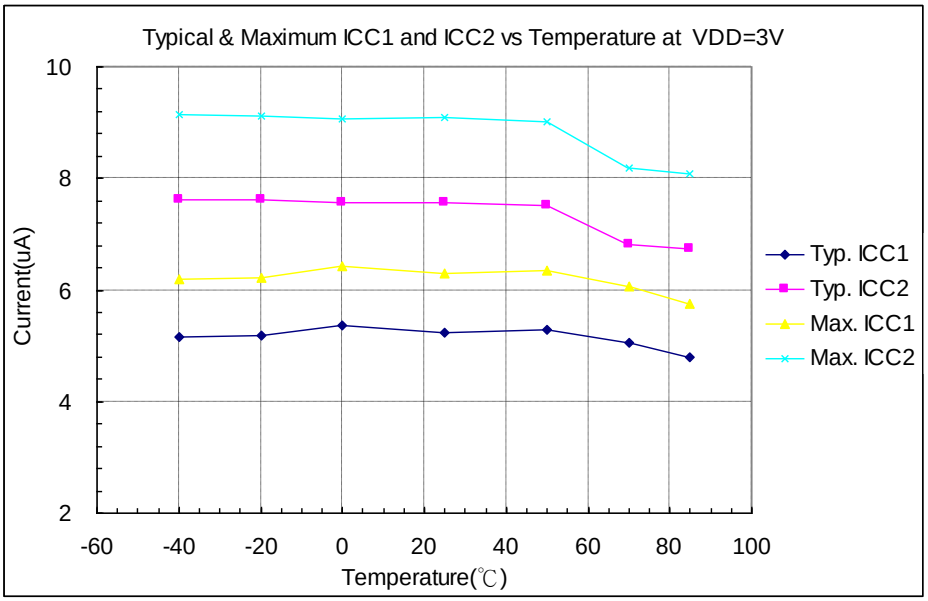


Figure 11-17 ICC1 and ICC2 vs. Temperature, VDD=3V

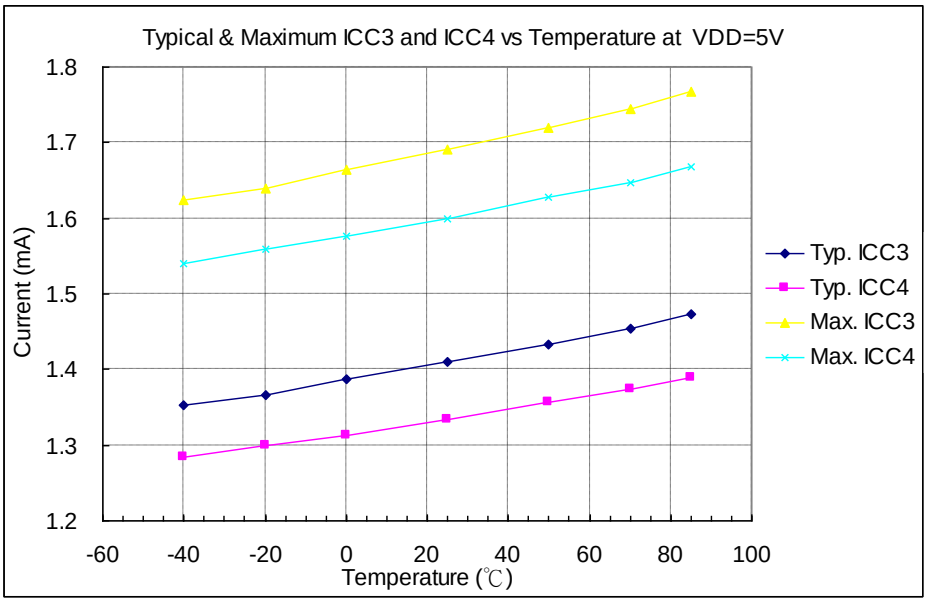


Figure 11-18 ICC3 and ICC4 vs. Temperature, VDD=5V

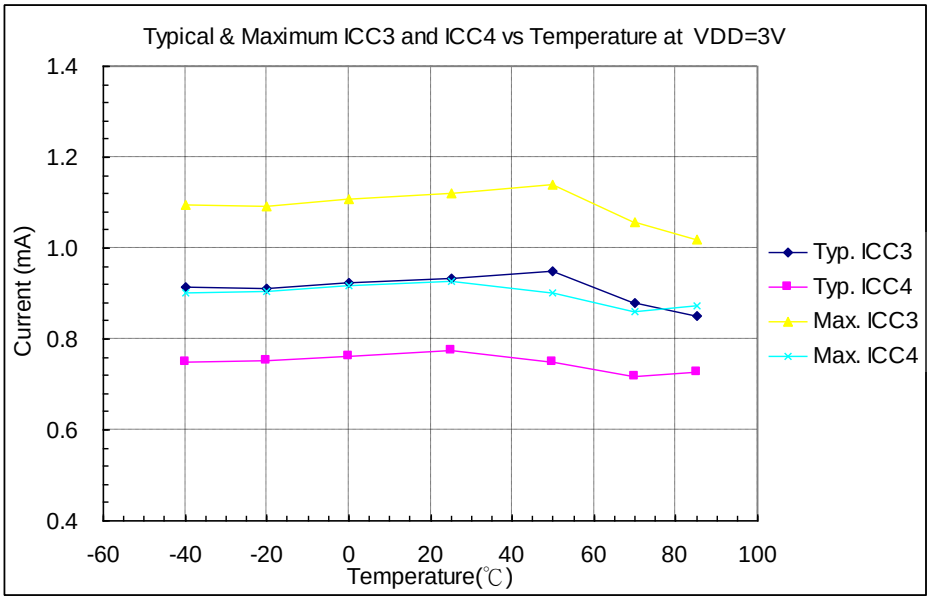


Figure 11-19 ICC3 and ICC4 vs. Temperature, VDD=3V

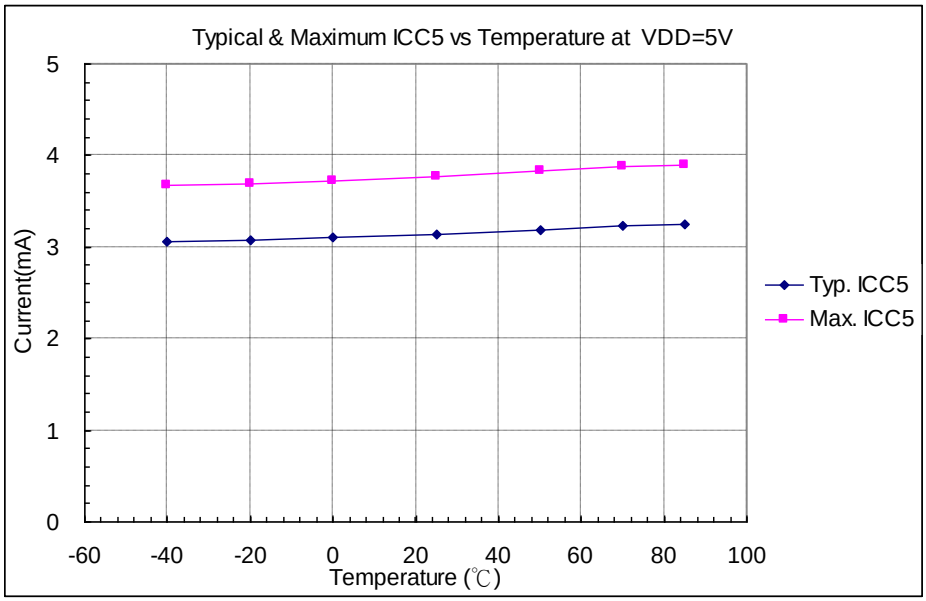


Figure 11-20 ICC5 vs. Temperature, VDD=5V

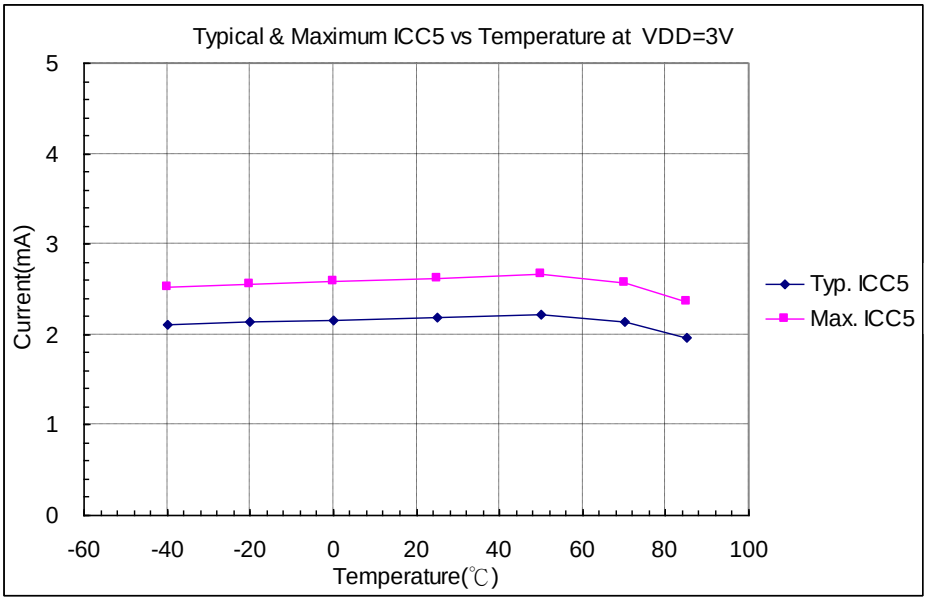


Figure 11-21 ICC5 vs. Temperature, VDD=3V

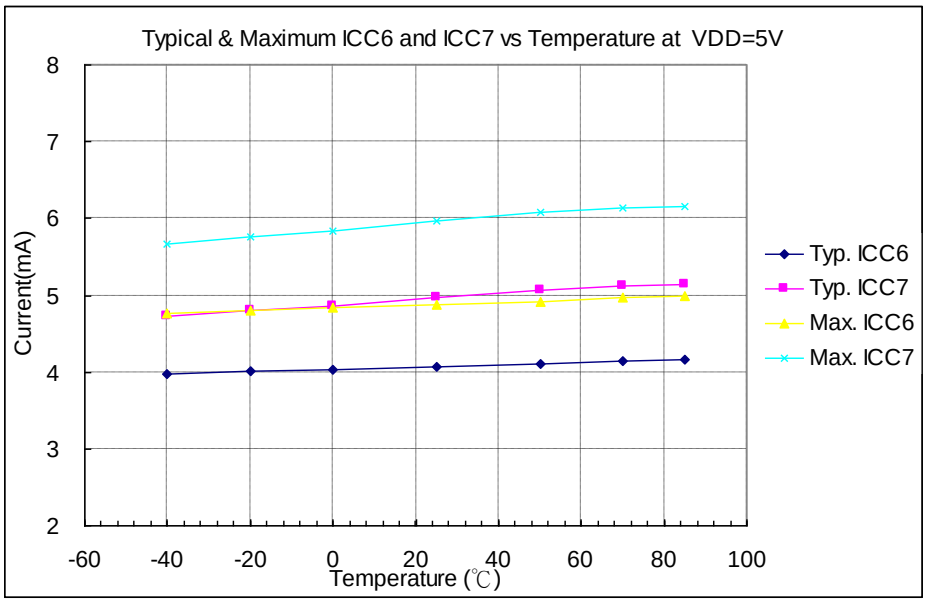


Figure 11-22 ICC6 and ICC7 vs. Temperature, VDD=5V

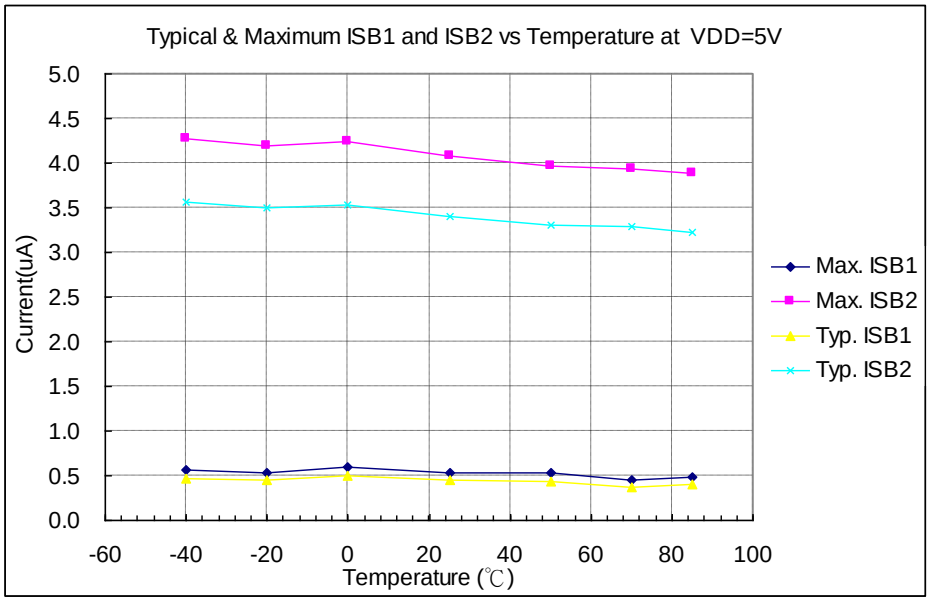


Figure 11-23 ISB1 and ISB2 vs. Temperature, VDD=5V

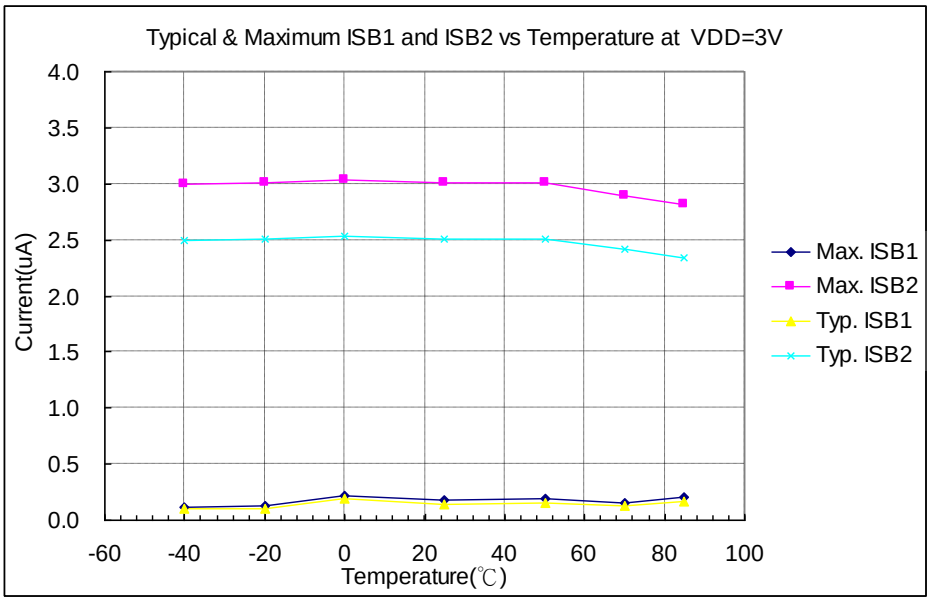


Figure 11-24 ISB1 and ISB2 vs. Temperature, VDD=3V

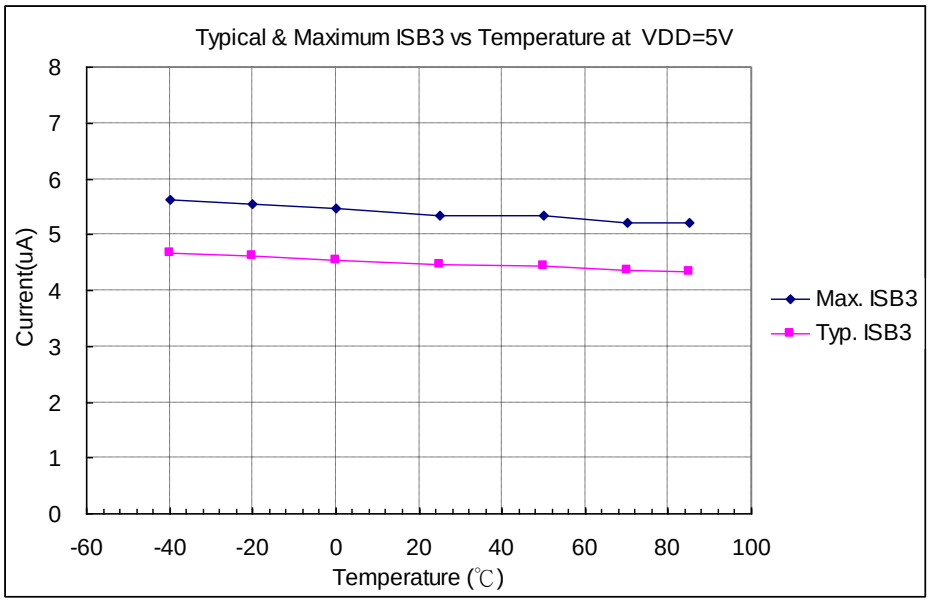


Figure 11-25 ISB3 and ISB4 vs. Temperature, VDD=5V

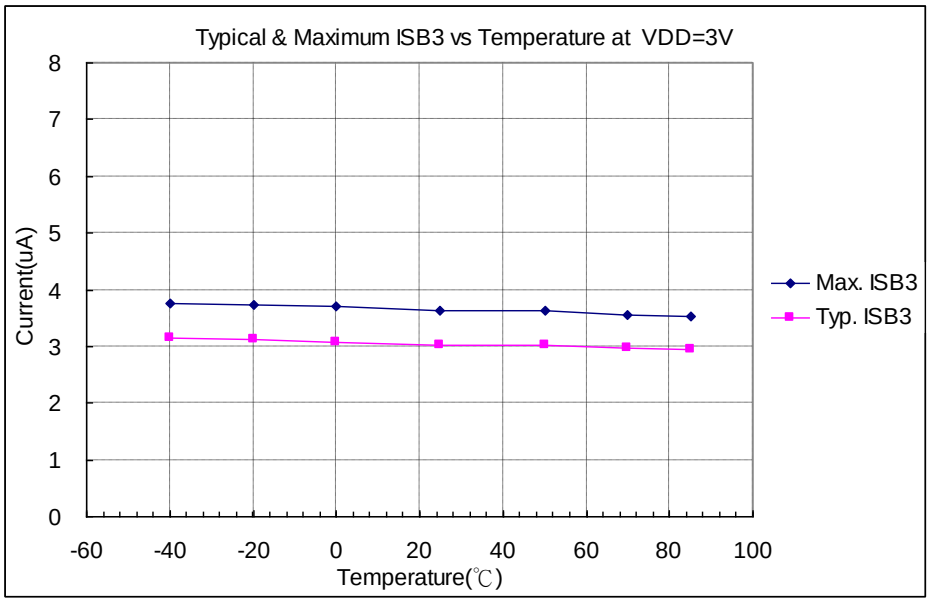


Figure 11-26 ISB3 and ISB4 vs. Temperature, VDD=3V

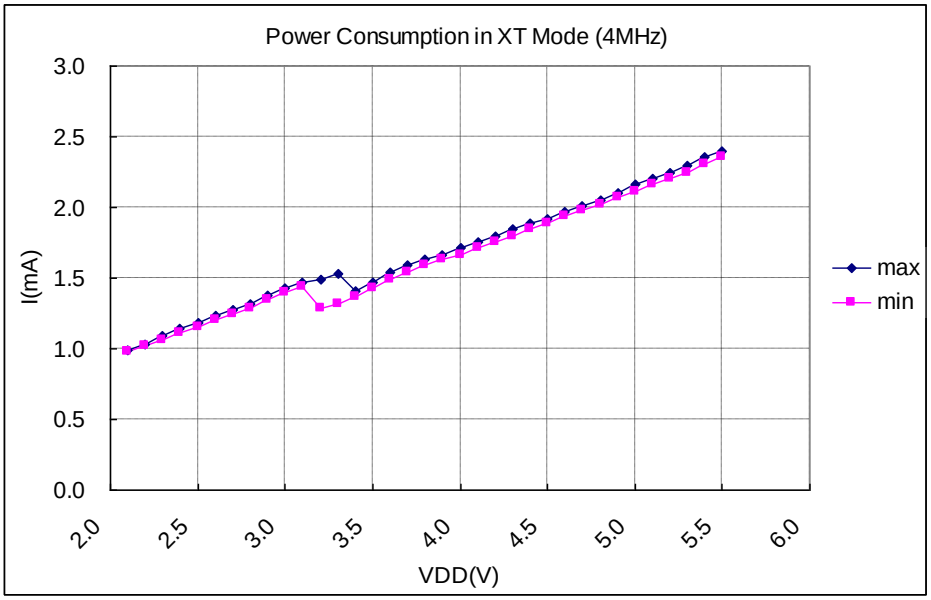


Figure 11-27 Power Consumption in XT Mode (4MHz)

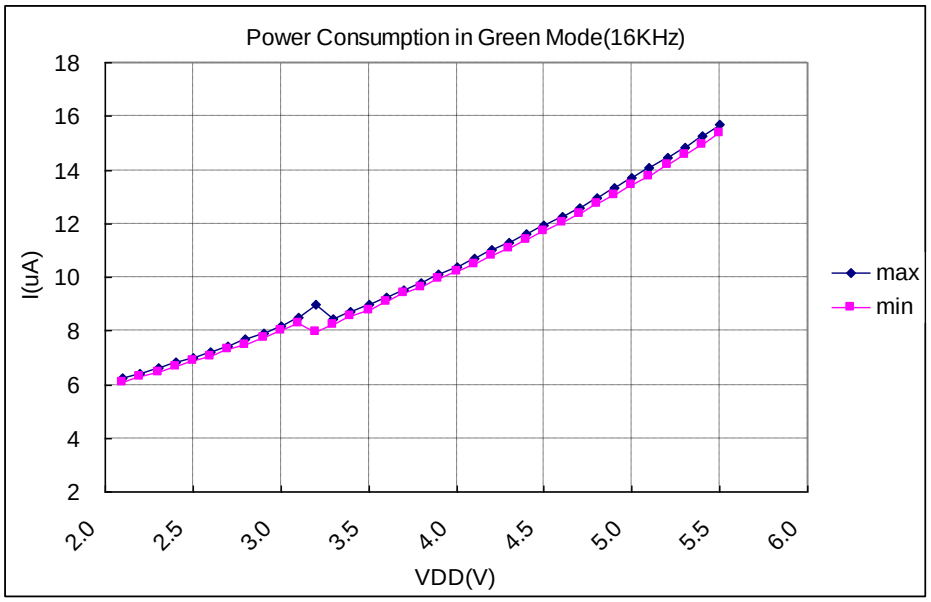


Figure 11-28 Power Consumption in Green Mode (16KHz)

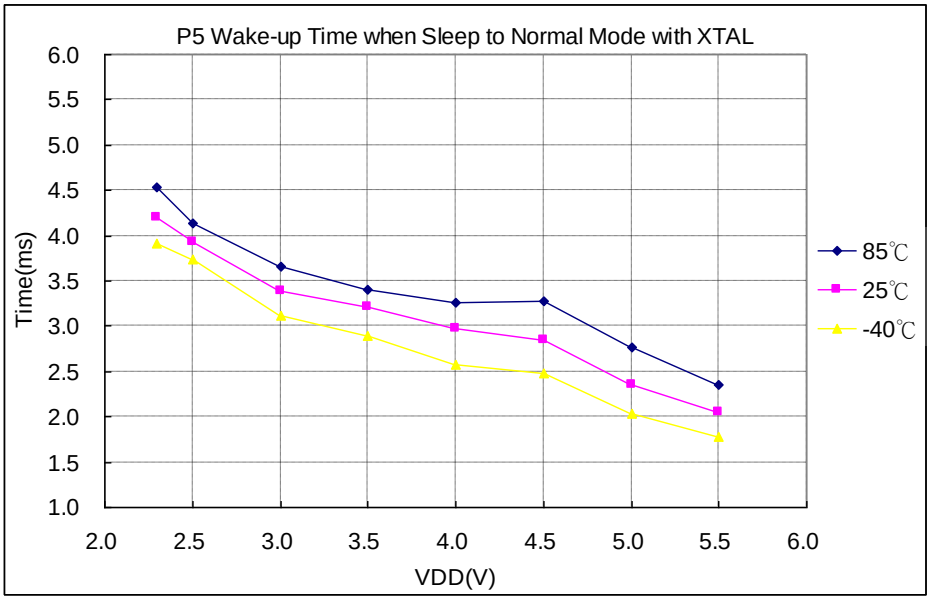


Figure 11-29 P5 Wake-up Time when Sleep to Normal, Crystal mode (Sub. Freq.=16kHz, 4 MHz)

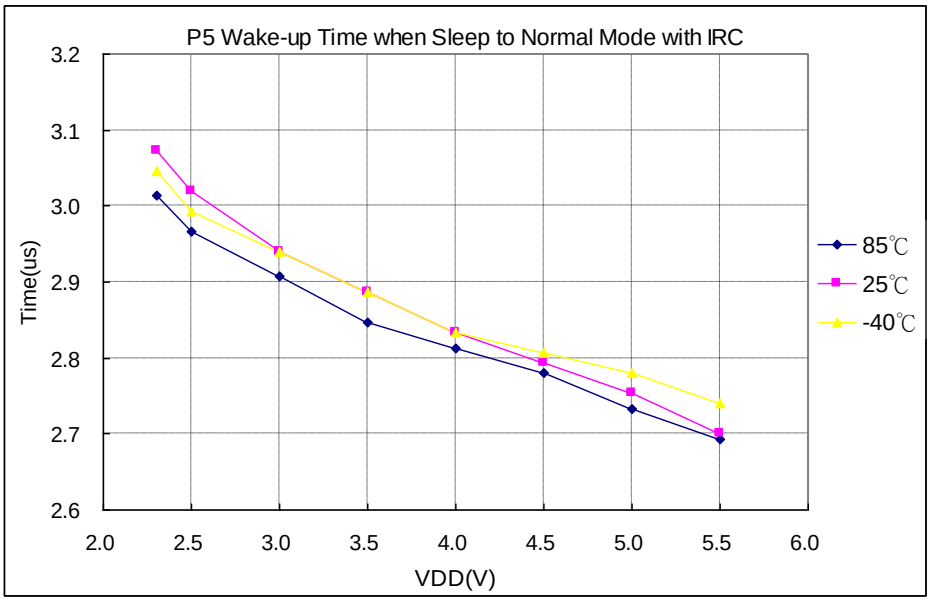


Figure 11-30 P5 Wake-up Time when Sleep to Normal, IRC mode (Sub. Freq.=16kHz, 4 MHz)

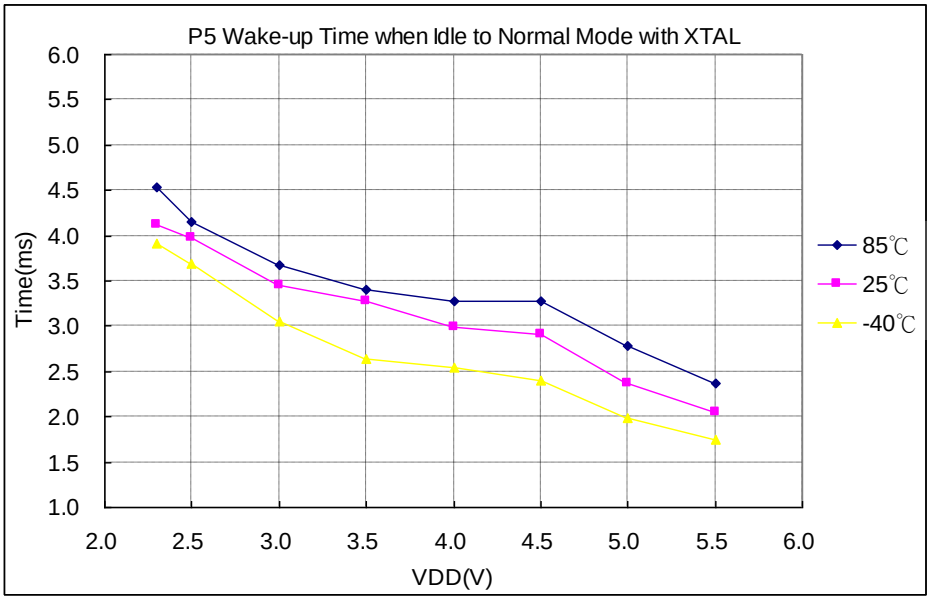


Figure 11-31 P5 Wake-up Time when Idle to Normal, Crystal mode (Sub. Freq.=16kHz, 4 MHz)

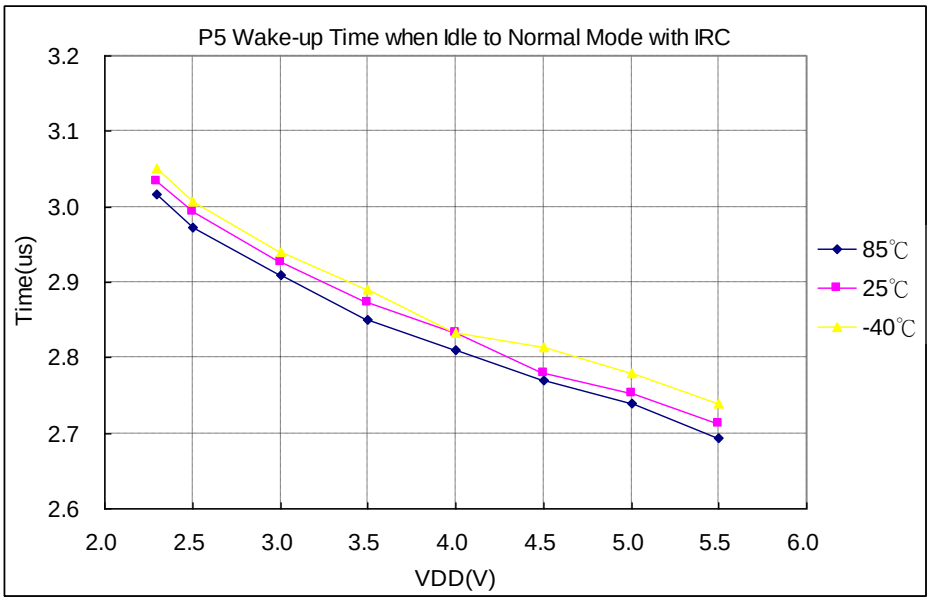


Figure 11-32 P5 Wake-up Time when Idle to Normal, IRC mode (Sub. Freq.=16kHz, 4 MHz)

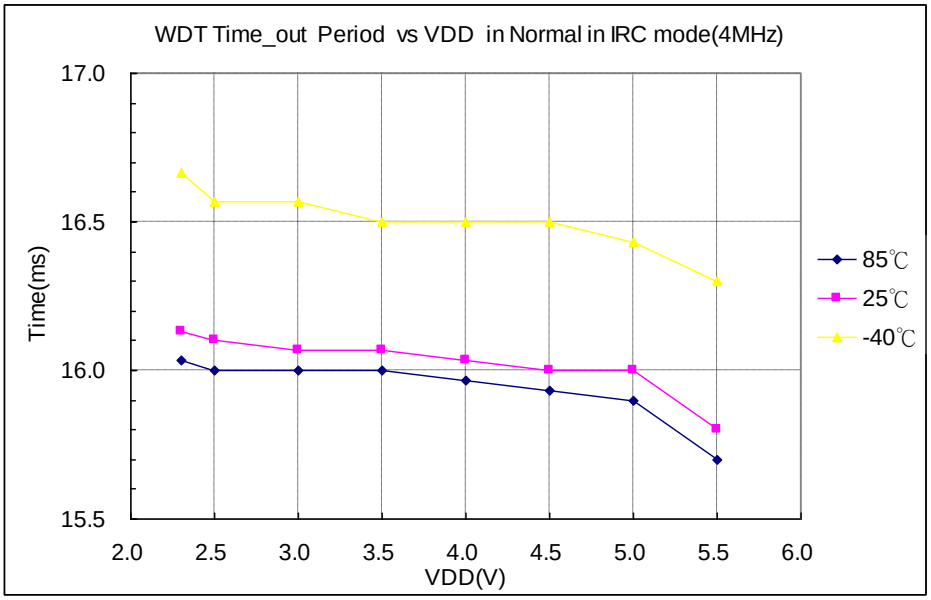


Figure 11-33 WDT Timer Time-out in Normal, IRC Mode (Sub. Freq.=16kHz, 4 MHz)

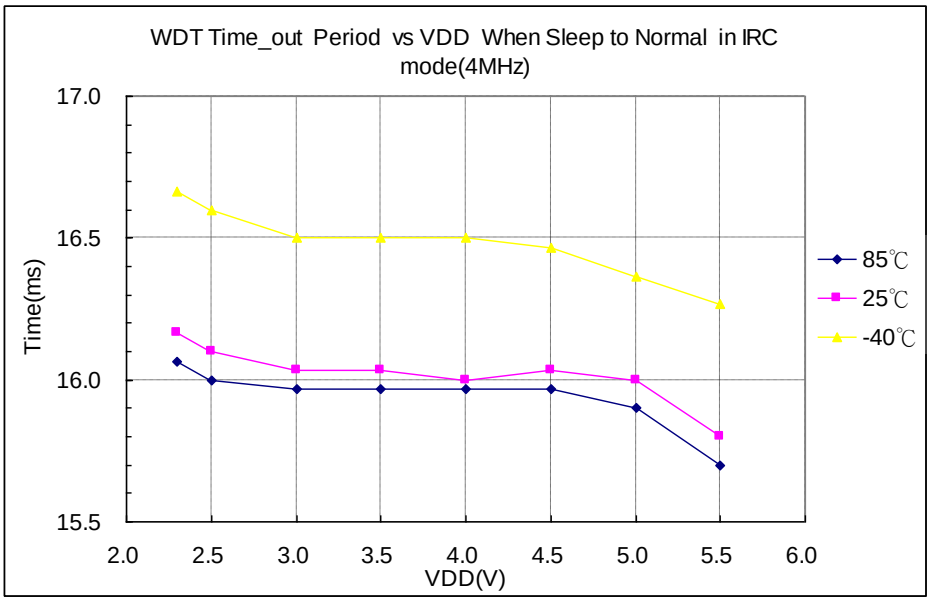


Figure 11-34 WDT Timer Time Out when Sleep to Normal, IRC Mode (4 MHz)

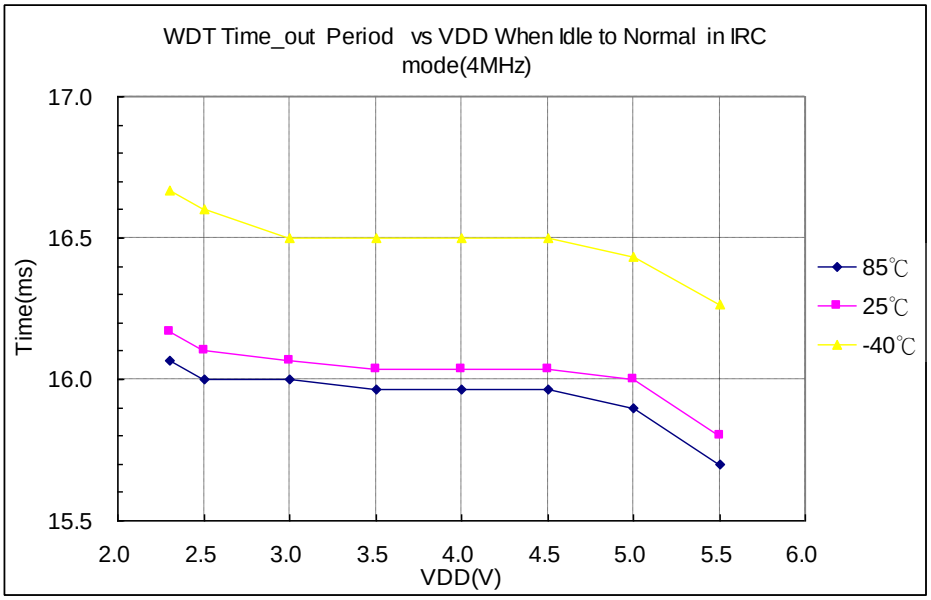


Figure 11-35 WDT Timer Time-out when in Idle to Normal, IRC Mode (4 MHz)

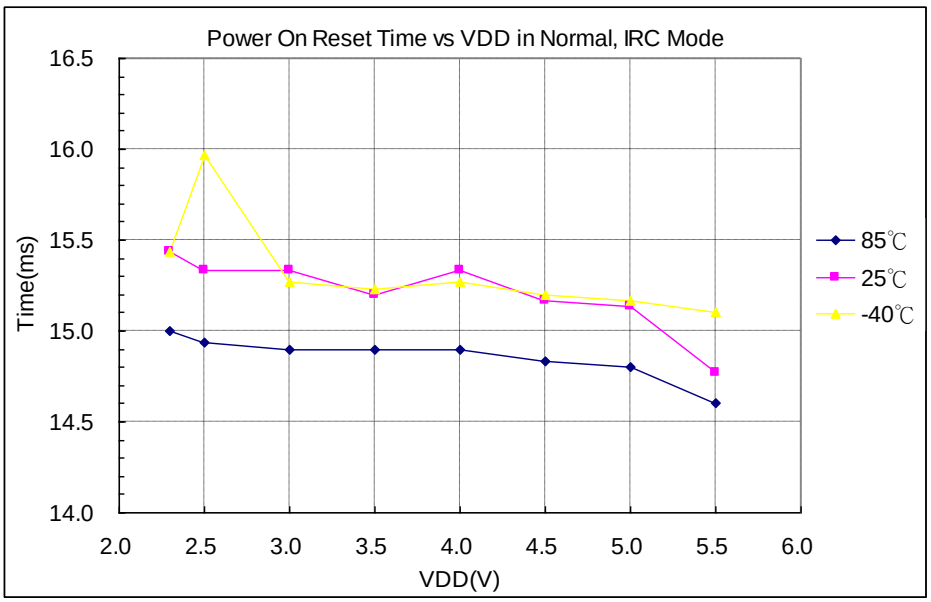


Figure 11-36 Power on Reset Time in Normal, IRC Mode (Sub. Freq.=16kHz, 4 MHz)

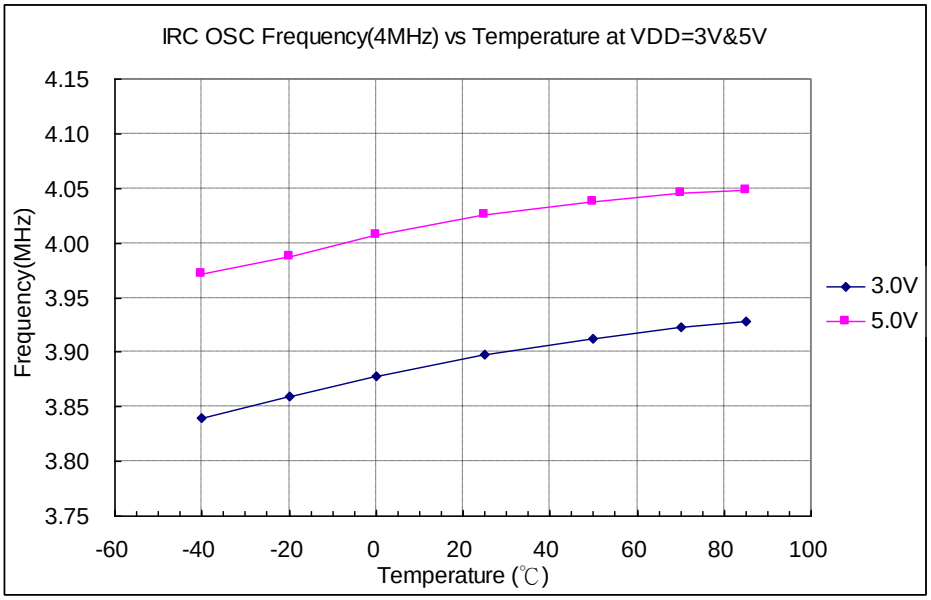


Figure 11-37 IRC OSC Freq, vs. Temp. (4MHz)

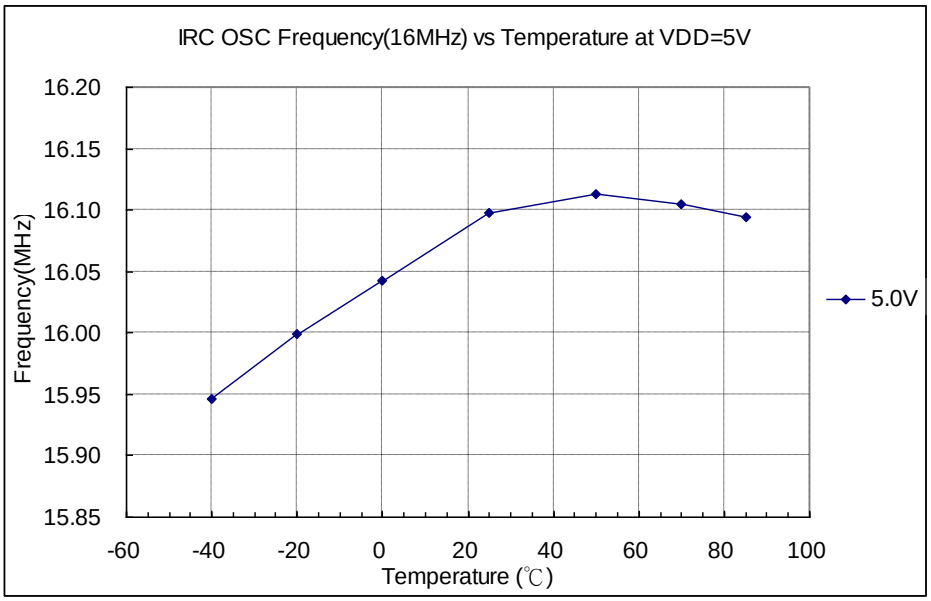


Figure 11-38 IRC OSC Freq, vs. Temp. (16 MHz)

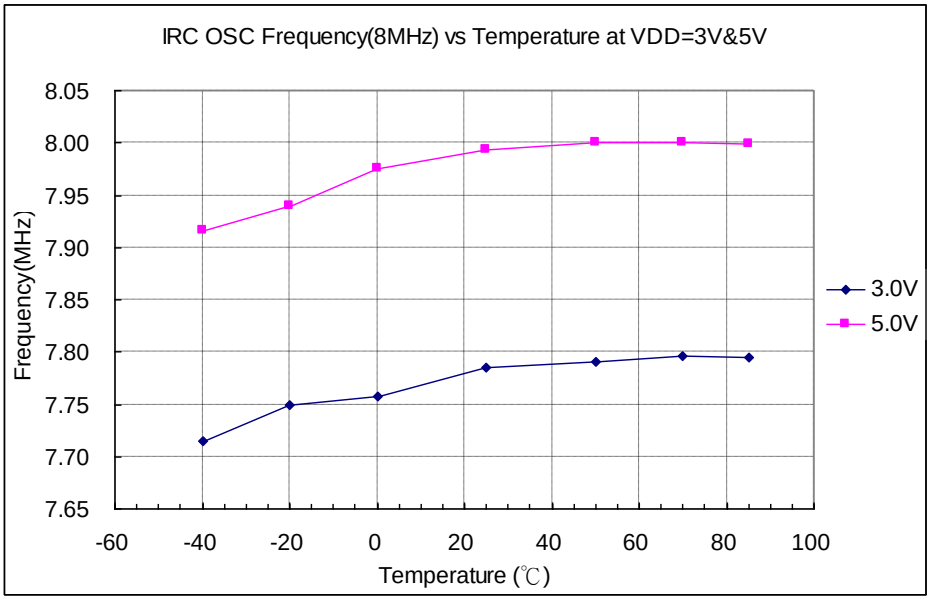


Figure 11-39 IRC OSC Freq, vs. Temp. (8MHz)

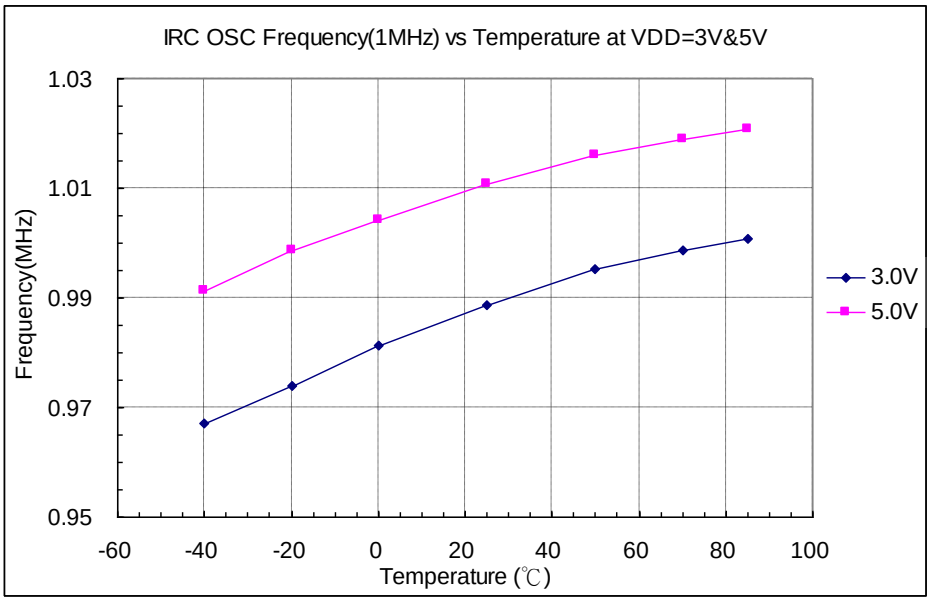


Figure 11-40 IRC OSC Freq, vs. Temp. (1MHz)

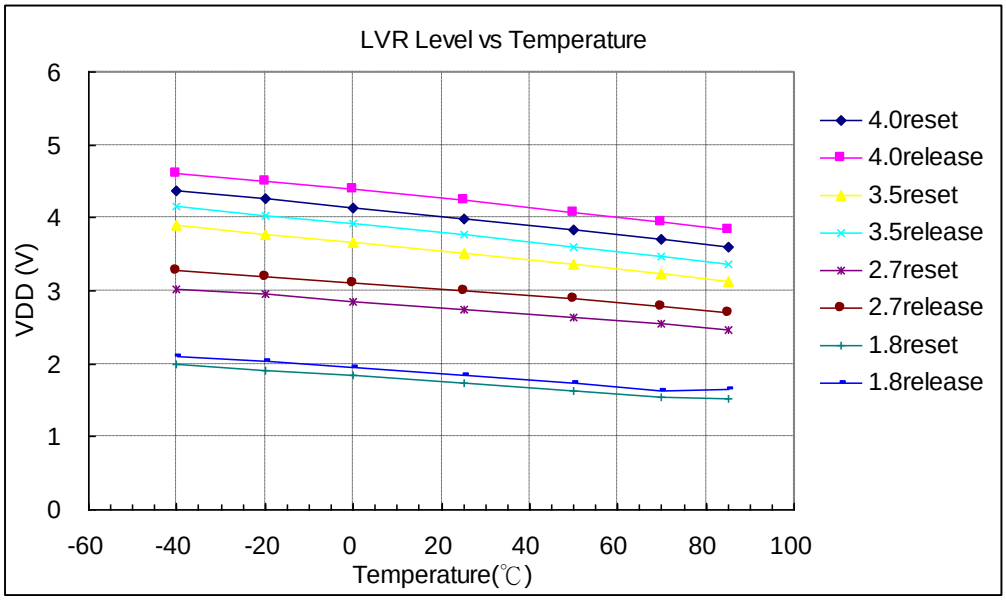


Figure 11-41 LVR Level vs Temperature

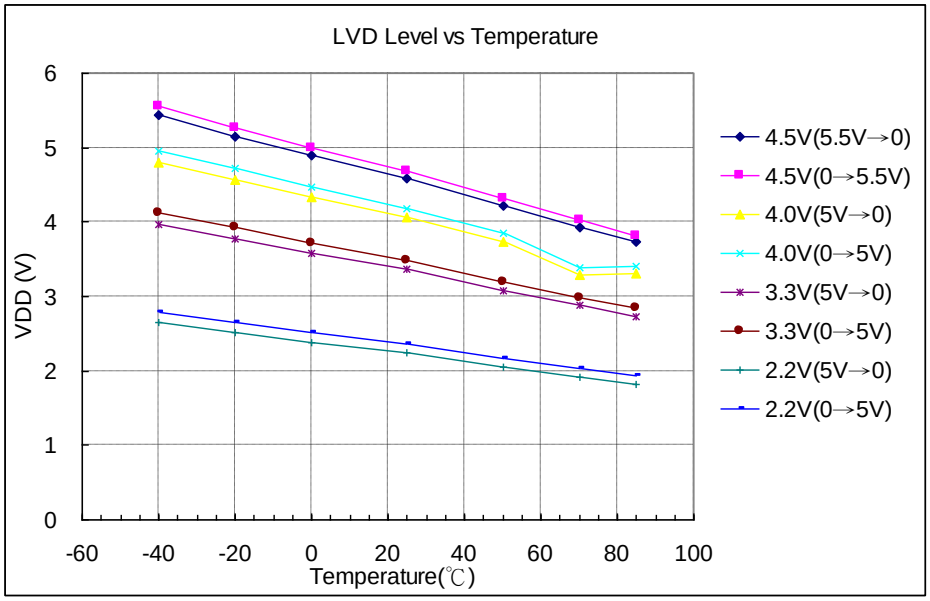
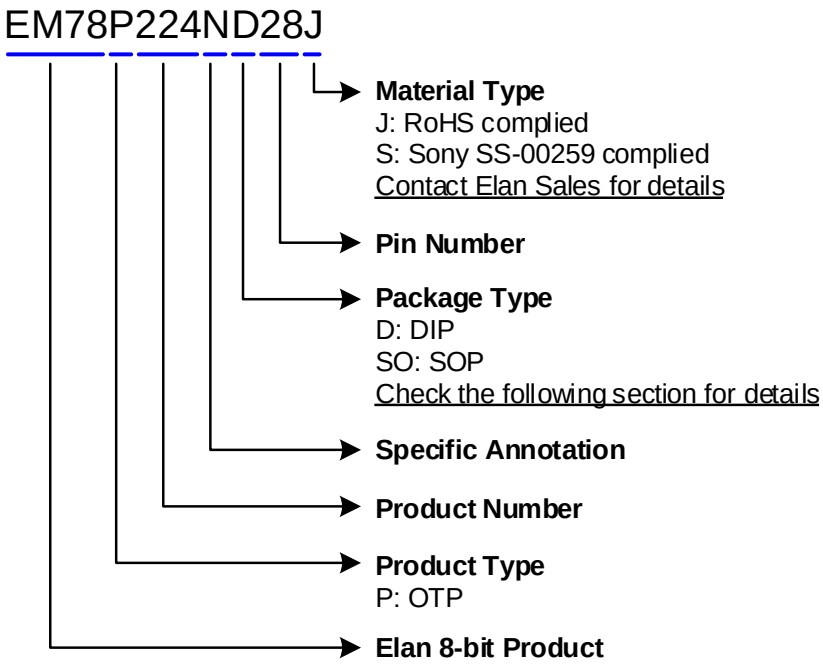


Figure 11-42 LVD Level vs. Temperature

APPENDIX

A Ordering and Manufacturing Information

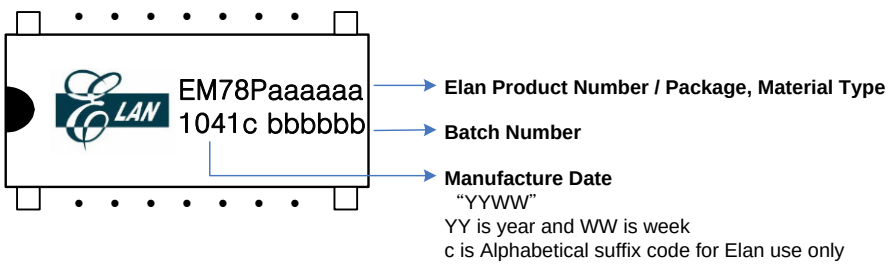


For example:

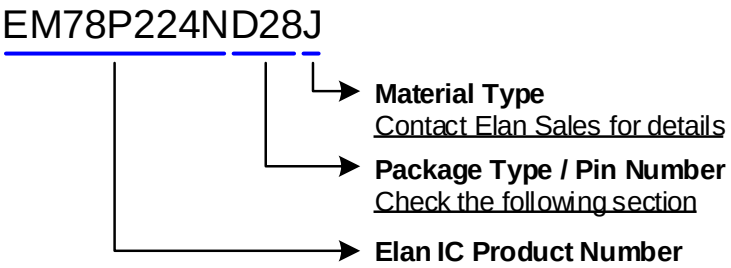
EM78P224ND28S

is EM78P224N with OTP program memory,
in 28-pin DIP 600mil package with Sony SS-00259 complied

IC Mark



Ordering Code



B Package Type

OTP MCU	Package Type	Pin Count	Package Size
EM78P224ND32	PDIP	32	600mil
EM78P224NSO32	SOP	32	450 mil
EM78P224NSO32A	SOP	32	300 mil
EM78P224ND28	PDIP	28	600 mil
EM78P224NK28A	Skinny DIP	28	400 mil
EM78P224NSO28	SOP	28	300 mil
EM78P224NSS28	SSOP	28	209 mil

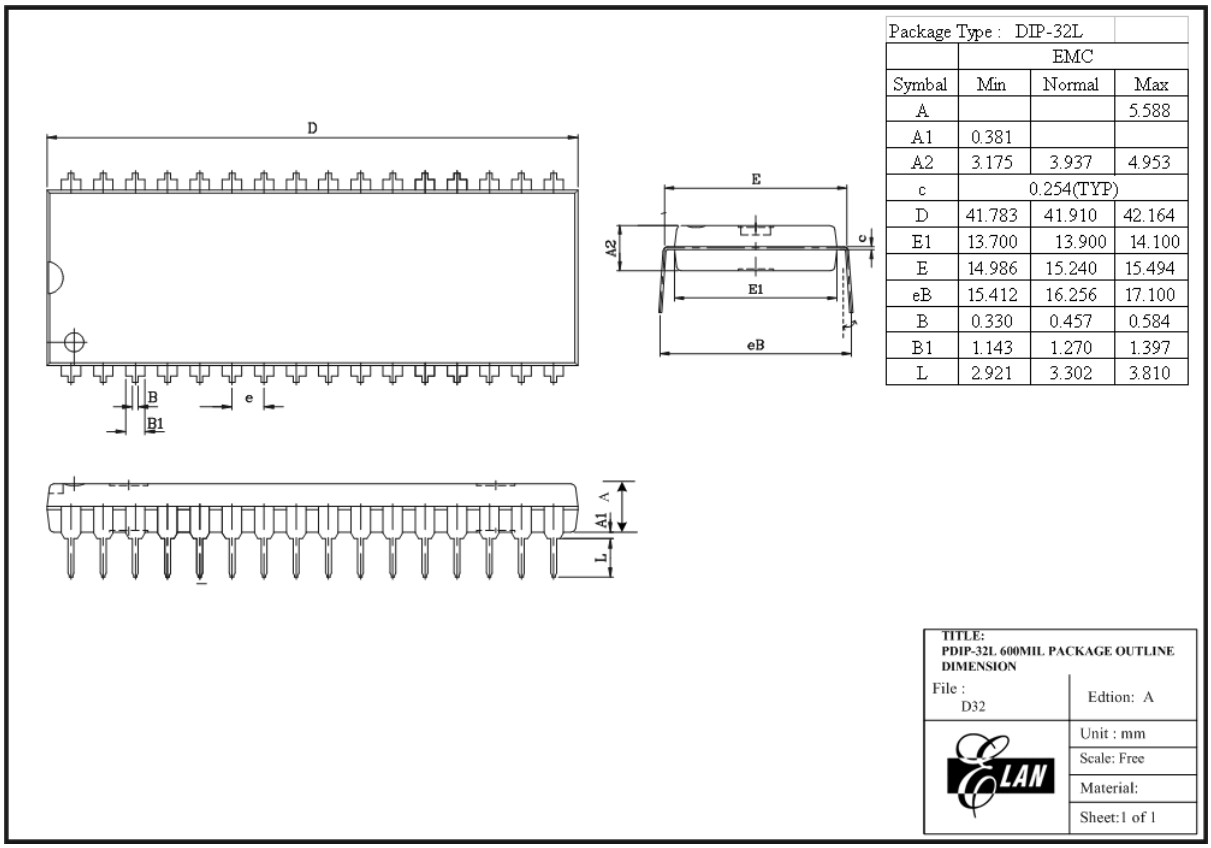
These are Green products which do not contain hazardous substances and comply with the third edition of Sony SS-00259 standard.

The Pb content is less than 100ppm and complies with Sony specifications.

Part No.	EM78P224NS/J
Electroplate type	Pure Tin
Ingredient (%)	Sn:100%
Melting point (°C)	232°C
Electrical resistivity (μΩ cm)	11.4
Hardness (hv)	8~10
Elongation (%)	>50%

C Packaging Information

C.1 EM78P224ND32 600mil

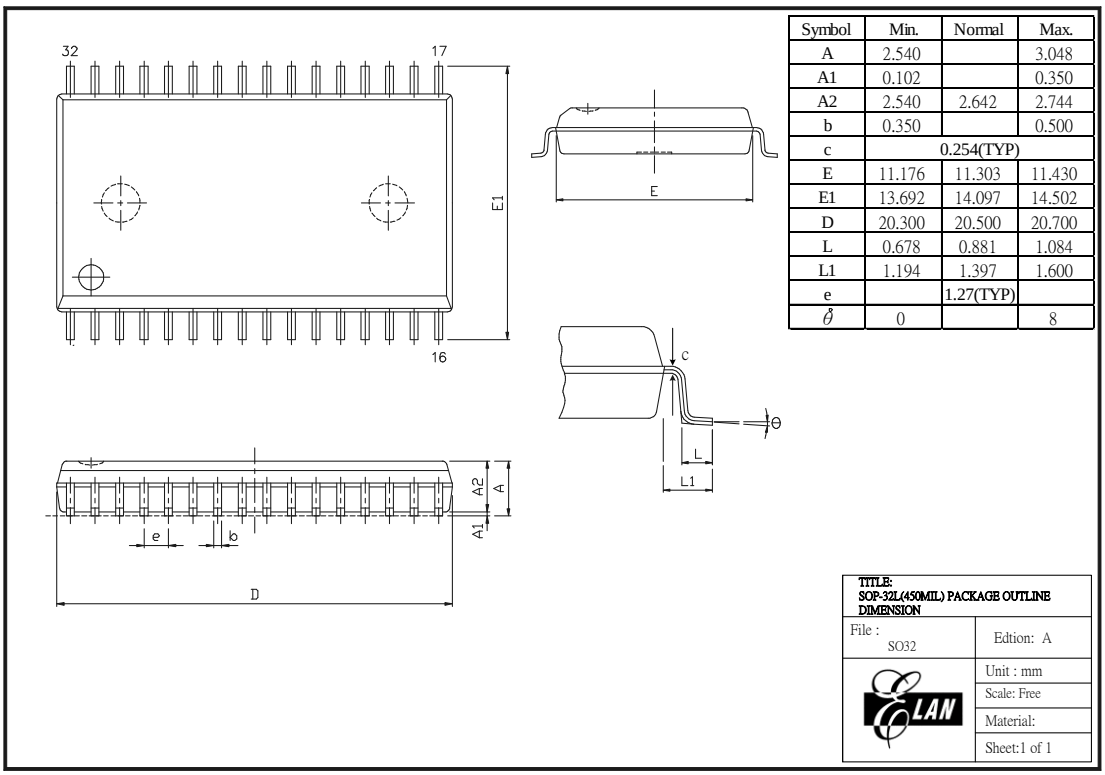


Package Type : DIP-32L			
	EMC		
Symbal	Min	Normal	Max
A			5.588
A1	0.381		
A2	3.175	3.937	4.953
c	0.254(TYP)		
D	41.783	41.910	42.164
E1	13.700	13.900	14.100
E	14.986	15.240	15.494
eB	15.412	16.256	17.100
B	0.330	0.457	0.584
B1	1.143	1.270	1.397
L	2.921	3.302	3.810

TITLE: PDIP-32L 600MIL PACKAGE OUTLINE DIMENSION	
File : D32	Edtion: A
	Unit : mm
	Scale: Free
	Material:
	Sheet:1 of 1

Figure C-1 EM78P224N 32-Pin PDIP Package Type

C.2 EM78P224NSO32 450 mil



Symbol	Min.	Normal	Max.
A	2.540		3.048
A1	0.102		0.350
A2	2.540	2.642	2.744
b	0.350		0.500
c		0.254(TYP)	
E	11.176	11.303	11.430
E1	13.692	14.097	14.502
D	20.300	20.500	20.700
L	0.678	0.881	1.084
L1	1.194	1.397	1.600
e		1.27(TYP)	
θ	0		8

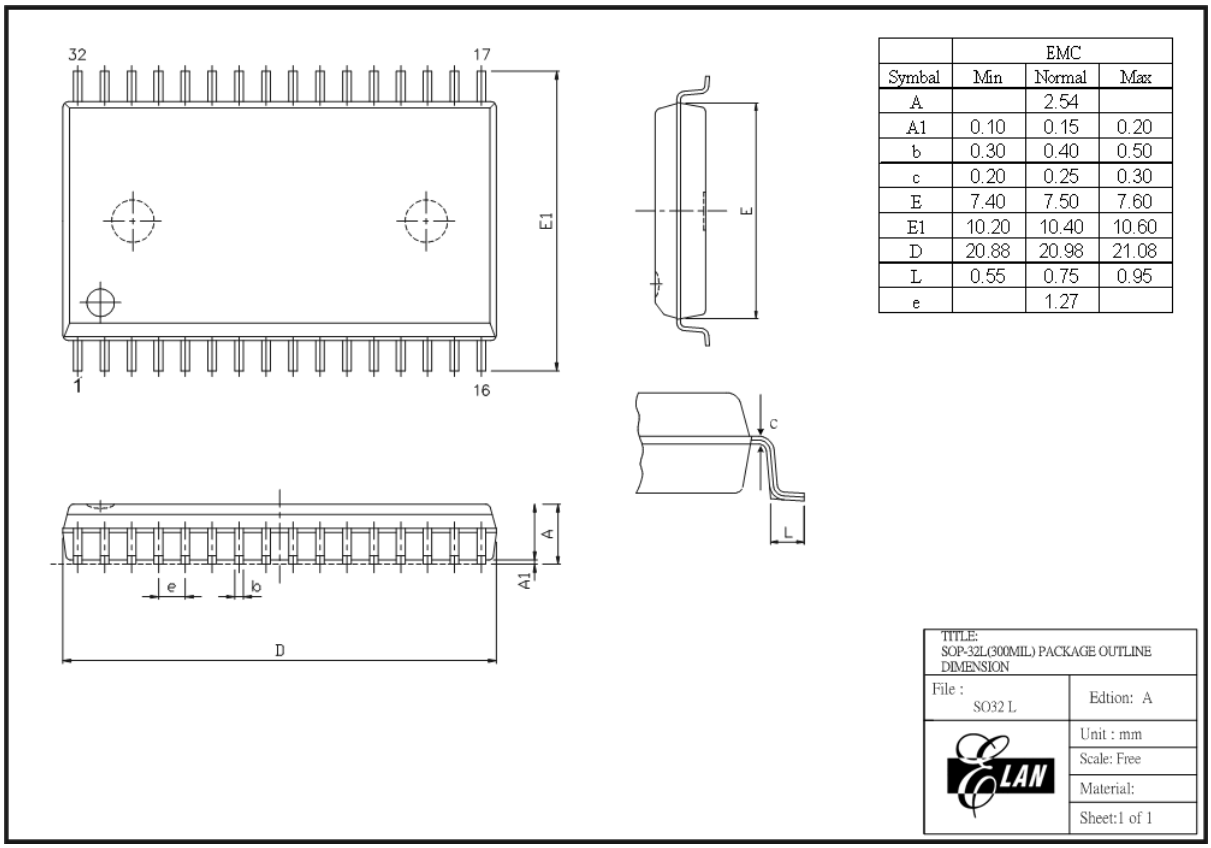
TITLE:
SOP-32L(450MIL) PACKAGE OUTLINE DIMENSION

File : SO32 | Edtion: A

Unit : mm
Scale: Free
Material:
Sheet:1 of 1

Figure C-2 EM78P224N 32-Pin SOP Package Type

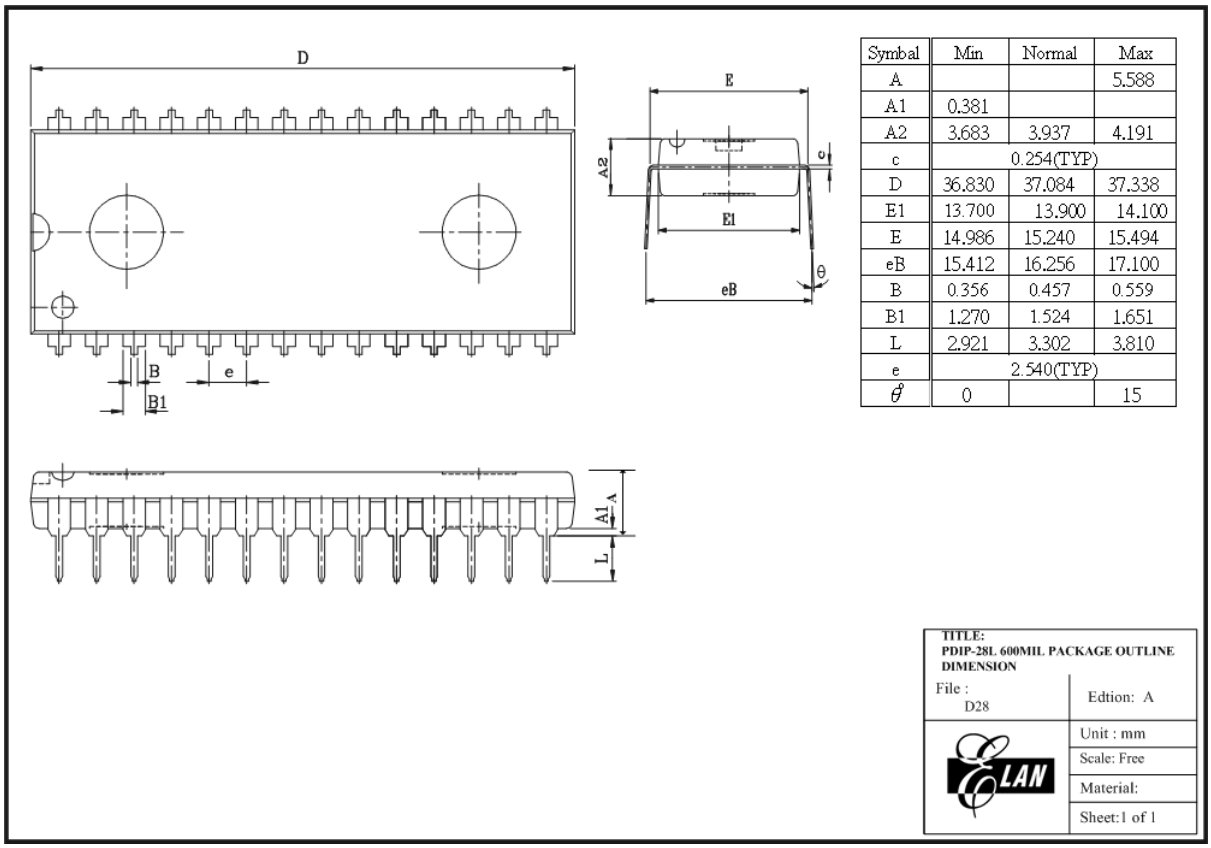
C.3 EM78P224NSO32A 300mil



	EMC		
Symbal	Min	Normal	Max
A		2.54	
A1	0.10	0.15	0.20
b	0.30	0.40	0.50
c	0.20	0.25	0.30
E	7.40	7.50	7.60
E1	10.20	10.40	10.60
D	20.88	20.98	21.08
L	0.55	0.75	0.95
e		1.27	

Figure C-3 EM78P224N 32-Pin SOP Package Type

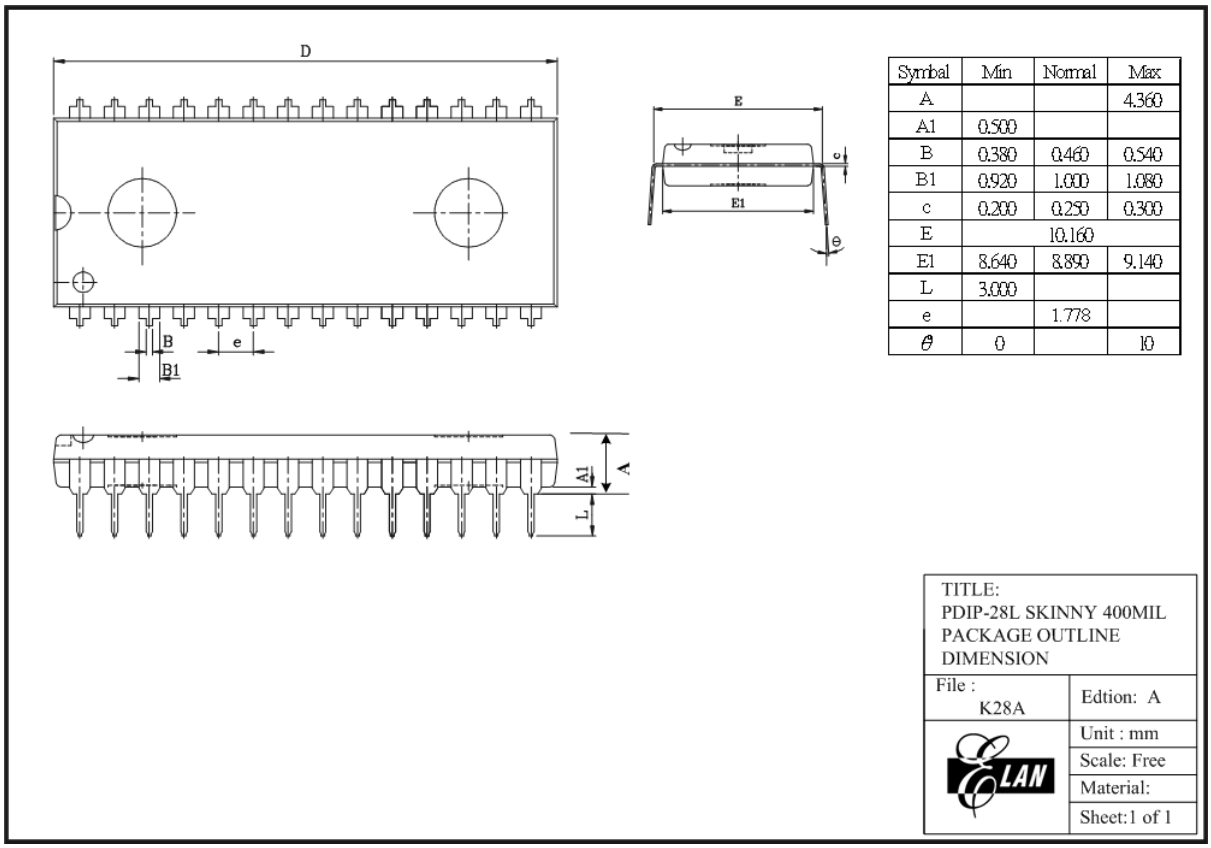
C.4 EM78P224ND28 600mil



Symbal	Min	Normal	Max
A			5.588
A1	0.381		
A2	3.683	3.937	4.191
c		0.254(TYP)	
D	36.830	37.084	37.338
E1	13.700	13.900	14.100
E	14.986	15.240	15.494
eB	15.412	16.256	17.100
B	0.356	0.457	0.559
B1	1.270	1.524	1.651
L	2.921	3.302	3.810
e		2.540(TYP)	
θ°	0		15

Figure C-4 EM78P224N 28-Pin PDIP Package Type

C.5 EM78P224NK28A 400mil

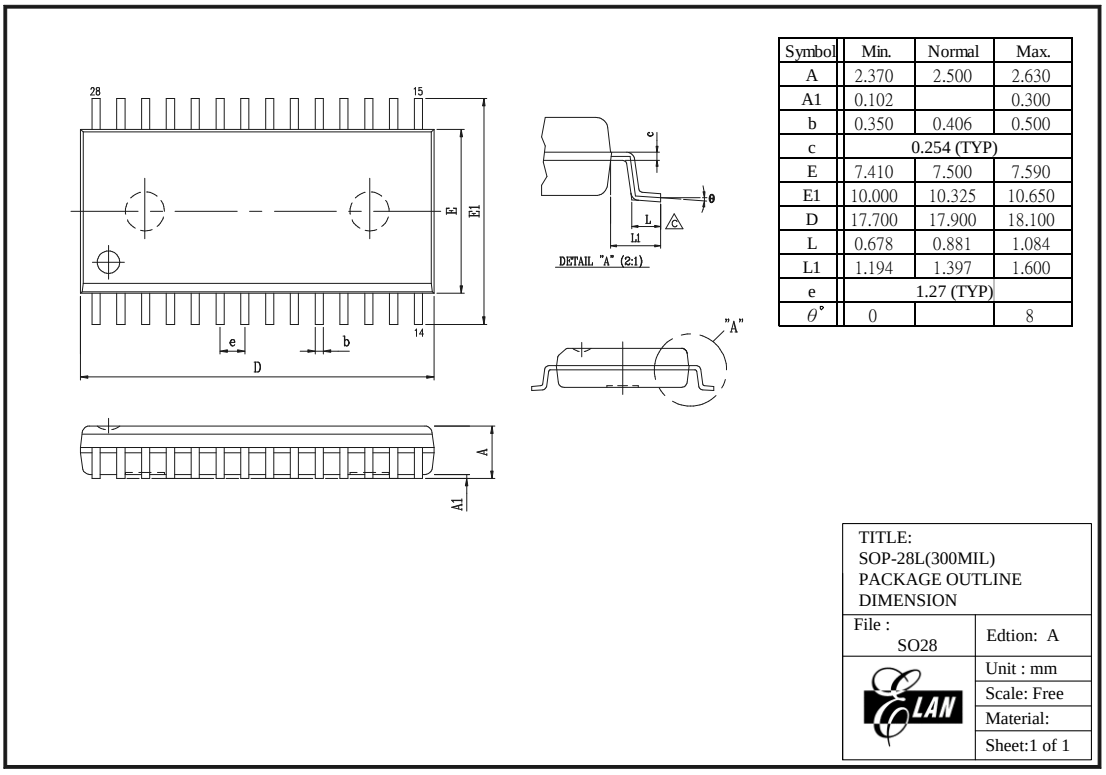


Symbal	Min	Normal	Max
A			4.360
A1	0.500		
B	0.380	0.460	0.540
B1	0.920	1.000	1.080
c	0.200	0.250	0.300
E		10.160	
E1	8.640	8.890	9.140
L	3.000		
e		1.778	
θ	0		10

TITLE: PDIP-28L SKINNY 400MIL PACKAGE OUTLINE DIMENSION	
File : K28A	Edtion: A
	Unit : mm
	Scale: Free
	Material:
	Sheet:1 of 1

Figure C-5 EM78P224N 28-Pin Skinny DIP Package Type

C.6 EM78P224NSO28 300mil

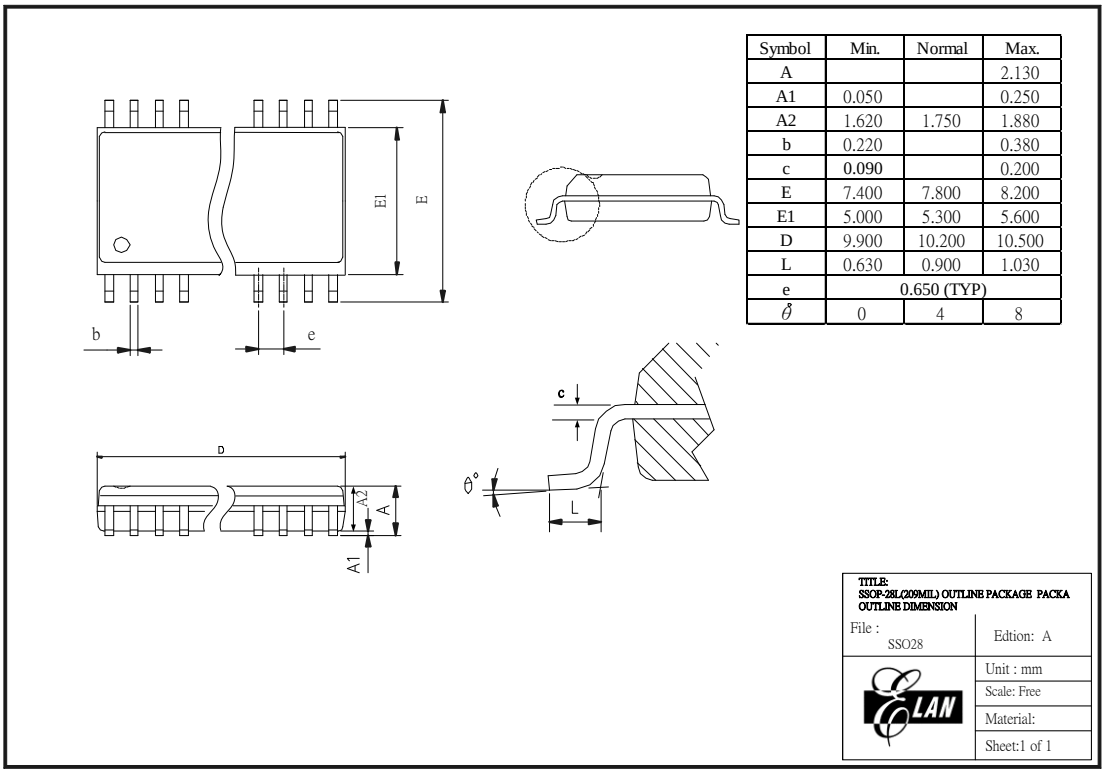


Symbol	Min.	Normal	Max.
A	2.370	2.500	2.630
A1	0.102		0.300
b	0.350	0.406	0.500
c		0.254 (TYP)	
E	7.410	7.500	7.590
E1	10.000	10.325	10.650
D	17.700	17.900	18.100
L	0.678	0.881	1.084
L1	1.194	1.397	1.600
e		1.27 (TYP)	
θ°	0		8

TITLE: SOP-28L(300MIL) PACKAGE OUTLINE DIMENSION	
File : SO28	Edtion: A
	Unit : mm
	Scale: Free
	Material:
	Sheet:1 of 1

Figure C-6 EM78P224N 28-Pin SOP Package Type

C.7 EM78P224NSS28 209mil



Symbol	Min.	Normal	Max.
A			2.130
A1	0.050		0.250
A2	1.620	1.750	1.880
b	0.220		0.380
c	0.090		0.200
E	7.400	7.800	8.200
E1	5.000	5.300	5.600
D	9.900	10.200	10.500
L	0.630	0.900	1.030
e	0.650 (TYP)		
θ	0	4	8

Figure C-7 EM78P224N 28-Pin SSOP Package Type

D Quality Assurance and Reliability

Test Category	Test Conditions	Remarks
Solderability	Solder temperature=245±5°C, for 5 seconds up to the stopper using a rosin-type flux	–
Pre-condition	Step 1: TCT, 65°C (15mins)~150°C (15mins), 10 cycles	For SMD IC (such as SOP, QFP, SOJ, etc)
	Step 2: Bake at 125°C, TD (endurance)=24 hrs	
	Step 3: Soak at 30°C/60%, TD (endurance)=192 hrs	
	Step 4: IR flow 3 cycles (Pkg thickness ≥ 2.5mm or Pkg volume ≥ 350mm^3 ----225±5°C) (Pkg thickness ≤ 2.5mm or Pkg volume ≤ 350mm^3 ----240±5°C)	
Temperature cycle test	-65°C (15 min) ~ 150°C (15 min), 200 cycles	–
Pressure cooker test	TA =121°C, RH=100%, pressure=2 atm, TD (endurance)= 96 hrs	–
High temperature / High humidity test	TA=85°C , RH=85%, TD (endurance) = 168 , 500 hrs	–
High-temperature storage life	TA=150°C, TD (endurance) = 500, 1000 hrs	–
High-temperature operating life	TA=125°C, VCC = Max. operating voltage, TD (endurance) = 168, 500, 1000 hrs	–
Latch-up	TA=25°C, VCC = Max. operating voltage, 800mA/40V	–
ESD (HBM)	TA=25°C, ≥ | ± 4KV |	IP_ND,OP_ND,IO_ND IP_NS,OP_NS,IO_NS IP_PD,OP_PD,IO_PD, IP_PS,OP_PS,IO_PS, VDD-VSS(+),VDD_VSS(-) mode
ESD (MM)	TA=25°C, ≥ | ± 400V |	

D.1 Address Trap Detect

An Address Trap Detect is one of the MCU embedded fail-safe functions that detects MCU malfunction caused by noise or the like. Whenever the MCU attempts to fetch an instruction from a certain section of ROM, an internal recovery circuit is auto started. If a noise-caused address error is detected, the MCU will repeat execution of the program until the noise is eliminated. The MCU will then continue to execute the next program.