EM78P349N

8-Bit Microcontroller

Product Specification

DOC. VERSION 1.3

ELAN MICROELECTRONICS CORP.

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APPENDIX

Specification Revision History

Doc. Version	Revision Description	Date
1.0	Initial released version	2009/1/13
1.1	Added a Note stating that the AD input channels ADIN12~ 14 cannot be simulated in ICE349. They can only be used in EM78P349N.	2009/8/18
1.2	1. Modified the format of the pin description 2. Added the figures of the temperature test	2010/4/8
1.3	1. Modified Shanghai and Shenzhen's address, and added Korea's address. 2. Modified the pin description	2012/02/24

1 General Description

EM78P349N is an 8-bit microprocessor designed and developed with low-power and high-speed CMOS technology. It has an on-chip 2K×13-bit Electrical One Time Programmable Read Only Memory (OTP-ROM).

With its enhanced OTP-ROM features, the EM78P349N provides a convenient way of developing and verifying user's programs. Moreover, this OTP device offers the advantages of easy and effective program updates, using development and programming tools. User can avail of the ELAN Writer to easily program his development code.

2 Features

- CPU configuration
  - 2K×13 bits on-chip ROM
  - (160+16) × 8 bits on chip registers (SRAM)
  - 8-level stacks for subroutine nesting
  - 4 programmable Level Voltage Detector (LVD) : 4.5V, 4.0V, 3.3V, 2.2V
  - 3 programmable Level Voltage Reset (LVR) : 4.0V, 3.0V, 2.5V
  - Less than 1.5 mA at 5V/4MHz
  - Typically 15 μA, at 3V/32kHz
  - Typically 2 μA, during sleep mode
- I/O port configuration
  - 3 bi-directional I/O ports
  - 8 programmable pull-down I/O pins
  - 8 programmable pull-high I/O pins
  - 8 programmable open-drain I/O pins
  - 2 external interrupt pins
- Operating voltage:
  - 2.3V~5.5V at -40°C~85°C (Industrial)
- Operating frequency range (base on 2 clocks)
  - Crystal mode:
    DC ~ 20 MHz, 5V ; DC ~ 8 MHz, 3V
  - IRC mode: DC ~ 8 MHz, 3V

Internal RC Frequency	Drift Rate			
	Temperature (-40°C~85°C)	Voltage (2.3V~5.5V)	Process	Total
4 MHz	± 5%	± 5%	± 4%	± 14%
8 MHz	± 5%	± 5%	± 4%	± 14%
1 MHz	± 5%	± 5%	± 4%	± 14%
455kHz	± 5%	± 5%	± 4%	± 14%

- Peripheral configuration
  - 8-bit real time clock/counter (TCC) with selective signal sources, trigger edges, and overflow interrupt
  - 15-bit multi-channel Analog-to-Digital Converter with 12-bit resolution
  - Three Pulse Width Modulation (PWM) with 10-bit resolution
- Power-down (Sleep) mode
- Six available interrupts
  - TCC overflow interrupt
  - Input-port status changed interrupt (wake-up from sleep mode)
  - External interrupt
  - ADC completion interrupt
  - PWM period match completion
  - Low voltage detector interrupt
- Programmable free running Watchdog Timer
- Power-on voltage detector available (1.9V±0.1V)
- Package Type
  - 24-pin Skinny DIP 300mil : EM78P349NK24S/J
  - 24 pin SOP 300mil : EM78P349NSO24S/J
  - 28-pin Skinny DIP 300mil : EM78P349NK28S/J
  - 28-pin SOP 300mil : EM78P349NSO28S/J

3 Pin Assignment

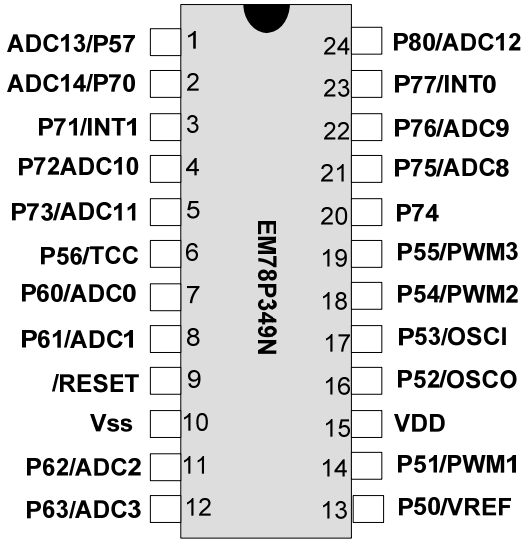


Figure 3-1 EM78P349NK24/SO24

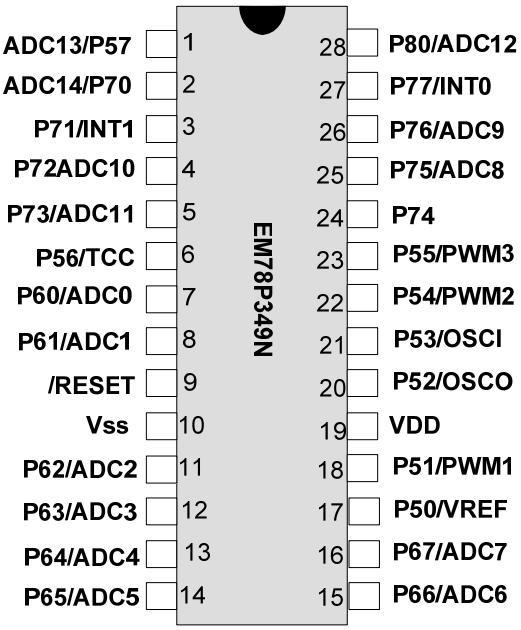


Figure 3-2 EM78P349NK28/SO28

4 Pin Description

4.1 EM78P349NK24/SO24

Name	Function	Input Type	Output Type	Description
P50/VREF	P50	ST	CMOS	Bidirectional I/O pin with programmable pull-high and open-drain
	VREF	AN	–	ADC external voltage reference
P51/PWM1	P51	ST	CMOS	Bidirectional I/O pin with programmable pull-high and open-drain
	PWM1	–	CMOS	PWM1 output
P52/OSCO	P52	ST	CMOS	Bidirectional I/O pin with programmable pull-high and open-drain
	OSCO	–	XTAL	Clock output of crystal/ resonator oscillator
P53/OSCI	P53	ST	CMOS	Bidirectional I/O pin with programmable pull-high and open-drain
	OSCI	XTAL	–	Clock input of crystal/ resonator oscillator
P54/PWM2	P54	ST	CMOS	Bidirectional I/O pin with programmable open-drain
	PWM2	–	CMOS	PWM2 output
P55/PWM3	P55	ST	CMOS	Bidirectional I/O pin with programmable open-drain
	PWM3	–	CMOS	PWM3 output
P56/TCC	P56	ST	CMOS	Bidirectional I/O pin with programmable open-drain
	TCC	ST	–	Real Time Clock/Counter clock input
P57/ADC13	P57	ST	CMOS	Bidirectional I/O pin with programmable open-drain
	ADC13	AN	–	ADC Input 13
P60/ADC0	P60	ST	CMOS	Bidirectional I/O pin with programmable pull-down and pin change wakeup
	ADC0	AN	–	ADC Input 0
P61/ADC1	P61	ST	CMOS	Bidirectional I/O pin with programmable pull-down and pin change wakeup
	ADC1	AN	–	ADC Input 1
P62/ADC2	P62	ST	CMOS	Bidirectional I/O pin with programmable pull-down and pin change wakeup
	ADC2	AN	–	ADC Input 2
P63/ADC3	P63	ST	CMOS	Bidirectional I/O pin with programmable pull-down and pin change wakeup
	ADC3	AN	–	ADC Input 3

Name	Function	Input Type	Output Type	Description
P70/ADC14	P70	ST	CMOS	Bidirectional I/O pin
	ADC14	AN	–	ADC Input 14
P71/INT1	P71	ST	CMOS	Bidirectional I/O pin
	/INT1	ST	–	External interrupt Pin 1
P72/ADC10	P72	ST	CMOS	Bidirectional I/O pin
	ADC10	AN	–	ADC Input 10
P73/ADC11	P73	ST	CMOS	Bidirectional I/O pin
	ADC11	AN	–	ADC Input 11
P74	P74	ST	CMOS	Bidirectional I/O pin
P75/ADC8	P75	ST	CMOS	Bidirectional I/O pin
	ADC8	AN	–	ADC Input 8
P76/ADC9	P76	ST	CMOS	Bidirectional I/O pin
	ADC9	AN	–	ADC Input 9
P77/INT0	P77	ST	CMOS	Bidirectional I/O pin
	/INT0	ST	–	External interrupt pin 0
P80/ADC12	P80	ST	CMOS	Bidirectional I/O pin
	ADC12	AN	–	ADC Input 12
/RESET	/RESET	ST	–	Reset pin
VDD	VDD	Power	–	Power
VSS	VSS	Power	–	Ground

4.2 EM78P349NK28/SO28

Name	Function	Input Type	Output Type	Description
P50/VREF	P50	ST	CMOS	Bidirectional I/O pin with programmable pull-high and open-drain
	VREF	AN	–	ADC external voltage reference
P51/PWM1	P51	ST	CMOS	Bidirectional I/O pin with programmable pull-high and open-drain
	PWM1	–	CMOS	PWM1 output
P52/OSCO	P52	ST	CMOS	Bidirectional I/O pin with programmable pull-high and open-drain
	OSCO	–	XTAL	Clock output of crystal/ resonator oscillator
P53/OSCI	P53	ST	CMOS	Bidirectional I/O pin with programmable pull-high and open-drain
	OSCI	XTAL	–	Clock input of crystal/ resonator oscillator
P54/PWM2	P54	ST	CMOS	Bidirectional I/O pin with programmable open-drain
	PWM2	–	CMOS	PWM2 output
P55/PWM3	P55	ST	CMOS	Bidirectional I/O pin with programmable open-drain
	PWM3	–	CMOS	PWM3 output
P56/TCC	P56	ST	CMOS	Bidirectional I/O pin with programmable open-drain
	TCC	ST	–	Real Time Clock/Counter clock input
P57/ADC13	P57	ST	CMOS	Bidirectional I/O pin with programmable open-drain
	ADC13	AN	–	ADC Input 13
P60/ADC0	P60	ST	CMOS	Bidirectional I/O pin with programmable pull-down, and pin change wakeup
	ADC0	AN	–	ADC Input 0
P61/ADC1	P61	ST	CMOS	Bidirectional I/O pin with programmable pull-down, and pin change wakeup
	ADC1	AN	–	ADC Input 1
P62/ADC2	P62	ST	CMOS	Bidirectional I/O pin with programmable pull-down, and pin change wakeup
	ADC2	AN		ADC Input 2
P63/ADC3	P63	ST	CMOS	Bidirectional I/O pin with programmable pull-down, and pin change wakeup
	ADC3	AN	–	ADC Input 3
P64/ADC4	P64	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, and pin change wakeup
	ADC4	AN	–	ADC Input 4

Name	Function	Input Type	Output Type	Description
P65/ADC5	P65	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, and pin change wakeup
	ADC5	AN	–	ADC Input 5
P66/ADC6	P66	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, and pin change wakeup
	ADC6	AN	–	ADC Input 6
P67/ADC7	P67	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, and pin change wakeup
	ADC7	AN	–	ADC Input 7
P70/ADC14	P70	ST	CMOS	Bidirectional I/O pin
	ADC14	AN	–	ADC Input 14
P71/INT1	P71	ST	CMOS	Bidirectional I/O pin
	/INT1	ST	–	External interrupt Pin 1
P72/ADC10	P72	ST	CMOS	Bidirectional I/O pin
	ADC10	AN	–	ADC Input 10
P73/ADC11	P73	ST	CMOS	Bidirectional I/O pin
	ADC11	AN	–	ADC Input 11
P74	P74	ST	CMOS	Bidirectional I/O pin
P75/ADC8	P75	ST	CMOS	Bidirectional I/O pin
	ADC8	AN	–	ADC Input 8
P76/ADC9	P76	ST	CMOS	Bidirectional I/O pin
	ADC9	AN	–	ADC input 9
P77/INT0	P77	ST	CMOS	Bidirectional I/O pin
	/INT0	ST	–	External interrupt Pin 0
P80/ADC12	P80	ST	CMOS	Bidirectional I/O pin
	ADC12	AN	–	ADC Input 12
/RESET	/RESET	ST	–	Reset pin
VDD	VDD	Power	–	Power
VSS	VSS	Power	–	Ground

5 Block Diagram

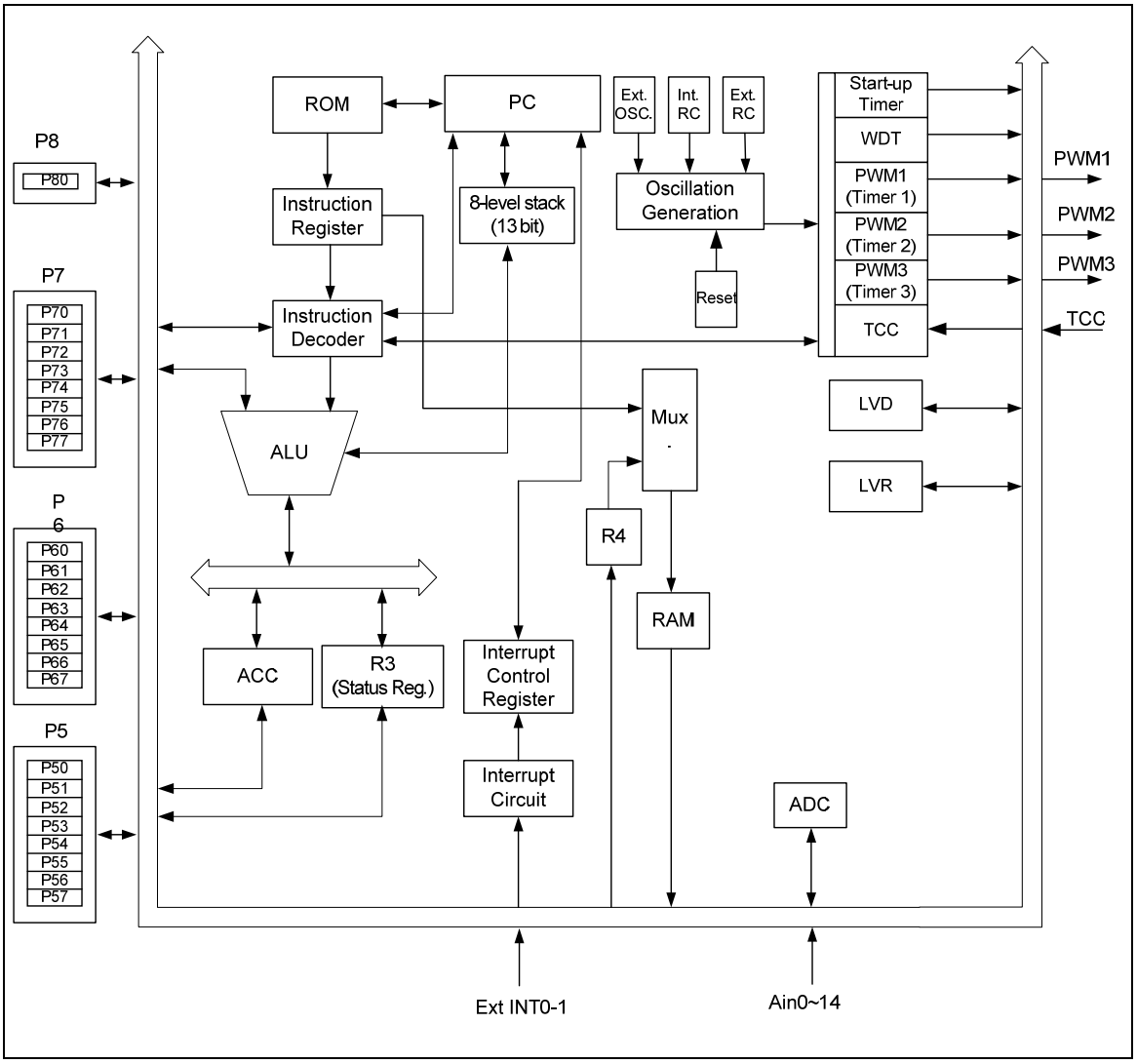


Figure 5 Functional Block Diagram of EM78P349N

6 Functional Description

6.1 Operational Registers

6.1.1 A (Accumulator)

Internal data transfer operation, or instruction operand holding usually involves the temporary storage function of the Accumulator. The Accumulator is not an addressable register.

6.1.2 CONT (Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTE	INT	TS	TE	PSTE	PST2	PST1	PST0

Bit 7 (INTE): INT signal edge

0 : interrupt occurs at a rising edge on the INT pin

1 : interrupt occurs at a falling edge on the INT pin

Bit 6 (INT): Interrupt Enable flag

0 : masked by DISI or hardware interrupt

1 : enabled by the ENI/RETI instructions

This bit is readable only.

Bit 5 (TS): TCC signal source

0 : internal instruction cycle clock. If P57 is used as I/O pin, TS must be 0.

1 : transition on the TCC pin

Bit 4 (TE): TCC signal edge

0 : increment if the transition from low to high takes place on the TCC pin

1 : increment if the transition from high to low takes place on the TCC pin.

Bit 3 (PSTE): Prescaler enable bit for TCC

0 : prescaler disable bit. The TCC rate is 1:1

1 : prescaler enable bit. The TCC rate is set at Bit 2 ~ Bit 0.

Bit 2 ~ Bit 0 (PST2 ~ PST0): TCC prescaler bits

PST2	PST1	PST0	TCC Rate
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

Note: Tcc time-out period [1/Fosc x prescaler × 256 (Tcc cnt) × 1 (CLK=2)]
Tcc time-out period [1/Fosc x prescaler × 256 (Tcc cnt) × 2 (CLK=4)]

6.1.3 R0 (Indirect Address Register)

R0 is not a physically implemented register. Its major function is to perform as an indirect address pointer. Any instruction using R0 as a pointer, actually accesses the data pointed by the RAM Select Register (R4).

6.1.4 R1 (Memory Switch Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
"0"	"0"	"0"	PS0	"0"	BS2	BS1	BS0

Bit 4 (PS0): readable only and used to get which page the program counter is.

Bit 2 ~ Bit 0 (BS2 ~ BS0): used to select Banks 0 ~ 4.

6.1.5 R2 (Program Counter) and Stack

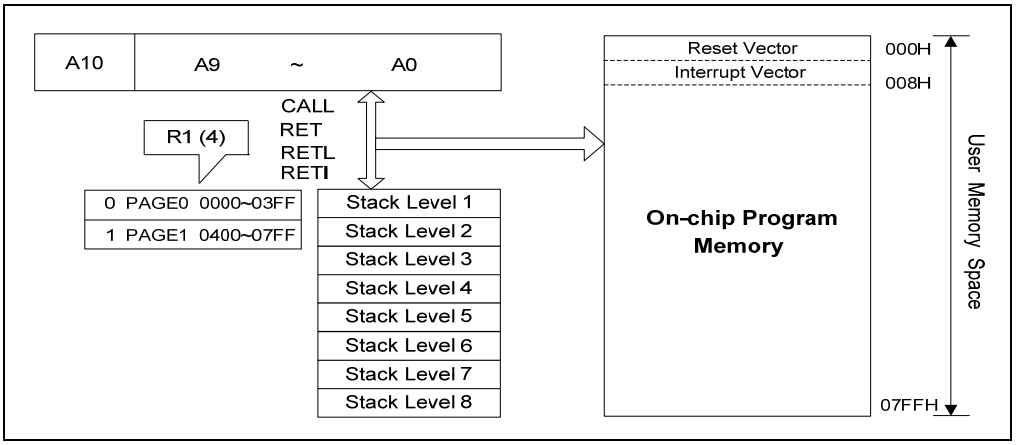


Figure 6-1 Program Counter Organization

- R2 and hardware stacks are 11-bit wide. The structure is depicted in the table under Section 6.1.5.1 *Data Memory Configuration* (next section).
- The configuration structure generates 2K×13 bits on-chip ROM addresses to the relative programming instruction codes. One program page is 1024 words long.
- The contents of R2 are all set to "0"s when a reset condition occurs.
- "JMP" instruction allows direct loading of the lower 10 program counter bits. Thus, "JMP" allows PC to jump to any location within a page (1K).
- "CALL" instruction loads the lower 10 bits of the PC and PC+1 are pushed onto the stack. Thus, the subroutine entry address can be located anywhere within a page (1K).
- "LJMP" instruction allows direct loading of the lower 11 program counter bits. Therefore, "LJMP" allows PC to jump to any location within 2K (2^{11}).
- "LCALL" instruction loads the lower 11 bits of the PC and PC+1 are pushed onto the stack. Thus, the subroutine entry address can be located anywhere within 2K (2^{11}).

- "RET" ("RETL k", "RETI") instruction loads the program counter with the contents of the top of the stack.
- "ADD R2, A" allows a relative address to be added to the current PC, and the ninth and above bits of the PC will increase progressively.
- "MOV R2, A" allows loading of an address from the "A" register to the lower 8 bits of the PC, and the ninth and tenth bits (A8 ~ A9) of the PC will remain unchanged.
- Any instruction (except "ADD R2, A") that is written to R2 (e.g., "MOV R2, A", "BC R2, 6" etc.) will cause the ninth bit and the tenth bit (A8 ~ A9) of the PC to remain unchanged.
- All instructions are single instruction cycle (fclk/2) except "LCALL" and "LJMP" instructions. The "LCALL" and "LJMP" instructions need two instructions cycle.

6.1.5.1 Data Memory Configuration

Address	Bank 0 Registers	Bank 1 Registers	Bank 2 Registers	Bank 3 Registers	Bank 4 Registers
00	**R0** (Indirect Addressing Register)				
01	**R1** (Memory Switch Register)				
02	**R2** (Program Counter)				
03	**R3** (Status Register)				
04	**R4** (Select Indirect Address)				
05	**R5** (Port 5)	**R5** (I/O Port Control Register)	**R5** (PRD1**:** PWM1 time period)	**R5** (Time Clock / Counter)	Reserve
06	**R6** (Port 6)	**R6** (I/O Port Control Register)	**R6** (PRD2**:** PWM2 time period)	Reserve	Reserve
07	**R7** (Port 7)	**R7** (I/O Port Control Register)	**R7** (PRD3**:** PWM3 time period)	Reserve	Reserve
08	**R8** (Port 8)	**R8** (I/O Port Control Register)	**R8** (DT1L**:**Duty cycle of PWM1)	Reserve	Reserve
09	**R9** (ADC Control Register)	**R9** (Timer Control Register 1)	**R9** (DT2L**:** Duty cycle of PWM2)	Reserve	Reserve
0A	**RA** (ADC Offset Calibration Register)	**RA**(Timer Control Register 2)	**RA** (DT3L**:** Duty cycle of PWM3)	Reserve	Reserve
0B	**RB** (ADDATA1H**:** ADC data Bit 11~Bit 4)	**RB** (Pull-down Control Register)	**RB** (DTH**:** Duty cycle of PWM)	Reserve	Reserve
0C	**RC** (ADDATA1L**:** ADC data Bit 3~Bit 0)	**RC**(Open-drain Control Register)	**RC** (PDH**:** Period cycle of PWM)	Reserve	Reserve
0D	**RD** (ADC Input Select Register)	**RD** (Pull-high Control Register)	**RD** (PWM Control Register)	Reserve	Reserve
0E	**RE** (Wake-up Control Register)	**RE** (WDT Control Register)	Reserve	Reserve	Reserve
0F	**RF** (Interrupt Status Register)	**RF** (Interrupt Mask Register)	Reserve	Reserve	Reserve
10 : 1F	General Registers (16×8 bits)				
20 : 3F	General Registers (32×8 bits)	General Registers (32×8 bits)	General Registers (32×8 bits)	General Registers (32×8 bits)	General Registers (32×8 bits)

6.1.6 R3 (Status Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
–	–	–	T	P	Z	DC	C

Bit 4 (T): Time-out bit. Set to 1 by the "SLEP" and "WDTC" commands or during power-on and reset to 0 by WDT time-out.

Bit 3 (P): Power-down bit. Set to 1 during power-on or by a "WDTC" command and reset to 0 by a "SLEP" command.

NOTE

Bit 4 and Bit 3 (T and P) are read only.

Bit 2 (Z): Zero flag. Set to "1" if the result of an arithmetic or logic operation is zero.

Bit 1 (DC): Auxiliary carry flag

Bit 0 (C): Carry flag

6.1.7 R4 (RAM Select Register)

Bit 5 ~ Bit 0: used to select registers (Address**:** 00 ~ 3F) in the indirect address mode.

6.1.8 Bank 0-R5 ~ R7 (Port 5 ~ Port 7)

R5, R6 and R7 are I/O registers.

6.1.9 Bank 0-R8 (Port 8)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LVDEN	/LVD	NREN	“0”	“0”	“0”	“0”	P80

Bit 7 (LVDEN): Low Voltage Detector Enable bits.

0 : Low voltage detector disabled.

1 : Low voltage detector enabled.

Bit 6 (/LVD): Low Voltage Detector state. This is a read only bit. When the VDD pin voltage is lower than the LVD voltage interrupt level (selected by LVD1 and LVD0), this bit will be cleared.

0 : Low voltage is detected.

1 : Low voltage is not detected or LVD function is disabled.

Bit 5 (NREN): Noise Rejection Enable

0 : Disable noise rejection

1 : Enable noise rejection (default). However, under Low XTAL oscillator (LXT) mode, the noise rejection circuit is always disabled.

Bit 0 (P80): P80 control register

6.1.10 Bank 0-R9 (ADCON: ADC Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
VREFS	CKR1	CKR0	ADRUN	ADIS3	ADIS2	ADIS1	ADIS0

Bit 7 (VREFS): The input source of the Vref of the ADC

0 : The Vref of the ADC is connected to Vdd (default value), and the P50/VREF pin carries out the function of P50

1 : The Vref of the ADC is connected to P50/VREF

NOTE

The P50/REF pin priority is as follows:

High	Low
VREF	P50

Bit 6 and Bit 5 (CKR1 and CKR0): The prescaler of oscillator clock rate of ADC

00 = 1**:** 16 (default value)

01 = 1**:** 4

10 = 1**:** 64

11 = 1**:** 8

CKR1 : CKR0	Operation Mode	Max. Operation Frequency
00	Fosc/16	4 MHz
01	Fosc/4	1 MHz
10	Fosc/64	16 MHz
11	Fosc/8	2 MHz

Bit 4 (ADRUN): ADC starts to RUN.

0 : Reset upon completion of the conversion. This bit **cannot** be reset through software.

1 : AD conversion is started. This bit can be set by software

Bit 3 ~ Bit 0 (ADIS3 ~ ADIS0): Analog Input Select

0000 : ADIN0/P60

0001 : ADIN1/P61

0010 : ADIN2/P62

0011 : ADIN3/P63

0100 : ADIN4/P64

0101 : ADIN5/P65

0110 : ADIN6/P66

0111 : ADIN7/P67

1000 : ADIN8/P75

1001 : ADIN9/P76

1010 : ADIN10/P72

1011 : ADIN11/P73

1100 : ADIN12/P80

1101 : ADIN13/P57

1110 : ADIN14/P70

These bits can only be changed when the ADIF bit (See Section 6.1.14) and the ADRUN bits are both low.

NOTE

The ADIN12~ 14 of the AD input channels cannot be simulated in ICE349. The ICE349 only supports 12-bit multi-channel Analog-to-Digital Converter.

6.1.11 Bank 0-RA (ADOC: ADC Offset Calibration Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CALI	SIGN	VOF[2]	VOF[1]	VOF[0]	ADPD	LVD1	LVD0

Bit 7 (CALI): Calibration enable bit for ADC offset

0 : Calibration is disabled

1 : Calibration is enabled

Bit 6 (SIGN): Polarity bit of the offset voltage

0 : Negative voltage

1 : Positive voltage

Bit 5 ~ Bit 3 (VOF[2] ~ VOF[0]): Offset voltage bits

VOF[2]	VOF[1]	VOF[0]	Offset Level
0	0	0	0 LSB
0	0	1	2 LSB
0	1	0	4 LSB
0	1	1	6 LSB
1	0	0	8 LSB
1	0	1	10 LSB
1	1	0	12 LSB
1	1	1	14 LSB

Bit 2 (ADPD): ADC Power-down mode

0 : Switch off the resistor reference to save power even while the CPU is operating.

1 : ADC is operating

Bits 1~0 (LVD1: 0): Low Voltage Detector level bits.

LVDEN <R8, 7>	LVD1, LVD0 <RA, 1, 0>	LVD Voltage Interrupt Level	LVDIF
1	11	2.2V	1*
1	10	3.3V	1*
1	01	4.0V	1*
1	00	4.5V	1*
0	××	NA	0

* If Vdd has crossover at LVD voltage interrupt level as Vdd changes, LVDIF =1.

6.1.12 Bank 0-RB (ADDATA1H: Converted Value of ADC)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AD11	AD10	AD9	AD8	AD7	AD6	AD5	AD4

When the AD conversion is completed, the result is loaded into the ADDATA1H. The ADRUN bit is cleared, and the ADIF (see Section 6.1.14) is set.

RB is read only.

6.1.13 Bank 0-RC (ADDATA1L: ADC Converted Value)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADE11	ADE10	ADE9	ADE8	AD3	AD2	AD1	AD0

Bit 7 (ADE11): AD converter enable bit of P73 pin

0 : Disable ADC11, P73 acts as I/O pin

1 : Enable ADC11 to act as analog input pin

Bit 6 (ADE10): AD converter enable bit of P72 pin

0 : Disable ADC10, P72 acts as I/O pin

1 : Enable ADC10 to act as analog input pin

Bit 5 (ADE9): AD converter enable bit of P76 pin

0 : Disable ADC9, P76 acts as I/O pin

1 : Enable ADC9 to act as analog input pin

Bit 4 (ADE8): AD converter enable bit of P75 pin

0 : Disable ADC8, P75 acts as I/O pin

1 : Enable ADC8 to act as analog input pin

Bit 3 ~ Bit 0 (AD3~0): When AD conversion is completed, the result is loaded into the ADDATA1L. The ADRUN bit is cleared, and the ADIF (see Section 6.1.14) is set.

6.1.14 Bank 0-RD (AISR: ADC Input Select Register)

The AISR register individually defines the pins of Port 6 as analog input or as digital I/O.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADE7	ADE6	ADE5	ADE4	ADE3	ADE2	ADE1	ADE0

Bit 7 (ADE7): AD converter enable bit of P67 pin

0 : Disable ADC7, P67 acts as I/O pin

1 : Enable ADC7 to act as analog input pin

Bit 6 (ADE6): AD converter enable bit of P66 pin

0 : Disable ADC6, P66 acts as I/O pin

1 : Enable ADC6 to act as analog input pin

Bit 5 (ADE5): AD converter enable bit of P65 pin

0 : Disable ADC5, P65 acts as I/O pin

1 : Enable ADC5 to act as analog input pin

Bit 4 (ADE4): AD converter enable bit of P64 pin

0 : Disable ADC4, P64 acts as I/O pin

1 : Enable ADC4 to act as analog input pin

Bit 3 (ADE3): AD converter enable bit of P63 pin

0 : Disable ADC3, P63 acts as I/O pin

1 : Enable ADC3 to act as analog input pin

Bit 2 (ADE2): AD converter enable bit of P62 pin

0 : Disable ADC2, P62 acts as I/O pin

1 : Enable ADC2 to act as analog input pin

Bit 1 (ADE1): AD converter enable bit of P61 pin

0 : Disable ADC1, P61 acts as I/O pin

1 : Enable ADC1 to act as analog input pin

Bit 0 (ADE0): AD converter enable bit of P60 pin

0 : Disable ADC0, P60 acts as I/O pin

1 : Enable ADC0 to act as analog input pin

6.1.15 Bank 0-RE (WUCR: Wake-up Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
"0"	LVDIF	LVDWE	ICWE	ADWE	ADE14	ADE13	ADE12

NOTE

- *Bank 0-RE <6> "1" means with interrupt request; "0" means no interrupt occurs.*
- *Bank 0-RE <6>can be cleared by instruction but cannot be set.*
- *Bank 1-RE <6> is the interrupt mask register.*
- *Reading Bank 0-RE <6> will result to "logic AND" of Bank 0-RE <6> and Bank 0-RE <6>*

Bit 6 (LVDIF): Low Voltage Detector Interrupt flag.

LVDIF is reset to "0" by software or hardware.

LVDEN Bank 0 <R8, 7>	LVD1, LVD0 <RA, 1, 0>	LVD Voltage Interrupt level	LVDIF
1	11	Vdd ≤ 2.2V	1
		Vdd > 2.2V	0
1	10	Vdd ≤ 3.3V	1
		Vdd > 3.3V	0
1	01	Vdd ≤ 4.0V	1
		Vdd > 4.0V	0
1	00	Vdd ≤ 4.5V	1
		Vdd > 4.5V	0
0	××	NA	0

Bit 5 (LVDWE): Low Voltage Detect wake-up enable bit.

0 : Disable Low Voltage Detect wake-up.

1 : Enable Low Voltage Detect wake-up.

When Low Voltage Detect is used to enter an interrupt vector or to wake-up the EM78P349N from sleep with Low Voltage Detect running, the LVDWE bit must be set to "Enable".

Bit 4 (ICWE): Port 6 input change wake-up status enable bit

0 : Disable Port 6 input change wake-up status

1 : Enable Port 6 input change wake-up status

When Port 6 Input Status Change is used to enter an interrupt vector or to wake-up the EM78P349N from sleep, the ICWE bit must be set to "Enable".

Bit 3 (ADWE): ADC wake-up enable bit

0 : Disable ADC wake-up

1 : Enable ADC wake-up

When ADC Complete is used to enter an interrupt vector or to wake-up the EM78P349N from sleep with AD conversion running, the ADWE bit must be set to "Enable".

Bit 2 (ADE14): AD converter enable bit of P70 pin

0 : Disable ADC14, P70 acts as I/O pin

1 : Enable ADC14 to act as analog input pin

Bit 1 (ADE13): AD converter enable bit of P57 pin

0 : Disable ADC13, P57 acts as I/O pin

1 : Enable ADC13 to act as analog input pin

Bit 0 (ADE12): AD converter enable bit of P80 pin

0 : Disable ADC12, P80 acts as I/O pin

1 : Enable ADC12 to act as analog input pin

6.1.16 Bank 0-RF (Interrupt Status Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EX1IF	PWM3IF	PWM2IF	PWM1IF	ADIF	EX0IF	ICIF	TCIF

NOTE

- *"1" means with interrupt request; "0" means no interrupt occurs.*
- *Bank 0-RF can be cleared by instruction but cannot be set.*
- *Bank 1-RF is the interrupt mask register.*
- *Reading Bank 0-RF will result to "logic AND" of Bank 0-RF and BANK 1-RF.*

Bit 7 (EX1IF): External interrupt flag. Set by INT1 pin. Reset by software.

Bit 6 (PWM3IF): PWM3 (Pulse Width Modulation) interrupt flag. Set when a selected duration is reached. Reset by software.

Bit 5 (PWM2IF): PWM2 (Pulse Width Modulation) interrupt flag. Set when a selected duration is reached. Reset by software.

Bit 4 (PWM1IF): PWM1 (Pulse Width Modulation) interrupt flag. Set when a selected duration is reached. Reset by software.

Bit 3 (ADIF): Interrupt flag for analog-to-digital conversion. Set when AD conversion is completed. Reset by software.

Bit 2 (EX0IF): External interrupt flag. Set by INT0 pin. Reset by software.

Bit 1 (ICIF): Port 6 input status change interrupt flag. Set when Port 6 input changes. Reset by software.

Bit 0 (TCIF): TCC overflow interrupt flag. Set when TCC overflows. Reset by software.

6.1.17 Bank 1-R5 ~R7 (I/O Port Control Register)

"**1**" puts the relative I/O pin into high impedance, while "**0**" defines the relative I/O pin as output. **Bank 1-R5**, **Bank 1-R6**, and **Bank 1-R7** registers are all readable and writable.

6.1.18 Bank 1-R8 (I/O Port Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
–	–	–	–	–	–	–	C80

Bit 0 (C80): **"1"** puts the relative I/O pin into high impedance, while **"0"** defines the relative I/O pin as output. They are both readable and writable.

6.1.19 Bank 1-R9 (TMRCON: Timer Control Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
T3EN	T2EN	T3P2	T3P1	T3P0	T2P2	T2P1	T2P0

Bit 7 (T3EN): TMR3 enable bit

0 : TMR3 is off (default value)

1 : TMR3 is on

Bit 6 (T2EN): TMR2 enable bit

0 : TMR2 is off (default value)

1 : TMR2 is on

Bit 5 ~ Bit 3 (T3P2 ~ T3P0): TMR3 clock prescaler option bits

T3P2	T3P1	T3P0	Prescale
0	0	0	1:1 (default)
0	0	1	1:2
0	1	0	1:4
0	1	1	1:8
1	0	0	1:16
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

Bit 2 ~ Bit 0 (T2P2 ~ T2P0): TMR2 clock prescaler option bits

T2P2	T2P1	T2P0	Prescale
0	0	0	1:1 (default)
0	0	1	1:2
0	1	0	1:4
0	1	1	1:8
1	0	0	1:16
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

6.1.20 Bank 1-RA (TMRCON: Timer Control Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EIS1	EIS0	–	–	T1EN	T1P2	T1P1	T1P0

Bit 7 (EIS1): Control bit used to define the function of the P71 (/INT1) pin

0 : P71, normal I/O pin

1 : /INT1, external interrupt pin. In this case, the I/O control bit of P71 (Bit 1 of Bank 1-R7) must be set to "1".

Bit 6 (EIS0): Control bit used to define the function of the P77 (/INT0) pin

0 : P77, normal I/O pin

1 : /INT0, external interrupt pin. In this case, the I/O control bit of P77 (Bit 7 of Bank 1-R7) must be set to "1".

NOTE

- *When EIS is "0," the path of /INT is masked. When EIS is "1," the status of the /INT pin can also be read by way of reading Port 7 (BANK0-R7). Refer to Figure 6-4 (I/O Port and I/O Control Register Circuit for P77 (/INT0) and P71 (/INT1) in Section 6.3 (I/O Ports).*
- *EIS is both readable and writable.*

Bit 3 (T1EN): TMR1 enable bit

0 : TMR1 is off (default value)

1 : TMR1 is on

Bit 2 ~ Bit 0 (T1P2 ~ T1P0): TMR1 clock prescale option bits

T3P2	T3P1	T3P0	Prescale
0	0	0	1:1 (default)
0	0	1	1:2
0	1	0	1:4
0	1	1	1:8
1	0	0	1:16
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

6.1.21 Bank 1-RB (Pull-down Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/PD7	/PD6	/PD5	/PD4	/PD3	/PD2	/PD1	/PD0

IOCB0 register is both readable and writable

Bit 7 (/PD7): Control bit used to enable internal pull-down of the P67 pin

0 : Enable internal pull-down

1 : Disable internal pull-down

Bit 6 (/PD6): Control bit used to enable internal pull-down of the P66 pin.

Bit 5 (/PD5): Control bit used to enable internal pull-down of the P65 pin.

Bit 4 (/PD4): Control bit used to enable internal pull-down of the P64 pin.

Bit 3 (/PD3): Control bit used to enable internal pull-down of the P63 pin.

Bit 2 (/PD2): Control bit used to enable internal pull-down of the P62 pin.

Bit 1 (/PD1): Control bit used to enable internal pull-down of the P61 pin.

Bit 0 (/PD0): Control bit used to enable internal pull-down of the P60 pin.

6.1.22 Bank 1-RC (Open-drain Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/OD7	/OD6	/OD5	/OD4	/OD3	/OD2	/OD1	/OD0

IOCC0 register is both readable and writable.

Bit 7 (OD7): Control bit used to enable open-drain output of the P57 pin.

0 : Enable open-drain output

1 : Disable open-drain output

Bit 6 (OD6): Control bit used to enable open-drain output of the P56 pin.

Bit 5 (OD5): Control bit used to enable open-drain output of the P55 pin.

Bit 4 (OD4): Control bit used to enable open-drain output of the P54 pin.

Bit 3 (OD3): Control bit used to enable open-drain output of the P53 pin.

Bit 2 (OD2): Control bit used to enable open-drain output of the P52 pin.

Bit 1 (OD1): Control bit used to enable open-drain output of the P51 pin.

Bit 0 (OD0): Control bit used to enable open-drain output of the P50 pin.

6.1.23 Bank 1-RD (Pull-high Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/PH7	/PH6	/PH5	/PH4	/PH3	/PH2	/PH1	/PH0

IOCD0 register is both readable and writable.

Bit 7 (/PH7): Control bit used to enable internal pull-high of the P67 pin.

0 : Enable internal pull-high

1 : Disable internal pull-high

Bit 6 (/PH6): Control bit used to enable internal pull-high of the P66 pin.

Bit 5 (/PH5): Control bit used to enable internal pull-high of the P65 pin.

Bit 4 (/PH4): Control bit used to enable internal pull-high of the P64 pin.

Bit 3 (/PH3): Control bit used to enable internal pull-high of the P53 pin.

Bit 2 (/PH2): Control bit used to enable internal pull-high of the P52 pin.

Bit 1 (/PH1): Control bit used to enable internal pull-high of the P51 pin.

Bit 0 (/PH0): Control bit used to enable internal pull-high of the P50 pin.

6.1.24 Bank 1-RE (WDT Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WDTE	LVDIE	PSWE	PSW2	PSW1	PSW0	”0”	“0”

NOTE

- *Bank 1-RE register is both readable and writable*
- *Individual interrupt is enabled by setting its associated control bit in Bank 1-RE to "1."*
- *Global interrupt is enabled by the ENI instruction and is disabled by the DISI instruction. Refer to Figure 6-8 (Interrupt Input Circuit) under Section 6.5 Interrupt.*

Bit 7 (WDTE): Control bit used to enable the Watchdog Timer

0 : Disable WDT

1 : Enable WDT

WDTE is both readable and writable.

Bit 6 (LVDIE): Low voltage Detector interrupt enable bit.

0 : Disable Low voltage Detector interrupt.

1 : Enable Low voltage Detector interrupt.

When the detect-low-level voltage status is used to enter an interrupt vector or enter next instruction, the LVDIE bit must be set to “Enable“.

Bit 5 (PSWE): Prescaler enable bit for WDT

0 : prescaler disable bit. WDT rate is 1:1

1 : prescaler enable bit. WDT rate is set at Bit 4~Bit 2

Bit 4 ~ Bit 2 (PSW2 ~ PSW0): WDT prescaler bits.

PSW2	PSW1	PSW0	WDT Rate
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

6.1.25 Bank 1-RF (Interrupt Mask Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
"0"	PWM3IE	PWM2IE	PWM1IE	ADIE	EXIE	ICIE	TCIE

NOTE

- *Bank 1-RF register is both readable and writable.*
- *Individual interrupt is enabled by setting its associated control bit in Bank 1-RF to "1."*
- *Global interrupt is enabled by the ENI instruction and is disabled by the DISI instruction. Refer to Figure 6-8 (Interrupt Input Circuit) under Section 6.5 (Interrupt).*

Bit 6 (PWM3IE): PWM3IF interrupt enable bit

0 : Disable PWM3 interrupt

1 : Enable PWM3 interrupt

Bit 5 (PWM2IE): PWM2IF interrupt enable bit

0 : Disable PWM2 interrupt

1 : Enable PWM2 interrupt

Bit 4 (PWM1IE): PWM1IF interrupt enable bit

0 : Disable PWM1 interrupt

1 : Enable PWM1 interrupt

Bit 3 (ADIE): ADIF interrupt enable bit

0 : Disable ADIF interrupt

1 : Enable ADIF interrupt

When ADC Complete is used to enter an interrupt vector or to enter the next instruction, the ADIE bit must be set to "Enable".

Bit 2 (EXIE): EXIF interrupt enable bit

0 : Disable EX0IF/EX1IF interrupt

1 : Enable EX0IF/EX1IF interrupt

Bit 1 (ICIE): ICIF interrupt enable bit

0 : Disable ICIF interrupt

1 : Enable ICIF interrupt

If Port 6 Input Status Change Interrupt is used to enter an interrupt vector (ICIE=1) or to enter next instruction (ICIE=0), the ICIE bit must be set to “Enable“ (“Disable”).

Bit 0 (TCIE): TCIF interrupt enable bit.

0 : Disable TCIF interrupt

1 : Enable TCIF interrupt

6.1.26 Bank 2-R5 (PRD1L: Least Significant Byte of PWM1 Time Period)

The contents of Bank 2-R5 is the time period (time base) of PWM1. The frequency of PWM1 is the reverse of the period. Most Significant Bits (Bits 9, 8) of the Period Cycle of PWM1 in Bank 2-RC<1, 0>.

6.1.27 Bank 2-R6 (PRD2L: Least Significant Byte of PWM2 Time Period)

The contents of Bank 2-R6 is the time period (time base) of PWM2. The frequency of PWM2 is the reverse of the period. Most Significant Bits (Bits 9, 8) of the Period Cycle of PWM2 in Bank 2-RC<3, 2>.

6.1.28 Bank 2-R7 (PRD3L: Least Significant Byte of PWM3 Time Period)

The contents of Bank 2-R7 is the time period (time base) of PWM3. The frequency of PWM3 is the reverse of the period. Most Significant Bits (Bits 9, 8) of the Period Cycle of PWM3 in Bank 2-RC<5, 4>.

6.1.29 Bank 2-R8 (DT1L: Least Significant Byte of PWM1 Duty Cycle)

A specified value keeps the output of PWM1 to remain high until the value matches with TMR1. Most Significant Bits (Bits 9, 8) of Duty Cycle of PWM1 in Bank 2-RB<1, 0>.

6.1.30 Bank 2-R9 (DT2L: Least Significant Byte of PWM2 Duty Cycle)

A specified value keeps the output of PWM2 to remain high until the value matches with TMR2. Most Significant Bits (Bits 9, 8) of Duty Cycle of PWM2 in Bank 2-RB<3, 2>.

6.1.31 Bank 2-RA (DT3L: Least Significant Byte of PWM3 Duty Cycle)

A specified value keeps the output of PWM3 to remain high until the value matches with TMR2. Most Significant Bits (Bits 9, 8) of Duty Cycle of PWM3 in Bank 2-RB<5, 4>.

6.1.32 Bank 2-RB (DTH: Most Significant Bits of PWM Duty Cycle)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
–	–	DT3[9]	DT3[8]	DT2[9]	DT2[8]	DT1[9]	DT1[8]

Bit 5 and Bit 4 (DT3[9], DT3[8]): Most Significant Bits of PWM3 Duty Cycle.

Bit 3 and Bit 2 (DT2[9], DT2[8]): Most Significant Bits of PWM2 Duty Cycle.

Bit 1 and Bit 0 (DT1[9], DT1[8]): Most Significant Bits of PWM1 Duty Cycle.

6.1.33 Bank 2-RC (PRDH: Most Significant Bits of PWM Time Period)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
–	–	PRD3[9]	PRD3[8]	PRD2[9]	PRD2[8]	PRD1[9]	PRD1[8]

Bit 5 and Bit 4 (PRD[9], PRD3[8]): Most Significant Bits of PWM3 period Cycle.

Bit 3 and Bit 2 (PRD2[9], PRD2[8]): Most Significant Bits of PWM2 period Cycle.

Bit 1 and Bit 0 (PRD1[9], PRD1[8]): Most Significant Bits of PWM1 period Cycle.

6.1.34 Bank 2-RD (PWMCON: PWM Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM3E	PWM2E	PWM1E	–	–	–	–	–

Bit 7 (PWM3E): PWM3 enable bit

0 : PWM3 is off (default), and its related pin carries out the P55 function.

1 : PWM3 is on, and its related pin is automatically set to output.

Bit 6 (PWM2E): PWM2 enable bit

0 : PWM2 is off (default), and its related pin carries out the P54 function.

1 : PWM2 is on, and its related pin is automatically set to output.

Bit 5 (PWM1E): PWM1 enable bit

0 : PWM1 is off (default), and its related pin carries out the P51 function;

1 : PWM1 is on, and its related pin is automatically set to output.

6.2 TCC/WDT and Prescaler

There are two 8-bit counters available as prescalers for the TCC and WDT respectively. The PST0 ~ PST2 bits of the CONT register are used to determine the ratio of the TCC prescaler, and the PWR0 ~ PWR2 bits of the Bank 1-RE register are used to determine the prescaler of WDT. The prescaler can be cleared by the instructions and TCC also can be written by the instructions. The WDT and prescaler will be cleared by the "WDTC" and "SLEP" instructions. Figure 6-1 depicts the block diagram of TCC/WDT.

TCC (Bank 3-R5) is an 8-bit timer/counter. The TCC clock source can be the internal clock or an external signal input (edge selectable from the TCC pin). If the TCC signal source is from the internal clock, TCC will increase by 1 per 1 clock (CLKS=0) or 2 clocks (CLKS=1) depending on the CLKS bit of the code option (without prescaler). If the TCC signal source is from an external clock input, TCC will increase by 1 at every falling edge or rising edge of the TCC pin. The TCC pin input time length (kept in High or Low level) must be greater than 1CLK. The TCC will stop running when sleep mode occurs. But when A/D conversion is running and sleep mode occurs, the TCC will keep on running.

The watchdog timer is a free running on-chip RC oscillator. The WDT will keep on running even when the oscillator frequency has been turned off (i.e., in sleep mode). During normal operation or sleep mode, a WDT time-out (if enabled) will cause the device to reset. The WDT can be enabled or disabled at any time during normal mode through software programming. Refer to WDTE bit of Bank 1-RE register. With no prescaler, the WDT time-out duration is approximately 18 ms.[1]

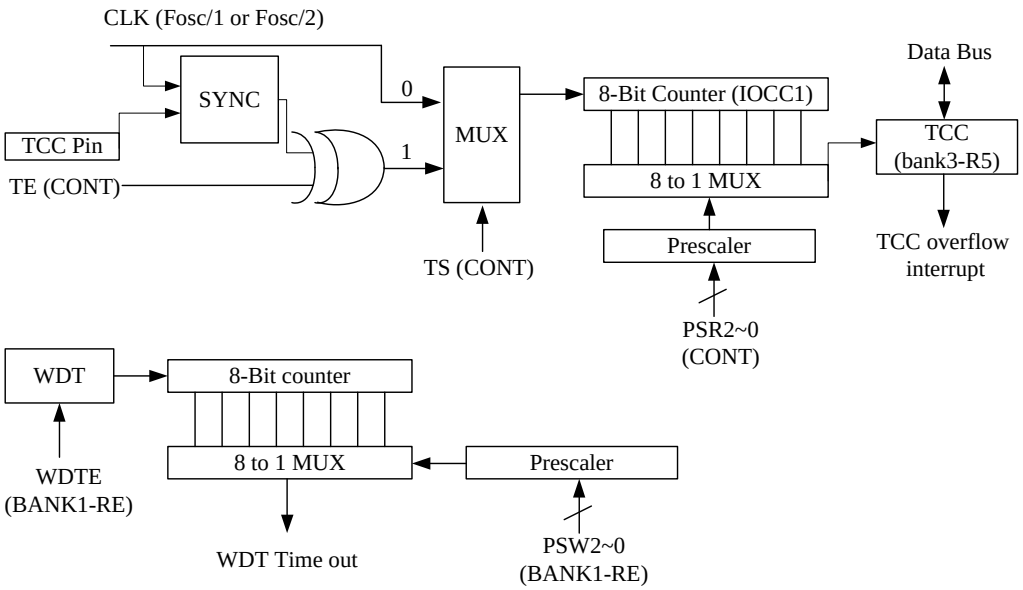
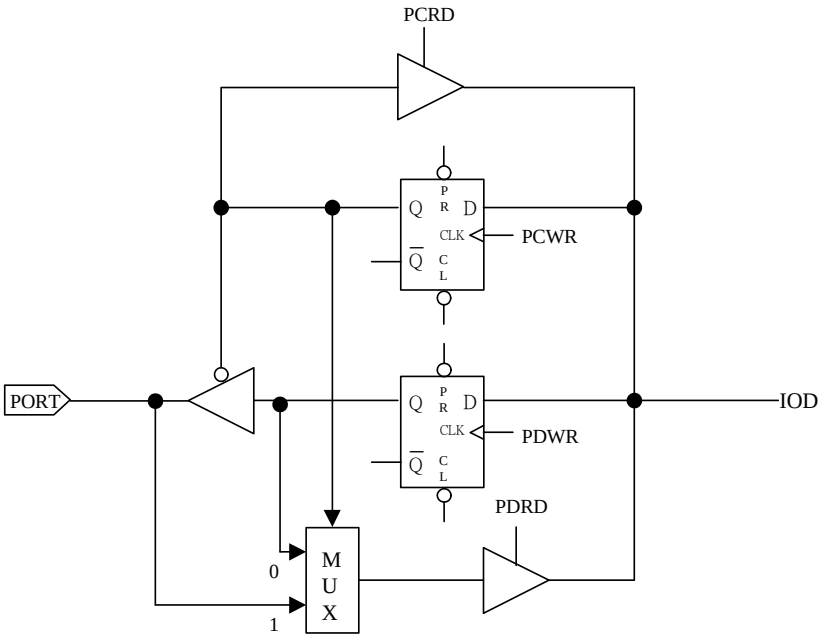


Figure 6-2 TCC and WDT Block Diagram

[1] VDD=5V, Setup time period = 16.5 ms ± 30%.
VDD=3V, Setup time period = 18 ms ± 30%.

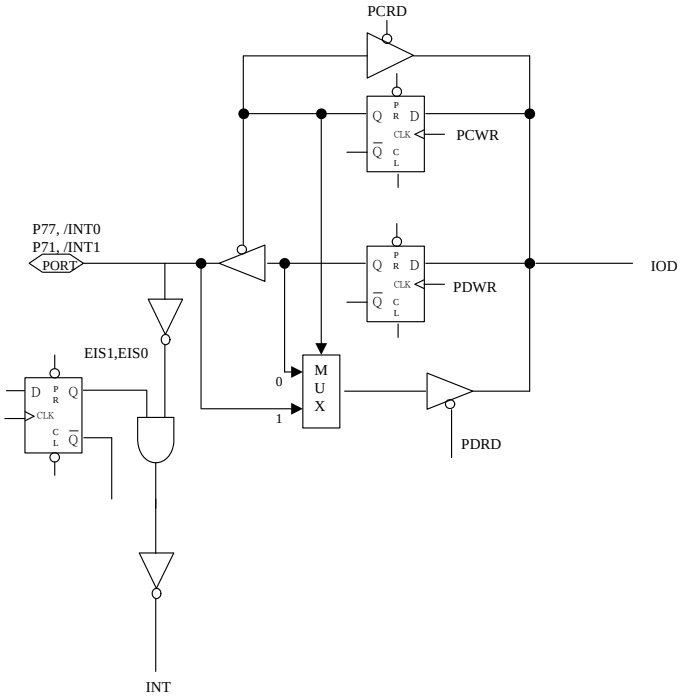
6.3 I/O Ports

The I/O registers (Port 5, Port 6, Port 7 and Port 8) are bidirectional tri-state I/O ports. The Pull-high, Pull-down, and Open-drain functions can be set internally by Bank 1-RB, Bank 1-RC, and Bank 1-RD respectively. Port 6 features an input status change interrupt (or wake-up) function. Each I/O pin can be defined as "input" or "output" pin by the I/O control registers (Bank 1-R5 ~ R8). The I/O registers and I/O control registers are both readable and writable. However, the initial state of these I/Os (Port 5, Port 6, Port 7, Port 8) are unknown input (high impedance). If an I/O pin is pulled to a level by external circuit, the pin must induce a voltage. Hence, it has to be taken into consideration whether the induced voltage causes a wrong action in the beginning of the system. The I/O interface circuits for Ports 5 ~ 8 are illustrated in Figures 6-3, 6-4, and 6-5 respectively. Port 6 with Input Change Interrupt/Wake-up is shown in Figure 6-6.



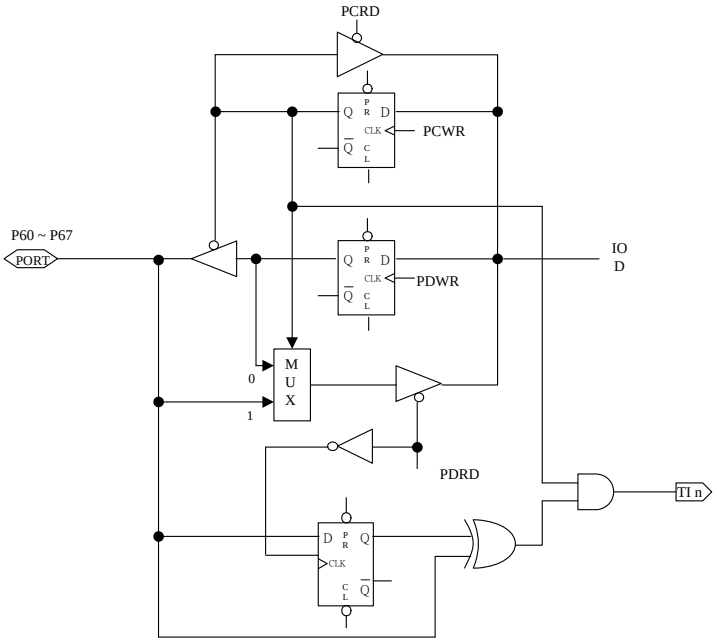
Note: Pull-high and Open-drain are not shown in the figure.

Figure 6-3 I/O Port and I/O Control Register Circuits for Port 5, Port 7 and Port 8



Note: Pull-high and Open-drain are not shown in the figure.

Figure 6-4 I/O Port and I/O Control Register Circuits for P77 (/INT0) and P71 (/INT1)



Note: Pull-high (down) and Open-drain are not shown in the figure.

Figure 6-5 I/O Port and I/O Control Register Circuits for P60~P67

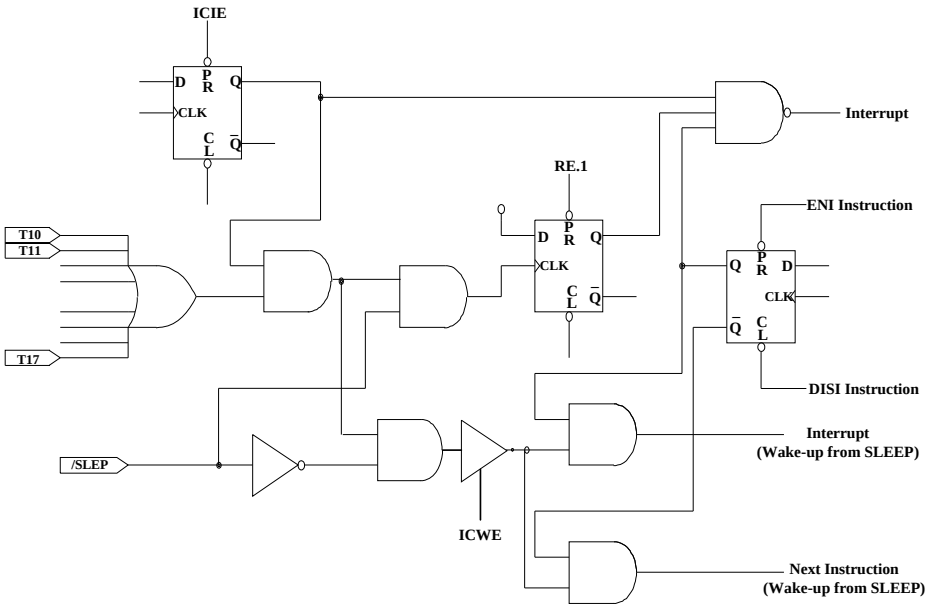


Figure 6-6 Block Diagram of Port 6 with Input changed Interrupt/Wake-up

6.3.1 Usage of Port 6 Input Change Wake-up/Interrupt Function

(1) Wake-up	(2) Wake-up and Interrupt
(a) Before Sleep 1. Disable WDT 2. Read I/O Port 6 (MOV R6,R6) 3. Execute "ENI" or "DISI" 4. Enable wake-up bit (Set ICWE =1) 5. Execute "SLEP" instruction (b) After wake-up → Next instruction	(a) Before Sleep 1. Disable WDT 2. Read I/O Port 6 (MOV R6,R6) 3. Execute "ENI" or "DISI" 4. Enable wake-up bit (Set ICWE =1) 5. Enable interrupt (Set ICIE =1) 6. Execute "SLEP" instruction (b) After wake-up 1. IF "ENI" → Interrupt vector (008H) 2. IF "DISI" → Next instruction

(3) Interrupt
(a) Before Port 6 pin change
1. Read I/O Port 6 (MOV R6,R6)
2. Execute "ENI" or "DISI"
3. Enable interrupt (Set Bank 1-RF ICIE =1)
(b) After Port 6 pin changed (interrupt)
1. IF "ENI" → Interrupt vector (008H)
2. IF "DISI" → Next instruction

6.4 Reset and Wake-up

6.4.1 Reset and Wake-up Function

A reset is initiated by one of the following events :

(1) Power-on reset

(2) /RESET pin input "low", or

(3) WDT time-out (if enabled)

A device is kept in a reset condition for a period of approximately 18 ms after the reset is detected. When in LXT mode, the reset time is 500 ms. Once a reset occurs, the following functions are performed (the initial Address is 000h)

1. The oscillator is running, or will be started (if in sleep mode)
2. The Program Counter (R2) is set to all "0"
3. All I/O port pins are configured as input mode (high-impedance state)
4. The Watchdog Timer and prescaler are cleared
5. When power is switched on, R1 is cleared
6. The CONT register bits are set to all "0" except for Bit 6 (INT flag)

The initial values of all registers are shown in the table.

Executing the “SLEP” instruction will assert the sleep (power down) mode. While entering sleep mode, the Oscillator, TCC, Timer 1, Timer 2 and Timer 3 are stopped. WDT (if enabled) is cleared but keeps on running. During A/D conversion and setting the “SLEP” instruction, the Oscillator, TCC, Timer 1, Timer 2 and Timer 3 keep on running.

The controller can be awakened by:

Case 1 External reset input on the /RESET pin

Case 2 WDT time-out (if enabled)

Case 3 Port 6 input status changes (if ICWE is enabled)

Case 4 AD conversion completed (if ADWE is enabled)

Case 5 Low Voltage Detector (if LVDWE is enabled)

The first two cases (1 and 2) will cause the EM78P349N to reset. The T and P flags of R3 can be used to determine the source of the reset (wake-up). Cases 3, 4, 5 are considered the continuation of program execution and the global interrupt ("ENI" or "DISI" being executed) determines whether or not the controller branches to the interrupt vector following wake-up. If ENI is executed before SLEP, the instruction will begin to execute from Address 0x8 after wake-up. If DISI is executed before SLEP, the execution will restart from the instruction next to SLEP after wake-up. All sleep mode wake-up time is 2 ms, no matter what the oscillator type or mode is (except when it’s in low Crystal mode). In low Crystal mode, wake-up time is 500 ms.

Case [a] WDT is enabled before SLEP and all of the RE bits are disabled. Hence, the EM78P349N can be awakened only with Case 1 or Case 2. Refer to the section on Interrupt (Section 6.5) for further details.

Case [b] If Port 6 Input Status Change is used to wake -up the EM78P349N and the ICWE bit of Bank 0-RE register is enabled before SLEP, WDT must be disabled. Hence, the EM78P349N can be awakened only with Case 3. Wake-up time depends on the oscillator mode. In RC mode the reset time is 32 clocks (for stable oscillators). In High Crystal mode, the reset time is 2 ms and 32 clocks (for stable oscillators), and in low Crystal mode, the reset time is 500 ms.

Case [c] If AD conversion completed is used to wake-up the EM78P349N and the ADWE bit of Bank 0-RE register is enabled before SLEP, WDT must be disabled by software. Hence, the EM78P349N can be awakened only with Case 4. The wake-up time is 15 TAD (ADC clock period). Wake-up time is dependent on the oscillator mode. In RC mode, the reset time is 32 clocks (for stable oscillators). In High Crystal mode, the reset time is 2 ms and 32 clocks (for stable oscillators), and in low Crystal mode, the reset time is 500 ms.

Case [d] If Low voltage detector is used to wake-up the EM78P349N and LVDWE bit of Bank 0-RE register is enabled before SLEP, WDT must be disabled by software. Hence, the EM78P349N can be awakened only with Case 5. Wake-up time is dependent on the oscillator mode. In RC mode, the reset time is 32 clocks (for stable oscillators). In High Crystal mode, reset time is 2 ms and 32 clocks (for stable oscillators); and in low Crystal mode, the reset time is 500 ms.

If Port 6 Input Status Change Interrupt is used to wake up the EM78P349N (as in Case b above), the following instructions must be executed before SLEP:

```
MOV           A, @000110xxb  ; Select WDT prescaler and disable
                             ; WDT
BANK          1
MOV           RE, A
WDTC                         ; Clear WDT and prescaler
BANK          0
MOV           R6, R6         ; Read Port 6
ENI (or DISI)                ; Enable (or disable) global
                             ; interrupt
MOV           A, @xxx1xxxxb  ; Enable Port 6 input change wake-up
                             ; bit
MOV           RE
MOV           A, @00000x1xb  ; Enable Port 6 input change
                             ; interrupt
BANK          1
MOV           RF, A
SLEP                         ; Sleep
```

6.4.2 Status of T, and P of the Status Register

A Reset condition is initiated by one of the following events:

(1) Power-on condition

(2) High-low-high pulse on /RESET pin, or

(3) Watchdog Timer time-out

The values of T and P, as listed in Table 1 below, are used to check how the processor wakes up. Table 2 shows the events, which may affect the status of T and P.

Table 1 Values of RST, T, and P after reset

Reset Type	T	P
Power-on	1	1
/RESET during Operating mode	*P	*P
/RESET wake-up during Sleep mode	1	0
WDT during Operating mode	0	*P
WDT wake-up during Sleep mode	0	0
Wake-up on pin change during Sleep mode	1	0

* P: Previous status before reset

Table 2 Status of RST, T and P being affected by Events

Event	T	P
Power-on	1	1
WDTC instruction	1	1
WDT time-out	0	*P
SLEP instruction	1	0
Wake-up on pin changed during Sleep mode	1	0

* P: Previous value before reset

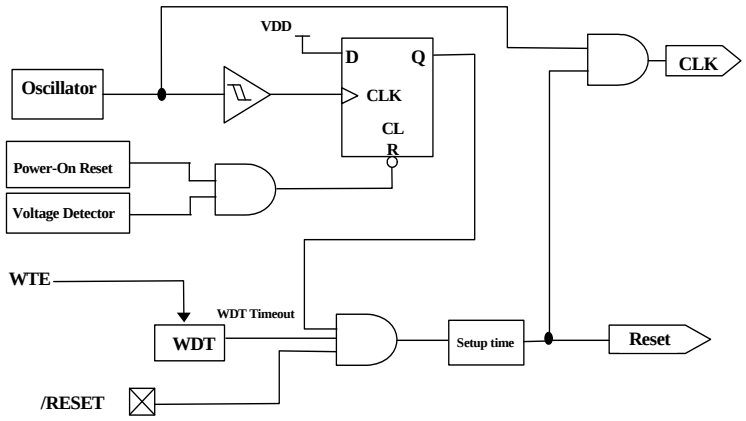


Figure 6-7 Block Diagram of the Reset Controller

6.4.3 Register Initial Values after Reset

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0×05	Bank 1-R5	Bit Name	C57	C56	C55	C54	C53	C52	C51	C50
		Power-on	1	1	1	1	1	1	1	1
		/RESET & WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×06	Bank 1-R6	Bit Name	C67	C66	C65	C64	C63	C62	C61	C60
		Power-on	1	1	1	1	1	1	1	1
		/RESET & WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×07	Bank 1-R7	Bit Name	C77	C76	C75	C74	C73	C72	C71	C70
		Power-on	1	1	1	1	1	1	1	1
		/RESET & WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×08	Bank 1-R8	Bit Name	“0”	“0”	“0”	“0”	“0”	“0”	“0”	C80
		Power-on	0	0	0	0	0	0	0	1
		/RESET & WDT	0	0	0	0	0	0	0	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×09	Bank 1-R9 (TMRCON)	Bit Name	T3EN	T2EN	T3P2	T3P1	T3P0	T2P2	T2P1	T2P0
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0A	Bank 1-RA (TMRCON)	Bit Name	EIS1	EIS0	“0”	“0”	T1EN	T1P2	T1P1	T1P0
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0B	Bank 1-RB	Bit Name	/PD7	/PD6	/PD5	/PD4	/PD3	/PD2	/PD1	/PD0
		Power-on	1	1	1	1	1	1	1	1
		/RESET & WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0C	Bank 1-RC	Bit Name	/OD7	/OD6	/OD5	/OD4	/OD3	/OD2	/OD1	/OD0
		Power-on	1	1	1	1	1	1	1	1
		/RESET & WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0×0D	Bank 1-RD	Bit Name	/PH7	/PH6	/PH5	/PH4	/PH3	/PH2	/PH1	/PH0
		Power-on	1	1	1	1	1	1	1	1
		/RESET & WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0E	Bank 1-RE	Bit Name	WDTE	LVDIE	PSWE	PSW2	PSW1	PSW0	“0”	“0”
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0F	Bank 1-RF	Bit Name	“0”	PMW3IE	PMW2IE	PWM1IE	ADIE	EXIE	ICIE	TCIE
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×05	Bank 2-R5 (PRD1L)	Bit Name	PRD1[7]	PRD1[6]	PRD1[5]	PRD1[4]	PRD1[3]	PRD1[2]	PRD1[1]	PRD1[0]
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×06	Bank 2-R6 (PRD2L)	Bit Name	PRD2[7]	PRD2[6]	PRD2[5]	PRD2[4]	PRD2[3]	PRD2[2]	PRD2[1]	PRD2[0]
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×07	Bank 2-R7 (PRD3L)	Bit Name	PRD3[7]	PRD3[6]	PRD3[5]	PRD3[4]	PRD3[3]	PRD3[2]	PRD3[1]	PRD3[0]
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×08	Bank 2-R8 (DT1L)	Bit Name	DT1[7]	DT1[6]	DT1[5]	DT1[4]	DT1[3]	DT1[2]	DT1[1]	DT1[0]
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×09	Bank 2-R9 (DT2L)	Bit Name	DT2[7]	DT2[6]	DT2[5]	DT2[4]	DT2[3]	DT2[2]	DT2[1]	DT2[0]
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0×0A	Bank 2-RA (DT3L)	Bit Name	DT3[7]	DT3[6]	DT3[5]	DT3[4]	DT3[3]	DT3[2]	DT3[1]	DT3[0]
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	0	P	P
0×0B	Bank 2-RB (DT1H, 2H, 3H)	Bit Name	-	-	DT3[9]	DT3[8]	DT2[9]	DT2[8]	DT1[9]	DT1[8]
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0C	Bank 2-RC (PRDH)	Bit Name	-	-	PRD3[9]	PRD3[8]	PRD2[9]	PRD2[8]	PRD1[9]	PRD1[8]
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0D	Bank 2-RD (PWMCON)	Bit Name	PWM3E	PWM2E	PWM1E	-	-	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	CONT	Bit Name	INTE	INT	TS	TE	PSTE	PST2	PST1	PST0
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×00	R0 (IAR)	Bit Name	-	-	-	-	-	-	-	-
		Power-on	U	U	U	U	U	U	U	U
		/RESET & WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0×01	R1 (MSR)	Bit Name	0	0	0	PS0	0	BS2	BS1	BS0
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×02	R2 (PC)	Bit Name	-	-	-	-	-	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	Jump to Address 0x08 or continue to execute next instruction							
0×03	R3 (SR)	Bit Name	-	-	-	T	P	Z	DC	C
		Power-on	0	0	0	1	1	U	U	U
		/RESET & WDT	0	0	0	t	t	P	P	P
		Wake-up from Pin Change	P	P	P	t	t	P	P	P
0×04	R4 (RSR)	Bit Name	-	-	RS5	RS4	RS3	RS2	RS1	RS0
		Power-on	0	0	U	U	U	U	U	U
		/RESET & WDT	0	0	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×05	Bank 0-R5	Bit Name	P57	P56	P55	P54	P53	P52	P51	P50
		Power-on	U	U	U	U	U	U	U	U
		/RESET & WDT	U	U	U	U	U	U	U	U
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×06	Bank 0-R6	Bit Name	P67	P66	P65	P64	P63	P62	P61	P60
		Power-on	U	U	U	U	U	U	U	U
		/RESET & WDT	U	U	U	U	U	U	U	U
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×07	Bank 0-R7	Bit Name	P77	P76	P75	P74	P73	P72	P71	P70
		Power-on	U	U	U	U	U	U	U	U
		/RESET & WDT	U	U	U	U	U	U	U	U
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×08	Bank 0-R8	Bit Name	LVDEN	/LVD	NREN	-	-	-	-	P80
		Power-on	U	U	U	U	U	U	U	U
		/RESET & WDT	U	U	U	U	U	U	U	U
		Wake-up from Pin Change	P	P	P	P	P	P	P	P

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0×09	Bank 0-R9 (ADCON)	Bit Name	VREFS	CKR1	CKR0	ADRUN	ADIS3	ADIS2	ADIS1	ADIS0
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0A	Bank 0-RA (ADOC)	Bit Name	CALI	SIGN	VOF[2]	VOF[1]	VOF[0]	ADPD	LVD1	LVD0
		Power-on	0	0	0	0	0	0	1	1
		/RESET & WDT	0	0	0	0	0	0	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0B	Bank 0-RB (ADDATA1H)	Bit Name	AD11	AD10	AD9	AD8	AD7	AD6	AD5	AD4
		Power-on	U	U	U	U	U	U	U	U
		/RESET & WDT	U	U	U	U	U	U	U	U
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0C	Bank 0-RC (ADDATA1L)	Bit Name	ADE11	ADE10	ADE9	ADE8	AD3	AD2	AD1	AD0
		Power-on	0	0	0	0	U	U	U	U
		/RESET & WDT	0	0	0	0	U	U	U	U
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0D	Bank 0-RD (AISR)	Bit Name	ADE7	ADE6	ADE5	ADE4	ADE3	ADE2	ADE1	ADE0
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0E	Bank 0-RE (WUCR)	Bit Name	“0”	LVDIF	LVDWE	ICWE	ADWE	ADE14	ADE13	ADE12
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0F	Bank 0-RF (ISR)	Bit Name	EX1IF	PWM3IF	PWM2IF	PWM1IF	ADIF	EX0IF	ICIF	TCIF
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0×10 ~ 0×1F	R10 ~ R1F	Bit Name	-	-	-	-	-	-	-	-
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×20 ~ 0×3F	Bank 0 ~ Bank 3 R20 ~ R3F	Bit Name	-	-	-	-	-	-	-	-
		Power-on	U	U	U	U	U	U	U	U
		/RESET & WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×01	Bank 3-R5 (TCC)	Bit Name	TCC7	TCC6	TCC5	TCC4	TCC3	TCC2	TCC1	TCC0
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×01	Bank 3- R6	Bit Name	C3	C2	C1	C0	RCM1	RCM0	-	-
		Power-on	1	1	1	1	1	1	U	U
		/RESET & WDT	1	1	1	1	1	1	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P

LEGEND:

– : not used.

U : unknown or don't care

t : check "Reset Type" table in Section 6.4.2

P : previous value before reset

6.5 Interrupt

The EM78P349N has six interrupts as listed below:

1. TCC overflow interrupt
2. Port 6 Input Status Change Interrupt
3. External Interrupt INT0, INT1
4. Analog-to-Digital conversion completed interrupt
5. Interrupt when Timer 1 / Timer 2 / Timer 3 match PRD1 / PRD2 / PRD3 respectively
6. Low Voltage Detector Interrupt

Before the Port 6 Input Status Change Interrupt is enabled, reading Port 6 (e.g., "MOV R6, R6") is necessary. Each Port 6 pin will have this feature if its status changes. Port 6 Input Status Change Interrupt will wake up the EM78P349N from sleep mode if it is enabled prior to going into sleep mode by executing SLEP. When wake-up occurs, the controller will continue to execute the succeeding program if the global interrupt is disabled. If enabled, it will branch out to the Interrupt Vector 008H.

The external interrupt has a built-in digital noise rejection circuit (if the input pulse is less than 8 system clock time, then it is eliminated as noise). Edge selection is possible with /INT. Refer to Word 1 Bits 8~7 (Section 6.12, Code Option Register (Word 1)) for digital noise rejection definition.

While power source is still unstable, like when there's external power noise interference or during EMS test condition, situations like that mentioned will cause the power to vibrate fiercely. At the time Vdd is unsettled, the supply voltage may be below the working voltage. When system supply voltage Vdd is below the working voltage, the IC kernel must keep all register status automatically.

Bank 0-RE and Bank 0-RF are the interrupt status register that records the interrupt requests in the relative flags/bits. Bank 1-RE and Bank 1-RF are Interrupt mask registers. The global interrupt is enabled by the ENI instruction and is disabled by the DISI instruction. When one of the interrupts (when enabled) occurs, the next instruction will be fetched from Address 008H. Once into the interrupt service routine, the source of an interrupt can be determined by polling the flag bits in Bank 0-RE and Bank 0-RF. The interrupt flag bit must be cleared by instructions before leaving the interrupt service routine to avoid recursive interrupts.

The flag in the Interrupt Status Register (RF) is set as the corresponding mask bit is enabled. Note that the result of Bank 0-RF will be the logic AND of Bank 0-RF and Bank 1-RF (refer to Figure 6-8) *Interrupt Input Circuit*. The RETI instruction ends the interrupt routine and enables the global interrupt (the ENI execution)

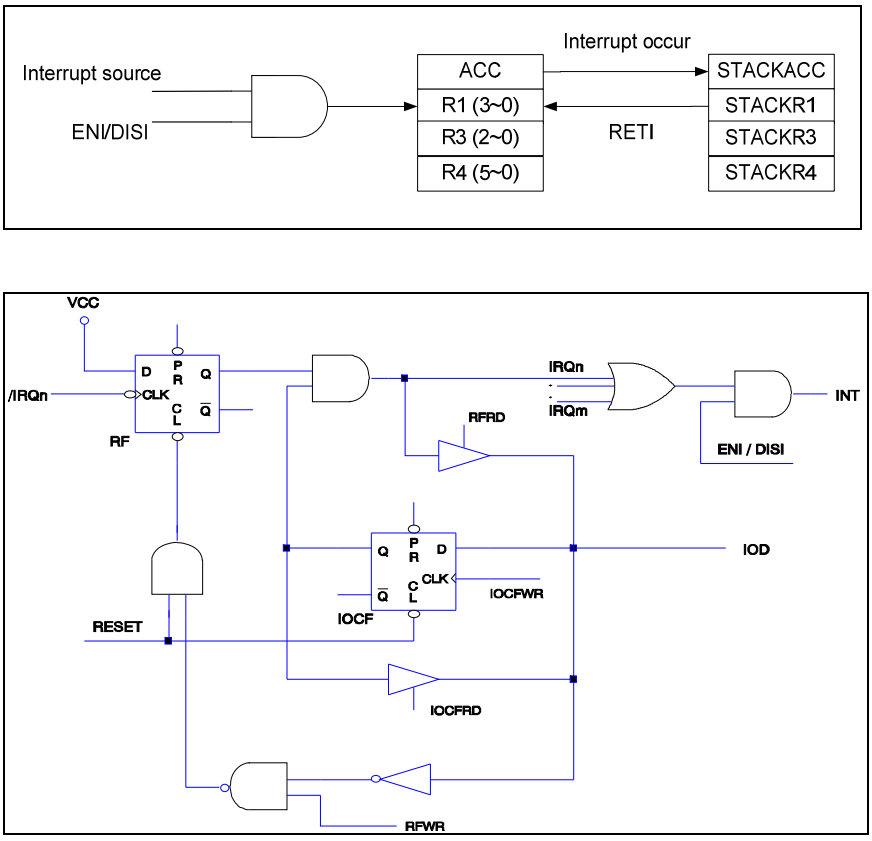


Figure 6-8 Interrupt Input Circuit

6.6 Analog-to-Digital Converter (ADC)

The analog-to-digital circuitry consists of 15-bit analog multiplexer; three control registers (AISR/RD, ADCON/R9 and ADOC/RA), two data registers (ADDATA1H/RB, and ADDATA1L/RC) and an ADC with 12-bit resolution as shown in the functional block diagram below. The analog reference voltage (Vref) and the analog ground are connected via separate input pins.

The ADC module utilizes successive approximation to convert the unknown analog signal into a digital value. The result is fed to the ADDATA1H and ADDATA1L. The Input channels are selected by the analog input multiplexer via the ADCON register Bits.

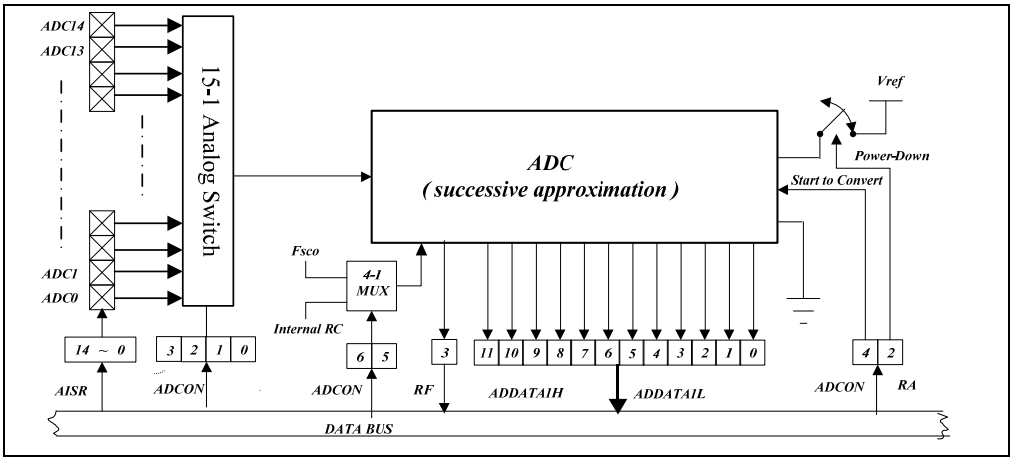


Figure 6-9 Analog-to-Digital Conversion Functional Block Diagram

6.6.1 ADC Control Register (ADCON/R9, ADOC/RA, AISR/RD)

6.6.1.1 Bank-R9 (ADCON: ADC Control Register)

Bit	7	6	5	4	3	2	1	0
Bank0-R9	VREFS	CKR1	CKR0	ADRUN	ADIS3	ADIS2	ADIS1	ADIS0
Bank0-RA	CALI	SIGN	VOF[2]	VOF[1]	VOF[0]	ADPD	–	–
Bank0-RB	AD11	AD10	AD9	AD8	AD7	AD6	AD5	AD4
Bank0-RC	ADE11	ADE10	ADE9	ADE8	AD3	AD2	AD1	AD0
Bank0-RD	ADE7	ADE6	ADE5	ADE4	ADE3	ADE2	ADE1	ADE0
Bank0-RE	–	–	–	–	ADWE	ADE14	ADE13	ADE12
Bank0-RF	–	–	–	–	ADIF	–	–	–
Bank1-RF	–	–	–	–	ADIE	–	–	–

6.6.2 ADC Data Register (ADDATA1H/RB, ADDATA1L/RC)

When the AD conversion is completed, the result is loaded to the ADDATA1H and ADDATA1L registers. The ADRUN bit is cleared, and the ADIF is set.

6.6.3 ADC Sampling Time

The accuracy, linearity, and speed of the successive approximation of the AD converter is dependent on the properties of the ADC and the comparator. The source impedance and the internal sampling impedance directly affect the time required to charge the sample holding capacitor. The application program controls the length of the sample time to meet the specified accuracy. Generally speaking, the program should wait for 2 μs for each KΩ of the analog source impedance and at least 2 μs for the low-impedance source. The maximum recommended impedance for the analog source is 10KΩ at Vdd=5V. After the analog input channel is selected, this acquisition time must be done before the conversion is started.

6.6.4 ADC Conversion Time

CKR1 and CKR0 select the conversion time (Tct), in terms of instruction cycles. This allows the MCU to run at the maximum frequency without sacrificing the AD conversion accuracy. For the EM78P349N, the conversion time per bit is 4 μs. The table below shows the relationship between Tct and the maximum operating frequencies.

CKR1:CKR0	Operation Mode	Max. Operation Frequency	Max. Conversion Rate/Bit	Max. Conversion Rate
00	Fosc/16	4 MHz	250kHz (4μs)	15×4μs=60μs (16.7kHz)
01	Fosc/4	1 MHz	250kHz (4μs)	15×4μs=60μs (16.7kHz)
10	Fosc/64	16 MHz	250kHz (4μs)	15×4μs=60μs (16.7kHz)
11	Fosc/8	2 MHz	250kHz (4μs)	15×4μs=60μs (16.7kHz)

NOTE

- *If AD input Pins are not used as an analog input pin, they can be used as regular input or output pins.*
- *"Sleep" instruction following immediately after setting the ADRUN bit can result in a more accurate AD conversion.*

6.6.5 ADC Operation during Sleep Mode

In order to obtain a more accurate ADC value and reduce power consumption, the AD conversion remains operational during sleep mode. As the SLEP instruction is executed, all the MCU operations will stop except for the Oscillator, TCC, Timer 1, Timer 2, Timer 3, and AD conversion.

The AD Conversion is considered completed as determined by:

1. ADRUN bit of R9 register is cleared (“0” value)
2. Wake-up from AD conversion (where it remains in operation during sleep mode)

The results are fed into the ADDATA1H and ADDATA1L registers when conversion is completed. If the ADWE is enabled, the device will wake up. Otherwise, AD conversion will be shut off, no matter what the status of the ADPD bit is.

6.6.6 Programming Process/Considerations

6.6.6.1 Programming Process

Follow these steps to obtain data from the ADC:

1. Write to the three bits (ADE14~ADE12) on the Bank0-RE, four bits (ADE11~ADE8) on the Bank0-RC and eight bits on the Bank0-RD (AISR) registers to define the characteristics of Bank0-R6, R7, P50, P57 and P80 (digital I/O, analog channels, or voltage reference pin).
2. Write to the Bank 0-R9/ADCON register to configure the AD module:
   a) Select ADC input channel (ADIS3:ADIS0).
   b) Define AD conversion clock rate (CKR1:CKR0).
   c) Select the VREFS input source of the ADC.
   d) Set the ADPD bit to 1 to begin sampling.
3. Set the ADWE bit, if the wake-up function is employed.
4. Set the ADIE bit, if the interrupt function is employed.
5. Write “ENI” instruction, if the interrupt function is employed.

   Set the ADRUN bit to 1

   Write “SLEP” instruction or Polling.
6. Wait for wake-up or for the ADRUN bit to be cleared (“0” value)
7. Read the ADDATA1H and ADDATA1L conversion data registers. If ADC input channel changes at this time, the ADDATA1H, and ADDATA1L values can be cleared to ‘0’.
8. Clear the interrupt flag bit (ADIF).
9. For next conversion, go to Step 1 or Step 2 as required. At least 2 Tct is required before the next acquisition starts.

NOTE

In order to obtain accurate values, it is necessary to avoid any data transition on the I/O pins during AD conversion.

6.6.6.2 Sample Demo Programs

A. Define the General Registers

R_0 == 0; Indirect addressing register

PSW == 3; Status register

PORT5 == 5

PORT6 == 6

RE== 0XE ; Wake-up control register

RF== 0XF ; Interrupt status register

B. Define a Control Register

BANK1-R5 == 0X5; Control Register of Port 5

BANK1-R6 == 0X6; Control Register of Port 6

BANK1-R6 == 0X7; Control Register of Port 7

BANK1-R6 == 0X8; Control Register of Port 8

BANK1-RF== 0XF; Interrupt Control Register

C. ADC Control Register

ADDATAH == 0xB; the contents (AD11~4) are the results of ADC

ADDATAL == 0xC; the contents (AD3~0) are the results of ADC

AISRL == 0x0D; ADC Input select register (ADE7~0)

AISRH == 0x0C; ADC Input select register (ADE11~8)

ADOC == 0x0A

ADCON == 0x9; 7 6 5 4 3 2 1 0

; VREFS CKR1 CKR0 ADRUN ADIS3 ADIS2 ADIS1 ADIS0

D. Define Bits ADRUN and ADPD

ADRUN == 0x4; ADC is executed as the bit is set

ADPD == 0x2; Power Mode of ADC

E. Program Starts

```
ORG 0; Initial address
JMP INITIAL;

ORG 0x08            ; Interrupt vector
;
;
;(User program section)
;
;
CLR RF              ; To clear the ADIF bit
BS ADCON, ADRUN     ; To start to execute the next AD conversion
                    ; if necessary
RETI
INITIAL:
BANK 0
MOV A,@0B00000001   ; To define P60 as an analog input
MOV AISR,A
BS  RA,ADPD         ; AD power on
MOV A,@0B00000000
MOV ADCON,A         ; and set clock rate at fosc/16
```

```
En_ADC:
BANK 1
MOV A, @0BXXXXXXX1  ; To define P60 as an input pin, and the others
MOV PORT6,A         ; are dependent on the applications
BANK 0
MOV A, @0BXXXX1XXX  ; Enable the ADWE wake-up function of ADC, "X"
                    ; by application
MOV RE,A
BANK 1
MOV A, @0BXXXX1XXX  ; Enable the ADIE interrupt function of ADC,
                    ; "X" by application
MOV BANK1-RF,A
ENI                 ; Enable the interrupt function
BANK 0
BS ADCON, ADRUN     ; Start to run the ADC

; If the interrupt function is employed, the following three lines
                    ; may be ignored

POLLING:
JBC ADCON, ADRUN    ; To check the ADRUN bit continuously
JMP POLLING
                    ; ADRUN bit will be reset as the AD conversion
                    ; is completed
;
;
;(User program section)
;
;
```

6.7 Three Sets of PWM (Pulse Width Modulation)

6.7.1 Overview

In PWM mode, PWM1, PWM2, and PWM3 pins produce up to 10-bit resolution PWM output (see. the functional block diagram). A PWM output consists of a time period and a duty cycle, and it keeps the output high. The baud rate of the PWM is the inverse of the time period. Figure 6-10 (*PWM Output Timing*) depicts the relationships between a time period and a duty cycle.

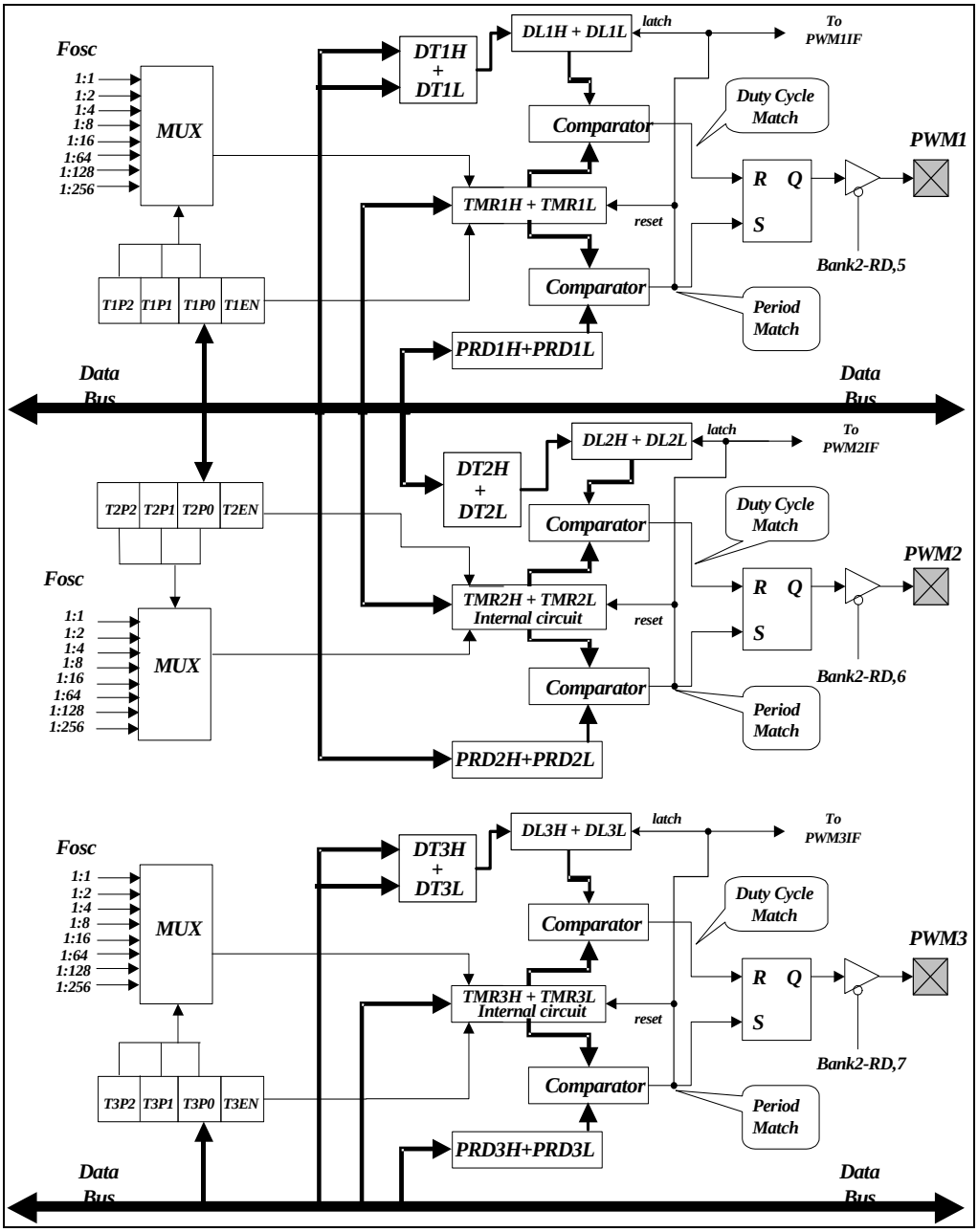


Figure 6-10 Three PWMs Functional Block Diagram

6.7.2 Increment Timer Counter (TMRX: TMR1H/TWR1L, TMR2H/TWR2L, or TMR3H/TWR3L)

TMRX are 10-bit clock counters with programmable prescalers. They are designed for the PWM module as baud rate clock generators. If employed, they can be turned off for power saving purposes by setting the T1EN bit [Bank 1-RA<3>], T2EN bit [Bank 1-R9<6>] or T3EN bit [Bank 1-R9<7>] to 0.

TMR1, TMR2 and TMR3 are internal designs and cannot be read.

6.7.3 PWM Time Period (PRDX : PRD1 or PRD2 or PRD3)

The PWM period is 10-bit resolution. The PWM time period is defined by writing to the PRDX register. When TMRX is equal to PRDX, the following events occur on the next increment cycle:

- TMRX is cleared
- The PWMX bit is set to 1
- The PWM duty cycle is latched from DT1/DT2/DT3 to DL1/DL2/DL3

NOTE

The PWM output will not be set, if the duty cycle is 0

- The PWMXIF pin is set to 1

The following formula describes how to calculate the PWM time period:

$$Period = (PRDX + 1) \times \left(\frac{1}{F_{OSC}}\right) \times \frac{CLKS}{2} \times (TMRX \ \ prescale\ value)$$

Example:

PRDX = 49; Fosc = 4 MHz; TMRX (0, 0, 0) = 1 : 1,

CLKS bit of the Code Option Register = 0 (two oscillator periods);

Then

$$Period = (49 + 1) \times \left(\frac{1}{4M}\right) \times \frac{2}{2} \times 1 = 12.5\,\mu s$$

6.7.4 PWM Duty Cycle (DTX: DT1H/ DT1L, DT2H/ DT2L and DT3H/DT3L; DLX: DL1H/DL1L, DL2H/DL2L and DL3H/DL3L)

The PWM duty cycle is defined by writing to the DTX register, and is latched from DTX to DLX while TMRX is cleared. When DLX is equal to TMRX, the PWMX pin is cleared. DTX can be loaded anytime. However, it cannot be latched into DLX until the current value of DLX is equal to TMRX.

The following formula describes how to calculate the PWM duty cycle**:**

$$Duty\ cycle\ =\ (DTX)\ \times\ \left(\frac{1}{F_{OSC}}\right)\ \times\ \frac{CLKS}{2}\ \times\ (TMRX\ \ prescale\ value)$$

Example:

DTX = 10; Fosc = 4 MHz; TMRX (0, 0, 0) = 1 : 1,

CLKS bit of the Code Option Register = 0 (two oscillator periods);

Then

$$Duty\ cycle\ =\ (10)\ \times\ \left(\frac{1}{4M}\right)\ \times\ \frac{2}{2}\ \times\ 1\ =\ 2.5\,\mu s$$

6.7.5 Comparator X

Changing the output status while matching occurs will simultaneously set the TMRXIF flag.

6.7.6 PWM Programming Process/Steps

1. Load the PWM duty cycle to DT.
2. Load the PWM time period to PRD.
3. Enable the interrupt function by writing Bank1-RF, if required.
4. Load a desired value for the timer prescaler and enable the timer and PWM.

6.8 Timer

6.8.1 Overview

Timer 1 (TMR1), Timer 2 (TMR2), and Timer 3 (TMR3) (TMRX) are 10-bit up-counters with programmable prescalers. They are designed for the PWM module as baud rate clock generators. TMRX can be read only. Timer 1, Timer 2, and Timer 3 will stop running when sleep mode occurs with AD conversion not running. However, if AD conversion is running when sleep mode occurs, Timer 1, Timer 2 and Timer 3 will keep on running.

6.8.2 Function Description

The following figure shows the TMRX block diagram followed by descriptions of its signals and blocks:

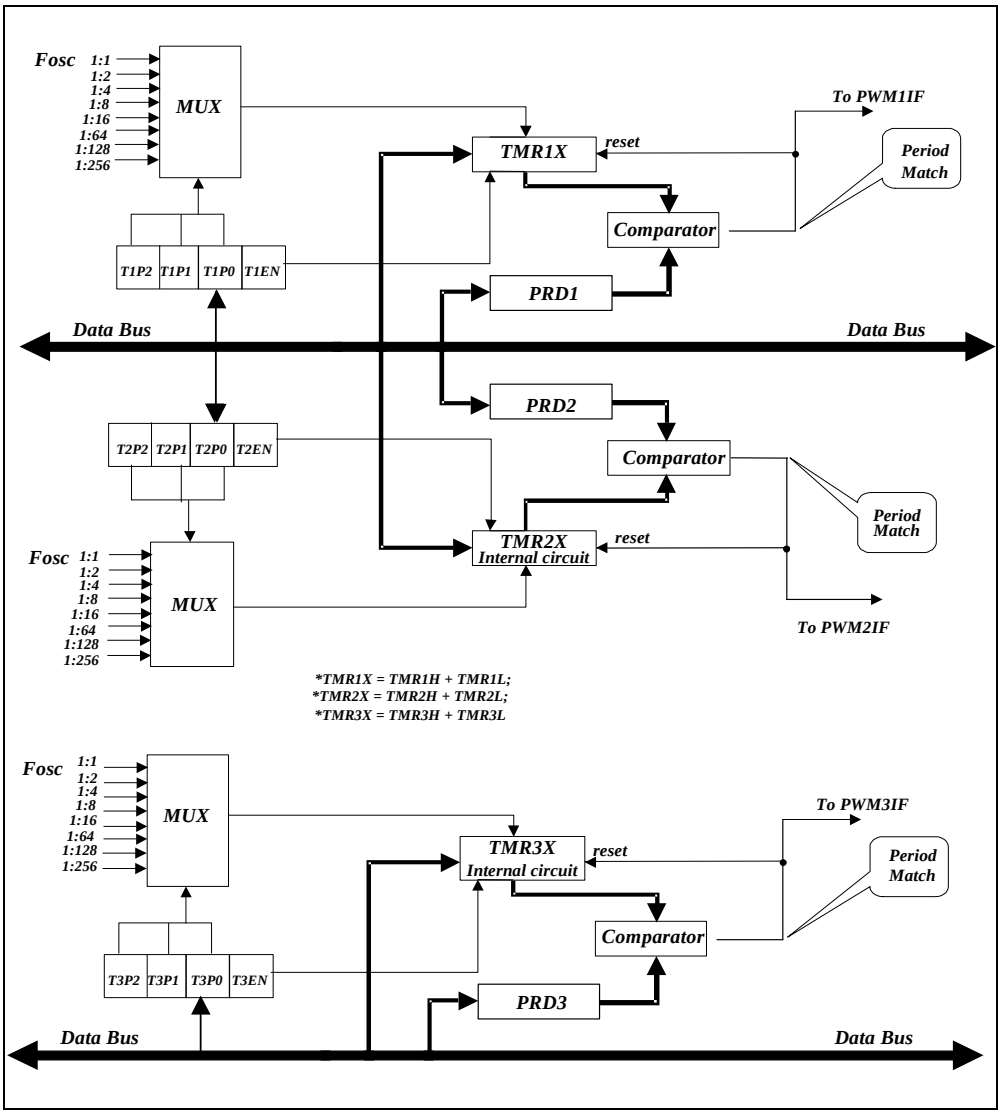


Figure 6-11 TMRX Block Diagram

Fosc: Input clock

Prescaler (T1P2, T1P1 and T1P0 / T2P2, T2P1 and T2P0 / T3P2, T3P1 and T3P0):
The options 1:1, 1:2, 1:4, 1:8, 1:16, 1:64, 1:128, and 1:256 are defined by TMRX. They are cleared when any type of reset occurs.

TMR1X (TMR1H/TWR1L): Timer 1 X register; TMRX is increased until it matches with PRDX, and then is reset to 1 (default valve).

PRDX (PRD1, PRD2 and PRD3):
PWM time period register.

Comparator X:
Reset TMRX while a match occurs. The TMRXIF flag is set at the same time.

6.8.3 Programming the Related Registers

When defining TMRX, refer to the operation of its related registers as shown in the table below. It must be noted that the PWMX bits must be disabled if their related TMRXs are employed. That is, Bit 7 ~ Bit 5 of the PWMCON register must be set to '0'.

6.8.3.1 Related Control Registers of TMR1, TMR2, and TMR3

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0×0A	Bank 2-RA	–	–	–	–	T1EN	T1P2	T1P1	T1P0
0×09	Bank 1-R9	T3EN	T2EN	T3P2	T3P1	T3P0	T2P2	T2P1	T2P0
0×0F	Bank 0-RF	–	PWM3IF	PWM2IF	PWM1IF	–	–	–	–
0×0F	Bank 1-RF	–	PWM3IE	PWM2IE	PWM1IE	–	–	–	–

6.8.4 Timer Programming Process/Steps

1. Load PRDX with the Timer duration
2. Enable interrupt function by writing Bank 1-RF, if required
3. Load a desired a TMRX prescaler value, enable TMRX and disable PWMX.

6.9 Oscillator

6.9.1 Oscillator Modes

The EM78P349N can be operated in four different oscillator modes, such as High Crystal oscillator mode (HXT), Low Crystal oscillator mode (LXT), External RC oscillator mode (ERC), and RC oscillator mode with Internal RC oscillator mode (IRC). User can select one of them by programming the OSC2, OCS1, and OSC0 in the Code Option register.

The Oscillator modes defined by OSC2, OCS1, and OSC0 are described below.

Oscillator Modes	OSC2	OSC1	OSC0
ERC[1] (External RC oscillator mode); P52/OSCO acts as P52	0	0	0
ERC[1] (External RC oscillator mode); P52/OSCO acts as OSCO	0	0	1
IRC[2] (Internal RC oscillator mode); P52/OSCO acts as P52	0	1	0
IRC[2] (Internal RC oscillator mode); P52/OSCO acts as OSCO	0	1	1
LXT[3] (Low Crystal oscillator mode)	1	1	0
HXT[3] High Crystal oscillator mode) (default)	1	1	1

[1] In ERC mode, OSCI is used as oscillator pin. OSCO/P52 is defined by Code Option Word 0 Bit 6~Bit 4.

[2] In IRC mode, P53 is normal I/O pin. OSCO/P52 is defined by code option Word 0 Bit 6 ~ Bit 4.

[3] In LXT and HXT modes; OSCI and OSCO are used as oscillator pins. These pins cannot and should not be defined as normal I/O pins.

NOTE

The transient point of the system frequency between HXT and LXT is 400kHz.

The maximum operating frequency limit of crystal/resonator at different VDDs, are as follows:

Conditions	VDD	Max. Freq. (MHz)
Two clocks	2.3	4
	3.0	8
	5.0	20

6.9.2 Crystal Oscillator/Ceramic Resonators (Crystal)

EM78P349N can be driven by an external clock signal through the OSCI pin as illustrated below.

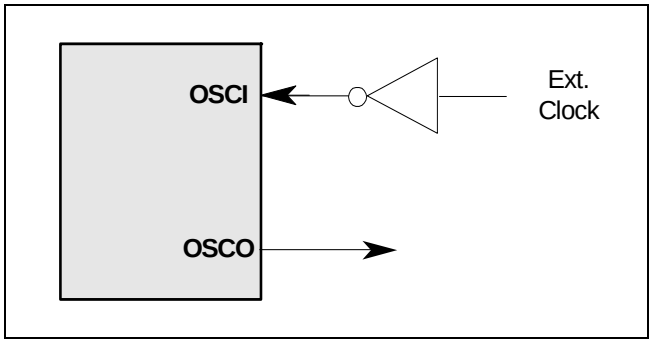


Figure 6-12 External Clock Input Circuit

In most applications, Pin OSCI and Pin OSCO can be connected with a crystal or ceramic resonator to generate oscillation. Figure 6-13 depicts such circuit. The same applies to the HXT mode and the LXT mode.

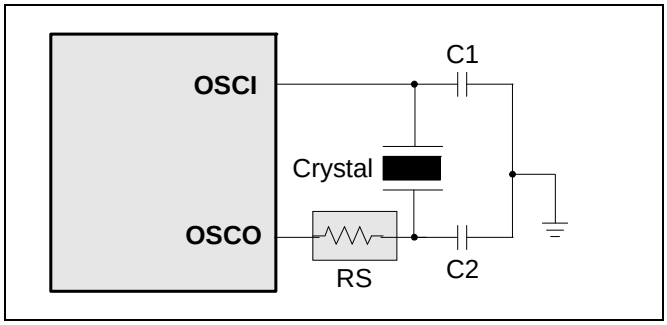


Figure 6-13 Crystal/Resonator Circuit

The following table provides the recommended values for C1 and C2. Since each resonator has its own attribute, user should refer to the resonator specifications for appropriate values of C1 and C2. A serial resistor, RS, may be required for AT strip cut crystal or low frequency mode.

Capacitor selection guide for crystal oscillator or ceramic resonators**:**

Oscillator Type	Frequency Mode	Frequency	C1 (pF)	C2 (pF)
Ceramic Resonators	HXT	455kHz	100~150	100~150
		2.0 MHz	20~40	20~40
		4.0 MHz	10~30	10~30
Crystal Oscillator	LXT	32.768kHz	25	15
		100kHz	25	25
		200kHz	25	25
	HXT	455kHz	20~40	20~150
		1.0 MHz	15~30	15~30
		2.0 MHz	15	15
		4.0 MHz	15	15

6.9.3 External RC Oscillator Mode

For some applications that do not require precise timing calculation, the RC oscillator (Figure 6-14 right) could offer you with effective cost savings. Nevertheless, it should be noted that the frequency of the RC oscillator is influenced by the supply voltage, the values of the resistor (Rext), the capacitor (Cext), and even by the operation temperature. Moreover, the frequency also changes slightly from one chip to another due to the manufacturing process variation.

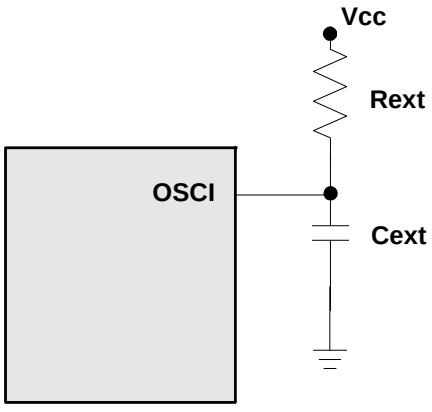


Figure 6-14 External RC Oscillator Mode Circuit

In order to maintain a stable system frequency, the values of the Cext should be not less than 20pF, and that the value of Rext should be not greater than 1MΩ.

If the frequency cannot be kept within this range, the frequency can be affected easily by noise, humidity, and leakage.

The smaller the Rext in the RC oscillator is, the faster its frequency will be. On the contrary, for very low Rext values, for instance, 1 KΩ, the oscillator will become unstable because the NMOS cannot discharge the capacitance current correctly.

Based on the above reasons, it must be kept in mind that all supply voltage, the operation temperature, the components of the RC oscillator, the package types, and the way the PCB is layout, have certain effect on the system frequency.

The RC Oscillator frequencies**:**

Cext	Rext	Average Fosc 5V, 25°C	Average Fosc 3V, 25°C
20 pF	3.3k	3.5 MHz	3.2 MHz
	5.1k	2.5 MHz	2.3 MHz
	10k	1.30 MHz	1.25 MHz
	100k	140kHz	140kHz
100 pF	3.3k	1.27 MHz	1.21 MHz
	5.1k	850kHz	820kHz
	10k	450kHz	450kHz
	100k	48kHz	50kHz
300 pF	3.3k	560kHz	540kHz
	5.1k	370kHz	360kHz
	10k	196kHz	192kHz
	100k	20kHz	20kHz

Note: 1. Measured on DIP packages.
2. Design reference only
3. The frequency drift is about ± 30%

6.9.4 Internal RC Oscillator Mode

EM78P349N offers a versatile internal RC mode with default frequency value of 4MHz. Internal RC oscillator mode has other frequencies (1 MHz, 8 MHz, and 455kHz) that can be set by Code Option (Word 1), RCM1, and RCM0. The table below describes the EM78P349N internal RC drift with the variation of voltage, temperature, and process.

Internal RC Drift Rate (Ta=25°C, VDD=3.7V±5%, VSS=0V)

Internal RC Frequency	Drift Rate			
	Temperature (-40°C~+85°C)	Voltage (2.3V~5.5V)	Process	Total
4 MHz	± 5%	± 5%	± 4%	± 14%
8 MHz	± 5%	± 5%	± 4%	± 14%
1 MHz	± 5%	± 5%	± 4%	± 14%
455kHz	± 5%	± 5%	± 4%	± 14%

Theoretical values are for reference only. Actual values may vary depending on the actual process.

6.10 Power-on Considerations

Any microcontroller is not warranted to start operating properly before the power supply has stabilized in a steady state. The EM78P349N is equipped with Power-on Voltage Detector (POVD) with detection level range of 1.8V to 2.0V. The circuitry eliminates the extra external reset circuit. It will work well if Vdd rises quickly enough (50 ms or less). However, under critical applications, extra devices are still required to assist in solving power-on problems.

6.10.1 External Power-on Reset Circuit

The circuit shown in the following figure implements an external RC to produce a reset pulse. The pulse width (time constant) should be kept long enough to allow Vdd to reach the minimum operating voltage. This circuit is used when the power supply has a slow power rise time. Because the current leakage from the /RESET pin is ± 5μA, it is recommended that R should not be greater than 40K. This way, the voltage at Pin /RESET is held below 0.2V. The diode (D) acts as a short circuit at power-down. The "C" capacitor is discharged rapidly and fully. Rin, the current-limited resistor, prevents high current discharge or ESD (electrostatic discharge) from flowing into Pin /RESET.

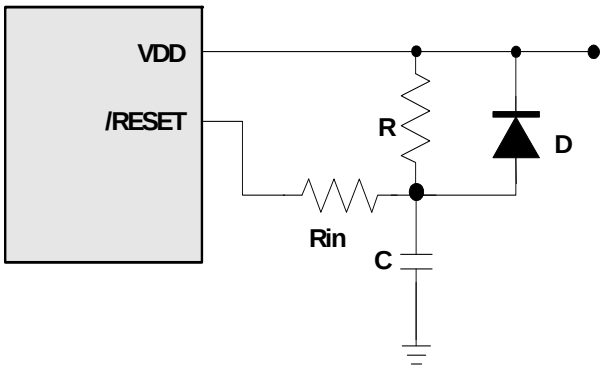


Figure 6-15 External Power on Reset Circuit

6.10.2 Residual Voltage Protection

When the battery is replaced, device power (Vdd) is removed but residual voltage remains. The residual voltage may trip below Vdd minimum, but not to zero. This condition may cause a poor power-on reset. Figure 6-16 and Figure 6-17 show how to create a protection circuit against residual voltage.

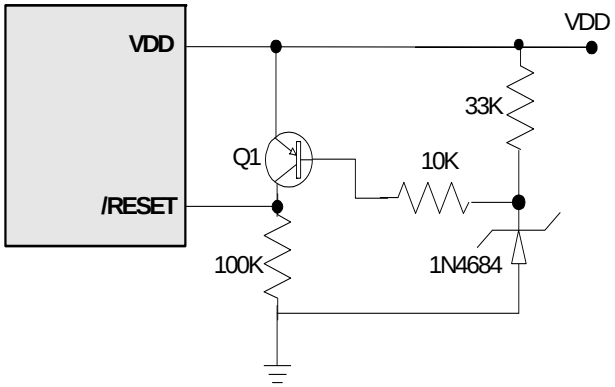


Figure 6-16 Residual Voltage Protection Circuit 1

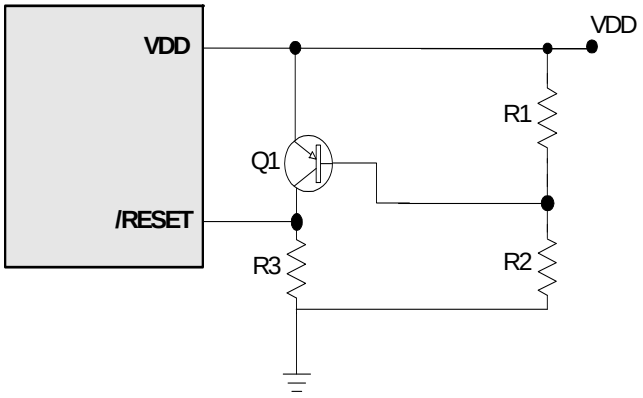


Figure 6-17 Residual Voltage Protection Circuit 2

6.11 Low Voltage Detector

During the power source unstable situation, such like external power noise interference or EMS test condition, it will cause the power vibrate fierce. At the time the Vdd is unsettled, it may be below working voltage. When the system supply voltage Vdd is below the working voltage, the IC kernel must keep all register status automatically.

6.11.1 Low Voltage Reset

LVR property is set at Code Option Word 0, Bits 10, 9. Detailed operation mode are as follows:

Word 0												
Bit 12	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
1	1	LVR1	LVR0	CLKS	ENWDTB	OSC2	OSC1	OSC0	HLP	PR2	PR1	PR0

Bits 10~9 (LVR1 ~ LVR0): Low Voltage Reset enable bits.

LVR1, LVR0	VDD Reset level
11	NA
10	2.5V
01	3.0V
00	4.0V

6.11.2 Low Voltage Detector

The LVD property is set at Registers RA, RE. Detailed operation modes are as follows:

6.11.2.1 Bank 0-RA (ADOC: ADC Offset Calibration Register)

Bit	7	6	5	4	3	2	1	0
Symbol	CALI	SIGN	VOF[2]	VOF[1]	VOF[0]	LVDEN	LVD1	LVD0
*Init_Value	0	0	0	0	0	0	1	1

**Init_Value: Initial value at power on reset*

Bits 1~0 (LVD1~LVD 0): Low Voltage Detector level bits.

LVDEN <RA, 2>	LVD1, LVD0 <RA, 1, 0>	LVD Voltage Interrupt Level	LVDIF
1	11	2.2V	1*
1	10	3.3V	1*
1	01	4.0V	1*
1	00	4.5V	1*
0	××	NA	0

** If Vdd has crossover at LVD voltage interrupt level as Vdd changes, LVDIF =1.*

6.11.2.2 Bank 0-R8 (Port 8)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LVDEN	/LVD	NREN	–	–	–	–	P80

Bit 7 (LVDEN): Low Voltage Detector Enable bits

0 : Low voltage detector disable

1 : Low voltage detector enable

Bit 6 (/LVD): Low voltage Detector state. This is a read only bit. When the VDD pin voltage is lower than LVD voltage interrupt level (selected by LVD1 and LVD0), this bit will be cleared.

0 : Low voltage is detected.

1 : Low voltage is not detected or LVD function is disabled.

6.11.2.3 Bank 0-RE (WUCR: Wake-up Control Register)

Bit	7	6	5	4	3	2	1	0
Symbol	–	LVDIF	LVDWE	ICWE	ADWE	–	–	–
*Init_Value	0	0	0	0	0	0	0	0

**Init_Value: Initial value at power-on reset*

NOTE

- *Bank 0-RE <6> "1" means with interrupt request; "0" means no interrupt occurs*
- *Bank 0-RE <6>can be cleared by instruction but cannot be set.*
- *Bank 1-RE <6> is the interrupt mask register.*
- *Reading Bank 0-RE <6> will result to "logic AND" of Bank 0-RE <6> and Bank 1-RE <6>.*

Bit 6 (LVDIF): Low Voltage Detector Interrupt flag

LVDIF reset to “0” by software or hardware.

LVDEN <RA, 2>	LVD1, LVD0 <RA, 1, 0>	LVD Voltage Interrupt Level	LVDIF
1	11	2.2V	1*
1	10	3.3V	1*
1	01	4.0V	1*
1	00	4.5V	1*
0	××	NA	0

* If Vdd has crossover at LVD voltage interrupt level as Vdd changes, LVDIF=1.

Bit 5 (LVDWE): Low Voltage Detect wake-up enable bit.

0 : Disable Low Voltage Detect wake-up.

1 : Enable Low Voltage Detect wake-up.

When the Low Voltage Detect is used to enter an interrupt vector or to wake-up IC from sleep with Low Voltage Detect running, the LVDWE bit must be set to “Enable“.

6.11.2.4 Bank 1-RE (WDT Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WDTE	LVDIE	PSWE	PSW2	PSW1	PSW0	–	–

Bit 6 (LVDIE): Low voltage Detector interrupt enable bit.

0 : Disable Low voltage Detector interrupt.

1 : Enable Low voltage Detector interrupt.

When the detect-low level voltage is used to enter an interrupt vector or enter the next instruction, the LVDIE bit must be set to “Enable“.

6.11.3 Programming Process

Follow these steps to obtain data from the LVD**:**

1. Write to the two bits (LVD1: LVD0) on the Bank 0-RA register to define the LVD level.
2. Set the LVDWE bit, if the wake-up function is employed.
3. Set the LVDIE bit, if the interrupt function is employed.
4. Write “ENI” instruction, if the interrupt function is employed.
5. Set LVDEN bit to 1
6. Write “SLEP” instruction or Polling /LVD bit.
7. Clear the interrupt flag bit (LVDIF) when Low Voltage Detector occurs.

The internal LVD module is using an internal circuit. When LVDEN is set to “1”, the LVD module is enabled.

During sleep mode at LVDWE=1, the LVD module continues to operate. If the device voltage drops slowly and crosses the detect point, the LVDIF bit will be set and the device will wake-up from Sleep mode. The LVD interrupt flag is still set as the prior status.

When the system resets, the LVD flag will be cleared.

Figure 6-18 shows the LVD module to detect the external voltage situation.

When Vdd drop from high to low at VLVD, LVDIF is set to “1”. When Vdd rises from low to high at VLVD, LVDIF is set to “1”. If global ENI enable and LVDIF = “1”, program counter will jump to interrupt vector. The LVD interrupt flag clear to “0” by software.

When Vdd drops below VRESET and is less than 5 μs, the system will keep all the register status and the system halts but oscillation remains active. When Vdd drops below VRESET and is more than 5 μs, a Reset occurs, as well as the following actions. Refer to Section 6.4.1 *Reset Description.*

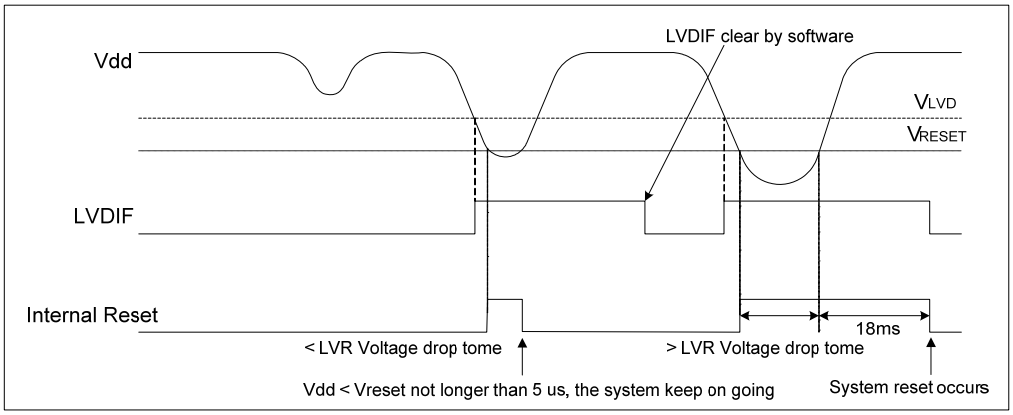


Figure 6-18 LVD Waveform Diagram

6.12 Code Option

The EM78P349N has two Code option words and one Customer ID word that are not part of the normal program memory.

Word 0	Word1	Word 2
Bit 12 ~ Bit 0	Bit 12 ~ Bit 0	Bit 12 ~ Bit 0

6.12.1 Code Option Register (Word 0)

Word 0												
Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	1	LVR1	LVR0	CLKS	ENWDTB	OSC2	OSC1	OSC0	HLP	PR2	PR1	PR0

Bits 12 ~ 11: Not used, set to "1" at all time

Bits 10 ~ 9 (LVR1 ~ LVR0): Low Voltage Reset Enable bits.

LVR1, LVR0	VDD Reset level
11	NA
10	2.5V
01	3.0V
00	4.0V

Bit 8 (CLKS): Instruction time period option bit

0 : two oscillator time periods

1 : four oscillator time periods (default)

Refer to Section 6.13 for the Instruction Set

Bit 7 (ENWDTB): Watchdog timer enable bit

0 : Enable

1 : Disable (default)

Bit 6, 5 and 4 (OSC2, OSC1 and OSC0): Oscillator Modes Selection bits

Oscillator Modes	OSC2	OSC1	OSC0
ERC[1] (External RC oscillator mode); P52/OSCO acts as P52	0	0	0
ERC[1] (External RC oscillator mode); P52/OSCO acts as OSCO	0	0	1
IRC[2] (Internal RC oscillator mode); P52/OSCO acts as P52	0	1	0
IRC[2] (Internal RC oscillator mode); P52/OSCO acts as OSCO	0	1	1
LXT[3] (Low Crystal oscillator mode)	1	1	0
HXT[3] High Crystal oscillator mode) (default)	1	1	1

[1] In ERC mode, OSCI is used as oscillator pin. OSCO/P52 is defined by Code Option Word 0 Bit 6 ~ Bit 4.

[2] In IRC mode, P53 is normal I/O pin. OSCO/P52 is defined by Code Option Word 0 Bit 6 ~ Bit 4.

[3] In LXT and HXT modes; OSCI and OSCO are used as oscillator pins. These pins cannot and should not be defined as normal I/O pins. The OSCI/P53 must be not defined as output pin.

NOTE

The transient point of the system frequency between HXT and LXT is 400kHz.

Bit 3 (HLP): Power consumption selection

0 : Low power consumption, applies to working frequency at 4 MHz or below 4 MHz

1 : High power consumption, applies to working frequency above 4 MHz

Bits 2~0 (PR2 ~ PR0): Protect bits. Each protect status is as follows:

PR2	PR1	PR0	Protect
0	0	0	Enable
1	1	1	Disable

6.12.2 Code Option Register (Word 1)

Word 1												
Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	TYPE	LPBW	RCOUT	NRHL	NRE	0	C3	C2	C1	C0	RCM1	RCM0

NOTE

The noise rejection function is turned off in the LXT and sleep mode.

Bit 12: Not used, set to “0” at all time

Bit 11 (TYPE): Package type

0 : 24 pin

1 : 28 pin

Bit 10 (LPBW): **L**ow pass filter bandwidth

0 : 20 MHz operating frequency at 5V
8 MHz operating frequency at 3V

1 : 8 MHz operating frequency at 5V
4 MHz operating frequency at 3V

Bit 9 (RCOUT): System clock output enable bit in IRC or ERC mode

0 : OSCO pin is open drain

1 : OSCO output system clock (default)

Bit 8 (NRHL): Noise rejection high/low pulses define bit. INT pin is falling edge trigger

0 : Pulses equal to 8/fc [s] is regarded as signal.

1 : Pulses equal to 32/fc [s] is regarded as signal (default)

Bit 7 (NRE): Noise Rejection Enable

0 : disable noise rejection

1 : enable noise rejection (default). However in Low Crystal oscillator (LXT) mode, the noise rejection circuit is always disabled.

Bit 6: Not used, set to “0” at all time

Bits 5, 4, 3 and Bit 2 (C3, C2, C1, and C0): Calibrator of internal RC mode. These bits must always be set to “1” only (auto calibration)

Bit 1 and Bit 0 (RCM1 and RCM0): RC mode selection bits

RCM 1	RCM 0	Frequency (MHz)
1	1	4
1	0	8
0	1	1
0	0	455kHz

6.12.3 Customer ID Register (Word 2)

Word 2												
Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
×	×	×	×	×	×	×	×	×	×	×	×	×

Bits 12 ~ 0: Customer’s ID code

6.13 Instruction Set

Each instruction in the instruction set is a 13-bit word divided into an OP code and one or more operands. Normally, all instructions are executed within one single instruction cycle (one instruction consists of 2 oscillator time periods), unless the program counter is changed by instructions "MOV R2,A," "ADD R2,A," or by instructions of arithmetic or logic operation on R2 (e.g., "SUB R2,A," "BS(C) R2,6," "CLR R2," etc.). In this case, these instructions need one or two instruction cycles as determined by Code Option Register CYES bit.

In addition, the instruction set has the following features**:**

1. Every bit of any register can be set, cleared, or tested directly.
2. The I/O registers can be regarded as general registers. That is, the same instruction can operate on I/O registers.

Convention:

R = Register designator that specifies which one of the registers (including operation and general purpose registers) is to be utilized by the instruction.

b = Bit field designator that selects the value for the bit located in the register R and which affects the operation.

k = 8 or 10-bit constant or literal value

The following are the list of the EM78P349N Instruction set**:**

Binary Instruction	HEX	Mnemonic	Operation	Status Affected
0 0000 0000 0000	0000	NOP	No Operation	None
0 0000 0000 0001	0001	DAA	Decimal Adjust A	C
0 0000 0000 0010	0002	CONTW	A → CONT	None
0 0000 0000 0011	0003	SLEP	0 → WDT, Stop oscillator	T, P
0 0000 0000 0100	0004	WDTC	0 → WDT	T, P
0 0000 0001 0000	0010	ENI	Enable Interrupt	None
0 0000 0001 0001	0011	DISI	Disable Interrupt	None
0 0000 0001 0010	0012	RET	[Top of Stack] → PC	None
0 0000 0001 0011	0013	RETI	[Top of Stack] → PC, Enable Interrupt	None
0 0000 0001 0100	0014	CONTR	CONT → A	None
0 0000 01rr rrrr	00rr	MOV R,A	A → R	None
0 0000 1000 0000	0080	CLRA	0 → A	Z
0 0000 11rr rrrr	00rr	CLR R	0 → R	Z
0 0001 00rr rrrr	01rr	SUB A,R	R-A → A	Z, C, DC
0 0001 01rr rrrr	01rr	SUB R,A	R-A → R	Z, C, DC
0 0001 10rr rrrr	01rr	DECA R	R-1 → A	Z
0 0001 11rr rrrr	01rr	DEC R	R-1 → R	Z
0 0010 00rr rrrr	02rr	OR A,R	A ∨ VR → A	Z
0 0010 01rr rrrr	02rr	OR R,A	A ∨ VR → R	Z
0 0010 10rr rrrr	02rr	AND A,R	A & R → A	Z
0 0010 11rr rrrr	02rr	AND R,A	A & R → R	Z
0 0011 00rr rrrr	03rr	XOR A,R	A ⊕ R → A	Z
0 0011 01rr rrrr	03rr	XOR R,A	A ⊕ R → R	Z
0 0011 10rr rrrr	03rr	ADD A,R	A + R → A	Z, C, DC
0 0011 11rr rrrr	03rr	ADD R,A	A + R → R	Z, C, DC
0 0100 00rr rrrr	04rr	MOV A,R	R → A	Z
0 0100 01rr rrrr	04rr	MOV R,R	R → R	Z
0 0100 10rr rrrr	04rr	COMA R	/R → A	Z
0 0100 11rr rrrr	04rr	COM R	/R → R	Z
0 0101 00rr rrrr	05rr	INCA R	R+1 → A	Z
0 0101 01rr rrrr	05rr	INC R	R+1 → R	Z
0 0101 10rr rrrr	05rr	DJZA R	R-1 → A, skip if zero	None
0 0101 11rr rrrr	05rr	DJZ R	R-1 → R, skip if zero	None
0 0110 00rr rrrr	06rr	RRCA R	R(n) → A(n-1), R(0) → C, C → A(7)	C
0 0110 01rr rrrr	06rr	RRC R	R(n) → R(n-1), R(0) → C, C → R(7)	C
0 0110 10rr rrrr	06rr	RLCA R	R(n) → A(n+1), R(7) → C, C → A(0)	C

Binary Instruction	HEX	Mnemonic	Operation	Status Affected
0 0110 11rr rrrr	06rr	RLC R	R(n) → R(n+1), R(7) → C, C → R(0)	C
0 0111 00rr rrrr	07rr	SWAPA R	R(0-3) → A(4-7), R(4-7) → A(0-3)	None
0 0111 01rr rrrr	07rr	SWAP R	R(0-3) ↔ R(4-7)	None
0 0111 10rr rrrr	07rr	JZA R	R+1 → A, skip if zero	None
0 0111 11rr rrrr	07rr	JZ R	R+1 → R, skip if zero	None
0 100b bbrr rrrr	0xxx	BC R,b	0 → R(b)	None[1]
0 101b bbrr rrrr	0xxx	BS R,b	1 → R(b)	None[2]
0 110b bbrr rrrr	0xxx	JBC R,b	if R(b)=0, skip	None
0 111b bbrr rrrr	0xxx	JBS R,b	if R(b)=1, skip	None
1 00kk kkkk kkkk	1kkk	CALL k	PC+1 → SP, (lower 10 bits of k) → PC	None
1 01kk kkkk kkkk	1kkk	JMP k	(lower 10 bits of k) → PC	None
1 1000 kkkk kkkk	18kk	MOV A,k	k → A	None
1 1001 kkkk kkkk	19kk	OR A,k	A ∨ k → A	Z
1 1010 kkkk kkkk	1Akk	AND A,k	A & k → A	Z
1 1011 kkkk kkkk	1Bkk	XOR A,k	A ⊕ k → A	Z
1 1100 kkkk kkkk	1Ckk	RETL k	k → A, [Top of Stack] → PC	None
1 1101 kkkk kkkk	1Dkk	SUB A,k	k-A → A	Z, C, DC
1 1110 1001 kkkk	1E9k	BANK k	k → R1(1:0)	None
1 1110 1010 kkkk k kkkk kkkk kkkk	1EAk	LCALL k	Next instruction: k kkkk kkkk kkkk; PC+1 → [SP], k → PC	None
1 1110 1011 kkkk k kkkk kkkk kkkk	1EBk	LJMP k	Next instruction: k kkkk kkkk kkkk; k → PC	None
1 1111 kkkk kkkk	1Fkk	ADD A,k	k+A → A	Z, C, DC

Note: [1] *This instruction is not recommended for RF operation*

[2] *This instruction cannot operate under RF.*

7 Absolute Maximum Ratings

Items	Rating		
Temperature under bias	-40°C	to	85°C
Storage temperature	-65°C	to	150°C
Input voltage	Vss-0.3V	to	Vdd+0.5V
Output voltage	Vss-0.3V	to	Vdd+0.5V
Working Voltage	2.3V	to	5.5V
Working Frequency	DC	to	20 MHz

8 DC Electrical Characteristics

Ta = 25°C, VDD = 5.0V, VSS = 0V

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
FXT	Crystal: VDD to 5V	Two cycles with two clocks	DC	–	20	MHz
	ERC: VDD to 5V	R: 5.1KΩ, C: 300 pF	F±30%	370	F±30%	kHz
IRC1	IRC: VDD to 5V	RCM0:RCM1=1:1	3.84	4	4.16	MHz
IRC2	IRC: VDD to 5V	RCM0:RCM1=1:0	7.68	8	8.32	MHz
IRC3	IRC: VDD to 5V	RCM0:RCM1=0:1	0.96	1	1.04	MHz
IRC4	IRC: VDD to 5V	RCM0:RCM1=0:0	436.8	455	473.2	kHz
VIHRC	Input High Threshold Voltage (Schmitt trigger)	OSCI in RC mode	–	3.5	–	V
VILRC	Input Low Threshold Voltage (Schmitt trigger)	OSCI in RC mode	–	1.5	–	V
IIL	Input Leakage Current for input pins	VIN = VDD, VSS	–1.0	0	1.0	µA
VIH1	Input High Voltage (Schmitt trigger)	Ports 5, 6, 7, 8	–	2.6	–	V
VIL1	Input Low Voltage (Schmitt trigger)	Ports 5, 6, 7, 8	–	2.2	–	V
VIHT1	Input High Threshold Voltage (Schmitt trigger)	/RESET	–	1.9	–	V
VILT1	Input Low Threshold Voltage (Schmitt trigger)	/RESET	–	1.2	–	V
VIHT2	Input High Threshold Voltage (Schmitt trigger)	TCC, INT	–	3.75	–	V
VILT2	Input Low Threshold Voltage (Schmitt trigger)	TCC, INT	–	1.25	–	V
VIHX1	Clock Input High Voltage	OSCI in crystal mode	–	3.5	–	V
VILX1	Clock Input Low Voltage	OSCI in crystal mode	–	1.5	–	V
IOH1	Output High Voltage (Ports 5, 6, 7, 8)	VOH = VDD-0.5V	–	-11.5	–	mA
IOL1	Output Low Voltage (Ports 5, 6,7,8)	VOL = GND+0.5V	–	22.5	–	mA

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
IPH	Pull-high current	Pull-high active, input pin at VSS	70	–	100	µA
IPL	Pull-low current	Pull-low active, input pin at Vdd	25	–	50	µA
ISB1	Power down current	All input and I/O pins at VDD, Output pin floating, WDT disabled LVR disabled, LVD disabled	–	2	–	µA
ISB2	Power down current	All input and I/O pins at VDD, Output pin floating, WDT enabled, LVR disabled, LVD disabled	–	10	–	µA
ISB3	Power down current	All input and I/O pins at VDD, Output pin floating, WDT disabled LVR enabled, LVD disabled	–	2.0	–	µA
ICC1	Operating supply current at two clocks	/RESET= 'High', Fosc=32.768kHz (Crystal type, CLKS="0"), Output pin floating, WDT disabled LVR disabled, LVD disabled	–	25	35	µA
ICC2	Operating supply current at two clocks	/RESET= 'High', Fosc=32.768kHz (Crystal type, CLKS="0"), Output pin floating, WDT enabled LVR disabled, LVD disabled	–	30	42	µA
ICC3	Operating supply current at two clocks	/RESET= 'High', Fosc=4 MHz (Crystal type, CLKS="0"), Output pin floating, WDT enabled LVR disabled, LVD disabled	–	2.0	2.4	mA
ICC4	Operating supply current at two clocks	/RESET= 'High', Fosc=10 MHz (Crystal type, CLKS="0"), Output pin floating, WDT enabled LVR disabled, LVD disabled	–	3.2	3.7	mA

Ta = 85°C, VDD = 5.0V, VSS = 0V

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
FXT	Crystal: VDD to 5V	Two cycle with two clocks	DC	–	20	MHz
	ERC: VDD to 5V	R: 5.1KΩ, C: 300 pF	F±30%	360	F±30%	kHz
IRC1	IRC: VDD to 5V	RCM0:RCM1=1:1	3.44	3.8	4.56	MHz
IRC2	IRC: VDD to 5V	RCM0:RCM1=1:0	6.88	7.6	9.12	MHz
IRC3	IRC: VDD to 5V	RCM0:RCM1=0:1	0.86	0.95	1.14	MHz
IRC4	IRC: VDD to 5V	RCM0:RCM1=0:0	391.3	432.2	518.7	kHz
VIHRC	Input High Threshold Voltage (Schmitt trigger)	OSCI in RC mode	–	3.4	–	V
VILRC	Input Low Threshold Voltage (Schmitt trigger)	OSCI in RC mode	–	1.4	–	V
IIL	Input Leakage Current for input pins	VIN = VDD, VSS	–1.0	0	1.0	μA
VIH1	Input High Voltage (Schmitt trigger)	Ports 5, 6, 7, 8	–	2.6	–	V
VIL1	Input Low Voltage (Schmitt trigger)	Ports 5, 6, 7, 8	–	2.2	–	V
VIHT1	Input High Threshold Voltage (Schmitt trigger)	/RESET	–	1.8	–	V
VILT1	Input Low Threshold Voltage (Schmitt trigger)	/RESET	–	1.1	–	V
VIHT2	Input High Threshold Voltage (Schmitt trigger)	TCC, INT	–	3.75	–	V
VILT2	Input Low Threshold Voltage (Schmitt trigger)	TCC, INT	–	1.25	–	V
VIHX1	Clock Input High Voltage	OSCI in crystal mode	–	3.4	–	V
VILX1	Clock Input Low Voltage	OSCI in crystal mode	–	1.4	–	V
IOH1	Output High Voltage (Ports 5, 6, 7, 8)	VOH = VDD-0.5V	–	-10.5	–	mA
IOL1	Output Low Voltage (Ports 5, 6,7,8)	VOL = GND+0.5V	–	19	–	mA

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
IPH	Pull-high current	Pull-high active, input pin at VSS	70	–	100	μA
IPL	Pull-low current	Pull-low active, input pin at Vdd	25	–	50	μA
ISB1	Power down current	All input and I/O pins at VDD, Output pin floating, WDT disabled LVR disabled, LVD disabled	–	2	–	μA
ISB2	Power down current	All input and I/O pins at VDD, Output pin floating, WDT enabled, LVR disabled, LVD disabled	–	10	–	μA
ISB3	Power down current	All input and I/O pins at VDD, Output pin floating, WDT disabled LVR enabled, LVD disabled	–	2.0	–	μA
ICC1	Operating supply current at two clocks	/RESET= 'High', Fosc=32.768kHz (Crystal type, CLKS="0"), Output pin floating, WDT disabled LVR disabled, LVD disabled	–	30	40	μA
ICC2	Operating supply current at two clocks	/RESET= 'High', Fosc=32.768kHz (Crystal type, CLKS="0"), Output pin floating, WDT enabled LVR disabled, LVD disabled	–	35	45	μA
ICC3	Operating supply current at two clocks	/RESET= 'High', Fosc=4 MHz (Crystal type, CLKS="0"), Output pin floating, WDT enabled LVR disabled, LVD disabled	–	1.7	2.2	mA
ICC4	Operating supply current at two clocks	/RESET= 'High', Fosc=10 MHz (Crystal type, CLKS="0"), Output pin floating, WDT enabled LVR disabled, LVD disabled	–	3.0	3.5	mA

Internal RC Electrical Characteristics (Ta=25°C, VDD=5V, VSS=0V)

Internal RC	Drift Rate				
	Temperature	Voltage	Min.	Typ.	Max.
4 MHz	25°C	5V	3.84 MHz	4 MHz	4.16 MHz
8 MHz	25°C	5V	7.68 MHz	8 MHz	8.32 MHz
1 MHz	25°C	5V	0.96 MHz	1 MHz	1.04 MHz
455kHz	25°C	5V	436.8kHz	455kHz	473.2kHz

Internal RC Electrical Characteristics (Ta=-40 ~85°C, VDD=2.3~5.5V, VSS=0V)

Internal RC	Drift Rate				
	Temperature	Voltage	Min.	Typ.	Max.
4 MHz	-40~85℃	2.3~5.5V	3.44 MHz	4 MHz	4.56 MHz
8 MHz	-40~85℃	2.3~5.5V	6.88 MHz	8 MHz	9.12 MHz
1 MHz	-40~85℃	2.3~5.5V	0.86 MHz	1 MHz	1.14 MHz
455kHz	-40~85℃	2.3~5.5V	391.3kHz	455kHz	518.7kHz

9 AC Electrical Characteristics

Ta=25℃, VDD=5V ± 5%, VSS=0V

Symbol	Parameter	Conditions	Min.	Type	Max.	Unit
Dclk	Input CLK duty cycle	–	45	50	55	%
Tins	Instruction cycle time (CLKS="0")	Crystal type	100	–	DC	ns
		RC type	500	–	DC	ns
Ttcc	TCC input time period	–	(Tins+20) × N*	–	–	ns
Tdrh	Device reset hold time	Ta = 25℃	11.3	16.2	21.6	ms
Trst	/RESET pulse width	Ta = 25℃	2000	–	–	ns
Twdt	Watchdog timer duration	Ta = 25℃	11.3	16.2	21.6	ms
Tset	Input pin setup time	–	–	0	–	ns
Thold	Input pin hold time	–	15	20	25	ns
Tdelay	Output pin delay time	Cload = 20 pF	45	50	55	ns
Tdrc	ERC delay time	Ta = 25℃	1	3	5	ns

* N = selected prescaler ratio

9.1 AD Converter Characteristics

Vdd=2.5V to 5.5V, Vss=0V, Ta=25°C

Symbol		Parameter	Condition	Min.	Typ.	Max.	Unit
V_{AREF}		Analog reference voltage	V_{AREF} - V_{ASS} ≥ 2.5V	2.5	–	Vdd	V
V_{ASS}				Vss	–	Vss	V
VAI		Analog input voltage	–	VASS	–	V_{AREF}	V
IAI1	Ivdd	Analog supply current	Vdd=V_{AREF}=5.0V, V_{ASS} = 0.0V (V reference from Vdd)	750	850	1000	µA
	Ivref			-10	0	+10	µA
IAI2	Ivdd	Analog supply current	Vdd=V_{AREF}=5.0V, V_{ASS} = 0.0V (V reference from VREF)	500	600	820	µA
	IVref			200	250	300	µA
IOP		OP current	Vdd=5.0V, OP used Output voltage swing 0.2V to 4.8V	450	550	650	µA
RN1		Resolution	ADREF=0, Internal VDD Vdd=5.0V, VASS=0.0V	–	9	10	Bits
RN2		Resolution	ADREF=1, External VREF VDD=VREF=5.0V, VSS = 0.0V	–	11	12	Bits
LN1		Linearity error	Vdd = 2.5 to 5.5V Ta=25℃	–	3	–	LSB
LN2		Linearity error	VDD= 2.5 to 5.5V Ta=25℃	–	2	–	LSB
DNL		Differential nonlinear error	Vdd = 2.5 to 5.5V Ta=25℃	0	± 0.5	± 0.9	LSB
FSE1		Full scale error	Vdd = V_{AREF} = 5.0V, V_{ASS} = 0.0V	–	–	–	LSB
FSE2		Full scale error	VDD = VREF = 5.0V, VSS = 0.0V	–	2	–	LSB
OE		Offset error	Vdd = V_{AREF} = 5.0V, V_{ASS} = 0.0V	–	1	–	LSB
ZAI		Recommended impedance of analog voltage source	–	0	8	10	KΩ
TAD		ADC clock duration	Vdd = V_{AREF} = 5.0V, V_{ASS} = 0V	4	–	–	µs
TCN		AD conversion time	Vdd = V_{AREF} = 5.0V, V_{ASS} = 0V	15	–	15	TAD
ADIV		ADC OP input voltage range	Vdd = V_{AREF} = 5.0V, V_{ASS} = 0V	0	–	V_{AREF}	V
ADOV		ADC OP output voltage swing	Vdd = V_{AREF} = 5.0V, V_{ASS} = 0.0V, RL=10KΩ	0	0.2	0.3	V
				4.7	4.8	5	
ADSR		ADC OP slew rate	Vdd = V_{AREF} = 5.0V, V_{ASS} = 0V	0.1	0.3	–	V/µs
PSR		Power Supply Rejection	Vdd = 5.0V ± 0.5V	± 0	–	± 2	LSB

Note: *1. These parameters are hypothetical (not tested) and are provided for design reference only.*

2. There is no current consumption when ADC is off other than minor leakage current.

3. AD conversion result will not decrease when the input voltage is increased, and no missing code will result.

4. These parameters are subject to change without prior notice.

10 Device Characteristics

The graphs provided in the following pages were derived based on a limited number of samples and are shown here for reference only. The device characteristics illustrated are not guaranteed for its accuracy. In some graphs, the data maybe out of the specified warranted operating range.

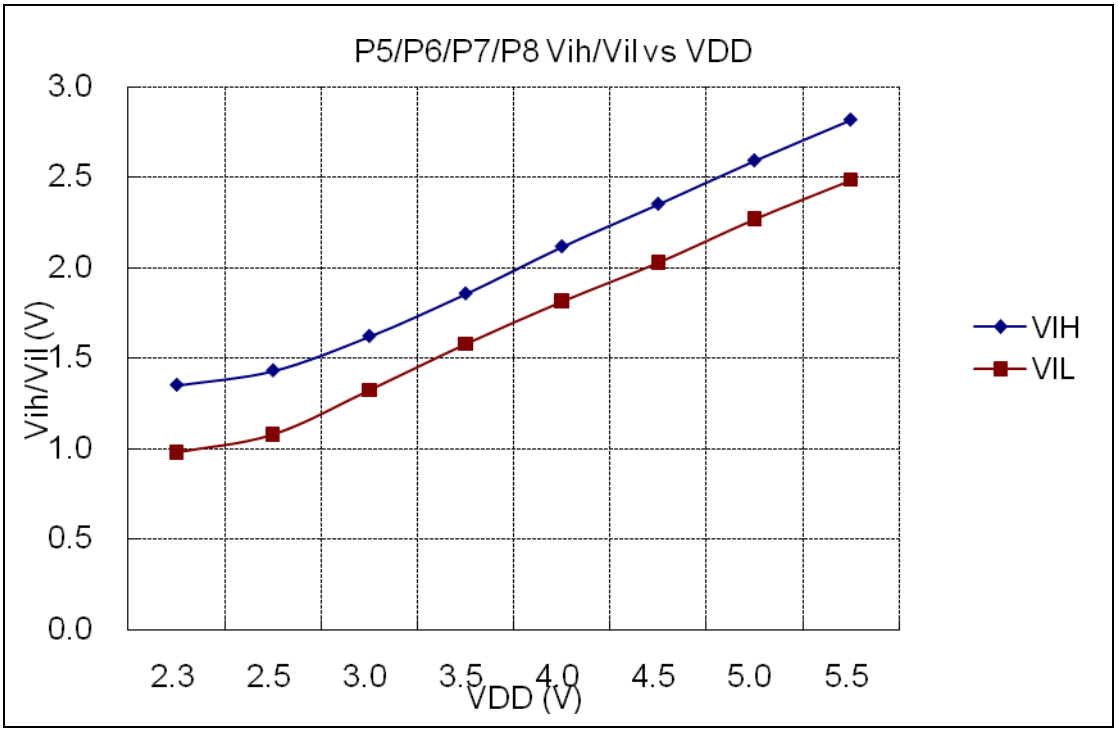


Figure 10-1 Vih, Vil vs VDD

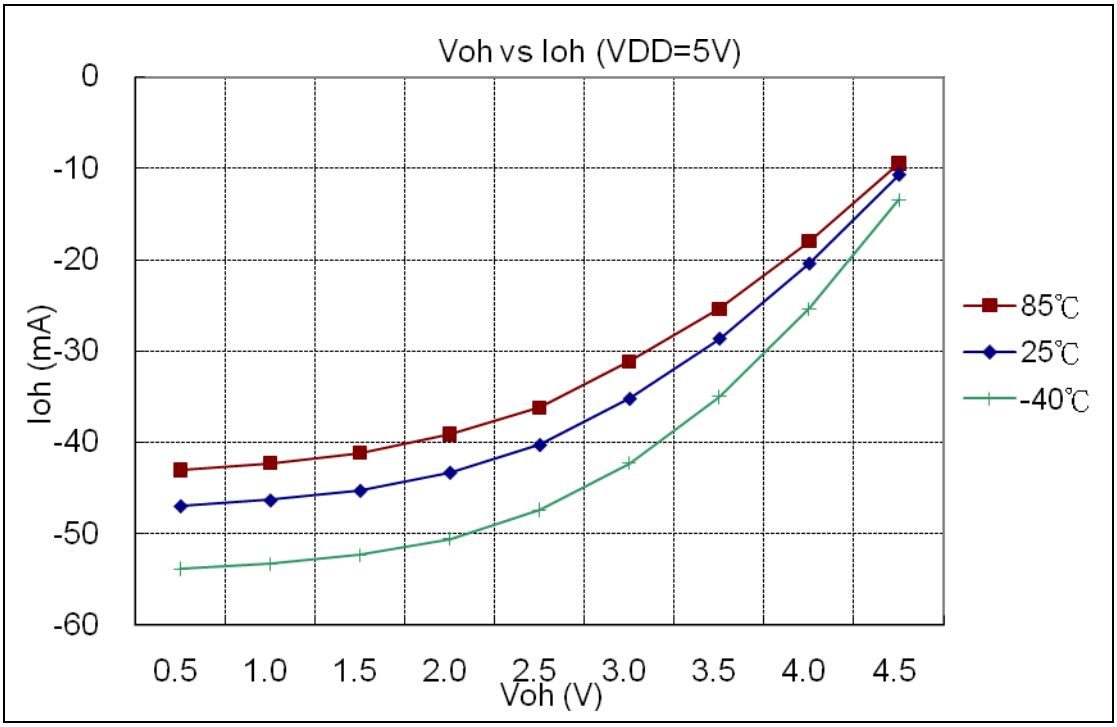


Figure 10-2 Voh vs Ioh, VDD=5V

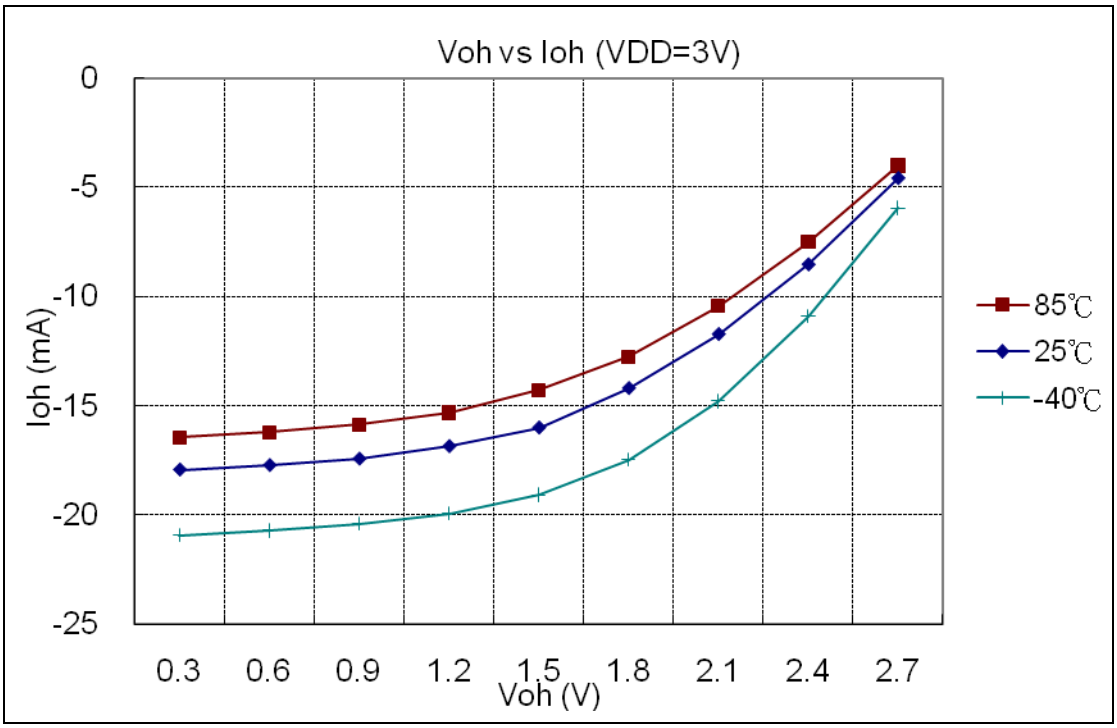


Figure 10-3 Voh vs Ioh, VDD=3V

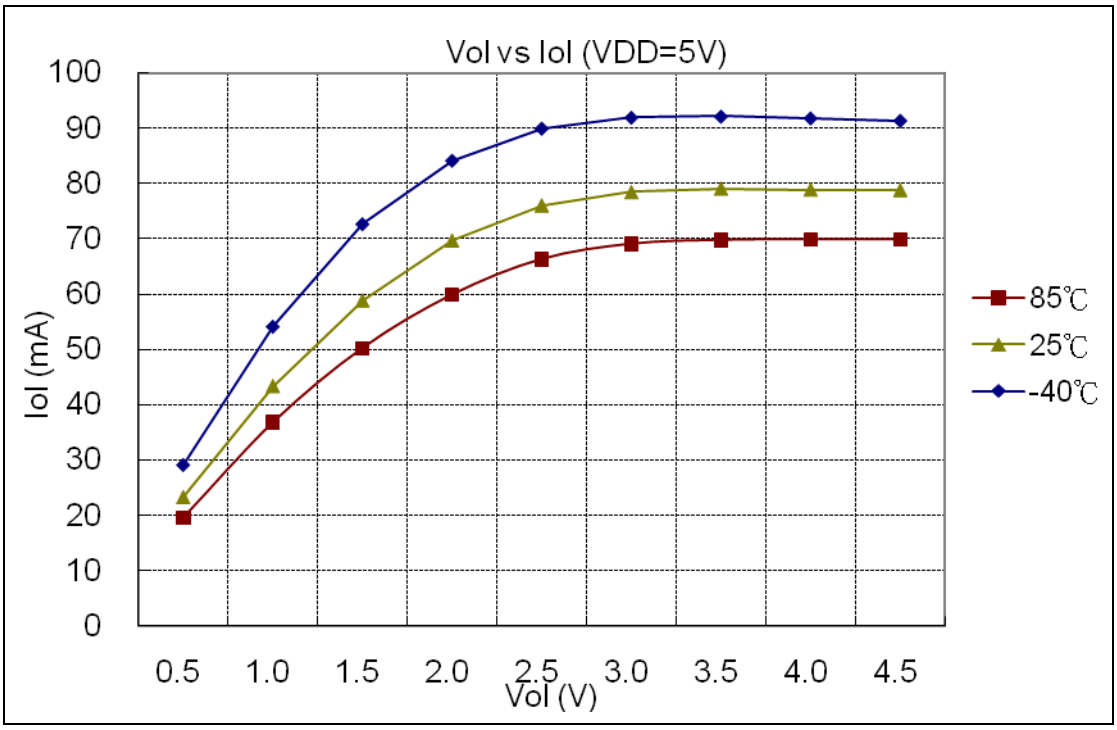


Figure 10-4 Vol vs Iol, VDD=5V

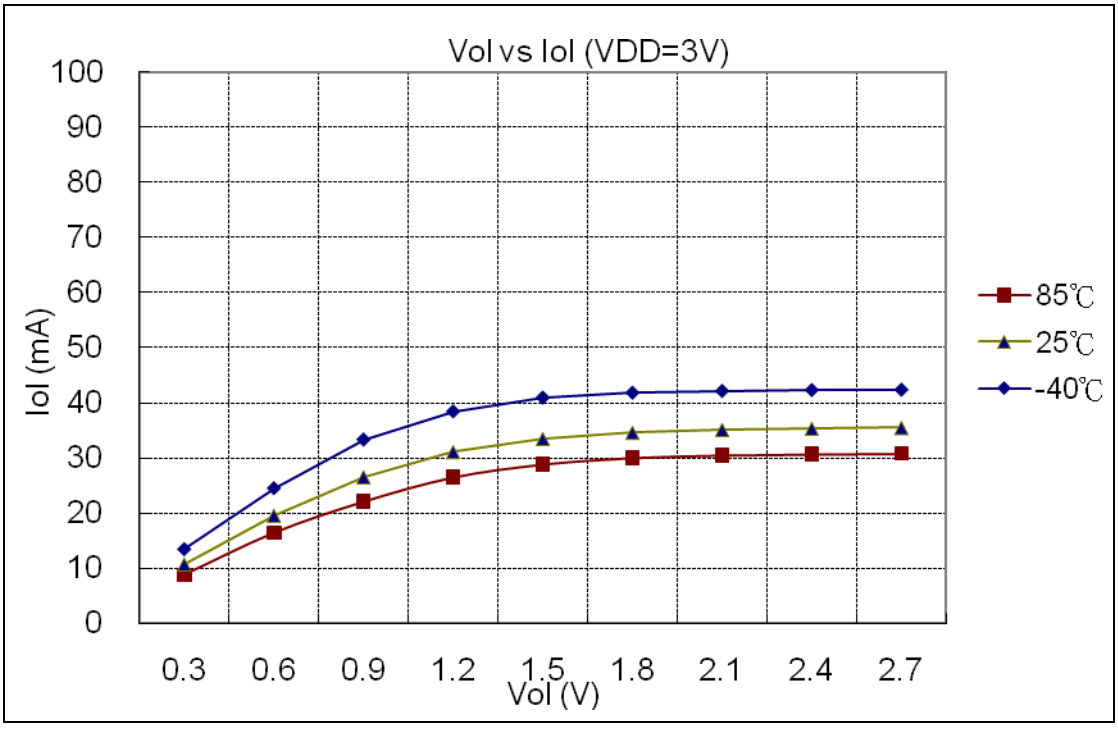


Figure 10-5 Vol vs Iol, VDD=3V

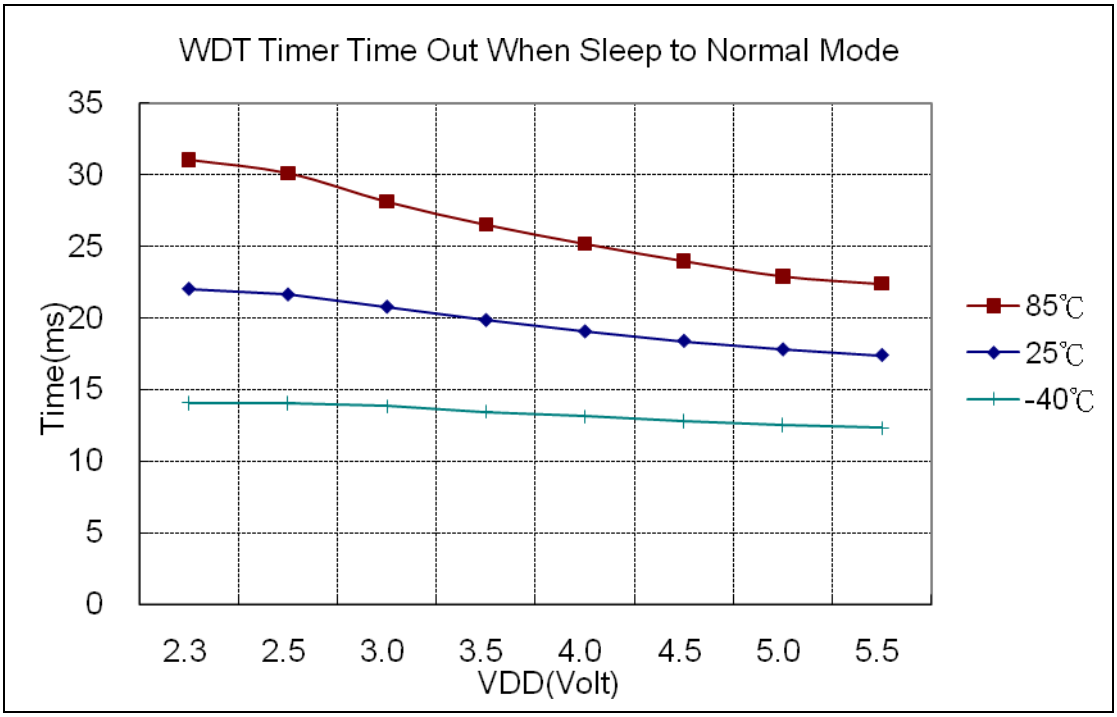


Figure 10-6 WDT Time out Period vs VDD, with Prescaler set to 1:1

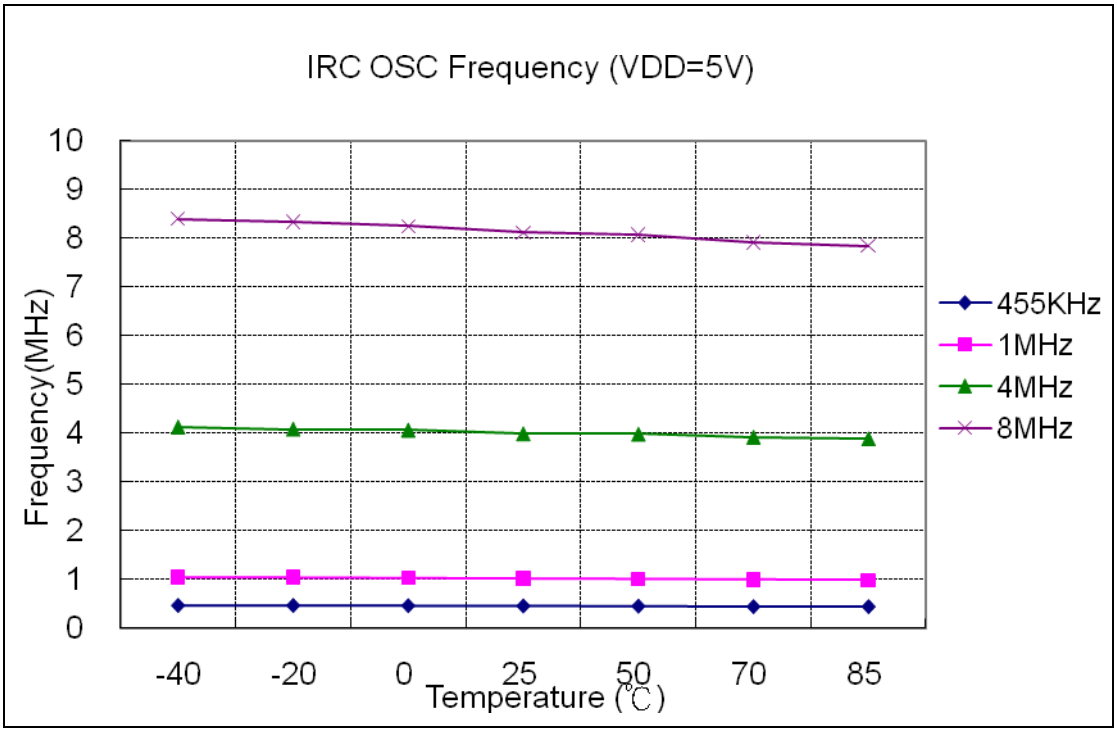


Figure 10-7 IRC Fosc vs VDD=5V

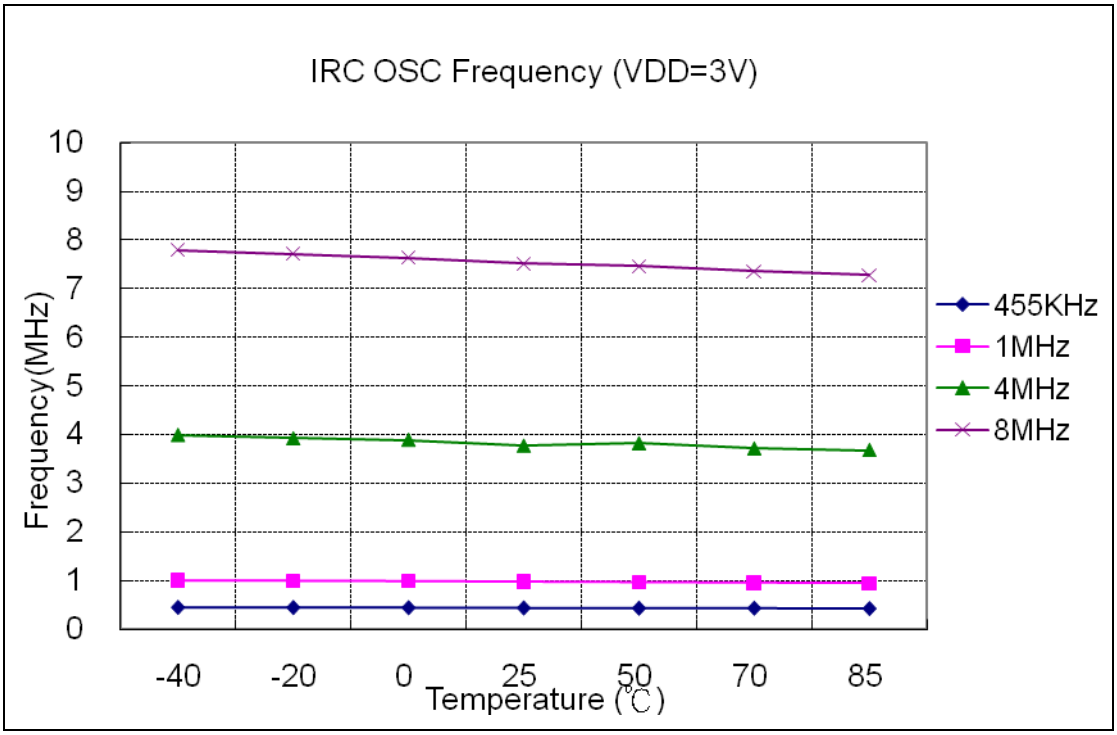


Figure 10-8 IRC Fosc vs VDD=3V

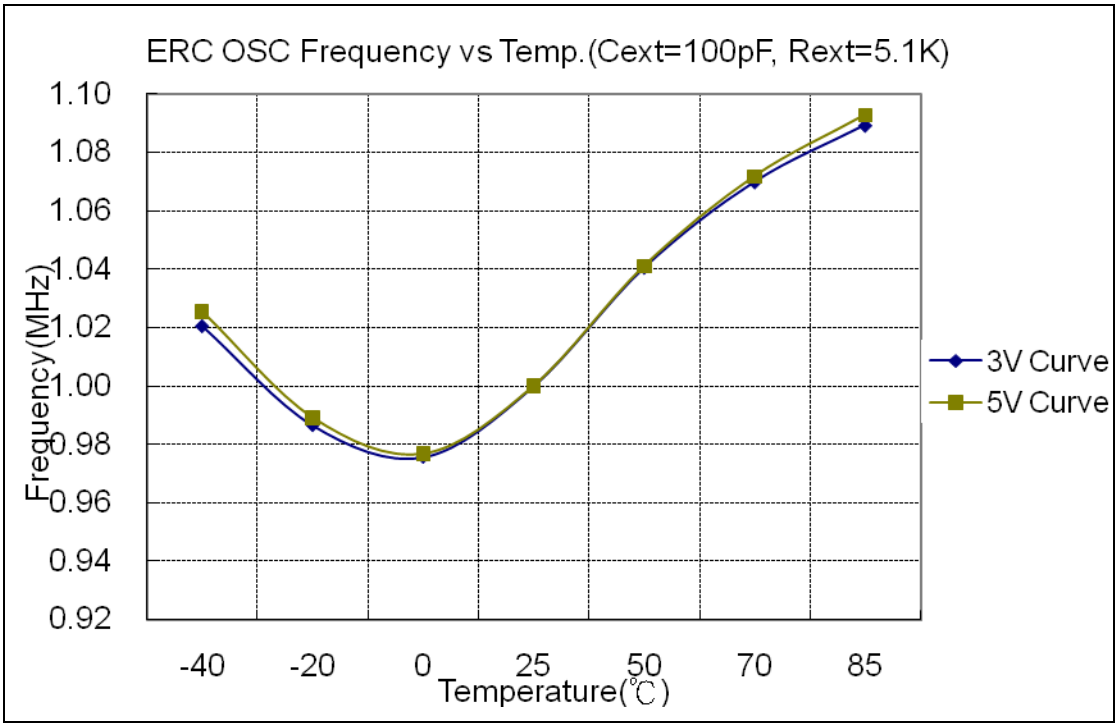


Figure 10-9 ERC Fosc vs VDD

There are three conditions with the Standby Current ISB1, ISB2, and ISB3. These conditions are as follows:

ISB1: WDT disable, LVR disable (Sleep mode)

ISB2: WDT enable, LVR disable (Sleep mode)

ISB3: WDT disable, LVR enable (Sleep mode)

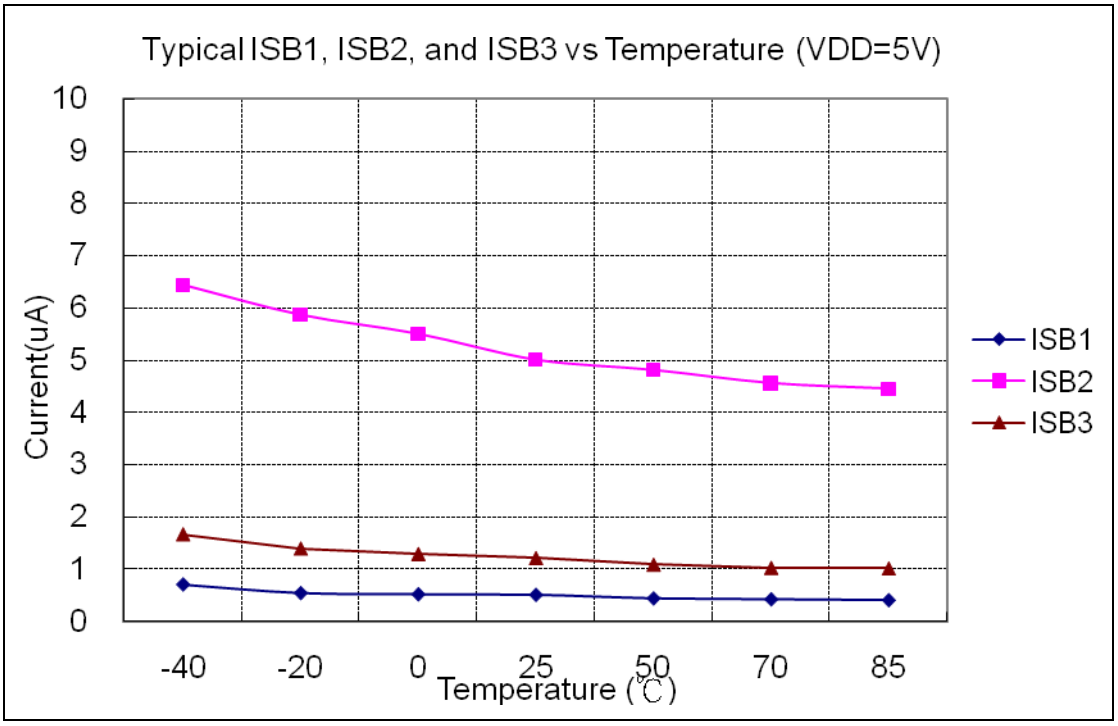


Figure 10-10 Typical Standby Current (VDD=5V) vs Temperature

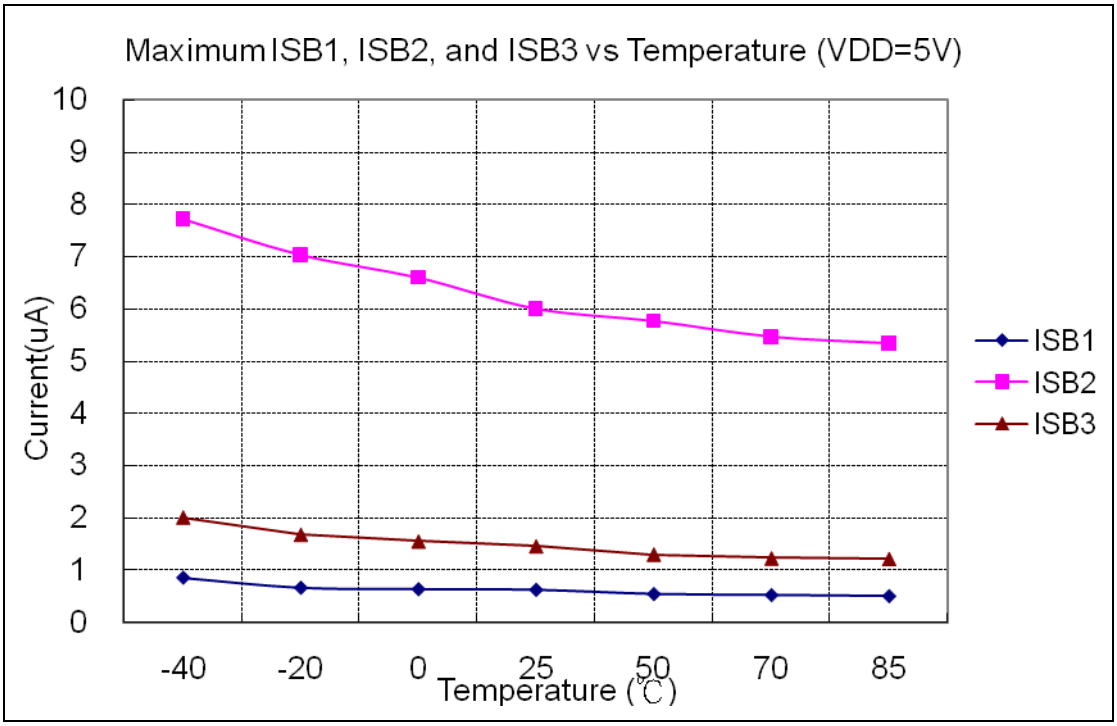


Figure 10-11 Maximum Standby Current (VDD=5V) vs Temperature

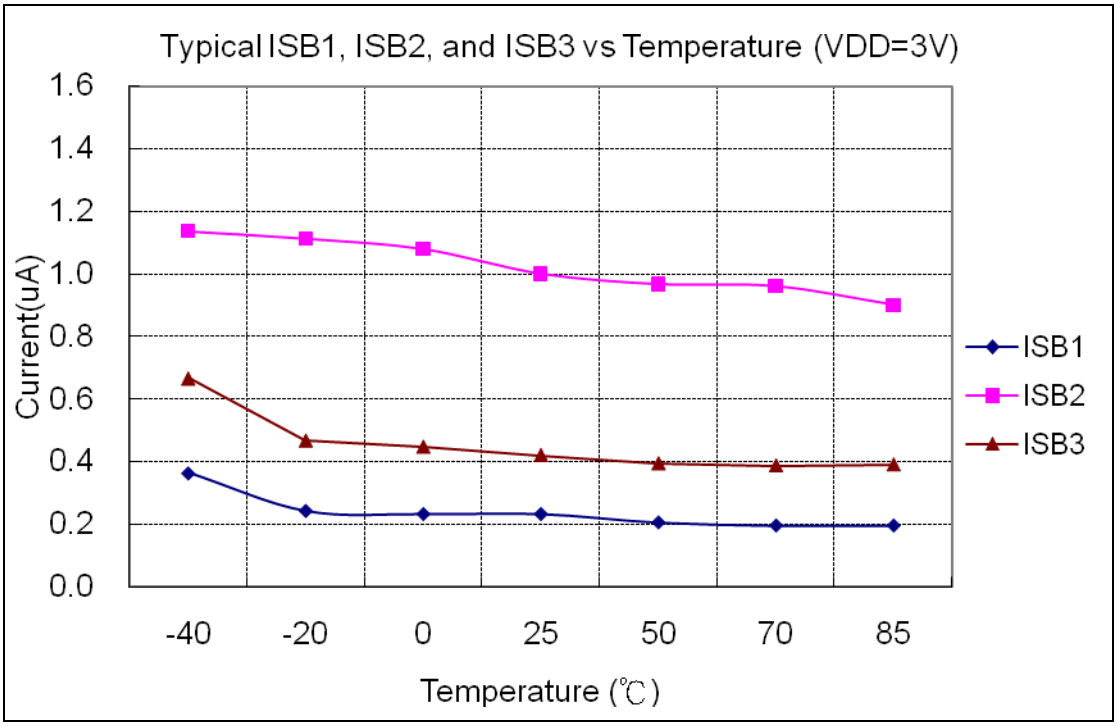


Figure 10-12 Typical Standby Current (VDD=3V) vs Temperature

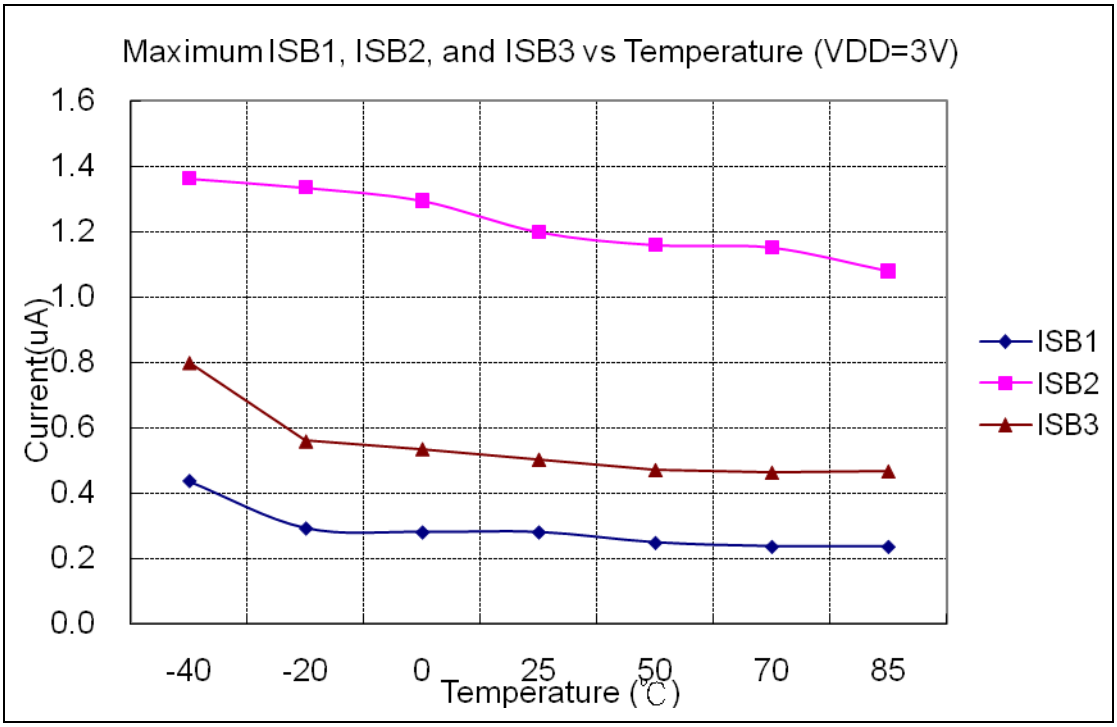


Figure 10-13 Maximum Standby Current (VDD=3V) vs Temperature

Four conditions exist with the Operating Current ICC1 to ICC4. These conditions are as follows:

ICC1: Fosc = 32.768kHz, 2 clocks, WDT disable (Normal mode)

ICC2: Fosc = 32.768kHz, 2 clocks, WDT enable (Normal mode)

ICC3: Fosc = 4 MHz, 2 clocks, WDT enable (Normal mode)

ICC4: Fosc = 10 MHz, 2 clocks, WDT enable (Normal mode)

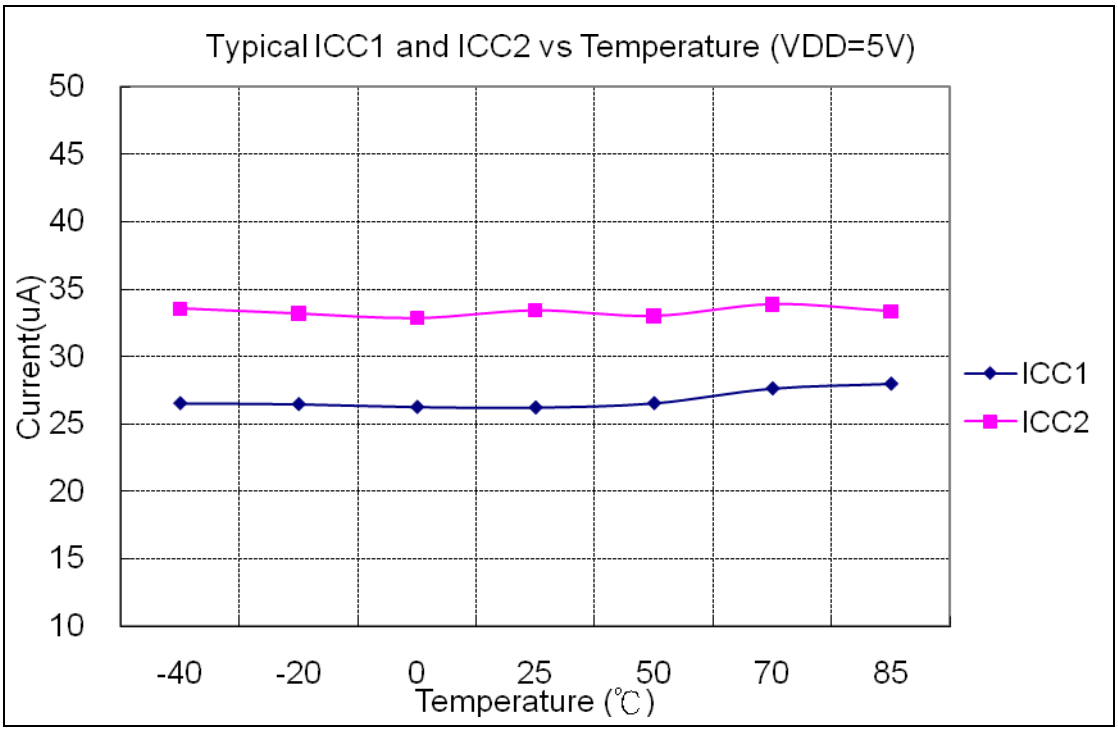


Figure 10-14 Typical operating current (VDD=5V) vs Temperature

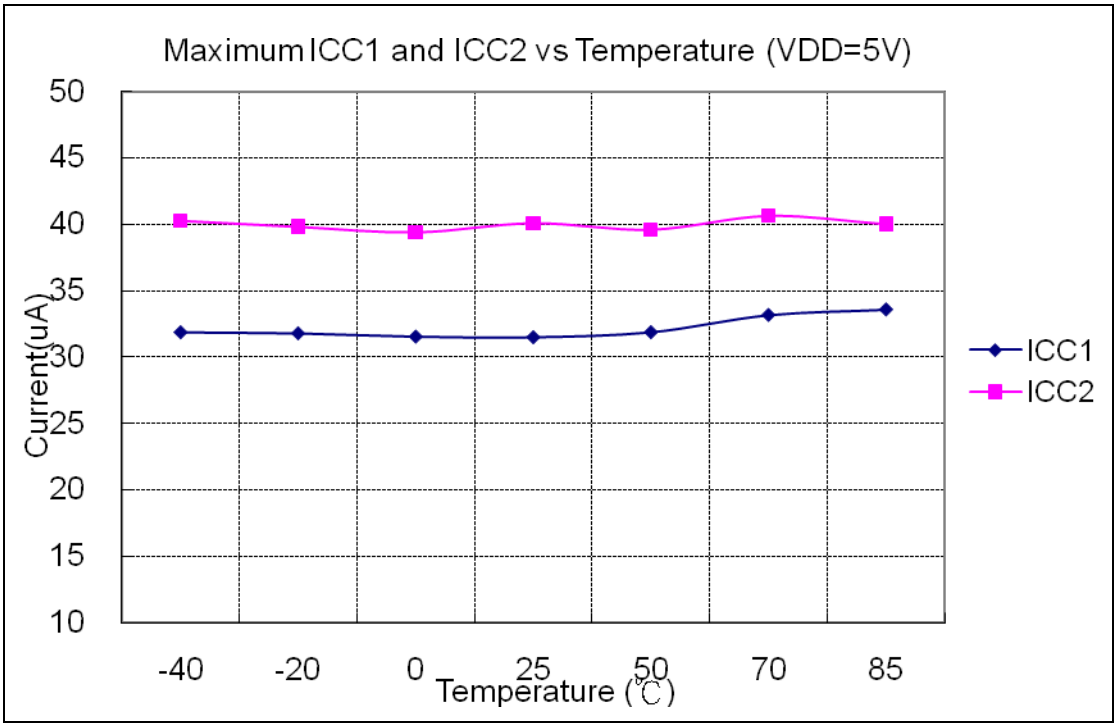


Figure 10-15 Maximum operating current (VDD=5V) vs Temperature

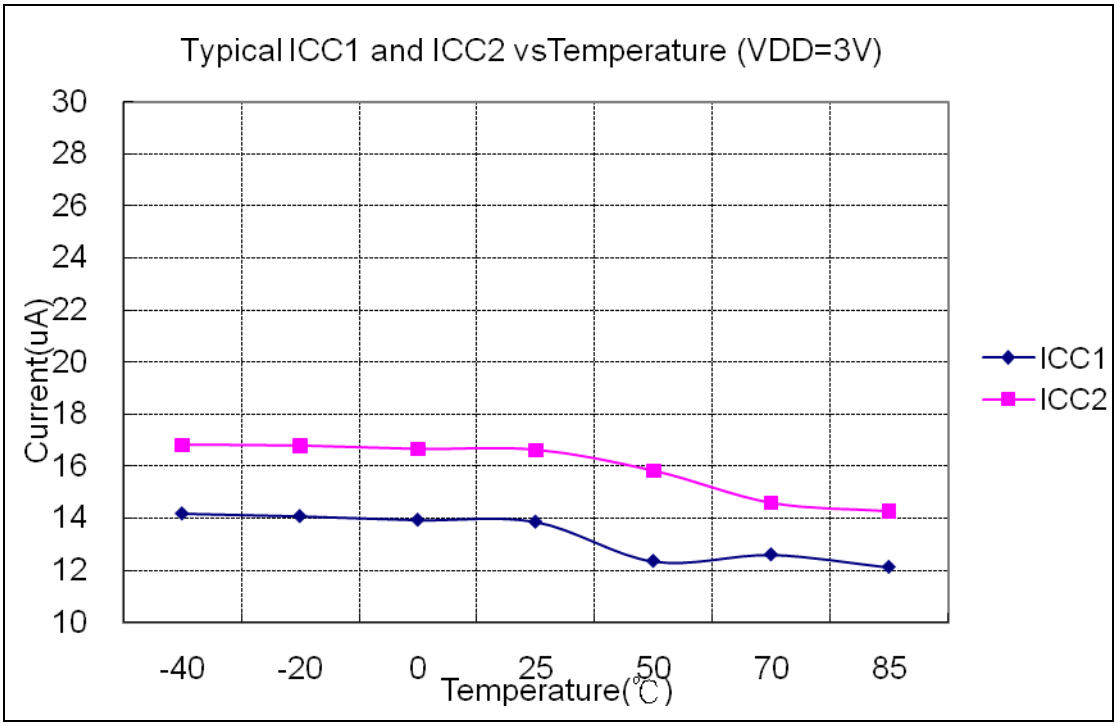


Figure 10-16 Typical operating current (VDD=3V) vs Temperature

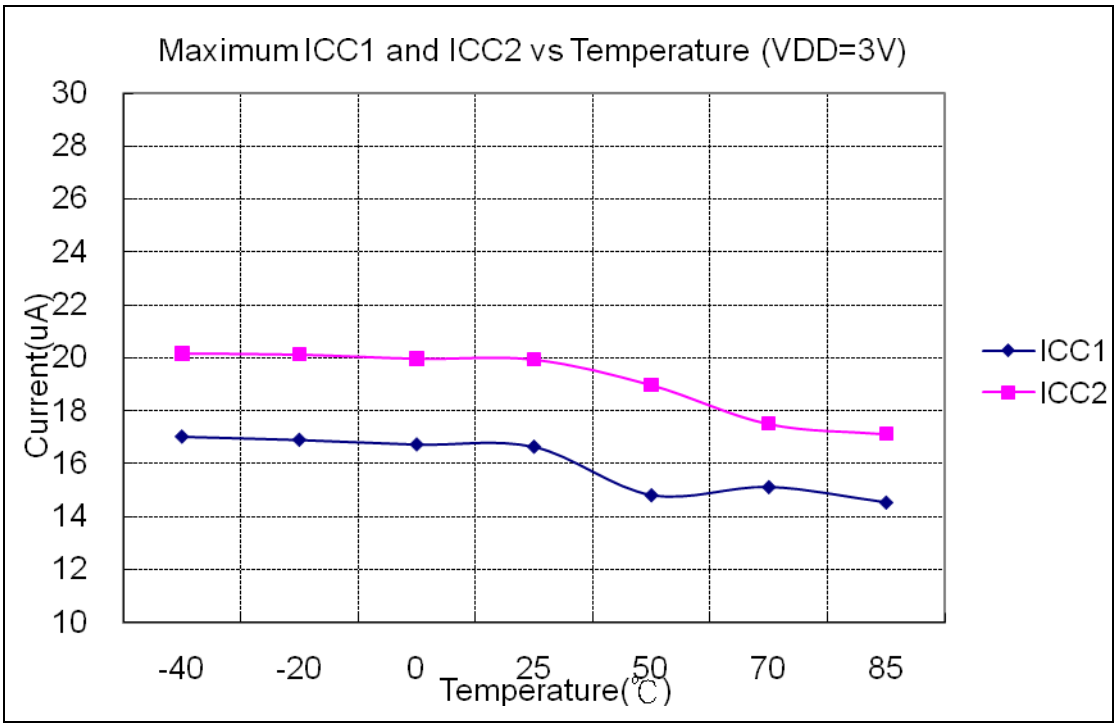


Figure 10-17 Maximum operating current (VDD=3V) vs Temperature

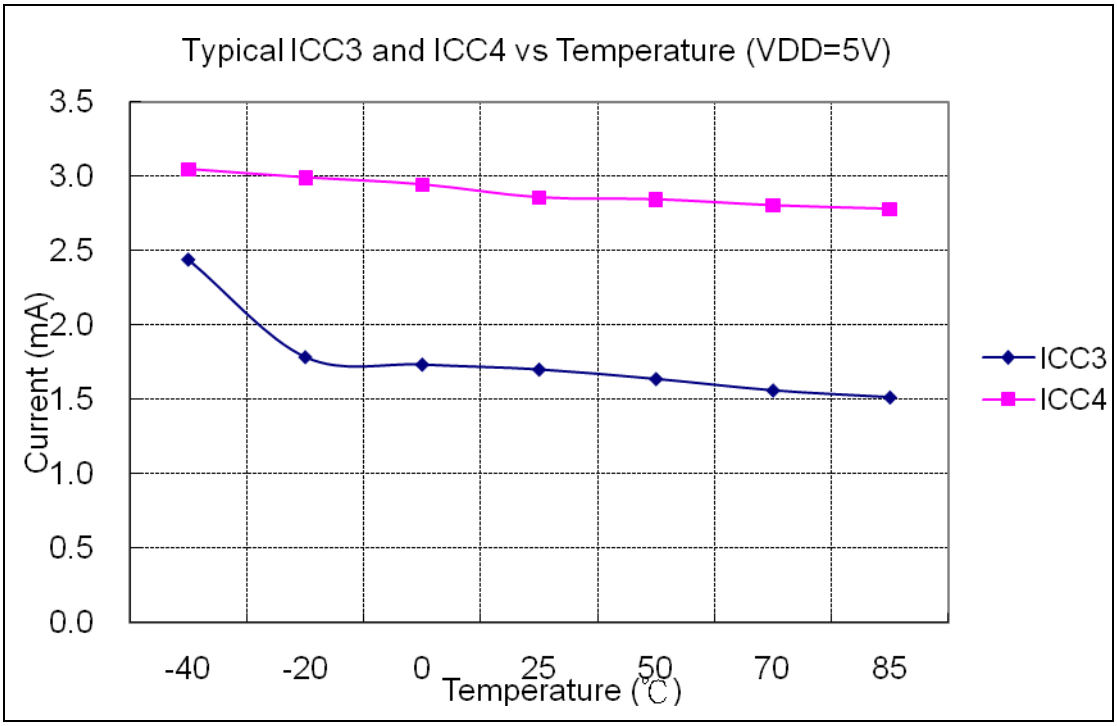


Figure 10-18 Typical operating current (VDD=5V) vs Temperature

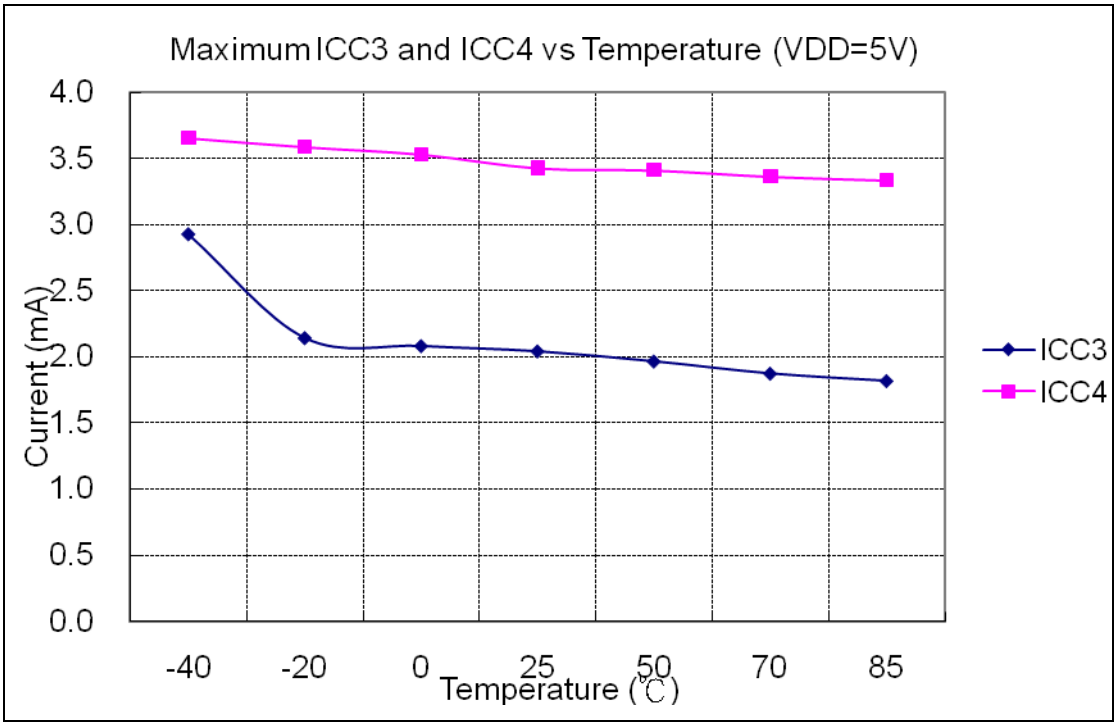


Figure 10-19 Maximum operating current (VDD=5V) vs Temperature

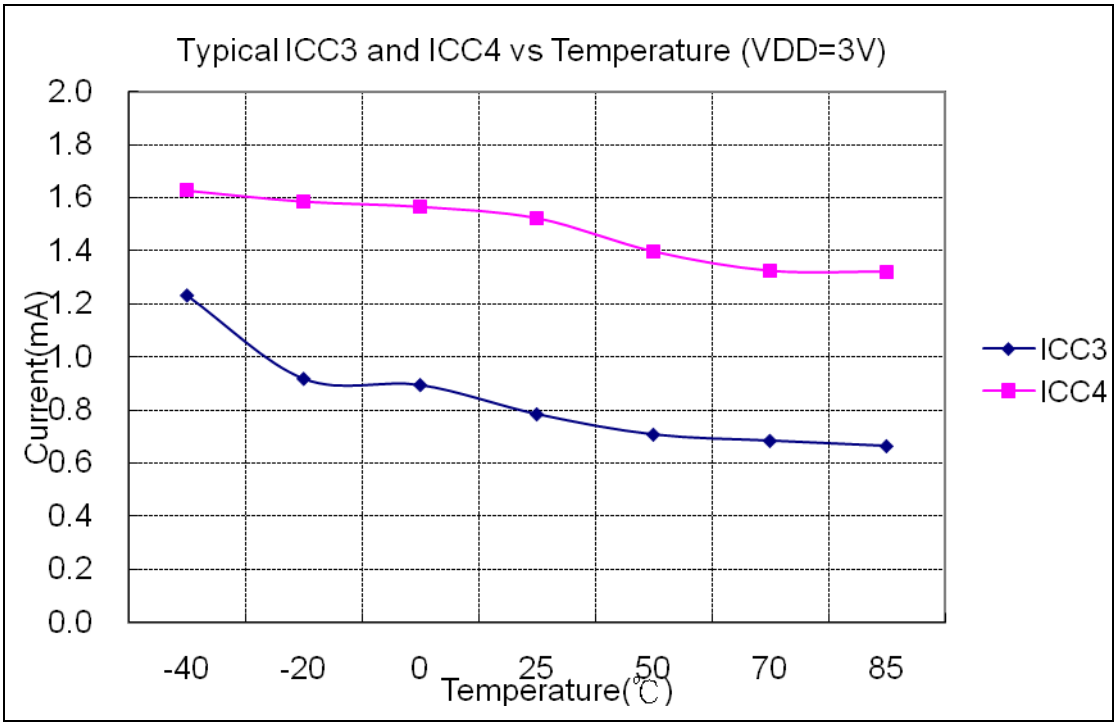


Figure 10-20 Typical operating current (VDD=3V) vs Temperature

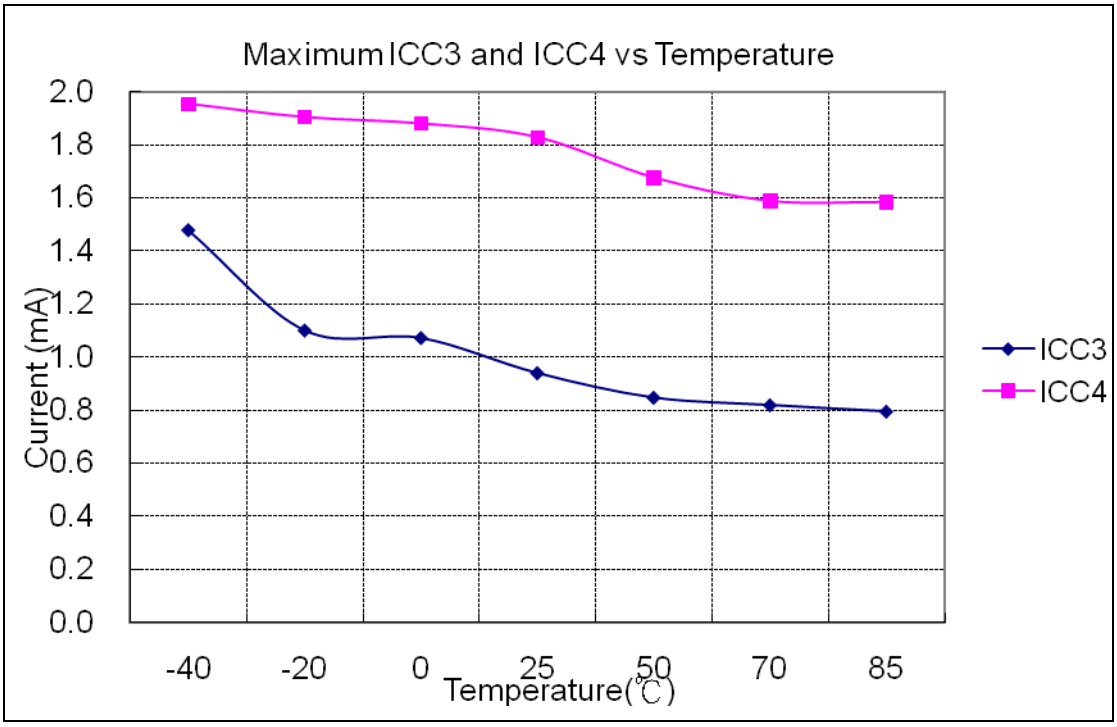
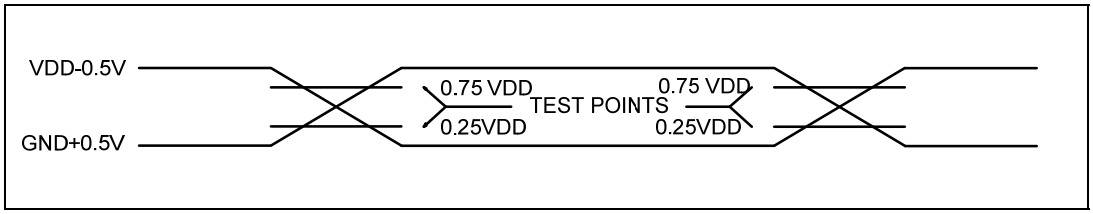


Figure 10-21 Maximum operating current (VDD=3V) vs Temperature

11 Timing Diagrams

AC Test Input/Output Waveform



Note: *AC Testing: Input is driven at VDD-0.5V for logic "**1**", and GND+0.5V for logic "**0**"*
*Timing measurements are made at 0.75V for logic "**1**", and 0.25VDD for logic "**0**"*

Figure 11-1a AC Test Input/Output Waveform Timing Diagram

Reset Timing (CLK = "0")

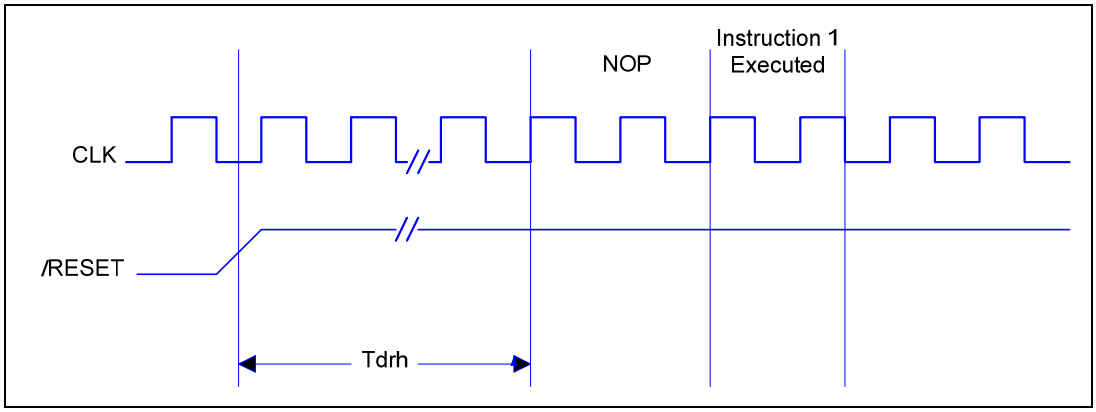


Figure 11-1b Reset Timing Diagram

TCC Input Timing (CLKS = "0")

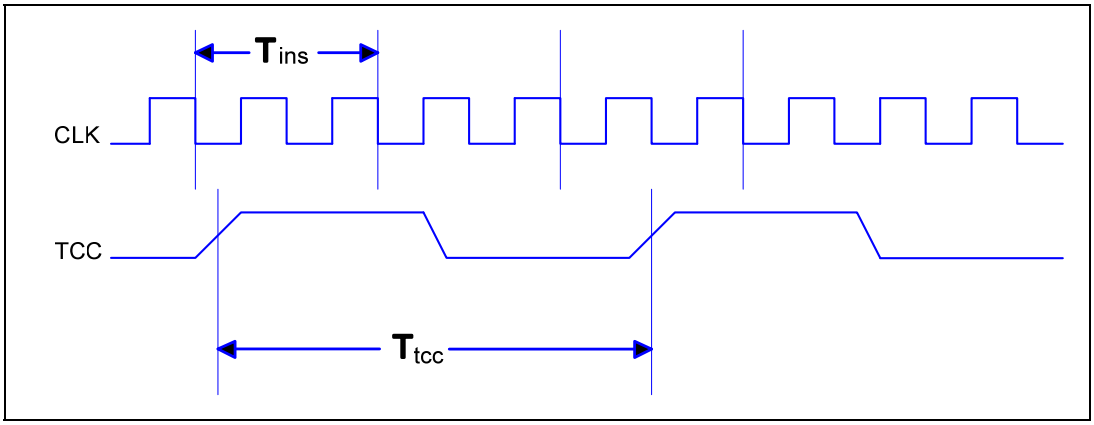


Figure 11-1c TCC Input Timing Diagram

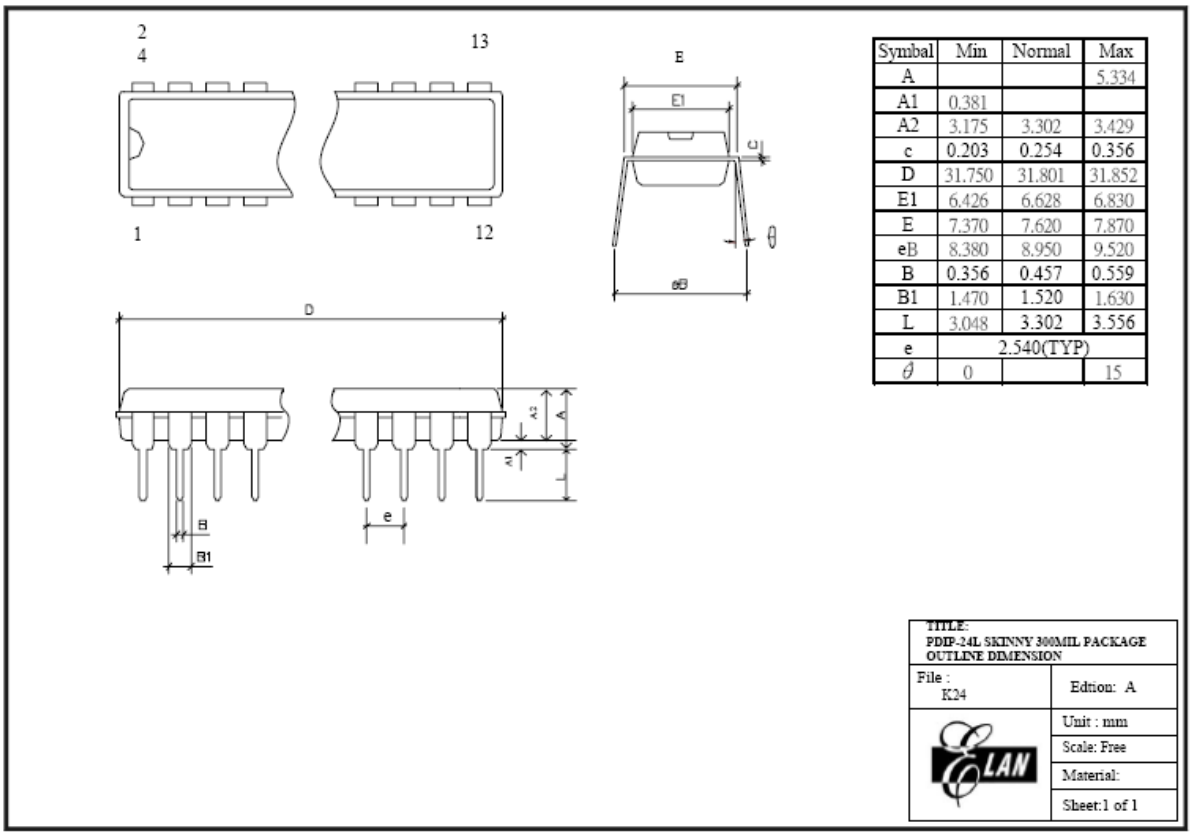
APPENDIX

A Package Type

OTP MCU	Package Type	Pin Count	Package Size
EM78P349NK24S/J	Skinny DIP	24	300 mil
EM78P349NSO24S/J	SOP	24	300 mil
EM78P349NK28S/J	Skinny DIP	28	300 mil
EM78P349NSO28S/J	SOP	28	300 mil

B Packaging Configurations

B.1 24-Lead Plastic Dual-in-Line Skinny Package (SDIP) – 300 mil

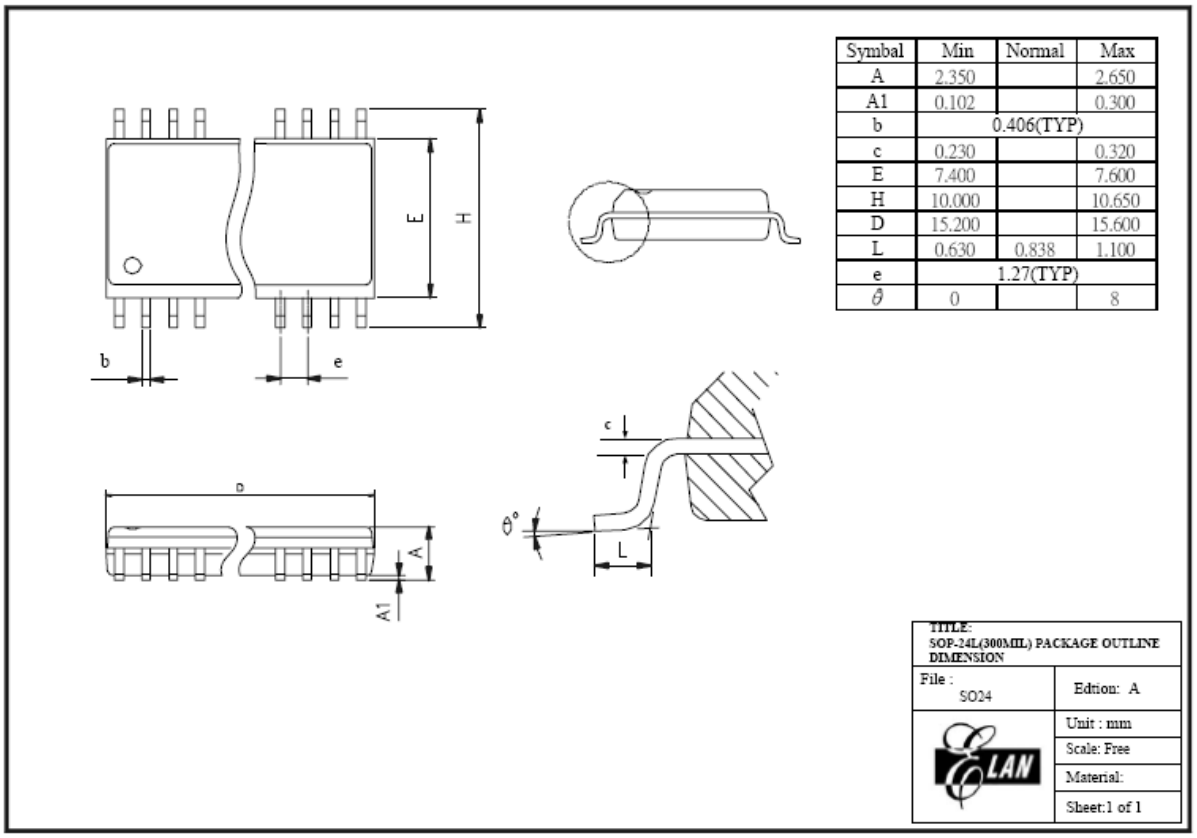


Symbal	Min	Normal	Max
A			5.334
A1	0.381		
A2	3.175	3.302	3.429
c	0.203	0.254	0.356
D	31.750	31.801	31.852
E1	6.426	6.628	6.830
E	7.370	7.620	7.870
eB	8.380	8.950	9.520
B	0.356	0.457	0.559
B1	1.470	1.520	1.630
L	3.048	3.302	3.556
e	2.540(TYP)		
θ	0		15

TITLE:
PDIP-24L SKINNY 300MIL PACKAGE OUTLINE DIMENSION

File : K24 | Edtion: A
Unit : mm
Scale: Free
Material:
Sheet:1 of 1

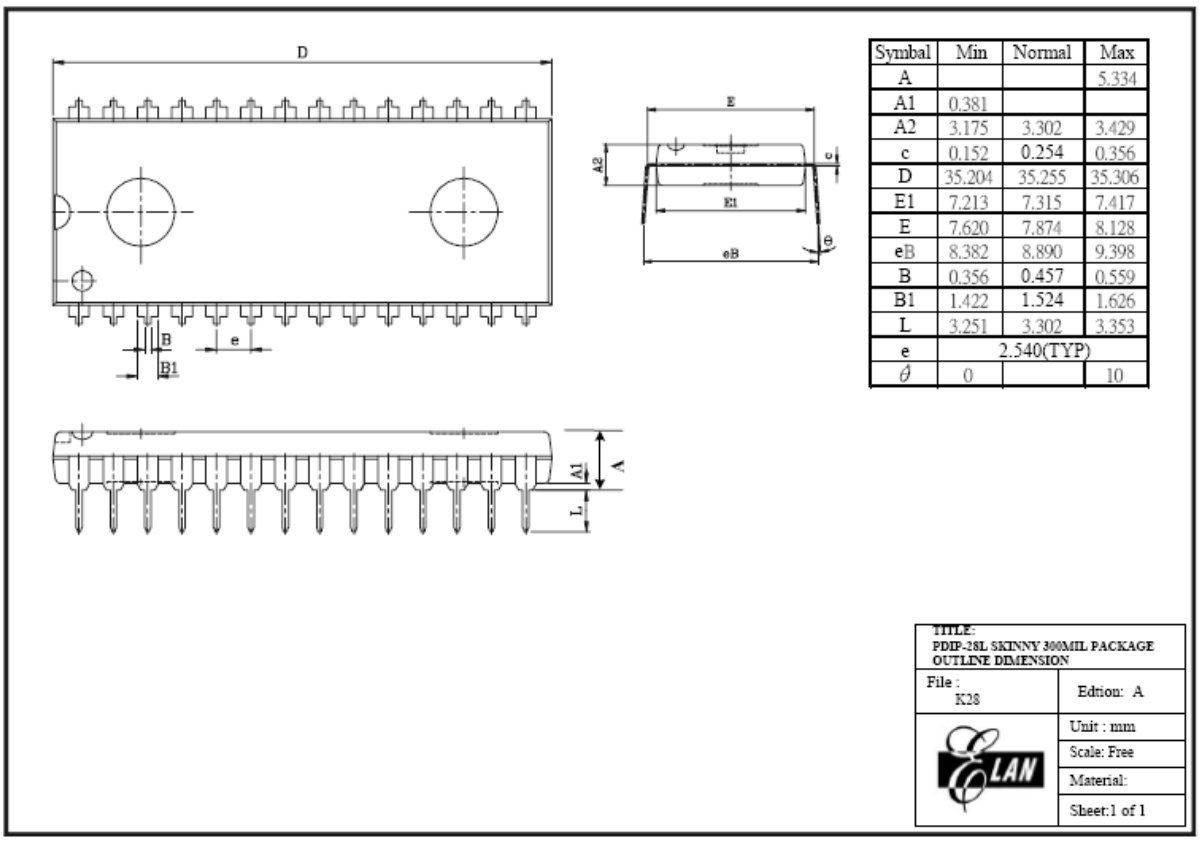
B.2 24-Lead Plastic Small Outline Package (SOP) – 300 mil



Symbal	Min	Normal	Max
A	2.350		2.650
A1	0.102		0.300
b	0.406(TYP)		
c	0.230		0.320
E	7.400		7.600
H	10.000		10.650
D	15.200		15.600
L	0.630	0.838	1.100
e	1.27(TYP)		
θ	0		8

TITLE: SOP-24L(300MIL) PACKAGE OUTLINE DIMENSION	
File : SO24	Edtion: A
	Unit : mm
	Scale: Free
	Material:
	Sheet:1 of 1

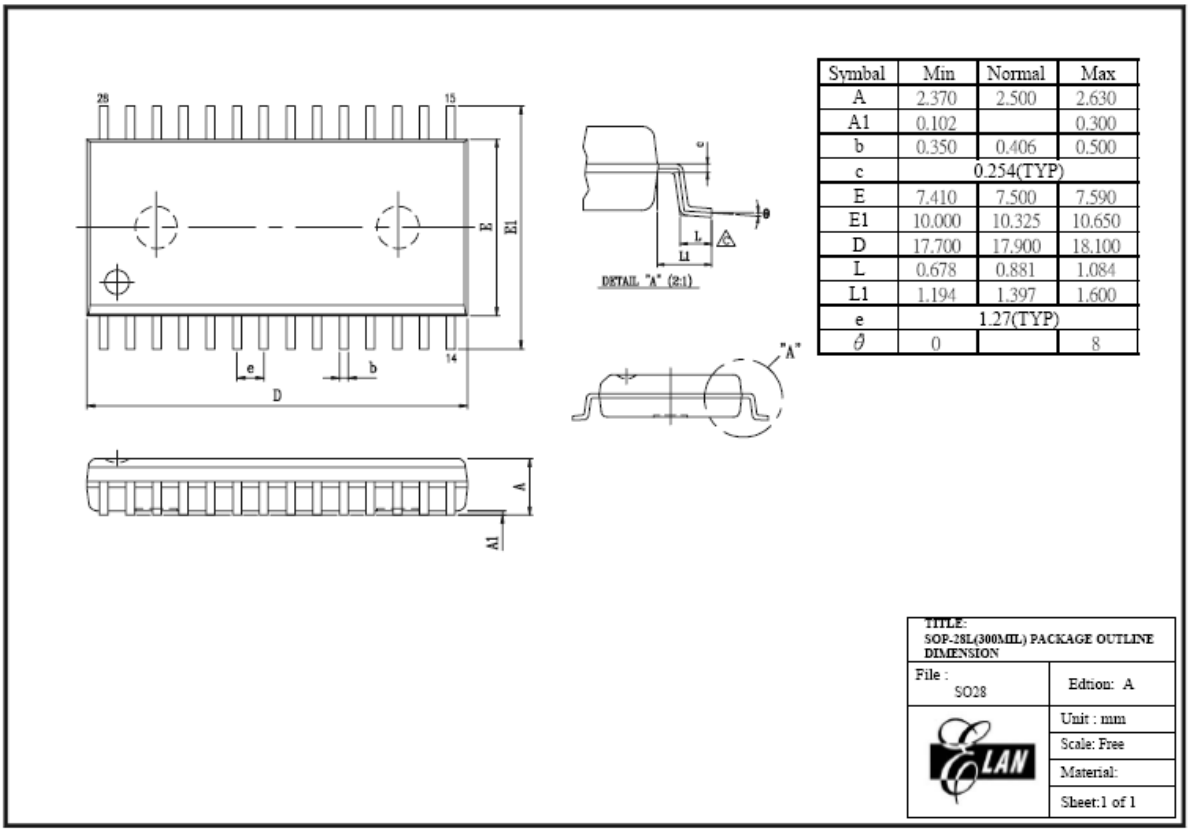
B.3 28-Lead Plastic Dual-in-Line Skinny Package (SDIP) – 300 mil



Symbal	Min	Normal	Max
A			5.334
A1	0.381		
A2	3.175	3.302	3.429
c	0.152	0.254	0.356
D	35.204	35.255	35.306
E1	7.213	7.315	7.417
E	7.620	7.874	8.128
eB	8.382	8.890	9.398
B	0.356	0.457	0.559
B1	1.422	1.524	1.626
L	3.251	3.302	3.353
e	2.540(TYP)		
θ	0		10

TITLE: PDIP-28L SKINNY 300MIL PACKAGE OUTLINE DIMENSION	
File : K28	Edition: A
	Unit : mm
	Scale: Free
	Material:
	Sheet:1 of 1

B.4 28-Lead Plastic Small Outline Package (SOP) – 300 mil



Symbal	Min	Normal	Max
A	2.370	2.500	2.630
A1	0.102		0.300
b	0.350	0.406	0.500
c		0.254(TYP)	
E	7.410	7.500	7.590
E1	10.000	10.325	10.650
D	17.700	17.900	18.100
L	0.678	0.881	1.084
L1	1.194	1.397	1.600
e		1.27(TYP)	
θ	0		8