EM78P374N

8-Bit Microcontroller

Product Specification

DOC. VERSION 1.5

ELAN MICROELECTRONICS CORP.

August 2014

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APPENDIX

Specification Revision History

Doc. Version	Revision Description	Date
1.0	Initial version	2011/04/26
1.1	1. Modified the Features 2. Modified the AD description 3. Modified the DC and AC Electrical Characteristics 4. Deleted VREFN	2011/08/17
1.2	1. Modified the Code Option Word 0 and Word 2	2012/08/30
1.3	1. Added LVR specification in the DC Electrical Characteristics section	2013/01/22
1.4	1. Removed the dead time register from Section 6.8.2 2. Removed dead time from Figure 6-13a 3. Modified VIH/VIL in Section 8	2014/01/06
1.5	1. Modified the discription of Section 6.2 2. Modified Code Option 0-HLP in Section 6.16.1 3. Modified Code Option 1-C5~C0 in Section 6.16.2 4. Modified Code Option 2-SC3~SC0 in Section 6.16.3	2014/08/27

1 General Description

The EM78P374N is an 8-bit microprocessor designed and developed with low-power, high-speed CMOS technology. It is used for 15 bits kernel simulation and it simulates the 4K×15-bit programmable ROM and 304×8-bit In-system programmable SRAM. Using the ICE370N, users can develop their program for ELAN's several OTP types of IC.

2 Features

- CPU Configuration
  - Support 4K×15 bits program ROM
  - 304×8 bits on-chip registers (SRAM)
  - More than 10 years data retention
  - 8-level stacks for subroutine nesting
  - Dual clock operation mode
  - Four programmable Level Voltage Detector (LVD) : 4.5V, 4V, 3.3V, 2.2V
  - Four programmable Level Voltage Reset (LVR) : 4.0V, 3.5V, 2.7V, 1.8V (POR)
  - Power on reset level Voltage: 1.8V~1.9V
  - Less than 1.0 mA at 5V/4MHz
  - Typically 15 μA, at 3V/16kHz
  - Typically 2 μA, during sleep mode
  - Four operation modes

Mode	CPU	Main clock	Sub clock
Sleep mode	Turn off	Turn off	Turn off
Idle Mode	Turn off	Turn off	Turn on
Green mode	Turn on	Turn off	Turn on
Normal mode	Turn on	Turn on	Turn on

- I/O Port Configuration
  - 6 bi-directional I/O ports : P5, P6 and P7
  - 22 I/O pins
  - 22 Programmable open-drain I/O pins
  - 21 programmable pull-high I/O pins
  - 21 programmable pull-down I/O pins
  - 21 programmable high sink/drive I/O pins
  - External interrupt : INT0
- Operating voltage range:
  - 2.1V~5.5V at 0~70°C (commercial)
  - 2.3V~5.5V at -40~85°C (industrial)
- Operating frequency range:
  - Crystal/IRC/ERC oscillation circuit selected by code option for system clock
  - IRC oscillation circuit selected by code option for sub clock

Main Clock

- Crystal mode:
  DC ~ 16 MHz at 5~5.5V
  DC ~ 8 MHz at 3~5.5V
  DC ~ 4 MHz at 2.1V~5.5V
- IRC mode:
  DC ~ 16 MHz at 5~5.5V
  DC ~ 8 MHz/2clks at 3V~5.5V
  DC ~ 4 MHz/2clks at 2.1V~5.5V

Internal RC Frequency	Drift Rate			
	Temperature (-40°C~+85°C)	Voltage (2.5V~5.5V)	Process	Total
1 MHz	± 2%	± 1%	± 1%	± 4%
4 MHz	± 2%	± 1%	± 1%	± 4%
8 MHz	± 2%	± 1%	± 1%	± 4%
16 MHz	± 2%	± 1%	± 1%	± 4%

Sub Clock

- IRC mode: 16kHz/32kHz

- Peripheral Configuration
  - 8-bit real time clock/counter (TCC) with selective signal sources and trigger edges
  - 14+2-channels Analog-to-Digital Converter with 12-bit resolution+ 1 internal reference for Vref+.
  - One 8-bit Timer/Counter
    TC1:
    Timer/Counter/capture//window/buzzer/PWM/PDO (programmable divider output) Mode selection
  - External interrupt wake-up. Function: rising or falling edge interrupt
  - I2C-bus available. Function; 7/10-bit address, 8-bit data transmit/receive mode
  - Port 56 input status change wake-up
  - Three 16 bits PWM
  - One Comparator/OP
- 16 available interrupts
- Special Features
  - Programmable free running watchdog timer
  - High ESD immunity
  - Power saving Sleep mode
  - Selectable Oscillation mode
- Package types:
  - 18 pin DIP 300mil : EM78P374ND18J/S
  - 18 pin SOP 300mil : EM78P374NSO18J/S
  - 20 pin DIP 300mil : EM78P374ND20J/S
  - 20 pin SOP 300mil : EM78P374NSO20J/S
  - 20 pin SSOP 209mil : EM78P374NSS20J/S
  - 24 pin skinny DIP 300mil : EM78P374NK24J/S
  - 24 pin SOP 300mil : EM78P374NSO24J/S
  - 24 pin SSOP 150mil : EM78P374NSS24J/S

Note: *These are Green product which do not contain*

3 Pin Configuration (Package)

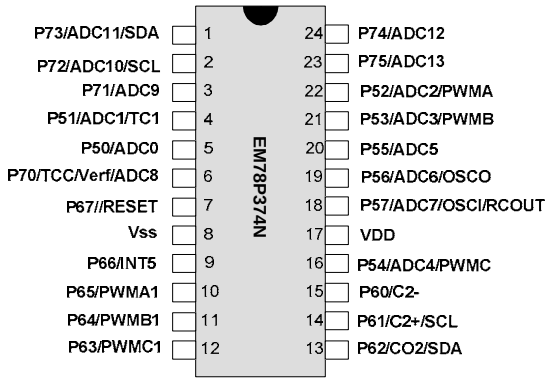


Figure 3-1a 24-Pin DIP/SOP/SSOP Pin Assignment

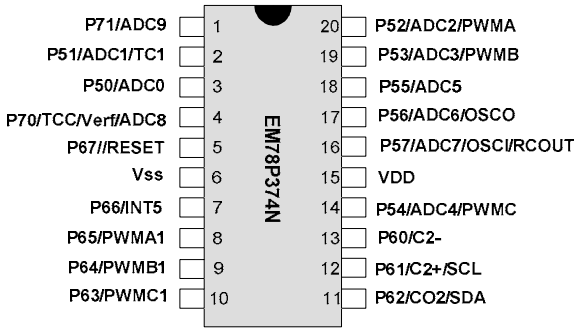


Figure 3-1b 20-Pin DIP/SOP/SSOP Pin Assignment

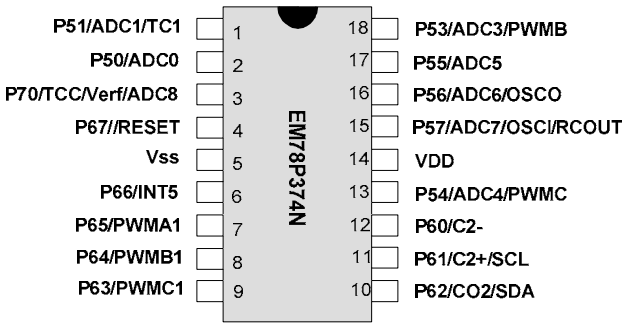


Figure 3-1c 18-Pin DIP/SOP Pin Assignment

4 Pin Description

Pin Name	Function	Input Type	Output Type	Description
P50/ADC0	P50	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, high sink, high drive, and pin change wake-up.
	ADC0	AN	-	ADC Input 0
P51/ADC1/ TC1	P51	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, high sink, high drive, and pin change wake-up.
	ADC1	AN	-	ADC Input 1
	TC1	ST	CMOS	Timer 1 clock input, capture input (TC1CAP), window input (TC1W), programmable divider output (PDO), pulse-width-modulation (PWM1), and buzzer ouput (BUZ)
P52/ADC2/ PWMA	P52	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, high sink, high drive, and pin change wake-up.
	ADC2	AN	-	ADC Input 2
	PWMA	-	CMOS	PWMA output
P53/ADC3/ PWMB	P53	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, high sink, high drive, and pin change wake-up.
	ADC3	AN	-	ADC Input 3
	PWMB	-	CMOS	PWMB output
P54/ADC4/ PWMC	P54	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, high sink, high drive, and pin change wake-up.
	ADC4	AN	-	ADC Input 4
	PWMC	-	CMOS	PWMC output
P55/ADC5	P55	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, high sink, high drive, and pin change wake-up.
	ADC5	AN	-	ADC Input 5
P56/ADC6/ OSCO	P56	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, high sink, high drive, and pin change wake-up.
	ADC6	AN	-	ADC Input 6
	OSCO	-	XTAL	Clock output of crystal/resonator oscillator

(Continuation)

Pin Name	Function	Input Type	Output Type	Description
P57/ADC7/ OSCI/ RCOUT	P57	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, high sink, high drive, and pin change wake-up.
	ADC7	AN	-	ADC Input 7
	OSCI	XTAL	-	Clock input of crystal/ resonator oscillator
	RCOUT	-	CMOS	Clock output of internal RC oscillator
P60/C2-	P60	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, high sink, high drive, and pin change wake-up.
	C2-	AN	-	Inverting end of Comparator 2 / OP2
P61/C2+/ SCL	P61	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, high sink, high drive, and pin change wake-up.
	C2+	AN	-	Non-inverting end of Comparator 2/OP2
	SCL	ST	CMOS	I^2C serial clock input/output (SCL)
P62/CO2/ SDA	P62	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, high sink, high drive, and pin change wake-up.
	CO2	-	CMOS	Output of Comparator 2
	SDA	ST	CMOS	I^2C serial data input/output (SDA)
P63/ PWMC1	P63	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, high sink, high drive, and pin change wake-up.
	PWMC1	-	CMOS	PWMC1 ouput (complementary PWM)
P64/ PWMB1	P64	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, high sink, high drive, and pin change wake-up
	PWMB1	-	CMOS	PWMB1 ouput (complementary PWM)
P65/ PWMA1	P65	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, high sink, high drive, and pin change wake-up.
	PWMA1	-	CMOS	PWMA1 ouput (complementary PWM)
P66/INT	P66	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, high sink, high drive, and pin change wake-up.
	INT	ST		External interrupt pin
P67/ /RESET	P67	ST	CMOS	Bidirectional I/O pin with programmable pull-down, high sink, and pin change wake-up. It is always open-drain
	/RESET	ST	-	Reset pin

(Continuation)

Pin Name	Function	Input Type	Output Type	Description
P70/TCC/ Verf/ADC8	P70	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, high sink, and high drive.
	TCC	ST	-	Real Time Clock/Counter clock input
	VREF	AN	-	ADC external voltage reference
	ADC8	AN	-	ADC Input 8
P71/ADC9	P71	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, high sink, and high drive.
	ADC9	AN	-	ADC Input 9
P72/ADC10/ SCL	P72	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, high sink, and high drive.
	ADC10	AN	-	ADC Input 10
	SCL	ST	CMOS	I^2C serial clock input/output (SCL)
P73/ADC11/ SDA	P73	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, high sink, and high drive.
	ADC11	AN	-	ADC Input 11
	SDA	ST	CMOS	I^2C serial data input/output (SDA)
P74/ADC12	P74	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, high sink, and high drive.
	ADC12	AN	-	ADC Input 12
P75/ADC13	P75	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, high sink, and high drive.
	ADC13	AN	-	ADC Input 13
VDD	VDD	Power	-	Power supply pin
VSS	VSS	Power	-	Ground

5 Functional Block Diagram

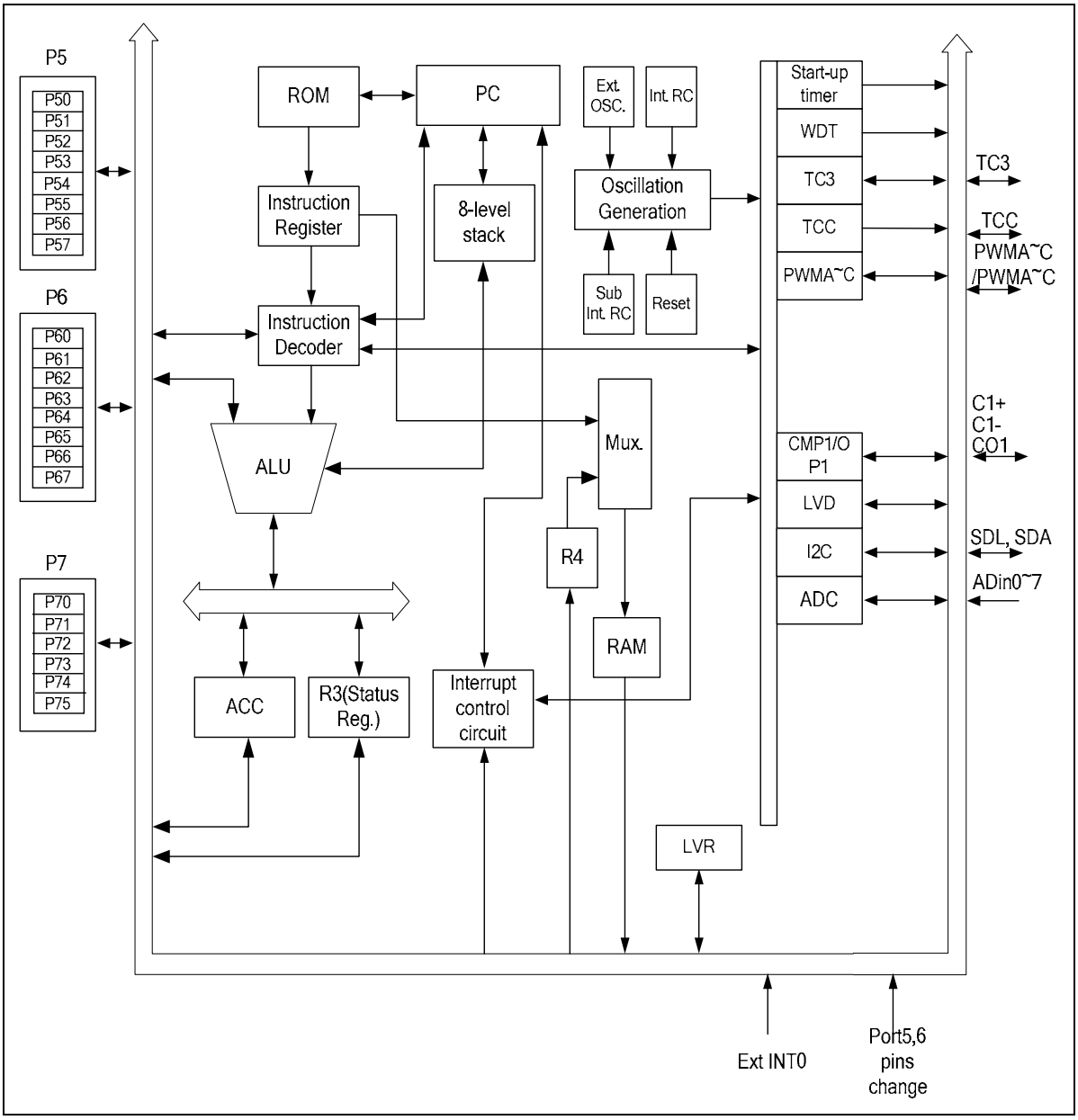


Figure 5-1 EM78P374N Functional Block Diagram

6 Functional Description

6.1 Operational Registers

6.1.1 R0: IAR (Indirect Addressing Register)

R0 is not a physically implemented register. Its major function is to perform as an indirect addressing pointer. Any instruction using R0 as a pointer actually accesses data pointed by the RAM Select Register (R4).

6.1.2 R1: BSR (Bank Select Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	SBS0	-	GBS2	GBS1	GBS0
-	-	-	R/W	-	R/W	R/W	R/W

Bits 7 ~ 5: Not used, set to "0" all the time.

Bit 4 (SBS0): Special register bank select bit. It is used to select Bank 0/1 of Special Registers **R5~R4F**.

0: Bank 0

1: Bank 1

Bit 3: Not used, fixed to "**0**" all the time.

Bits 2 ~ 0 (GBS2 ~ GBS0): General register bank select bit. It is used to select Banks 0~7 of General Registers **R80~RFF**.

GBS2	GBS1	GBS0	RAM Bank
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

6.1.3 R2: PCL (Program Counter Low)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7 ~ 0 (PC7~PC0): Low byte of the program counter.

- Depending on the device type, R2 and hardware stack are 14-bit wide. The structure is depicted in Figure 6-1.

- Generates 4K×15 bits on-chip Flash ROM addresses to the relative programming instruction codes. One program page is 4096 words long.
- R2 is set as all "**0**"s when under reset condition.
- "JMP" instruction allows direct loading of the lower 12 program counter bits. Thus, "JMP" allows the PC to go to any location within a page.
- "CALL" instruction loads the lower 12 bits of the PC, and the current PC value will be incremented by 1 and is pushed onto the stack. Thus, the subroutine entry address can be located anywhere within a page.
- "LJMP" instruction allows direct loading of the lower 15 program counter bits. Therefore, "LJMP" allows the PC to jump to any location within 4K (2^{12}).
- "LCALL" instruction loads the lower 15 bits of the PC, and PC+1 are pushed onto the stack. Thus, the subroutine entry address can be located anywhere within 4K (2^{12}).
- "RET" ("RETL k", "RETI") instruction loads the program counter with the contents of the top-level stack.
- "ADD R2, A" allows a relative address to be added to the current PC, and the ninth and above bits of the PC will increase progressively.
- "MOV R2, A" allows to load an address from the "A" register to the lower 8 bits of the PC, and the ninth and above bits of the PC will remain unchanged.
- Any instruction, except “ADD R2,A” that is written to R2 (e.g., "MOV R2, A", "BC R2, 6",·etc.) will cause the ninth bit and the above bits (A8~A12) of the PC to remain unchanged.
- All instructions are single instruction cycle (Fsys/2), except “LCALL” and “LJMP” instructions. The “LCALL” and “LJMP” instructions need two instruction cycles.

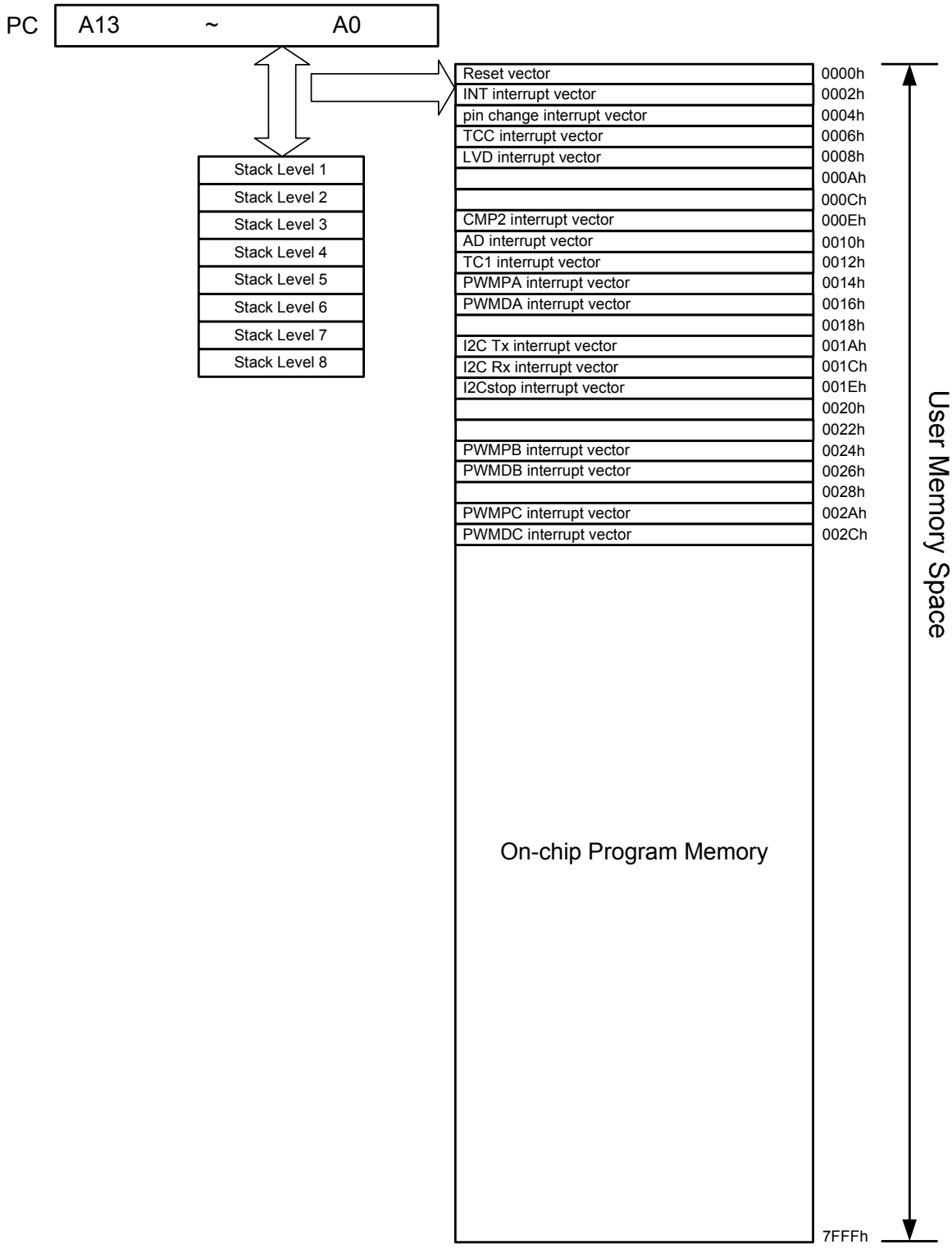


Figure 6-1 EM78P374N Program Counter Organization

■ Data Memory Configuration

Address	Bank 0	Bank 1
0X00	IAR (Indirect Addressing Register)	-
0X01	BSR (Bank Select Control Register)	
0X02	PC (Program Counter)	
0X03	SR (Status Register)	
0X04	RSR (RAM Select Register)	
0X05	Port 5	-
0X06	Port 6	-
0X07	Port 7	-
0X08	-	P5PHCR
0X09	-	P6PHCR
0X0A	-	P7PHCR
0x0B	IOC5	P5PLCR
0X0C	IOC6	P6PLCR
0X0D	IOC7	P7PLCR
0X0E	OMCR (Operating Mode Control Reg.)	P5HDSCR
0X0F	IESCR	P6HDSCR
0X10	WUCR1	P7HDSCR
0X11	WUCR2	P5ODCR
0X12	WUCR3	P6ODCR
0X13	-	P7ODCR
0X14	SFR1 (Status Flag Register 1)	-
0X15	SFR2 (Status Flag Register 2)	-
0X16	SFR3 (Status Flag Register 3)	PWMSCR
0X17	SFR4 (Status Flag Register 4)	PWMACR
0X18	SFR5 (Status Flag Register 5)	PRDAL
0X19	-	PRDAH
0X1A	-	DTAL
0X1B	IMR1 (Interrupt Mask Register 1)	DTAH
0X1C	IMR2 (Interrupt Mask Register 2)	TMRAL
0X1D	IMR3 (Interrupt Mask Register 3)	TMRAH
0X1E	IMR4 (Interrupt Mask Register 4)	PWMBCR
0X1F	IMR5 (Interrupt Mask Register 5)	PRDBL
0X20	-	PRDBH
0X21	WDTCR	DTBL
0X22	TCCCR	DTBH
0X23	TCCD	TMRBL
0X24	TC1CR1	TMRBH
0X25	TC1CR2	PWMCCR
0X26	TC1DA	PRDCL
0X27	TC1DB	PRDCH
0X28	-	DTCL
0X29	-	DTCH
0X2A	-	TMRCL
0x2B	-	TMRCH

(Continuation)

Address	Bank 0	Bank 1
0X2C	-	-
0X2D	-	-
0X2E	-	-
0X2F	-	-
0X30	I2CCR1	-
0X31	I2CCR2	-
0X32	I2CSA	-
0X33	I2CDB	-
0X34	I2CDAL	-
0X35	I2CDAH	-
0X36	-	-
0X37	-	-
0X38	-	-
0X39	-	-
0X3A	-	-
0x3B	CMP2CR	-
0X3C	CMP3CR	-
0X3D	-	-
0X3E	ADCR1	-
0X3F	ADCR2	-
0X40	ADISR	-
0X41	ADER1	-
0X42	ADER2	-
0X43	ADDL	-
0X44	ADDH	-
0X45	ADCVL	TBPTL
0X46	ADCVH	TBPTH
0X47	Unused	STKMON
0X48	-	PCH
0X49	-	LVDCR
0X4A	-	-
0x4B	-	-
0X4C	-	-
0X4D	-	-
0X4E	-	-
0X4F	-	-
0X50	**General Purpose Register**	
0X51		
:		
:		
0X7F		

(Continuation)

Address	Bank 0	Bank 1
0X80	Bank 0	Bank 1
0X81 : : : 0XFE 0XFF		

6.1.4 R3: SR (Status Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INT	-	-	T	P	Z	DC	C
F	-	-	R/W	R/W	R/W	R/W	R/W

Bit 7 (INT): Interrupt Enable flag

0: Interrupt masked by DISI or hardware interrupt

1: Interrupt enabled by ENI/DISI instructions

Bits 6 ~ 5: Not used, set to "**0**" all the time.

Bit 4 (T): Time-out bit

Set to "**1**" with the "SLEP" and "WDTC" commands, or during power up.

Reset to "**0**" by WDT time-out.

Bit 3 (P): Power down bit

Set to "**1**" during power on or by a "WDTC" command

Reset to "**0**" by a "SLEP" command.

Bit 2 (Z): Zero flag

Set to "**1**" if the result of an arithmetic or logic operation is zero.

Bit 1 (DC): Auxiliary carry flag

Bit 0 (C): Carry flag

6.1.5 R4: RSR (RAM Select Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RSR7	RSR6	RSR5	RSR4	RSR3	RSR2	RSR1	RSR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7 ~ 0 (RSR7 ~ RSR0): These bits are used to select registers (Address: 00~FF) in the indirect address mode. For more details, refer to the table on Data Memory Configuration in Section 6.1.3, *R2: PCL (Program Counter Low)*.

6.1.6 Bank 0 R5 ~ R7: (Port 5 ~ Port 7)

R5, R6 and R7 are I/O data registers.

6.1.7 Bank 0 R8~RA:

(Not used. Set to "0" all the time)

6.1.8 Bank 0 RB~RD: (IOCR5 ~ IOCR7)

These registers are used to control I/O port direction. They are both readable and writable.

0: Put the relative I/O pin as output

1: Put the relative I/O pin into high impedance

6.1.9 Bank 0 RE: OMCR (Operating Mode Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CPUS	IDLE	-	-	-	-	RCM1	RCM0
R/W	R/W	-	-	-	-	R/W	R/W

Bit 7 (CPUS): CPU Oscillator Source Select

0: Fs: sub-oscillator

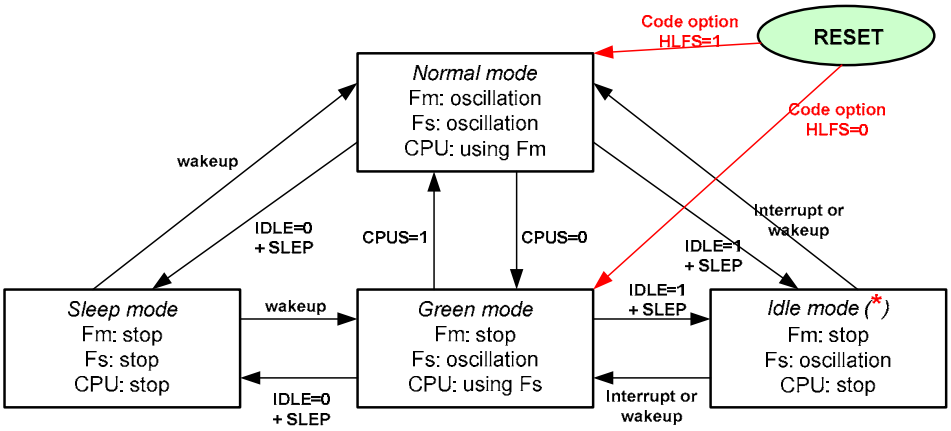
1: Fm: main-oscillator

When CPUS=0, the CPU oscillator selects the sub-oscillator and the main oscillator is stopped.

Bit 6 (IDLE): Idle Mode Enable Bit. This bit determines which mode (see figure below) is to be activated after SLEP instruction.

0: "IDLE=0"+SLEP instruction → Sleep mode

1: "IDLE=1"+SLEP instruction → Idle mode



** Switching operation mode at Idle → Normal, Idle → Green:*

If the clock source of timer is Fs, the timer/counter must continue to count in Idle mode. When the matching condition of the timer/counter occurs during Idle mode, the interrupt flag of timer/counter will be active. However, the MCU will jump to interrupt vector when the corresponding interrupt is enabled.

Figure 6-2 CPU Operation Mode

■ Oscillation Characteristics

Oscillation Mode	CPU Mode Switch	Waiting Time before CPU Starts to Work
Crystal Mode	Sleep → Normal	WSTO + 510 clocks (main frequency)
	Idle → Normal	WSTO + 510 clocks (main frequency)
	Green → Normal	WSTO + 510 clocks (main frequency)
	Sleep → Green	WSTO + 8 clocks (sub frequency)
	Idle → Green	WSTO + 8 clocks (sub frequency)
IRC Mode	Sleep → Normal	WSTO + 8 clocks (main frequency)
	Idle → Normal	WSTO + 8 clocks (main frequency)
	Green → Normal	WSTO + 8 clocks (main frequency)
	Sleep → Green	WSTO + 8 clocks (sub frequency)
	Idle → Green	WSTO + 8 clocks (sub frequency)

***WSTO:** Waiting time of Start-to-Oscillation*

Bits 5 ~ 3: Not used. Set to "**0**" all the time

Bits 2 ~ 1 (RCM1 ~ RCM0): Internal RC mode selection bits

RCM1	RCM0	Frequency (MHz)
0	0	1
0	1	8
1	0	16
1	1	4

6.1.10 Bank 0 RF: IESCR (External Interrupt Edge Select Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	EIES54	-	-	-	-	-
-	-	R/W	-	-	-	-	-

Bits 5 (EIES54): External interrupt edge select bit

0: Falling edge interrupt

1: Rising edge interrupt

6.1.11 Bank 0 R10: WUCR1 (Wake-up Control Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CMP2WK	-	LVDWK	ADWK	-	-	-	-
R/W	-	R/W	R/W	-	-	-	-

Bit 7 (CMP2WK): Comparator 2 Wake-up Enable bit

0: Disable Comparator 2 wake-up.

1: Enable Comparator 2 wake-up.

Bit 6: Not used. Set to "**0**" all the time.

Bit 5 (LVDWK): Low Voltage Detect Wake-up Enable bit

0: Disable Low Voltage Detect wake-up.

1: Enable Low Voltage Detect wake-up.

Bit 4 (ADWK): A/D Converter Wake-up Function Enable bit

0: Disable AD converter wake-up

1: Enable AD converter wake-up

When the AD Complete status is used to enter an interrupt vector or to wake-up IC from Sleep/Idle mode with AD conversion running, the ADWK bit must be set to "Enable".

Bits 3 ~ 0: Not used. Set to "**0**" all the time

6.1.12 Bank 0 R11: WUCR2 (Wake-up Control Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	I2CWK	-	-
-	-	-	-	-	R/W	-	-

Bits 7 ~ 3: Not used. Set to "**0**" all the time.

Bit 2 (I2CWK): I2C wake-up enable bit. It is available when I2C works in Slave mode.

0: Disable

1: Enable

Bits 1 ~ 0: Not used. Set to "**0**" all the time.

6.1.13 Bank 0 R12: WUCR3 (Wake-up Control Register 3)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	ICWKP6	ICWKP5	-	-	INTWK5	-
-	-	R/W	R/W	-	-	R/W	-

Bits 5 ~ 4 (ICWKP6 ~ 5): (Ports 6 ~ 5) Pin-change Wake-up Function Enable Bit

0: Disable external interrupt wake-up

1: Enable external interrupt wake-up

When the External Interrupt status change is used to enter an interrupt vector or to wake-up the IC from Sleep/Idle, the INTWK bits must be set to “Enable“.

Pin Change Wake-up Function Enable*				
CPU Mode	**Normal / Green**		**Sleep / Idle**	
Global interrupt	DISI	ENI	DISI	ENI
ICIE = 0 Next instruction	(ICSF=1 or 0)** Next instruction	(ICSF=1 or 0) Wake up (ICSF=1)	+	Next instruction Wake up (ICSF=1)
ICIE = 1 Next instruction	(ICSF=1 or 0) Interrupt vector	(ICSF=1) Wake up (ICSF=1)	+	Next instruction Wake up (ICSF=1)

* *If the Pin Change Wake-up function is disabled, the ICSF is always equals to “**0**”.*

** *When the ICSF is equal to “**1**”, the MCU will wake-up from Sleep or Idle mode. If ICSF is equal to “**0**”, pin change condition does NOT occur. Hence, the MCU will NOT be awakened by pin change.*

Bits 7 ~ 6, 3 ~ 2, 0: Not used. Set to “**0**” all the time.

Bit 1 (INTWK5): External Interrupt (INT pin) Wake-up Function Enable bit

0: Disable external interrupt wake-up

1: Enable external interrupt wake-up

When the External Interrupt status change is used to enter an interrupt vector or to wake-up the MCU from Sleep/Idle mode, the EXWE bits must be set to “Enable“.

6.1.14 Bank 0 R13:

(Not used. Set to “0” all the time)

6.1.15 Bank 0 R14: SFR1 (Status Flag Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CMP2SF	-	LVDSF	ADSF	-	-	-	TCSF
F	-	F	F	-	-	-	F

Each corresponding status flag is set to "**1**" when interrupt condition is triggered.

Bit 7 (CMP2SF): Comparator 2 status flag. Set when a change occurs in the output of Comparator 2. Reset by software.

Bit 6: Not used. Set to "**0**" all the time.

Bit 5 (LVDSF): Low Voltage Detector status flag**:**

LVDEN	LVDS2, LVDS1, LVDS0	LVD Voltage Interrupt Level	LVDSF
1	011	2.2V	1*
1	010	3.3V	1*
1	001	4.0V	1*
1	000	4.5V	1*
0	XX	NA	0

* *If Vdd crossovers at the LVD voltage interrupt level as Vdd varies, LVDSF =1.*

Bit 4 (ADSF): Status flag for analog to digital conversion. Set when AD conversion is completed. Reset by software.

Bits 3 ~ 1: Not used. Set to "**0**" all the time.

Bit 0 (TCSF): TCC overflow status flag. Set when TCC overflows. Reset by software.

NOTE

If a function is enabled, the corresponding status flag will be active regardless whether the interrupt mask is enabled or not.

6.1.16 Bank 0 R15: SFR2 (Status Flag Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	-	-	TC1DSF
-	-	-	-	-	-	-	F

Each corresponding status flag is set to "**1**" when interrupt condition is triggered.

Bits 7 ~ 1: Not used. Set to "**0**" all the time.

Bit 0 (TC1DSF): 8-bit Timer/Counter 1 status flag. Clear by software.

NOTE

If a function is enabled, the corresponding status flag will be active regardless whether the interrupt mask is enabled or not.

6.1.17 Bank 0 R16: SFR3 (Status Flag Register 3)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	PWMCPSF	PWMCDSF	PWMBPSF	PWMBDSF	PWMAPSF	PWMADSF
-	-	F	F	F	F	F	F

Bits 7 ~ 6: Not used. Set to "**0**" all the time.

Bit 5 (PWMCPSF): Status flag of period-matching for PWMC (Pulse Width Modulation). Set when a selected period is reached. Reset by software.

Bit 4 (PWMCDSF): Status flag of duty-matching for PWMC (Pulse Width Modulation). Set when a selected duty is reached. Reset by software.

Bit 3 (PWMBPSF): Status flag of period-matching for PWMB (Pulse Width Modulation). Set when a selected period is reached. Reset by software.

Bit 2 (PWMBDSF): Status flag of duty-matching for PWMB (Pulse Width Modulation). Set when a selected duty is reached. Reset by software.

Bit 1 (PWMAPSF): Status flag of period-matching for PWMA (Pulse Width Modulation). Set when a selected period is reached. Reset by software.

Bit 0 (PWMADSF): Status flag of duty-matching for PWMA (Pulse Width Modulation). Set when a selected duty is reached. Reset by software.

NOTE

If a function is enabled, the corresponding status flag will be active regardless whether the interrupt mask is enabled or not.

6.1.18 Bank 0 R17: SFR4 (Status Flag Register 4)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	P6ICSF	P5ICSF	-	I2CSTPSF	I2CRSF	I2CTSF
-	-	F	F	-	F	F	F

Bits 7 ~ 6: Not used. Set to "**0**" all the time.

Bit 5 (P6ICSF): Port 6 status flag. Flag is cleared by software.

Bit 4 (P5ICSF): Port 5 status flag. Flag is cleared by software.

Bit 3: Not used. Set to "**0**" all the time.

Bit 2 (I2CSTPSF): I2C stop status flag. Set when I2C stop signal occurs.

Bit 1 (I2CRSF): I2C receive status flag. Set when I2C receives 1 byte data and responds with an ACK signal. Reset by firmware or disable I2C.

Bit 0 (I2CTSF): I2C transmit status flag. Set when I2C transmits 1 byte data and receives a handshake signal (ACK or NACK). Reset by firmware or disable I2C.

NOTE

If a function is enabled, the corresponding status flag will be active regardless whether the interrupt mask is enabled or not.

6.1.19 Bank 0 R18: SFR5 (Status Flag Register 5)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	EXSF5	-	-	-
-	-	-	-	F	-	-	-

Each corresponding status flag is set to "**1**" when interrupt condition is triggered.

Bits 7 ~ 4, 2 ~ 0: Not used. Set to "**0**" all the time.

Bit 3 (EXSF5): External interrupt status flag

INT Pin	Enable Condition	Edge	Digital Noise Reject
INTX	(ENI+) EXIEX	Rising or Falling	8/Fc or 32/Fc

NOTE

If a function is enabled, the corresponding status flag will be active regardless whether the interrupt mask is enabled or not.

6.1.20 Bank 0 R1B: IMR1 (Interrupt Mask Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CMP2IE	-	LVDIE	ADIE	-	-	-	TCIE
R/W	-	R/W	R/W		-	-	R/W

Bit 7 (CMP2IE): CMP2SF interrupt enable bit

0: Disable CMP2SF interrupt

1: Enable CMP2SF interrupt

When the Comparator output status change is used to enter interrupt vector, the CMP2IE bit must be set to "Enable".

Bit 6: Not used. Set to "**0**" all the time.

Bit 5 (LVDIE): LVDSF interrupt enable bit

0: Disable LVDSF interrupt

1: Enable LVDSF interrupt

Bit 4 (ADIE): ADSF interrupt enable bit

0: Disable ADSF interrupt

1: Enable ADSF interrupt.

Bits 3~1: Not used. Set to "**0**" all the time.

Bit 0 (TCIE): TCSF interrupt enable bit.

0: Disable TCSF interrupt

1: Enable TCSF interrupt

NOTE

If the interrupt mask is enabled, the program counter would jump into the corresponding interrupt vector when the corresponding status flag is set.

6.1.21 Bank 0 R1C: IMR2 (Interrupt Mask Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	-	-	TC1DIE
-	-	-	-	-	-	-	R/W

Bits 7 ~ 1: Not used. Set to "**0**" all the time.

Bit 0 (TC1DIE): Interrupt enable bit

0: Disable TC1DSF interrupt

1: Enable TC1DSF interrupt

NOTE

If the interrupt mask is enabled, the program counter would jump into the corresponding interrupt vector when the corresponding status flag is set.

6.1.22 Bank 0 R1D IMR3 (Interrupt Mask Register 3)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	PWMCPIE	PWMCDIE	PWMBPIE	PWMBDIE	PWMAPIE	PWMADIE
-	-	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7 ~ 6: Not used. Set to "**0**" all the time.

Bit 5 (PWMCPIE): PWMCPSF interrupt enable bit

0: Disable period-matching of PWMC interrupt

1: Enable period-matching of PWMC interrupt

Bit 4 (PWMCDIE): PWMCDSF interrupt enable bit

0: Disable duty-matching of PWMC interrupt

1: Enable duty-matching of PWMC interrupt

Bit 3 (PWMBPIE): PWMBPSF interrupt enable bit

0: Disable period-matching of PWMB interrupt

1: Enable period-matching of PWMB interrupt

Bit 2 (PWMBDIE): PWMBDSF interrupt enable bit

0: Disable duty-matching of PWMB interrupt

1: Enable duty-matching of PWMB interrupt

Bit 1 (PWMAPIE): PWMAPSF interrupt enable bit

0: Disable period-matching of PWMA interrupt

1: Enable period-matching of PWMA interrupt

Bit 0 (PWMADIE): PWMADSF interrupt enable bit.

0: Disable duty-matching of PWMA interrupt

1: Enable duty-matching of PWMA interrupt

NOTE

If the interrupt mask is enabled, the program counter would jump into the corresponding interrupt vector when the corresponding status flag is set.

6.1.23 Bank 0 R1E: IMR4 (Interrupt Mask Register 4)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	P6ICIE	P5ICIE	-	I2CSTPIE	I2CRIE	I2CTIE
-	-	R/W	R/W	-	R/W	R/W	R/W

Bits 7 ~ 6: Not used. Set to "**0**" all the time.

Bit 5 (P6ICIE): Port 6 pin-change Interrupt Enable bit

0: Disable P6ICSF interrupt

1: Enable P6ICSF interrupt

Bit 4 (P5ICIE): Port 5 pin-change Interrupt Enable bit

0: Disable P5ICSF interrupt

1: Enable P5ICSF interrupt

Bit 3: Not used. Set to "**0**" all the time.

Bit 2 (I2CSTPIE): I2C stop interrupt enable bit

0: Disable interrupt

1: Enable interrupt

Bit 1 (I2CRIE): I2C Interface Rx Interrupt Enable bit

0: Disable interrupt

1: Enable interrupt

Bit 0 (I2CTIE): I2C Interface Tx Interrupt Enable bit

0: Disable interrupt

1: Enable interrupt

NOTE

If the interrupt mask is enabled, the program counter would jump into the corresponding interrupt vector when the corresponding status flag is set.

6.1.24 Bank 0 R1F: IMR5 (Interrupt Mask Register 5)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	EXIE5	-	-	-
-	-	-	-	R/W	-	-	-

Bits 7~ 4, 2 ~ 0: Not used. Set to "**0**" all the time.

Bit 3 (EXIE5): EXSF5 interrupt enable bit

0: Disable EXSF5 interrupt

1: Enable EXSF5 interrupt

NOTE

If the interrupt mask is enabled, the program counter would jump into the corresponding interrupt vector when the corresponding status flag is set.

6.1.25 Bank 0 R21: WDTCR (Watchdog Timer Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WDTE	-	-	-	PSWE	WPSR2	WPSR1	WPSR0
R/W	-	-	-	R/W	R/W	R/W	R/W

Bit 7 (WDTE): Watchdog Timer enable bit. WDTE is both readable and writable.

0: Disable WDT

1: Enable WDT

Bit 3 (PSWE): Prescaler enable bit for WDT

0: Prescaler disable bit. WDT rate is 1:1.

1: Prescaler enable bit. WDT rate is set at Bits 2~0.

Bits 2 ~ 0 (WPSR2 ~ WPSR0): WDT Prescale bits

WPSR2	WPSR1	WPSR0	WDT Rate
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

6.1.26 Bank 0 R22: TCCCR (TCC Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	TCCS	TS	TE	PSTE	TPSR2	TPSR1	TPSR0
-	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7: Not used. Set to "**0**" all the time.

Bit 6 (TCCS): TCC Clock Source Select Bit

0: Fs (sub clock)

1: Fm (main clock)

Bit 5 (TS): TCC signal source

0: Internal instruction cycle clock

1: Transition on the TCC pin. The TCC period must be larger than internal instruction clock period.

Bit 4 (TE): TCC Signal Edge

0: Increment if the transition from low to high takes place on the TCC pin.

1: Increment if the transition from high to low takes place on the TCC pin.

Bit 3 (PSTE): Prescaler enable bit for TCC

0: Prescaler disable bit. TCC rate is 1:1.

1: Prescaler enable bit. TCC rate is set at Bit 2 ~ Bit 0.

Bits 2 ~ 0 (TPSR2 ~ TPSR0): TCC Prescaler bits

TPSR2	TPSR1	TPSR0	TCC Rate
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

6.1.27 Bank 0 R23: TCCD (TCC Data Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TCC7	TCC6	TCC5	TCC4	TCC3	TCC2	TCC1	TCC0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7 ~ 0 (TCC7 ~ TCC0): TCC data

Increase by an external signal edge through the TCC pin, or by the instruction cycle clock. The External signal of TCC trigger pulse width must be greater than one instruction. The signals to increase the counter are determined by Bit 4 and Bit 5 of the TCCCR register. They are writable and readable as any other registers. If there is an overflow, the value previously written to TCCD will be auto-reloaded to the TCC circuit.

6.1.28 Bank 0 R24: TC1CR1 (Timer/Counter 1 Control Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TC1S	TC1RC	TC1SS1	-	TC1FF	TC1OMS	TC1IS1	TC1IS0
R/W	R/W	R/W	-	R/W	R/W	R/W	R/W

Bit 7 (TC1S): Timer/Counter 1 start control

0: Stop and clear the counter (default)

1: Start Timer/Counter 1

Bit 6 (TC1RC): Timer 1 Read Control bit

0: When this bit is set to "**0**", data from TC1DB can't be read (default).

1: When this bit is set to "**1**", data is read from TC1DB. The read data is the enumerated counting number.

Bit 5 (TC1SS1): Timer/Counter 1 clock source select bit

0: Select internal clock as count source (Fc) - Fs/Fm (default)

1: Select external TC1 pin as count source (Fc). It is used only for timer/counter mode.

Bit 4: Not used. Set to "**0**" all the time.

Bit 3 (TC1FF): Inversion for Timer/Counter 1 as PWM

0: Duty is Logic 1 (default)

1: Duty is Logic 0

Bit 2 (TC1OMS): Timer Output Mode select bit

0: Repeat mode (default)

1: One–shot mode

NOTE

One-shot mode means the Timer only counts a cycle.

Bits 1 ~ 0 (TC1IS1 ~ TC1IS0): Timer 1 Interrupt Type select bits. These two bits are used when the Timer operates in PWM mode.

TC1IS1	TC1IS0	Timer 1 Interrupt Type Select
0	0	TC1DA (period) matching
0	1	TC1DB (duty) matching
1	×	TC1DA and TC1DB matching

6.1.29 Bank 0 R25: TC1CR2 (Timer/Counter 1 Control Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TC1M2	TC1M1	TC1M0	TC1SS0	TC1CK3	TC1CK2	TC1CK1	TC1CK0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7 ~ 5 (TC1M2 ~ TC1M0): Timer/Counter 1 operation mode select

TC1M2	TC1M1	TC1M0	Operating Mode Select
0	0	0	Timer/Counter Rising Edge
0	0	1	Timer/Counter Falling Edge
0	1	0	Capture Mode Rising Edge
0	1	1	Capture Mode Falling Edge
1	0	0	Window mode
1	0	1	Programmable Divider output
1	1	0	Pulse Width Modulation output
1	1	1	Buzzer (output timer/counter clock source. The duty cycle of the clock source must be 50/50)

Bit 4 (TC1SS0): Timer/Counter 1 clock source selection bit

0: Fs is used as count source (Fc) (default)

1: Fm is used as count source (Fc)

Bits 3~0 (TC1CK3~TC1CK0): Timer/Counter 1 clock source prescaler select**:**

TC3CK3	TC3CK2	TC3CK1	TC3CK0	Clock Source	Resolution 8 MHz	Max. Time 8 MHz	Resolution 16kHz	Max. Time 16kHz
				Normal	F_C=8M	F_C=8M	F_C=16K	F_C=16K
0	0	0	0	F_C	125ns	32μs	62.5μs	16ms
0	0	0	1	$F_C/2$	250ns	64μs	125μs	32ms
0	0	1	0	$F_C/2^2$	500ns	128μs	250μs	64ms
0	0	1	1	$F_C/2^3$	1μs	256μs	500μs	128ms
0	1	0	0	$F_C/2^4$	2μs	512μs	1ms	256ms
0	1	0	1	$F_C/2^5$	4μs	1024μs	2ms	512ms
0	1	1	0	$F_C/2^6$	8μs	2048μs	4ms	1024ms
0	1	1	1	$F_C/2^7$	16μs	4096μs	8ms	2048ms
1	0	0	0	$F_C/2^8$	32μs	8192μs	16ms	4096ms
1	0	0	1	$F_C/2^9$	64μs	16384μs	32ms	8192ms
1	0	1	0	$F_C/2^{10}$	128μs	32768μs	64ms	16384ms
1	0	1	1	$F_C/2^{11}$	256μs	65536μs	128ms	32768ms
1	1	0	0	$F_C/2^{12}$	512μs	131072μs	256ms	65536ms
1	1	0	1	$F_C/2^{13}$	1.024ms	262144μs	512ms	131072ms
1	1	1	0	$F_C/2^{14}$	2.048ms	524.288ms	1.024s	262144ms
1	1	1	1	$F_C/2^{15}$	4.096ms	1.048s	2.048s	524288ms

6.1.30 Bank 0 R26: TC1DA (Timer/Counter 1 Data Buffer A)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TC1DA7	TC1DA6	TC1DA5	TC1DA4	TC1DA3	TC1DA2	TC1DA1	TC1DA0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7 ~ 0 (TC1DA7 ~ TC1DA0): Data Buffer A of 8 bit Timer/Counter 1

6.1.31 Bank 0 R27: TC1DB (Timer/Counter 1 Data Buffer B)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TC1DB7	TC1DB6	TC1DB5	TC1DB4	TC1DB3	TC1DB2	TC1DB1	TC1DB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7 ~ 0 (TC1DB7 ~ TC1DB0): Data Buffer B of 8 bit Timer/Counter 1

NOTE

1. *When Timer / Counter x is used in PWM mode, the duty value stored at register TCxDB must be smaller than or equal to the period value stored at register TCxDA, i.e., duty ≦ period. Then the PWM waveform is generated. If the duty is larger than period, the PWM output waveform is kept at high voltage level.*
2. *The period value set by users is extra plus 1 in the inner circuit.*

   For example: When the period value is set as 0x4F, the PWM waveform will actually generate 0x50 period length.

   When the period value is set as 0xFF, the PWM waveform will actually generate 0x100 period length.

6.1.32 Bank 0 R28~R2F: *(Not used. Set to "0" all the time)*

6.1.33 Bank 0 R30: I2CCR1 (I2C Status and Control Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Strobe/Pend	IMS	ISS	STOP	SAR_EMPTY	ACK	FULL	EMPTY
R	R/W	R/W	R	R	R	R	R

Bit 7 (Strobe/Pend): In Master mode, it is used as strobe signal to control the I2C circuit from sending SCL clock. Automatically resets after receiving or transmitting a handshake signal (ACK or NACK).
In Slave mode, it is used as pending signal. User should clear it after writing data into the Tx buffer or taking data from the Rx buffer to inform the Slave I2C circuit to release the SCL signal.

Bit 6 (IMS): I2C Master/Slave mode select bit.

0: Slave

1: Master

Bit 5 (ISS): I2C Fast/Standard mode select bit (if Fm is 6 MHz and I2CTS1~0<0,0>)

0: Standard mode (100kbit/s)

1: Fast mode (400kbit/s)

Bit 4 (STOP): In Master mode, if STOP=1 and R/nW=1, then the MCU must return a nACK signal to the Slave device before sending a STOP signal. If STOP=1 and R/nW=0, then the MCU sends a STOP signal after receiving an ACK signal. Reset when the MCU sends a STOP signal to the Slave device.
In Slave mode, if STOP=1 and R/nW=0, then the MCU must return a nACK signal to the Master device.

Bit 3 (SAR_EMPTY): Set when the MCU transmits a 1 byte data from the I2C Slave Address Register and receives an ACK (or nACK) signal. Reset when the MCU writes a 1 byte data to the I2C Slave Address Register.

Bit 2 (ACK): The ACK condition bit is set to "**1**" by hardware when the device responds acknowledge (ACK). Resets when the device responds with a "not-acknowledge" (nACK) signal.

Bit 1 (FULL): Set by hardware when the I2C Receive Buffer register is full. Reset by hardware when MCU reads data from the I2C Receive Buffer register.

Bit 0 (EMPTY): Set by hardware when the I2C Transmit Buffer register is empty and receives an ACK (or nACK) signal. Reset by hardware when the MCU writes new data to I2C Transmit Buffer register.

6.1.34 Bank 0 R31: I2CCR2 (I2C Status and Control Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
I2CBF	GCEN	-	BBF	I2CTS1	I2CTS0	I2CCS	I2CEN
R	R/W	-	R	R/W	R/W	R/W	R/W

Bit 7 (I2CBF): I2C Busy Flag Bit

0: Clear to "**0**" in Slave mode if the received STOP signal or the I2C Slave Address does not match.

1: Set when I2C communicates with Master in Slave mode.

Bit 6 (GCEN): I2C General Call Function Enable Bit

0: Disable General Call Function

1: Enable General Call Function

Bit 5: Not used. Set to "**0**" all the time.

Bit 4 (BBF): Busy Flag Bit. I2C detection is busy in Master mode. Read only.

Bits 3~2 (I2CTS1~I2CTS0): I2C Transmit Clock select bits. When using different operating frequency (Fm), these bits must be set correctly in order for the SCL clock to be consistent in Standard/Fast mode.

- I2CCR1 Bit 5=0, Standard mode**:**

I2CTS1	I2CTS0	SCL CLK	Operating Fm (MHz)
0	0	Fm/40	4
0	1	Fm/80	8
1	0	Fm/120	12
1	1	Fm/160	16

- I2CCR1 Bit 5=1, Fast mode**:**

I2CTS1	I2CTS0	SCL CLK	Operating Fm (MHz)
0	0	Fm/10	4
0	1	Fm/20	8
1	0	Fm/30	12
1	1	Fm/40	16

Bit 1 (I2CCS): I2C Clock Source select bit

0: Fm (main clock)

1: Fs (sub clock). This is applicable in Master mode only.

Bit 0 (I2CEN): I2C Enable Bit

0: Disable I2C mode

1: Enable I2C mode

6.1.35 Bank 0 R32: I2CSA (I2C Slave Address Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SA6	SA5	SA4	SA3	SA2	SA1	SA0	IRW
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7 ~ 1 (SA6 ~ SA0): When the MCU is used as Master device for I2C application, these bits are the Slave Device Address register.

Bit 0 (IRW): When the MCU is used as Master device for I2C application, this bit is Read/Write transaction control bit.

0: Write

1: Read

6.1.36 Bank 0 R33: I2CDB (I2C Data Buffer Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7 ~ 0 (DB7~DB0): I2C Receive/Transmit Data Buffer

6.1.37 Bank 0 R34: I2CDAL (I2C Device Address Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7 ~ 0 (DA7 ~ DA0): When MCU used as slave device for I2C application, this register stores the address of the MCU. It is used to identify the data on the I2C bus to extract the message delivered to the MCU.

6.1.38 Bank 0 R35: I2CDAH (I2C Device Address Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	-	DA9	DA8
-	-	-	-	-	-	R/W	R/W

Bits 7 ~ 2: Not used. Set to "**0**" all the time.

Bits 1 ~ 0 (DA9 ~ DA8): Device address bits

6.1.39 Bank 0 R36~R3A: *(Not used. Set to "0" all the time)*

6.1.40 Bank 0 R3B: CMP2CR (Comparator 2 Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
C2RS	CP2OUT	C2S1	C2S0	-	-	-	SDPWMB
R/W	R	R/W	R/W	-	-	-	R/W

Bit 7 (C2RS): Selects the reference source for Comparator 2/OP2 non-inverting terminal.

0: CIN+ is connected to pad (default)

1: CIN+ is connected to internal reference

Bit 6 (CP2OUT): The result of the Comparator 2 output

Bits 5 ~ 4 (C2S1 ~ C2S0): Comparator 2 select bits

C2S1	C2S0	Function Description
0	0	Comparator 2 and OP2 are not used
0	1	Comparator 2 is used and its output is not connected to pad.
1	0	Comparator 2 is used and its output is connected to pad
1	1	OP

Bits 3 ~ 1: Not used. Set to "**0**" all the time.

Bit 0 (SDPWMB): Shut-down PMWB

0: Disable (default value)

1: Enable. The PWMBE and /PWMBE are disabled at the falling edge of Comparator 2.

NOTE

When using internal reference, you need to wait for at least 6 µs (when code option is IRCIRS=0) and 50 µs (when code option is IRCIRS=1) after control bits "CIRL11~CIRL10" are set, so as to obtain accurate output result. Otherwise, the output result would be inaccurate. It is also recommended that the control bits "C2S1~C2S0" should not be set at (1:0) or (1:1) to avoid occurrence of unexpected results.

6.1.41 Bank 0 R3C: CMP3CR (Comparator 3 Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	CIRL11	CIRL10	-
-	-	-	-	-	R/W	R/W	-

Bits 7 ~ 3: Not used. Set to "**0**" all the time.

Bits 2 ~ 1 (CIRL11~CIRL10): Internal voltage reference**:**

CIRL11	CIRL10	Voltage Reference
0	0	Disable (default)
0	1	4V
1	0	3V
1	1	2V

Bit 0: Not used. Set to "**0**" all the time.

6.1.42 Bank 0 R3D: (Not used. Set to "0" all the time)

6.1.43 Bank 0 R3E: ADCR1 (ADC Control Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CKR2	CKR1	CKR0	ADRUN	ADP	ADOM	SHS1	SHS0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7 ~ 5 (CKR2 ~ 0): Clock Rate select of ADC

System Mode	CKR[2:0]	Clock Rate
Normal Mode	000	$F_{Main}/16$
	001	$F_{Main}/8$
	010	$F_{Main}/4$
	011	$F_{Main}/2$
	100	$F_{Main}/64$
	101	$F_{Main}/32$
	110	$F_{Main}/1$
	111	F_{Sub}
Green Mode	xxx	F_{Sub}

Bit 4 (ADRUN): ADC starts to run

Single mode:

0: Reset on completion of the conversion by hardware. This bit cannot be reset by software.

1: A/D conversion starts. This bit can be set by software

Continuous mode:

0: ADC is stopped.

1: ADC is running unless this bit is reset by software

Bit 3 (ADP): ADC Power

0: ADC is in power down mode.

1: ADC is operating normally.

Bit 2 (ADOM): ADC Operation Mode Selection

0: ADC operates in single mode

1: ADC operates in continuous mode

Bits 1 ~ 0 (SHS1 ~ 0): Sample and Hold Timing Select

SHS[1:0]*	Sample and Hold Timing
00	2 x T_{AD}
01	4 x T_{AD}
10	8 x T_{AD}
11	12 x T_{AD}

SHS[1~0]=10 *is recommended*

6.1.44 Bank 0 R3F: ADCR2 (ADC Control Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	ADIM	ADCMS	VPIS1	VPIS0	VREFP	-
-	-	R/W	R/W	R/W	R/W	R/W	-

Bits 7 ~ 6: Not used. Set to "**0**" all the time.

Bit 5 (ADIM): ADC Interrupt Mode

0: Normal mode. Interrupt occurs after AD conversion is completed.

1: Compare mode. Interrupt occurs when comparison result conforms to the ADCMS bits setting. Using continuous mode is recommended.

Bit 4 (ADCMS): ADC Comparison Mode select

Compare mode:

0: Interrupt occurs when AD conversion data is equal to or greater than the data in ADCD register (which means when ADD > ADCD, interrupt occurs).

1: Interrupt occurs when AD conversion data is equal to or less than the data in ADCD register (which means when ADD < ADCD, interrupt occurs).

Normal mode:

No effect

Bits 3 ~ 2 (VPIS1 ~ 0): Internal Positive Reference Voltage select

VPIS[1:0]	Reference Voltage
00	AVDD
01	4V
10	3V
11	2V

Bit 1 (VREFP): Positive Reference Voltage select

0: Internal positive reference voltage. The actual voltage is set by VPIS [1:0] bit

1: From VREFP pin

NOTE

When using internal reference, users need to wait for at least 6 µs (when code option is IRCIRS=0) and 50 µs (when code option is IRCIRS=1) before control bit "ADRUN" is set, so as to obtain accurate AD conversion result. Otherwise, the conversion result would be inaccurate.

6.1.45 Bank 0 R40: ADISR (Analog to Digital Converter Input Channel Select Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	ADIS4	ADIS3	ADIS2	ADIS1	ADIS0
-	-	-	R/W	R/W	R/W	R/W	R/W

Bits 7 ~ 5: Not used. Set to "**0**" all the time.

Bits 4 ~ 0 (ADIS4 ~ 0): ADC input channel select bits

ADIS[4:0]	Selected Channel	ADIS[4:0]	Selected Channel
00000	Ch 0	10000*	1/4 VDD Power Detect
00001	Ch 1	10001*	N/A
00010	Ch 2	10010*	OPA 2
00011	Ch 3	10011*	N/A
00100	Ch 4	10100*	N/A
00101	Ch 5	10101	N/A
00110	Ch 6	10110	N/A
00111	Ch 7	10111	N/A
01000	Ch 8	11000	N/A
01001	Ch 9	11001	N/A
01010	Ch 10	11010	N/A
01011	Ch 11	11011	N/A
01100	Ch 12	11100	N/A
01101	Ch 13	11101	N/A
01110	N/A	11110	N/A
01111	N/A	11111	N/A

* *Used for internal signal source. User only need to set ADIS[4:0]=10000~10100. These AD input channels are instantly active.*

6.1.46 Bank 0 R41: ADER1 (Analog to Digital Converter Input Control Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADE7	ADE6	ADE5	ADE4	ADE3	ADE2	ADE1	ADE0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7 (ADE7): AD converter enable bit of P57 pin

0: Disable ADC7, P57 acts as I/O pin

1: Enable ADC7 to act as analog input pin

Bit 6 (ADE6): AD converter enable bit of P56 pin

0: Disable ADC6, P56 acts as I/O pin

1: Enable ADC6 to act as analog input pin

Bit 5 (ADE5): AD converter enable bit of P55 pin

0: Disable ADC5, P55 acts as I/O pin

1: Enable ADC5 to act as analog input pin

Bit 4 (ADE4): AD converter enable bit of P54 pin.

0: Disable ADC4, P54 acts as I/O pin

1: Enable ADC4 to act as analog input pin

Bit 3 (ADE3): AD converter enable bit of P53 pin.

0: Disable ADC3, P53 acts as I/O pin

1: Enable ADC3 to act as analog input pin

Bit 2 (ADE2): AD converter enable bit of P52 pin.

0: Disable ADC2, P52 acts as I/O pin

1: Enable ADC2 to act as analog input pin

Bit 1 (ADE1): AD converter enable bit of P51 pin

0: Disable ADC1, P51 acts as I/O pin

1: Enable ADC1 to act as analog input pin

Bit 0 (ADE0): AD converter enable bit of P50 pin

0: Disable ADC0, P50 acts as I/O pin

1: Enable ADC0 to act as analog input pin

6.1.47 Bank 0 R42: ADER2 (Analog to Digital Converter Input Control Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	ADE13	ADE12	ADE11	ADE10	ADE9	ADE8
-	-	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7 ~ 6: Not used. Set to "**0**" all the time.

Bit 5 (ADE13): AD converter enable bit of P75 pin

0: Disable ADC13, P75 acts as I/O pin

1: Enable ADC13 to act as analog input pin

Bit 4 (ADE12): AD converter enable bit of P74 pin

0: Disable ADC12, P74 acts as I/O pin

1: Enable ADC12 to act as analog input pin

Bit 3 (ADE11): AD converter enable bit of P73 pin

0: Disable ADC11, P73 acts as I/O pin

1: Enable ADC11 to act as analog input pin

Bit 2 (ADE10): AD converter enable bit of P72 pin

0: Disable ADC10, P72 acts as I/O pin

1: Enable ADC10 to act as analog input pin

Bit 1 (ADE9): AD converter enable bit of P71 pin

0: Disable ADC9, P71 acts as I/O pin

1: Enable ADC9 to act as analog input pin

Bit 0 (ADE8): AD converter enable bit of P70 pin

0: Disable ADC8, P70 acts as I/O pin

1: Enable ADC8 to act as analog input pin

6.1.48 Bank 0 R43: ADDL (Low Byte of Analog to Digital Converter Data)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADD7	ADD6	ADD5	ADD4	ADD3	ADD2	ADD1	ADD0
R	R	R	R	R	R	R	R

Bits 7 ~ 0 (ADD7 ~ 0): Low Byte of AD Data Buffer

6.1.49 Bank 0 R44: ADDH (High Byte of Analog to Digital Converter Data)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADD15	ADD14	ADD13	ADD12	ADD11	ADD10	ADD9	ADD8
R	R	R	R	R	R	R	R

Bits 7 ~ 0 (ADD15 ~ 8): High Byte of AD Data Buffer.

The AD data format is dependent on code option ADFM. The following table shows how the data justify the different ADFM settings**:**

ADFM			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
12 bits	0	ADDH	-	-	-	-	ADD11	ADD10	ADD9	ADD8
		ADDL	ADD7	ADD6	ADD5	ADD4	ADD3	ADD2	ADD1	ADD0
	1	ADDH	ADD11	ADD10	ADD9	ADD8	ADD7	ADD6	ADD5	ADD4
		ADDL	-	-	-	-	ADD3	ADD2	ADD1	ADD0

6.1.50 Bank 0 R45 ADCVL (Low Byte of Analog to Digital Converter Comparison)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADCV7	ADCV6	ADCV5	ADCV4	ADCV3	ADCV2	ADCV1	ADCV0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7 ~ 0 (ADCV7 ~ 0): Low Byte Data for AD comparison
User should use the same data format as with ADDH and ADDL registers. Otherwise, faulty values will result after AD comparison.

6.1.51 Bank 0 R46 ADCVH (High Byte of Analog to Digital Converter Comparison)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADCV15	ADCV14	ADCV13	ADCV12	ADCV11	ADCV10	ADCV9	ADCV8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7 ~ 0 (ADCV15 ~ 8): High Byte Data for AD comparison
User should use the same data format as with ADDH and ADDL registers. Otherwise, faulty values will result after AD comparison.

6.1.52 Bank 1 R5 ~ R7: *(Not used. Set to "0" all the time)*

6.1.53 Bank 1 R8: P5PHCR (Port 5 Pull-high Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PH57	PH56	PH55	PH54	PH53	PH52	PH51	PH50
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7 (PH57): Control bit used to enable pull-high of the P57 pin

0: Enable internal pull-high

1: Disable internal pull-high

Bit 6 (PH56): Control bit used to enable pull-high of the P56 pin

Bit 5 (PH55): Control bit used to enable pull-high of the P55 pin

Bit 4 (PH54): Control bit used to enable pull-high of the P54 pin

Bit 3 (PH53): Control bit used to enable pull-high of the P53 pin

Bit 2 (PH52): Control bit used to enable pull-high of the P52 pin

Bit 1 (PH51): Control bit used to enable pull-high of the P51 pin

Bit 0 (PH50): Control bit used to enable pull-high of the P50 pin

6.1.54 Bank 1 R9: P6PHCR (Port 6 Pull-high Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	PH66	PH65	PH64	PH63	PH62	PH61	PH60
-	R/W	R/W	R/W	R/W	R/W	R/W	R/W

All bits are low active.

Bit 7 (PH67): Not used. Set to "**1**" all the time.

Bit 6 (PH66): Control bit used to enable pull-high of the P66 pin

Bit 5 (PH65): Control bit used to enable pull-high of the P65 pin

Bit 4 (PH64): Control bit used to enable pull-high of the P64 pin

Bit 3 (PH63): Control bit used to enable pull-high of the P63 pin

Bit 2 (PH62): Control bit used to enable pull-high of the P62 pin

Bit 1 (PH61): Control bit used to enable pull-high of the P61 pin

Bit 0 (PH60): Control bit used to enable pull-high of the P60 pin

6.1.55 Bank 1 RA: P7PHCR (Port 7 Pull-high Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	-	P7HPH	P7LPH
-	-	-	-	-	-	R/W	R/W

All bits are low active

Bits 7 ~ 2: Not used. Set to "**1**" all the time

Bit 1 (P7HPH): Control bit used to enable pull-high of the Port 7 high nibble pin

Bit 0 (P7LPH): Control bit used to enable pull-high of the Port 7 low nibble pin

6.1.56 Bank 1 RB: P5PLCR (Port 5 Pull-low Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PL57	PL56	PL55	PL54	PL53	PL52	PL51	PL50
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7 (PL57): Control bit used to enable pull-low of the P57 pin

0: Enable internal pull-low

1: Disable internal pull-low

Bit 6 (PL56): Control bit used to enable pull-low of the P56 pin

Bit 5 (PL55): Control bit used to enable pull-low of the P55 pin

Bit 4 (PL54): Control bit used to enable pull-low of the P54 pin

Bit 3 (PL53): Control bit used to enable pull-low of the P53 pin

Bit 2 (PL52): Control bit used to enable pull-low of the P52 pin

Bit 1 (PL51): Control bit used to enable pull-low of the P51 pin

Bit 0 (PL50): Control bit used to enable pull-low of the P50 pin

6.1.57 Bank 1 RC: P6PLCR (Port 6 Pull-low Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PL67	PL66	PL65	PL64	PL63	PL62	PL61	PL60
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

All bits are low active

Bit 7 (PL67): Control bit used to enable pull-low of the P67 pin

Bit 6 (PL66): Control bit used to enable pull-low of the P66 pin

Bit 5 (PL65): Control bit used to enable pull-low of the P65 pin

Bit 4 (PL64): Control bit used to enable pull-low of the P64 pin

Bit 3 (PL63): Control bit used to enable pull-low of the P63 pin

Bit 2 (PL62): Control bit used to enable pull-low of the P62 pin

Bit 1 (PL61): Control bit used to enable pull-low of the P61 pin

Bit 0 (PL60): Control bit used to enable pull-low of the P60 pin

6.1.58 Bank 1 RD: P7PLCR (Port 7 Pull-low Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	-	P7HPL	P7LPL
-	-	-	-	-	-	R/W	R/W

All of these bits are low active.

Bits 7 ~ 2: Not used. Set to "**1**" all the time.

Bit 1 (P7HPL): Control bit used to enable pull-low of the Port 7 high nibble pin

Bit 0 (P7LPL): Control bit used to enable pull-low of the Port 7 low nibble pin

6.1.59 Bank 1 RE: P5HDSCR (Port 5 High Drive/Sink Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
H57	H56	H55	H54	H53	H52	H51	H50
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7 ~ 0 (H57 ~ H50): P57~P50 high drive/sink current control bits

0: Enable high drive/sink

1: Disable high drive/sink

6.1.60 Bank 1 RF: P6HDSCR (Port 6 High Drive/Sink Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
H67	H66	H65	H64	H63	H62	H61	H60
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7 ~ 0 (H67 ~ H60): P67~P60 high drive/sink current control bits (only P67 has high sink).

0: Enable high drive/sink

1: Disable high drive/sink

6.1.61 Bank 1 R10: P7HDSCR (Port 7 High Drive/Sink Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	-	P7HHDS	P7LHDS
-	-	-	-	-	-	R/W	R/W

All bits are low active.

Bits 7 ~ 2: Not used. Set to "**1**" all the time.

Bit 1 (P7HHDS): Control bit used to enable high drive/sink of Port 7 high nibble pin

Bit 0 (P7LHDS): Control bit used to enable high drive/sink of Port 7 low nibble pin

6.1.62 Bank 1 R11: P5ODCR (Port 5 Open-drain Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OD57	OD56	OD55	OD54	OD53	OD52	OD51	OD50
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7 ~ 0 (OD57 ~ OD50): Open-drain control bits

0: Disable open-drain function

1: Enable open-drain function

6.1.63 Bank 1 R12: P6ODCR (Port 6 Open-drain Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	OD66	OD65	OD64	OD63	OD62	OD61	OD60
-	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7: Not used. Set to "**0**" all the time.

Bits 6 ~ 0 (OD66~OD60): Open-drain control bits

0: Disable open-drain function

1: Enable open-drain function

6.1.64 Bank 1 R13: P7ODCR (Port 7 Open-drain Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	-	P7HOD	P7LOD
-	-	-	-	-	-	R/W	R/W

All bits are high active.

Bits 7 ~ 2: Not used. Set to "**0**" all the time.

Bit 1 (P7HOD): Control bit used to enable open-drain of Port 7 high nibble pin

Bit 0 (P7LOD): Control bit used to enable open-drain of Port 7 low nibble pin

6.1.65 Bank 1 R14~R15: (Not used. Set to "0" all the time)

6.1.66 Bank 1 R16: PWMSCR (PWM Source Clock Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	PWMCS	PWMBS	PWMAS
-	-	-	-	-	R/W	R/W	R/W

Bits 7 ~ 3: Not used. Set to "**0**" all the time.

Bit 2 (PWMCS): Clock select for PWMC timer

0: Fs (default)

1: Fm

Bit 1 (PWMBS): Clock select for PWMB timer

0: Fs (default)

1: Fm

Bit 0 (PWMAS): Clock select for PWM timer

0: Fs (default)

1: Fm

6.1.67 Bank 1 R17: PWMACR (PWMA Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWMAE	IPWMAE	-	-	TAEN	TAP2	TAP1	TAP0
R/W	R/W	-	-	R/W	R/W	R/W	R/W

Bit 7 (PWMAE): PWMA enable bit

0: Disable (default)

1: Enable

Bit 6 (IPWMAE): Inverse PWMA enable bit

0: Disable (default)

1: Enable.

Bits 5 ~ 4: Not used. Set to "**0**" all the time.

Bit 3 (TAEN): TMRA enable bit. All PWM functions are valid only when this bit is set.

0: TMRA is off (default value)

1: TMRA is on

PWMXEN	TXEN	Function Description
0	0	Not used as PWM function, I/O pin, or as any other pin function.
0	1	Timer function, I/O pin, or other pin function
1	0	PWM function, the waveform is kept at inactive level
1	1	PWM function, normal PWM output waveform.

Bits 2 ~ 0 (TAP2 ~ TAP0): TMRA clock prescale option bits

TAP2	TAP1	TAP0	Prescale
0	0	0	1:1 (default)
0	0	1	1:2
0	1	0	1:4
0	1	1	1:8
1	0	0	1:16
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

6.1.68 Bank 1 R18: PRDAL (Low Byte of PWMA Period)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PRDA7	PRDA6	PRDA5	PRDA4	PRDA3	PRDA2	PRDA1	PRDA0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7 ~ 0 (PRDA7 ~ 0): The contents of the register are the low byte of the PWMA period.

6.1.69 Bank 1 R19: PRDAH (High Byte of PWMA Period)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PRDA15	PRDA14	PRDA13	PRDA12	PRDA11	PRDA10	PRDA9	PRDA8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (PRDA15~8): The contents of the register are the high byte of PWMA period.

6.1.70 Bank 1 R1A: DTAL (Low Byte of PMWA Duty)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DTA7	DTA6	DTA5	DTA4	DTA3	DTA2	DTA1	DTA0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7 ~ 0 (DTA7 ~ 0): The contents of the register are the low byte of the PWMA duty.

6.1.71 Bank 1 R1B: DTAH (High Byte of PMWA Duty)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DTA15	DTA14	DTA13	DTA12	DTA11	DTA10	DTA9	DTA8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7 ~ 0 (DTA15 ~ 8): The contents of the register are the high byte of the PWMA duty.

6.1.72 Bank 1 R1C: TMRAL (Low Byte of Timer A)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TMRA7	TMRA6	TMRA5	TMRA4	TMRA3	TMRA2	TMRA1	TMRA0
R	R	R	R	R	R	R	R

Bits 7 ~ 0 (TMRA7 ~ 0): The contents of the register are the low byte of the PWMA timer which is counting. This is read-only.

6.1.73 Bank 1 R1D: TMRAH (High Byte of Timer A)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TMRA15	TMRA14	TMRA13	TMRA12	TMRA11	TMRA10	TMRA9	TMRA8
R	R	R	R	R	R	R	R

Bits 7 ~ 0 (TMRA15 ~ 8): The contents of the register are the high byte of the PWMA timer which is counting. This is read-only

6.1.74 Bank 1 R1E: PWMBCR (PWMB Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWMBE	IPWMBE	-	-	TBEN	TBP2	TBP1	TBP0
R/W	R/W	-	-	R/W	R/W	R/W	R/W

Bit 7 (PWMBE): PWMB enable bit

0: Disable (default)

1: Enable

Bit 6 (IPWMBE): Inverse PWMB enable bit

0: Disable (default)

1: Enable

Bits 5 ~ 4: Not used. Set to "**0**" all the time.

Bit 3 (TBEN): TMRB enable bit. All PWM functions are valid only as this bit is set

0: TMRB is off (default value)

1: TMRB is on

Bits 2 ~ 0 (TBP2 ~ TBP0): TMRB clock prescale option bits

TBP2	TBP1	TBP0	Prescale
0	0	0	1:1 (default)
0	0	1	1:2
0	1	0	1:4
0	1	1	1:8
1	0	0	1:16
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

6.1.75 Bank 1 R1F: PRDBL (Low Byte of PWMB Period)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PRDB7	PRDB6	PRDB5	PRDB4	PRDB3	PRDB2	PRDB1	PRDB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7 ~ 0 (PRDB7 ~ 0): The contents of the register are the low byte of the PWMB period.

6.1.76 Bank 1 R20: PRDBH (High Byte of PWMB Period)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PRDB15	PRDB14	PRDB13	PRDB12	PRDB11	PRDB10	PRDB9	PRDB8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7 ~ 0 (PRDB15 ~ 8): The contents of the register are the high byte of PWMB period.

6.1.77 Bank 1 R21: DTBL (Low Byte of PMWB Duty)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DTB7	DTB6	DTB5	DTB4	DTB3	DTB2	DTB1	DTB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7 ~ 0 (DTB7 ~ 0): The contents of the register are the low byte of the PWMB duty.

6.1.78 Bank 1 R22: DTBH (High Byte of PMWB Duty)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DTB15	DTB14	DTB13	DTB12	DTB11	DTB10	DTB9	DTB8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7 ~ 0 (DTB15 ~ 8): The contents of the register are the high byte of the PWMB duty.

6.1.79 Bank 1 R23: TMRBL (Low Byte of Timer B)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TMRB7	TMRB6	TMRB5	TMRB4	TMRB3	TMRB2	TMRB1	TMRB0
R	R	R	R	R	R	R	R

Bits 7 ~ 0 (TMRB7 ~ 0): The contents of the register are the low byte of the PWMB timer which is counting. This is read-only.

6.1.80 Bank 1 R24: TMRBH (High Byte of Timer B)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TMRB15	TMRB14	TMRB13	TMRB12	TMRB11	TMRB10	TMRB9	TMRB8
R	R	R	R	R	R	R	R

Bits 7 ~ 0 (TMRB15 ~ 8): The contents of the register are the high byte of the PWMB timer which is counting. This is read-only.

6.1.81 Bank 1 R25: PWMCCR (PWMC Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWMCE	IPWMCE	-	-	TCEN	TCP2	TCP1	TCP0
R/W	R/W	-	-	R/W	R/W	R/W	R/W

Bit 7 (PWMCE): PWMC enable bit

0: Disable (default)

1: Enable

Bit 6 (IPWMCE): Inverse PWMC enable bit

0: Disable (default)

1: Enable

Bits 5 ~ 4: Not used. Set to "**0**" all the time.

Bit 3 (TCEN): TMRC enable bit. All PWM functions are valid only if this bit is set.

0: TMRC is off (default value)

1: TMRC is on

Bits 2~0 (TCP2~TCP0): TMRC clock prescale option bits

TCP2	TCP1	TCP0	Prescale
0	0	0	1:1 (default)
0	0	1	1:2
0	1	0	1:4
0	1	1	1:8
1	0	0	1:16
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

6.1.82 Bank 1 R26: PRDCL (Low Byte of PWMC Period)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PRDC7	PRDC6	PRDC5	PRDC4	PRDC3	PRDC2	PRDC1	PRDC0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7 ~ 0 (PRDC7 ~ 0): The contents of the register are the low byte of the PWMC period.

6.1.83 Bank 1 R27: PRDCH (High Byte of PWMC Period)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PRDC15	PRDC14	PRDC13	PRDC12	PRDC11	PRDC10	PRDC9	PRDC8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7 ~ 0 (PRDC15 ~ 8): The contents of the register are the high byte of PWMC period.

6.1.84 Bank 1 R28: DTCL (Low Byte of PMWC Duty)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DTC7	DTC6	DTC5	DTC4	DTC3	DTC2	DTC1	DTC0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7 ~ 0 (DTC7 ~ 0): The contents of the register are the low byte of the PWMC duty.

6.1.85 Bank 1 R29: DTCH (High Byte of PMWC Duty)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DTC15	DTC14	DTC13	DTC12	DTC11	DTC10	DTC9	DTC8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7 ~ 0 (DTC15 ~ 8): The contents of the register are the high byte of the PWMC duty.

6.1.86 Bank 1 R2A: TMRCL (Low Byte of Timer C)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TMRC7	TMRC6	TMRC5	TMRC4	TMRC3	TMRC2	TMRC1	TMRC0
R	R	R	R	R	R	R	R

Bits 7 ~ 0 (TMRC7 ~ 0): The contents of the register are the low byte of the PWMC timer which is counting. This is read-only.

6.1.87 Bank 1 R2B: TMRCH (High Byte of Timer C)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TMRC15	TMRC14	TMRC13	TMRC12	TMRC11	TMRC10	TMRC9	TMRC8
R	R	R	R	R	R	R	R

Bits 7 ~ 0 (TMRC15 ~ 8): The contents of the register are the high byte of the PWMC timer which is counting. This is read-only.

R2C ~ R3F: Not used. Set to "**0**" all the time.

6.1.88 Bank 1 R41 (Reserved)

6.1.89 Bank 1 R42 (Reserved)

6.1.90 Bank 1 R43 (Reserved)

6.1.91 Bank 1 R44 (Reserved)

6.1.92 Bank 1 R45: TBPTL (Table Pointer Low Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TB7	TB6	TB5	TB4	TB3	TB2	TB1	TB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7 ~ 0 (TB7 ~ TB0): Table Pointer Address Bits 7~0.

6.1.93 Bank 1 R46: TBPTH (Table Pointer High Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
HLB	-	-	-	TB11	TB10	TB9	TB8
R/W	-	-	-	R/W	R/W	R/W	R/W

Bit 7 (HLB): Take MLB or LSB at machine code

Bit 6 ~ 4: Not used. Set to "**0**" all the time.

Bits 3 ~ 0 (TB11 ~ TB8): Table Pointer Address Bits 11~8.

6.1.94 Bank 1 R48: PCH (Program Counter High)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	PC11	PC10	PC9	PC8
-	-	-	-	R/W	R/W	R/W	R/W

Bits 7 ~ 4: Not used. Set to "**0**" all the time.

Bits 3 ~ 0 (PC11 ~ PC8): The low byte of program counter

6.1.95 Bank 1 R49: LVDCR (Low Voltage Detector Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LVDEN	-	LVDS1	LVDS0	LVDB	-	-	-
R/W	-	R/W	R/W	R	-	-	-

Bit 7 (LVDEN): Low Voltage Detector Enable Bit

0: Disable low voltage detector

1: Enable low voltage detector

Bit 6: Not used. Set to "**0**" all the time.

Bits 5 ~ 4 (LVDS1 ~ LVDS0): Low Voltage Detector Level bits.

LVDEN	LVDS1, LVDS0	LVD Voltage Interrupt Level	LVDB
1	11	VDD <2.2V	0
		VDD >2.2V	1
1	10	VDD <3.3V	0
		VDD >3.3V	1
1	01	VDD <4.0V	0
		VDD >4.0V	1
1	00	VDD <4.5V	0
		VDD >4.5V	1
0	XX	NA	1

Bit 3 (LVDB): Low Voltage Detector State bit. This is a read only bit. When the VDD pin voltage is lower than LVD voltage interrupt level (selected by LVDS2 ~ LVDS0), this bit will be cleared.

0: The low voltage is detected.

1: The low voltage is not detected or LVD function is disabled.

6.1.96 Bank 1 R4A~R4C (Reserved)

6.1.97 Bank 1 R4D (Reserved)

6.1.98 Bank 1 R4E (Reserved)

6.1.99 Bank 1 R4F (Reserved)

6.2 TCC/WDT and Prescaler

Two 8-bit counters prescalers are available for the TCC and WDT respectively. The TPSR0~ TPSR2 bits of the TCCCR register (Bank 0 R22) are used to determine the ratio of the TCC prescaler. Likewise, the WPSR0~WPSR2 bits of the WDTCR register (Bank0 R21) are used to determine the prescaler for the WDT. The prescaler counter is cleared by the instructions each time they are written into TCC. The WDT and prescaler are cleared by the "WDTC" and "SLEP" instructions. Figure 6-3 below depicts the circuit diagram of TCC/WDT.

TCCD (Bank 0 R23) is an 8-bit timer/counter. The TCC clock source can be either internal clock or external signal input (edge selectable from the TCC pin). As illustrated below, if the TCC signal source is from internal clock, TCC will increase by 1 at every instruction cycle (without prescaler). If the TCC signal source is from THE external clock input, The TCC will be incremented by 1 at every falling edge or rising edge of the TCC pin. The TCC pin input time length (kept in High or Low level) must be greater than 1CLK. **The TCC will stop running when Sleep mode occurs.**

The watchdog timer is a free running on-chip RC oscillator. The WDT will keep on running even after the oscillator driver has been turned off (i.e., in Sleep mode). During Normal operation or Sleep mode, a WDT time-out (if enabled) will cause the device to reset. The WDT can be enabled or disabled at any time during Normal mode by software programming (see WDTE bit of WDTCR register in Section 6.1.25). With no prescaler, the WDT time-out period is approximately 16ms[1] (one oscillator start-up timer period).

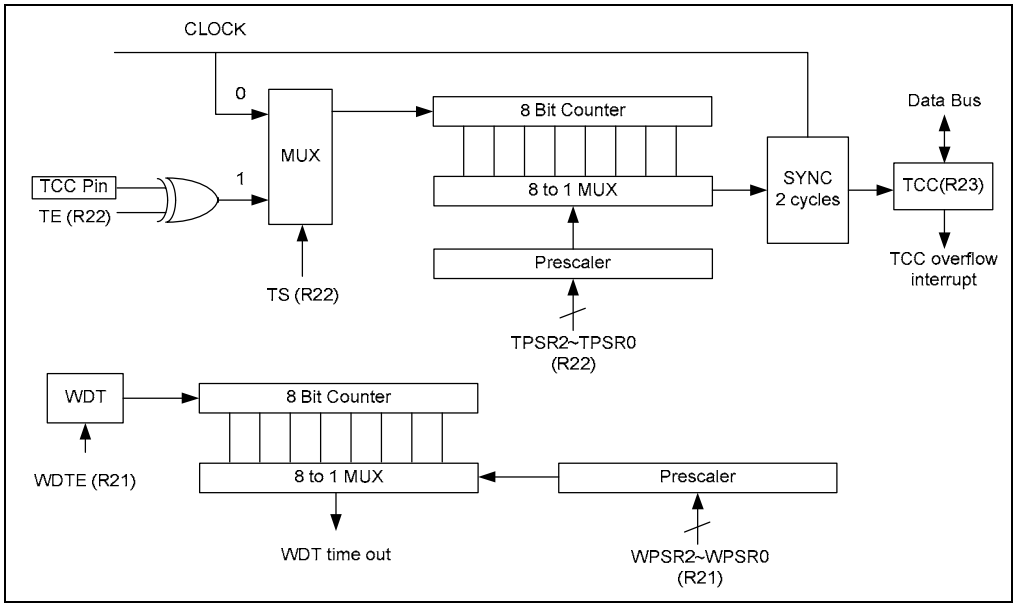


Figure 6-3 TCC and WDT Block Diagram

[1] *VDD=5V, 25°C WDT time-out period = 16ms ±38%.*

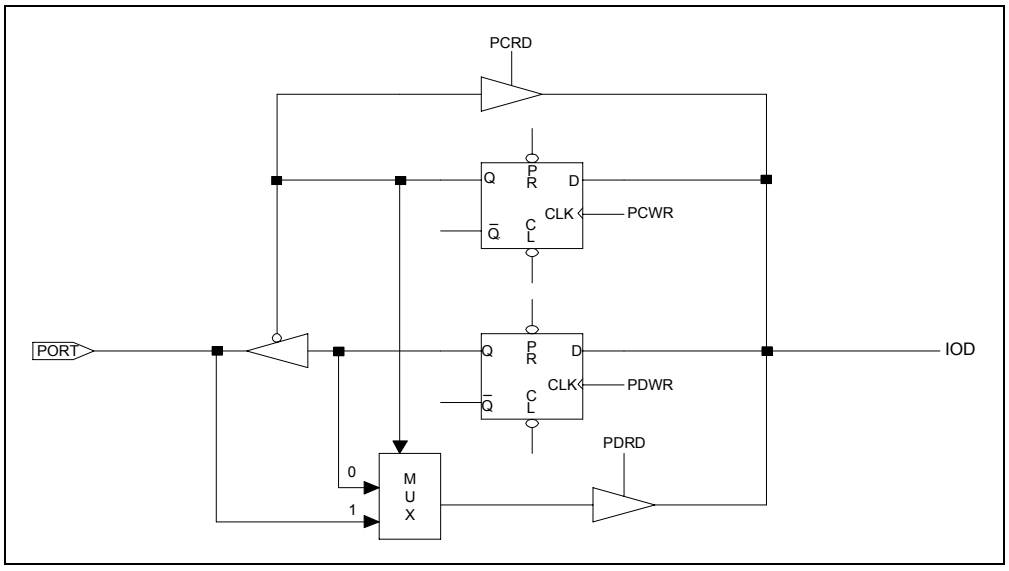
6.3 I/O Ports

The I/O registers, Port 5~Port 7 are bi-directional tri-state I/O ports. All ports can be pulled high and pulled low internally by software. Furthermore, they can also be set as open-drain output and high sink/drive by software. Port 5 and Port 6 feature wake-up and interrupt functions, as well as input status change interrupt function. Each I/O pin can be defined as "input" or "output" pin by the I/O Control registers (IOC5 ~ IOC7).

The I/O registers and I/O Control registers are both readable and writable. The I/O interface circuits for Port 5 ~ Port 7 are shown in the subsequent Figures 6-4a to 6-4d.

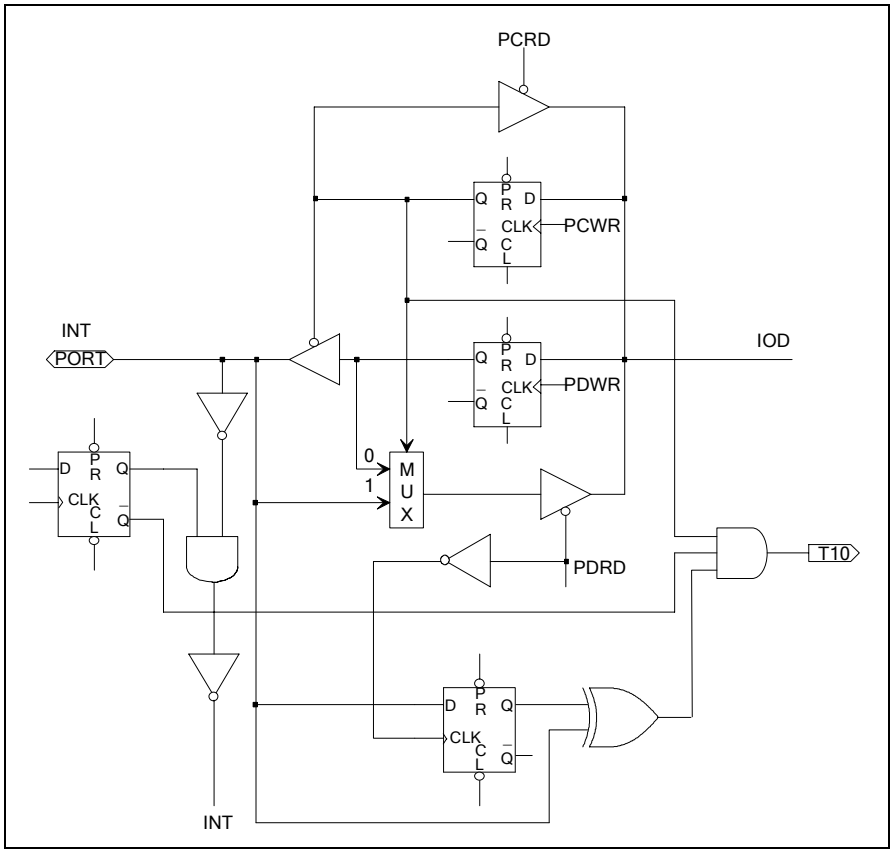
The EM78P374N has three different types of packaging with different number of pins. To achieve lowest power consumption, it is highly recommended to program the “not-used” P52, P71, and P72 ~ P75 on the 18-pin DIP/SOP package, and P72 ~P75 on the 20-pin DIP/SOP package as follows**:**

1. When the “not-used” pins need to be defined as output ports, the pins should be set as output high or pull low relative to its pull high/low status.
2. When the “not-used” pins need to be defined as input ports, the pins should be set as input pull high or pull low.



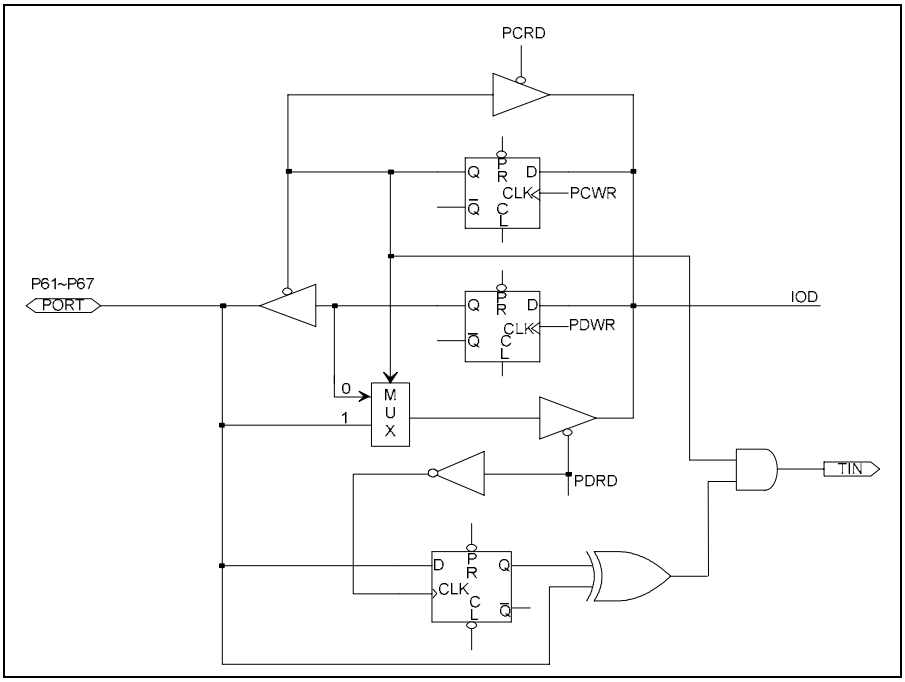
Note: *Pull-down is not shown in the figure.*

Figure 6-4a I/O Port and I/O Control Register Circuit for Ports 5~7



Note: *Pull-high (down) and Open-drain are not shown in the figure.*

Figure 6-4b I/O Port and I/O Control Register Circuit for /INT



Note: *Pull-high (down) and Open-drain are not shown in the figure.*

Figure 6-4c I/O Port and I/O Control Register Circuit for Ports 5~7

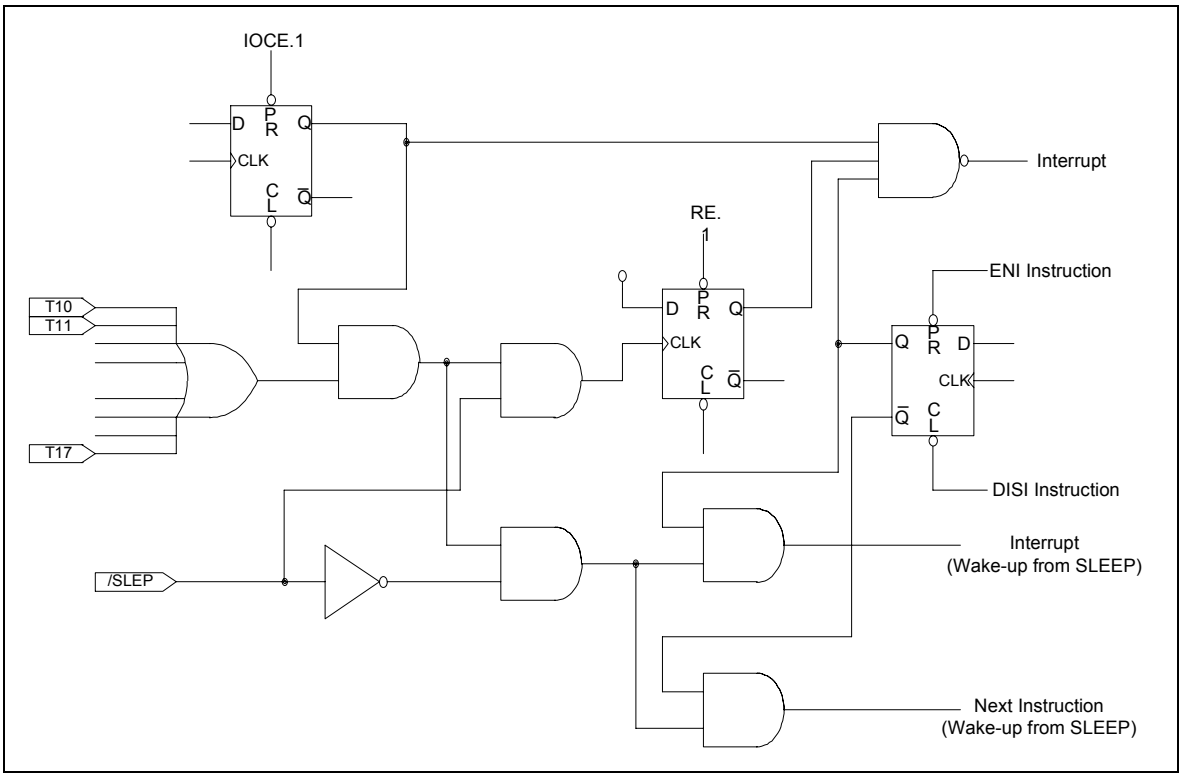


Figure 6-4d I/O Port 5~6 with Input Change Interrupt/Wake-up Block Diagram

6.3.1 Usage of Ports 5~6 Input Change Wake-up/Interrupt Function

1. Wake-up
a) Before Sleep:
1) Disable WDT
2) Read I/O Port (MOV R6,R6)
3) Execute "ENI" or "DISI"
4) Enable Wake-up bit (Set WUE6H =1, WUE6L =1)
5) Execute "SLEP" instruction
b) After wake-up:
→ Next instruction

2. Wake-up and Interrupt
a) Before Sleep
1) Disable WDT
2) Read I/O Port (MOV R6, R6)
3) Execute "ENI" or "DISI"
4) Enable wake-up bit (Set WUE6H =1, WUE6L =1)
5) Enable interrupt (Set ICIE =1)
6) Execute "SLEP" instruction
b) After Wake-up
1) IF "ENI" → Interrupt vector (0006H)
2) IF "DISI" → Next instruction

6.4 Reset and Wake-up Operation

A reset is initiated by one of the following events:

1) Power on reset

2) /RESET pin input "low"

3) WDT time-out (if enabled)

4) LVR (if enabled)

The device is kept in a reset condition for a period of approximately 16ms (one oscillator start-up timer period) after the Power-on reset is detected. And if the /RESET pin goes “low” or WDT time-out is active, a reset is generated. In RC mode the reset time is 8/32 clocks, and in XTAL mode; the reset time is 510 clocks. Once a reset occurs, the following functions are performed:

- The oscillator continues to run
- The Program Counter (R2) is set to all "**0**".
- The contents of the stack are cleared to all “**0**”.
- All I/O port pins are configured at input mode (high-impedance state).
- The Watchdog Timer and prescaler are cleared.
- When power is switched on, R1 is cleared.
- The control register bits are set according to the table shown in Section 6.4.3, *Summary of the Registers Initialized Values*.

Executing the “SLEP” instruction will assert the Sleep (power down) mode. While entering Sleep mode, the Oscillator, TCC, and Timer 1 are stopped. The WDT (if enabled) is cleared but keeps on running. Wake-up is then generated (in RC mode, Wake-up time is WSTO + 8 clocks; in High XTAL mode, Wake-up time is WSTO+ 510 clocks). The controller can be awakened by any of the following events:

1) External reset input on /RESET pin

2) WDT time-out (if enabled)

3) Port input status changes (if ICWE is enabled)

4) External Interrupt status changes (if INTWK is enabled)

5) Low Voltage Detector (if LVDWE is enabled)

6) A/D conversion completed (if ADWE is enabled)

7) I2C received data while acting as Slave device (if I2CWE is enabled)

8) Comparator output status changes (if the corresponding control bit is enabled)

The first two events (1 and 2) will cause the MCU to reset. The T and P flags of R3 can be used to determine the source of the reset (Wake-up). Events 3~8 are considered the continuation of program execution and the global interrupt ("ENI" or "DISI" being executed) decides whether or not the controller branches to the interrupt vector following Wake-up. If ENI is executed before SLEP, the instruction will begin to execute from the Address 0x03~0x36 of each interrupt vector after Wake-up. If DISI is executed before SLEP, the execution will restart from the instruction right next to SLEP after Wake-up. From Sleep to Normal mode, Wake-up time is 510 clocks + warm-up time with Crystal oscillator and 8 clocks (Fm) + warm-up time with IRC oscillator. From Idle to Green mode, only warm-up time is needed. From Sleep to Green mode the wake-up time is 8 clocks (Fs) + warm-up time.

One or more of Events 3 to 9 can be enabled before entering Sleep mode. That is**:**

a) If WDT is enabled before SLEP, all Wake-up bits are disabled. Hence, the MCU can be awakened only by Events 1 or 2. Refer to Section 6.5, *Interrupt*; for further details.

b) If Port Input Status Change is used to Wake-up the MCU, the Bank 0-0x12 register must be enabled and the WDT disabled before SLEP. The MCU can then be awakened by Event 3.

c) If External Interrupt Status Change is used to Wake-up the MCU, the INTWK bit must be enabled and the WDT disabled before SLEP. The MCU can then be awakened by Event 4

d) If Low Voltage Detector is used to Wake-up the MCU, the LVDWK bit of Bank 0-R10 register must be enabled and the WDT disabled before SLEP. The MCU can then be awakened by Event 5.

e) If AD Conversion Completed is used to Wake-up the MCU, the ADWK bit of Bank 0-R10 register must be enabled and the WDT disabled before SLEP. The MCU can then be awakened by Event 6.

f) When I^2C is acting as Slave device and it is used to Wake-up the MCU after receiving data, the I2CWK bit of Bank 0-R11 register must be enabled and the WDT disabled by software before SLEP. The MCU can then be awakened by Event 7.

g) If Comparator Output Status Change is used to Wake-up the MCU, the CMP2WK bit of Bank 0-0x10 register must be enabled and the WDT disabled before SLEP. The MCU can then be awakened by Event 8.

6.4.1 Summary of Wake-up and Interrupt Modes

Wake-up Signal	Condition Signal	Sleep Mode		Idle Mode		Green Mode		Normal Mode	
		DISI	ENI	DISI	ENI	DISI	ENI	DISI	ENI
TCC (Used as Timer)	TCIE = 0	Wake-up is invalid		Wake-up is invalid		Interrupt is invalid		Interrupt is invalid	
	TCIE = 1			Wake up + Next Instruction	Wake up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
TCC (Used as Counter)	TCIE = 0	Wake-up is invalid		Wake-up is invalid		Interrupt is invalid		Interrupt is invalid	
	TCIE = 1	Wake up + Next Instruction	Wake up + Interrupt Vector	Wake up + Next Instruction	Wake up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
PWMA/B/C When Timer A/B/C match PRDA/B/C	PWMxPIE=0	Wake-up is invalid		Wake-up is invalid		Interrupt is invalid		Interrupt is invalid	
	PWMxPIE=1			Wake up + Next Instruction	Wake up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
PWMA/B/C (When Timer A/B/C match DTA/B/C)	PWMxDIE = 0	Wake-up is invalid		Wake-up is invalid		Interrupt is invalid		Interrupt is invalid	
	PWMxDIE = 1			Wake up + Next Instruction	Wake up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
TC1 Interrupt (Used as Timer)	TC1/2/3IE = 0	Wake-up is invalid		Wake-up is invalid		Interrupt is invalid		Interrupt is invalid	
	TC1/2/3IE = 1			Wake up + Next Instruction	Wake up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
TC1 Interrupt (Used as Counter)	TC1/2/3IE = 0	Wake-up is invalid		Wake-up is invalid		Interrupt is invalid		Interrupt is invalid	
	TC1/2/3IE = 1	Wake up + Next Instruction	Wake up + Interrupt Vector	Wake up + Next Instruction	Wake up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
External INT	INTWKx = 0, EXIEx = 0	Wake-up is invalid		Wake-up is invalid		Interrupt is invalid		Interrupt is invalid	
	INTWKx = 0, EXIEx = 1	Wake-up is invalid		Wake-up is invalid		Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
	INTWKx = 1, EXIEx = 0	Wake up + Next Instruction		Wake up + Next Instruction		Interrupt is invalid		Interrupt is invalid	
	INTWKx = 1, EXIEx = 1	Wake up + Next Instruction	Wake up + Interrupt Vector	Wake up + Next Instruction	Wake up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector

(Continuation)

Wake-up Signal	Condition Signal	Sleep Mode		Idle Mode		Green Mode		Normal Mode	
		DISI	ENI	DISI	ENI	DISI	ENI	DISI	ENI
Pin change	ICWKPx = 0 PxICIE = 0	Wake-up is invalid		Wake-up is invalid		Interrupt is invalid		Interrupt is invalid	
	ICWKPx = 0 PxICIE = 1	Wake-up is invalid		Wake-up is invalid		Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
	ICWKPx = 1 PxICIE = 0	Wake up + Next Instruction		Wake up + Next Instruction		Interrupt is invalid		Interrupt is invalid	
	ICWKPx = 1, PxICIE = 1	Wake up + Next Instruction	Wake up + Interrupt Vector	Wake up + Next Instruction	Wake up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
Comparator x (Comparator output status change, x=2)	CMPxWK=0 CMPxIE=0	Wake-up is invalid		Wake-up is invalid		Interrupt is invalid		Interrupt is invalid	
	CMPxWK=0 CMPxIE=1	Wake-up is invalid		Wake-up is invalid		Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
	CMPxWK=1 CMPxIE=0	Wake up + Next Instruction		Wake up + Next Instruction		Interrupt is invalid		Interrupt is invalid	
	CMPxWK=1 CMPxIE=1	Wake up + Next Instruction	Wake up + Interrupt Vector	Wake up + Next Instruction	Wake up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
AD Conversion complete	ADWK = 0 ADIE = 0	Wake-up is invalid		Wake-up is invalid		Interrupt is invalid		Interrupt is invalid	
	ADWK = 0 ADIE = 1	Wake-up is invalid		Wake-up is invalid		Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
	ADWK = 1 ADIE = 0	Wake up + Next Instruction		Wake up + Next Instruction		Interrupt is invalid		Interrupt is invalid	
	ADWK = 1 ADIE = 1	Wake up + Next Instruction	Wake up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
I2C (Slave mode)	I2CWK=0 I2CRIE=0	Wake-up is invalid		Wake-up is invalid		Interrupt is invalid		Interrupt is invalid	
	I2CWK=0 I2CRIE=1	Wake-up is invalid		Wake-up is invalid		Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
	I2CWK=1 I2CRIE=0	Wake up + Next Instruction		Wake up + Next Instruction		Interrupt is invalid		Interrupt is invalid	
	I2CWK=1 I2CRIE=1	Wake up + Next Instruction	Wake up + Interrupt Vector	Wake up + Next Instruction	Wake up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector

Wake-up Signal	Condition Signal	Sleep Mode		Idle Mode		Green Mode		Normal Mode	
		DISI	ENI	DISI	ENI	DISI	ENI	DISI	ENI
Low Voltage Detector	LVDWK = 0 LVDIE = 0	Wake-up is invalid		Wake-up is invalid		Interrupt is invalid		Interrupt is invalid	
	LVDWK = 0 LVDIE = 1	Wake-up is invalid		Wake-up is invalid		Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
	LVDWK = 1 LVDIE = 0	Wake up + Next Instruction		Wake up + Next Instruction		Interrupt is invalid.		Interrupt is invalid.	
	LVDWK = 1 LVDIE = 1	Wake up + Next Instruction	Wake up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
Low Voltage Reset		Wake up + Reset		Wake up + Reset		Reset		Reset	
WDT Timeout		Wake up + Reset		Wake up + Reset		Reset		Reset	

6.4.2 Status of RST, T, and P of Status Register

A reset condition is initiated by one of the following events:

1) Power-on condition,

2) High-low-high pulse on /RESET pin, and

3) Watchdog timer time-out.

4) LVR occur

The values of T and P, as listed in the following table are used to check how the MCU wakes up. The next table shows the events that may affect the status of T and P.

■ **Values of RST, T and P after reset:**

Reset Type	T	P
Power-on	1	1
/RESET during Operating mode	*P	*P
/RESET Wake-up during Sleep mode	1	0
WDT during Operating mode	0	*P
WDT Wake-up during Sleep mode	0	0
Wake-up on pin change during Sleep mode	1	0

** **P:** Previous status before reset*

■ **Status of T and P being affected by Events:**

Event	T	P
Power-on	1	1
WDTC instruction	1	1
WDT time-out	0	*P
SLEP instruction	1	0
Wake-up on pin change during Sleep mode	1	0

** **P:** Previous value before reset*

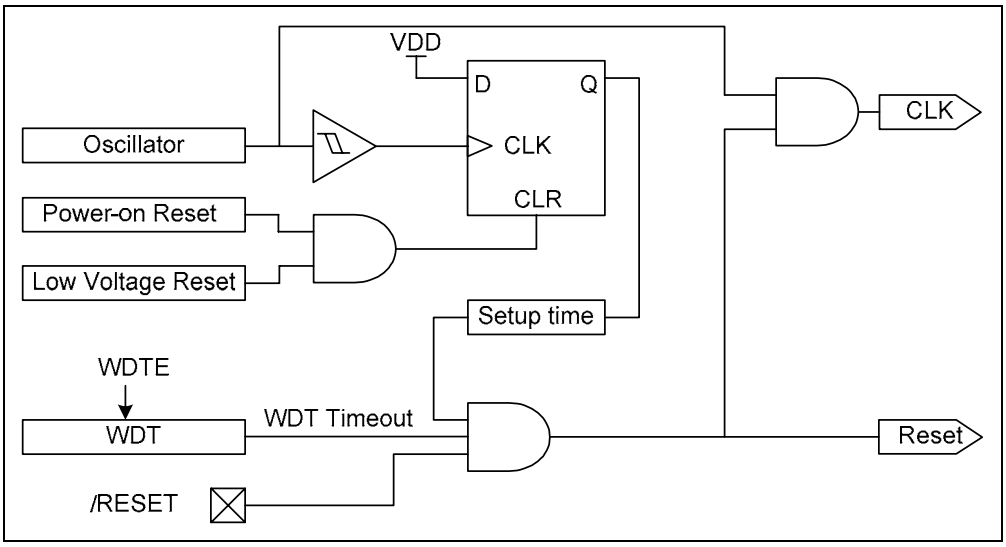


Figure 6-5 Controller Reset Block Diagram

6.4.3 Summary of Register Initial Values after Reset

Legend: ***U:*** *Unknown or don't care* ***P:*** *Previous value before reset*
C: *Same with Code option* ***t:*** *Check tables under Section 6.4.2*

Addr.	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x00	R0 (IAR)	Bit Name	-	-	-	-	-	-	-	-
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0x01	R1 (BSR)	Bit Name	-	-	-	SBS0	-	GBS2	GBS1	GBS0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	0	0	0	P	0	0	0	P
0x02	R2 (PCL)	Bit Name	-	-	-	-	-	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0x03	R3 (SR)	Bit Name	INT	-	-	T	P	Z	DC	C
		Power-on	0	0	0	1	1	U	U	U
		/RESET and WDT	0	0	0	t	t	P	P	P
		Wake-up from Sleep/Idle	P	0	0	t	t	P	P	P

(Continuation)

Addr.	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x04	R4 (RSR)	Bit Name	RSR7	RSR6	RSR5	RSR4	RSR3	RSR2	RSR1	RSR0
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X05	Bank 0, R5 (Port 5)	Bit Name	P57	P56	P55	P54	P53	P52	P51	P50
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0x06	Bank 0, R6 (Port 6)	Bit Name	P67	P66	P65	P64	P63	P62	P61	P60
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0x07	Bank 0, R7 (Port 7)	Bit Name	-	-	P75	P74	P73	P72	P71	P70
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X0B	Bank 0, RB (IOCR5)	Bit Name	IOC57	IOC56	IOC55	IOC54	IOC53	IOC52	IOC51	IOC50
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0x0C	Bank 0, RC (IOCR6)	Bit Name	IOC67	IOC66	IOC65	IOC64	IOC63	IOC62	IOC61	IOC60
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X0D	Bank 0, RD (IOCR7)	Bit Name	-	-	IOC75	IOC74	IOC73	IOC72	IOC71	IOC70
		Power-on	0	0	1	1	1	1	1	1
		/RESET and WDT	0	0	1	1	1	1	1	1
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0x0E	Bank 0, RE (OMCR)	Bit Name	CPUS	IDLE	-	-	-	-	RCM1	RCM0
		Power-on	1	1	0	0	0	0	C	C
		/RESET and WDT	1	1	0	0	0	0	C	C
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P

(Continuation)

Addr.	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0F	Bank 0, RF (IESCR)	Bit Name	-	-	EIES54	-	-	-	-	-
		Power-on	0	0	1	0	0	0	0	0
		/RESET and WDT	0	0	1	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	0	0
0x10	Bank 0, R10 (WUCR1)	Bit Name	CMP2WK	-	LVDWK	ADWK	-	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	0	0
0x11	Bank 0, R11 (WUCR2)	Bit Name	-	-	-	-	-	I2CWK	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	0	0	P	P	0	0
0x12	Bank 0, R12 (WUCR3)	Bit Name	-	-	ICWKP6	ICWKP5	-	-	INTWK5	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X13	Bank 0, R13	Bit Name	-	-	-	-	-	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	0	0	0	0	P	P	0	0
0X14	Bank 0, R14 (SFR1)	Bit Name	CMP2SF	-	LVDSF	ADSF	-	-	-	TCSF
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X15	Bank 0, R15 (SFR2)	Bit Name	-	-	-	-	-	-	-	TC1DSF
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P

(Continuation)

Addr.	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0X16	Bank 0, R16 (SFR3)	Bit Name	-	-	PWM CPSF	PWM CDSF	PWM BPSF	PWMB DSF	PWM APSF	PWM ADSF
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X17	Bank 0, R17 (SFR4)	Bit Name	-	-	P6ICSF	P5ICSF	-	I2CSTPSF	I2CRSF	I2CTSF
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X18	Bank 0, R18 (SFR5)	Bit Name	-	-	-	-	EXSF5	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X1B	Bank 0, R1B (IMR1)	Bit Name	CMP2IE	-	LVDIE	ADIE	-	-	-	TCIE
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X1C	Bank 0, R1C (IMR2)	Bit Name	-	-	-	-	-	-	-	TC1DIE
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X1D	Bank 0, R1D (IMR3)	Bit Name	-	-	PWM CPIE	PWM CDIE	PWM BPIE	PWM BDIE	PWM APIE	PWM ADIE
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	0	0	P	P	P	P	P	P
0X1E	Bank 0, R1E (IMR4)	Bit Name	-	-	P6ICE	P5ICE	-	I2CSTPIE	I2CRIE	I2CTIE
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	0	0	P	P	P	P	P	P

(Continuation)

Addr.	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0X1F	Bank 0, R1F (IMR5)	Bit Name	-	-	-	-	EXIE5	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X21	Bank 0, R21 (WDTCR)	Bit Name	WDTE	-	-	-	PSWE	WPSR2	WPSR1	WPSR0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X22	Bank 0, R22 (TCCCR)	Bit Name	-	TCCS	TS	TE	PSTE	TPSR2	TPSR1	TPSR0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X23	Bank 0, R23 (TCCD)	Bit Name	TCC7	TCC6	TCC5	TCC4	TCC3	TCC2	TCC1	TCC0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X24	Bank 0, R24 (TC1CR1)	Bit Name	TC1S	TC1RC	TC1SS1	-	TC1FF	TC1OMS	TC1IS1	TC1IS0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X25	Bank 0, R25 (TC1CR2)	Bit Name	TC1M2	TC1M1	TC1M0	TC1SS0	TC1CK3	TC1CK2	TC1CK1	TC1CK0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X26	Bank 0, R26 (TC1DA)	Bit Name	TC1DA7	TC1DA6	TC1DA5	TC1DA4	TC1DA3	TC1DA2	TC1DA1	TC1DA0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X27	Bank 0, R27 (TC1DB)	Bit Name	TC1DB7	TC1DB6	TC1DB5	TC1DB4	TC1DB3	TC1DB2	TC1DB1	TC1DB0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P

(Continuation)

Addr.	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0X30	Bank 0, R30 (I2CCR1)	Bit Name	STROBE /PEND	IMS	ISS	STOP	SAR_ EMPTY	ACK	FULL	EMPTY
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X31	Bank 0, R31 (I2CCR2)	Bit Name	I2CBF	GCEN	-	BBF	I2CTS1	I2CTS0	I2CCS	I2CEN
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X32	Bank 0, R32 (I2CSA)	Bit Name	SA6	SA5	SA4	SA3	SA2	SA1	SA0	IRW
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X33	Bank 0, R33 (I2CDB)	Bit Name	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	0	0	P	P	P	P	P	P
0X34	Bank 0, R34 (I2CDAL)	Bit Name	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X35	Bank 0, R35 (I2CDAH)	Bit Name	-	-	-	-	-	-	DA9	DA8
		Power-on	0	0	0	0	0	0	1	1
		/RESET and WDT	0	0	0	0	0	0	1	1
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P

(Continuation)

Addr.	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0X3B	Bank 0, R3B (CMP2CR)	Bit Name	C2RS	CP2OUT	C2S1	C2S0	-	-	-	SDPWMB
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X3C	Bank 0, R3C (CMP3CR)	Bit Name	-	-	-	-	-	CIRL11	CIRL10	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X3D	Bank 0, R3D (CMP4CR)	Bit Name	-	-	-	-	-	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X3E	Bank 0, R3E (ADCR1)	Bit Name	CKR2	CKR1	CKR0	ADRUN	ADP	ADOM	SHS1	SHS0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X3F	Bank 0, R3F (ADCR2)	Bit Name	-	-	ADIM	ADCMS	VPIS1	VPIS0	VREFP	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	P	P
0X40	Bank 0, R40 (ADISR)	Bit Name	-	-	-	ADIS4	ADIS3	ADIS2	ADIS1	ADIS0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X41	Bank 0, R41 (ADER1)	Bit Name	ADE7	ADE6	ADE5	ADE4	ADE3	ADE2	ADE1	ADE0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P

(Continuation)

Addr.	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0X42	Bank 0, R42 (ADER2)	Bit Name	-	-	ADE13	ADE12	ADE11	ADE10	ADE9	ADE8
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X43	Bank 0, R43 (ADDL)	Bit Name	ADD7	ADD6	ADD5	ADD4	ADD3	ADD2	ADD1	ADD0
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Sleep/Idle	P	P	P	0	0	P	P	P
0X44	Bank 0, R44 (ADDH)	Bit Name	ADD15	ADD14	ADD13	ADD12	ADD11	ADD10	ADD9	ADD8
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Sleep/Idle	0	0	0	P	P	P	P	P
0X45	Bank 0, R45 (ADCVL)	Bit Name	ADCV7	ADCV6	ADCV5	ADCV4	ADCV3	ADCV2	ADCV1	ADCV0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Sleep/Idle	0	0	0	P	P	P	P	P
0X46	Bank 0, R46 (ADCVH)	Bit Name	ADCV15	ADCV14	ADCV13	ADCV12	ADCV11	ADCV10	ADCV9	ADCV8
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X08	Bank 1, R8 (P5PHCR)	Bit Name	PH57	PH56	PH55	PH54	PH53	PH52	PH51	PH50
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X09	Bank 1, R9 (P6PHCR)	Bit Name	-	PH66	PH65	PH64	PH63	PH62	PH61	PH60
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P

(Continuation)

Addr.	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0X0A	Bank 1, RA (P7PHCR)	Bit Name	-	-	-	-	-	-	P7HPH	P7LPH
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X0B	Bank 1, RB (P5PLCR)	Bit Name	PL57	PL56	PL55	PL54	PL53	PL52	PL51	PL50
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X0C	Bank 1, RC (P6PLCR)	Bit Name	PL67	PL66	PL65	PL64	PL63	PL62	PL61	PL60
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X0D	Bank 1, RD (P7PLCR)	Bit Name	-	-	-	-	-	-	P7HPL	P7LPL
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X0E	Bank 1, RE (P5HDSCR)	Bit Name	H57	H56	H55	H54	H53	H52	H51	H50
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X0F	Bank 1, RF (P6HDSCR)	Bit Name	H67	H66	H65	H64	H63	H62	H61	H60
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X10	Bank 1, R10 (P7HDSCR))	Bit Name	-	-	-	-	-	-	P7HHDS	P7LHDS
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X11	Bank 1, R11 (P5ODCR)	Bit Name	OD57	OD56	OD55	OD54	OD53	OD52	OD51	OD50
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P

(Continuation)

Addr.	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0X12	Bank 1, R12 (P6ODCR)	Bit Name	-	OD66	OD65	OD64	OD63	OD62	OD61	OD60
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X13	Bank 1, R13 (P7ODCR)	Bit Name	-	-	-	-	-	-	P7HOD	P7LOD
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X16	Bank 1, R16 (PWMSCR)	Bit Name	-	-	-	-	-	PWMCS	PWMBS	PWMAS
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X17	Bank 1, R17 (PWMACR)	Bit Name	PWMAE	IPWMAE	-	-	TAEN	TAP2	TAP1	TAP0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X18	Bank 1, R18 (PRDAL)	Bit Name	PRDA7	PRDA6	PRDA5	PRDA4	PRDA3	PRDA2	PRDA1	PRDA0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X19	Bank 1, R19 (PRDAH)	Bit Name	PRDA15	PRDA14	PRDA13	PRDA12	PRDA11	PRDA10	PRDA9	PRDA8
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X1A	Bank 1, R1A (DTAL)	Bit Name	DTA7	DTA6	DTA5	DTA4	DTA3	DTA2	DTA1	DTA0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X1B	Bank 1, R1B (DTAH)	Bit Name	DTA15	DTA14	DTA13	DTA12	DTA11	DTA10	DTA9	DTA8
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	0	0	P	P	P	P	P	P

(Continuation)

Addr.	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0X1C	Bank 1, R1C (TMRAL)	Bit Name	TMRA7	TMRA6	TMRA5	TMRA4	TMRA3	TMRA2	TMRA1	TMRA0
		Power-on	0	0	0	0	0	0	0	1
		/RESET and WDT	0	0	0	0	0	0	0	1
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X1D	Bank 1, R1D (TMRAH)	Bit Name	TMRA15	TMRA14	TMRA13	TMRA12	TMRA11	TMRA10	TMRA9	TMRA8
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X1E	Bank 1, R1E (PWMBCR)	Bit Name	PWMBE	IPWMBE	-	-	TBEN	TBP2	TBP1	TBP0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X1F	Bank 1, R1F (PRDBL)	Bit Name	PRDB7	PRDB6	PRDB5	PRDB4	PRDB3	PRDB2	PRDB1	PRDB0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X20	Bank 1, R20 (PRDBH)	Bit Name	PRDB15	PRDB14	PRDB13	PRDB12	PRDB11	PRDB10	PRDB9	PRDB8
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X21	Bank 1, R21 (DTBL)	Bit Name	DTB7	DTB6	DTB5	DTB4	DTB3	DTB2	DTB1	DTB0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	0	0	0	0	P	P	P	P
0X22	Bank 1, R22 (DTBH)	Bit Name	DTB15	DTB14	DTB13	DTB12	DTB11	DTB10	DTB9	DTB8
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X23	Bank 1, R23 (TMRBL)	Bit Name	TMRB7	TMRB6	TMRB5	TMRB4	TMRB3	TMRB2	TMRB1	TMRB0
		Power-on	0	0	0	0	0	0	0	1
		/RESET and WDT	0	0	0	0	0	0	0	1
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P

(Continuation)

Addr.	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0X24	Bank 1, R24 (TMRBH)	Bit Name	TMRB15	TMRB14	TMRB13	TMRB12	TMRB11	TMRB10	TMRB9	TMRB8
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X25	Bank 1, R25 (PWMCCR)	Bit Name	PWMCE	IPWMCE	-	-	TCEN	TCP2	TCP1	TCP0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X26	Bank 1, R26 (PRDCL)	Bit Name	PRDC7	PRDC6	PRDC5	PRDC4	PRDC3	PRDC2	PRDC1	PRDC0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X27	Bank 1, R27 (PRDCH)	Bit Name	PRDC15	PRDC14	PRDC13	PRDC12	PRDC11	PRDC10	PRDC9	PRDC8
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X28	Bank 1, R28 (DTCL)	Bit Name	DTC7	DTC6	DTC5	DTC4	DTC3	DTC2	DTC1	DTC0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X29	Bank 1, R29 (DTCH)	Bit Name	DTC15	DTC14	DTC13	DTC12	DTC11	DTC10	DTC9	DTC8
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X2A	Bank 1, R2A (TMRCL)	Bit Name	TMRC7	TMRC6	TMRC5	TMRC4	TMRC3	TMRC2	TMRC1	TMRC0
		Power-on	0	0	0	0	0	0	0	1
		/RESET and WDT	0	0	0	0	0	0	0	1
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X2B	Bank 1, R2B (TMRCH)	Bit Name	TMRC15	TMRC14	TMRC13	TMRC12	TMRC11	TMRC10	TMRC9	TMRC8
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P

(Continuation)

Addr.	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0X45	Bank 1, R45 (TBPTL)	Bit Name	TB7	TB6	TB5	TB4	TB3	TB2	TB1	TB0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X46	Bank 1, R46 (TBPTH)	Bit Name	HLB	-	-	-	TB11	TB10	TB9	TB8
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X48	Bank 1, R48 (PCH)	Bit Name	-	-	-	-	PC11	PC10	PC9	PC8
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X49	Bank 1, R49 (LVDCR)	Bit Name	LVDEN	-	LVDS1	LVDS0	LVDB	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X4A	Bank 1, R4A	Bit Name	-	-	-	-	-	-	-	-
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X4B	Bank 1, R4B	Bit Name	-	-	-	-	-	-	-	-
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X4C	Bank 1, R4C	Bit Name	-	-	-	-	-	-	-	-
		Power-on	1	0	1	1	1	1	1	1
		/RESET and WDT	1	0	1	1	1	1	1	1
		Wake-up from Sleep/Idle	P	0	P	P	0	P	P	P

6.5 Interrupt

The EM78P374N has 16 interrupts as listed below**:**

Interrupt Source		Enable Condition	Int. Flag	Int. Vector	Priority
Internal / External	Reset	-	-	0	High 0
External	INT	ENI + EXIE=1	EXSF	2	1
External	Pin change	ENI +ICIE=1	ICSF	4	2
Internal	TCC	ENI + TCIE=1	TCSF	6	3
Internal	LVD	ENI+LVDEN & LVDIE=1	LVDSF	8	4
External	Comparator 2	ENI+CMP2IE=1	CMP2SF	E	5
Internal	AD	ENI + ADIE=1	ADSF	10	6
Internal	TC1 (TCXDA)	ENI + TC1IE=1	TC1SF	12	7
Internal	PWMPA	ENI+PWMPAIE=1	PWMPASF	14	8
Internal	PWMDA	ENI+PWMDAIE=1	PWMDASF	16	9
Internal	I2C Transmit	ENI+ I2CTIE	I2CTSF	1A	10
Internal	I2C Receive	ENI+ I2CRIE	I2CRSF	1C	11
Internal	I2CSTOP	ENI+ I2CSTPIE	I2CSTPSF	1E	12
Internal	PWMPB	ENI+PWMPBIE=1	PWMPBSF	24	13
Internal	PWMDB	ENI+PWMDBIE=1	PWMDBSF	26	14
Internal	PWMPC	ENI+PWMPCIE=1	PWMPCSF	2A	15
Internal	PWMDC	ENI+PWMDCIE=1	PWMDCSF	2C	16

Bank 0 R14 ~ R1F are the interrupt status registers that record the interrupt requests in the relative flags/bits. Bank 0 R1B ~ R1F are the Interrupt Mask registers. The global interrupt is enabled by the ENI instruction and is disabled by the DISI instruction. When one of the enabled interrupts occurs, the next instruction will be fetched from individual address. The interrupt flag bit must be cleared by instructions before leaving the interrupt service routine and before interrupts are enabled to avoid recursive interrupts.

The flag (except ICSF bit delete) in the Interrupt Status Register is set regardless of the status of its mask bit or the execution of ENI. The RETI instruction ends the interrupt routine and enables the global interrupt (the execution of ENI).

External interrupt is equipped with digital noise rejection circuit (input pulse of less than **four system clock time** is eliminated as noise if code option NRHL=0), **but in Low XTAL oscillator (LXT) mode, the noise rejection circuit is disabled**. When an interrupt (Falling edge) is generated by the External interrupt (if enabled), the next instruction will be fetched from Address 003H.

Before the interrupt subroutine is executed, the contents of ACC, R3, and R4 registers are saved by hardware. If another interrupt occurs, the ACC, R3, and R4 registers will be replaced by the new interrupt. After the interrupt service routine is finished, ACC, R3, and R4 registers are restored.

When a reset (POR, LVR, WDT, and /RESET) occurs, the contents of the stack are cleared to all "**0**".

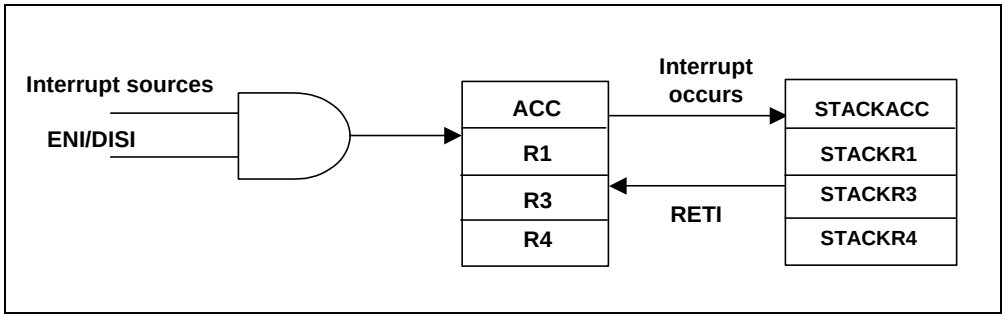


Figure 6-6a Interrupt Backup Diagram

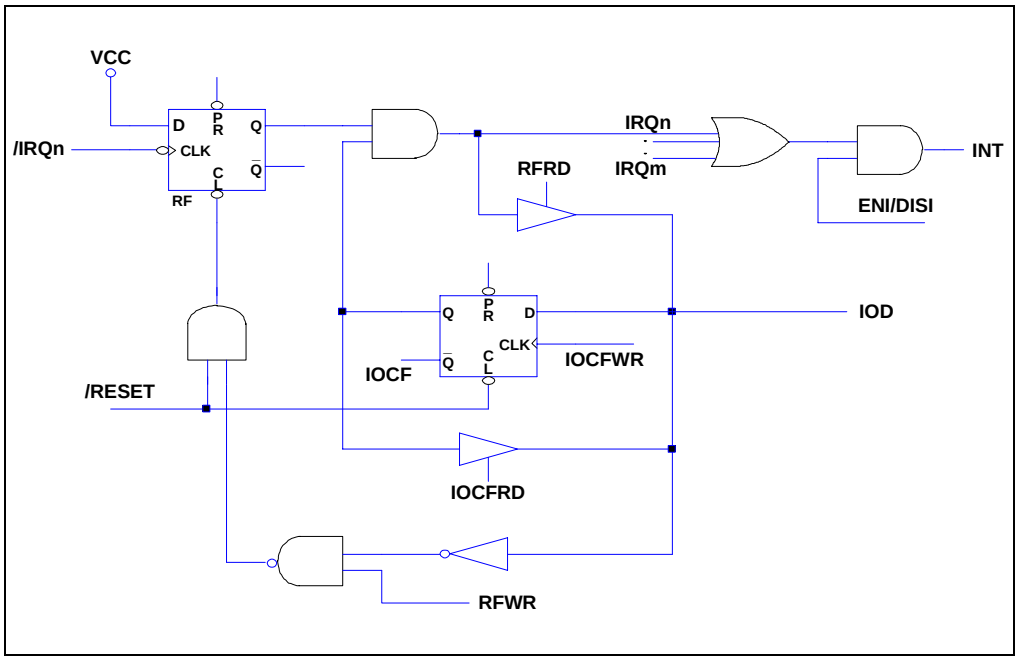


Figure 6-6b Interrupt Input Circuit

6.6 Analog-to-Digital Converter (ADC)

R_Bank	Addr.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bank 0	0x3E	ADCR1	CKR2	CKR1	CKR0	ADRUN	ADP	ADOM	SHS1	SHS0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 0	0x3F	ADCR2	-	-	ADIM	ADCMS	VPIS1	VPIS0	VREFP	-
			-	-	R/W	R/W	R/W	R/W	R/W	-
Bank 0	0x40	ADISR	-	-	-	ADIS4	ADIS3	ADIS2	ADIS1	ADIS0
			-	-	-	R/W	R/W	R/W	R/W	R/W
Bank 0	0x41	ADER1	ADE7	ADE6	ADE5	ADE4	ADE3	ADE2	ADE1	ADE0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 0	0x42	ADER2	-	-	ADE13	ADE12	ADE11	ADE10	ADE9	ADE8
			-	-	R/W	R/W	R/W	R/W	R/W	R/W
Bank 0	0x44	ADDH	ADD15	ADD14	ADD13	ADD12	ADD11	ADD10	ADD9	ADD8
			R	R	R	R	R	R	R	R
Bank 0	0x45	ADDL	ADD7	ADD6	ADD5	ADD4	ADD3	ADD2	ADD1	ADD0
			R	R	R	R	R	R	R	R
Bank 0	0x46	ADCDH	ADCD15	ADCD14	ADCD13	ADCD12	ADCD11	ADCD10	ADCD9	ADCD8
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 0	0x45	ADCDL	ADCD7	ADCD6	ADCD5	ADCD4	ADCD3	ADCD2	ADCD1	ADCD0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 0	0x10	WUCR2	-	-	-	ADWK	-	-	-	-
			-	-	-	R/W	-	-	-	-
Bank 0	0x15	ISR1	-	-	-	ADSF	-	-	-	-
			-	-	-	R/W	-	-	-	-
Bank 0	0x1B	IMR1	-	-	-	ADIE	-	-	-	-
			-	-	-	R/W	-	-	-	-

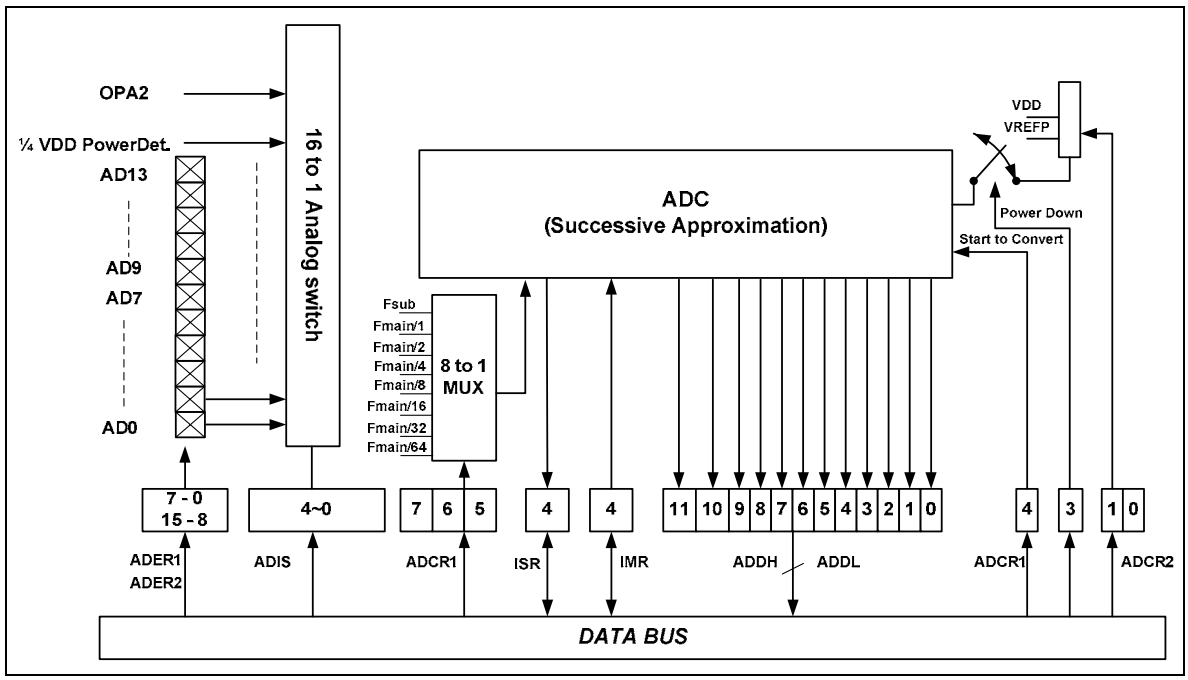


Figure 6-7 AD Converter Functional Block Diagram

This is a 12-bit successive approximation register analog to digital converter (SAR ADC) with two reference voltages. The positive reference voltage can select either internal AVDD internal voltage sources or external input pin by setting the VREFP and VPIS[1:0] bits in ADCR2. Connecting to external positive reference voltage provides more accuracy than using internal AVDD.

6.6.1 ADC Data Register

When the AD conversion is completed, the result is loaded into the ADDH and ADDL. The ADSF is set if ADIE is enabled.

6.6.2 A/D Sampling Time

The accuracy, linearity, and speed of the successive approximation AD converter are dependent on the properties of the ADC. The source impedance and the internal sampling impedance directly affect the time required to charge the sample and hold capacitor. The application program controls the length of the sample time to meet the specified accuracy. The maximum recommended impedance for the analog source is 10 KΩ at VDD=5V. After the analog input channel is selected; this acquisition time must be done before AD conversion can be started.

6.6.3 A/D Conversion Time

CKR [2:0] select the conversion time, in terms of instruction cycles (T_{AD}). This allows the MCU to run at maximum frequency without sacrificing the accuracy of the AD conversion. The following two tables are examples that show the relationship between T_{AD} and the maximum operating frequencies. The T_{AD} is 0.5 µs for 3V~5.5V and T_{AD} is 2 µs for 2.5V~3V.

- Vdd = 3V ~ 5.5V

System Mode	CKR [2:0]	$F_{AD}=1/T_{AD}$	Max. F_{MAIN} (Vdd=3V~5.5V)	Conversion Time (SHS[1~0]=10)
Normal Mode	000	$F_{Main}/16$	-	-
	001	$F_{Main}/8$	16 MHz	10 µs
	010	$F_{Main}/4$	8 MHz	10 µs
	011	$F_{Main}/2$	4 MHz	10 µs
	100	$F_{Main}/64$	-	-
	101	$F_{Main}/32$	-	-
	110	$F_{Main}/1$	2 MHz	10 µs
	111	F_{Sub}	-	-
Green Mode	xxx	F_{Sub}	-	-

- Vdd = 2.5V ~ 3V

System Mode	CKR [2:0]	$F_{AD}=1/T_{AD}$	Max. F_{MAIN} (Vdd=2.5V~3V)	Conversion Time (SHS[1~0]=10)
Normal Mode	000	$F_{Main}/16$	8 MHz	40 µs
	001	$F_{Main}/8$	4 MHz	40 µs
	010	$F_{Main}/4$	2 MHz	40 µs
	011	$F_{Main}/2$	1 MHz	40 µs
	100	$F_{Main}/64$	-	-
	101	$F_{Main}/32$	16 MHz	40 µs
	110	$F_{Main}/1$	0.5 MHz	40 µs
	111	F_{Sub}	-	-
Green Mode	xxx	F_{Sub}	-	-

6.6.4 ADC Operation during Sleep Mode

In order to obtain a more accurate ADC value and reduce power consumption, the AD conversion remains operational during Sleep mode. While the SLEP instruction is being executed, all the MCU operations will stop except for the Oscillator, TCC, TC1, PWMA~C timers, and AD conversion.

The AD Conversion is considered completed as determined by**:**

1) The ADRUN bit of the Bank 0-R3E register is cleared to "**0**".
2) The ADSF bit of the Bank 0-R15 register is set to "**1**".
3) The ADWK bit of the Bank 0-R10 register is set to "**1**". Wakes up from ADC conversion (where it remains in operation during Sleep mode).

4) Wake up and execute the next instruction if the ADIE bit of the Bank 0-R1B is enabled and the “DISI” instruction is executed.

5) Wake up and enter into Interrupt vector if the ADIE bit of the Bank 0-R1B is enabled and the “ENI” instruction is executed.

6) Enter into an Interrupt vector if the ADIE bit of the Bank 0-R1B is enabled and the “ENI” instruction is executed.

The results are fed into the ADDL and ADDH registers when the conversion is completed. If the ADWK is enabled, the device will wake-up. Otherwise, AD conversion is shut off, no matter what the status of the ADPD bit is.

6.6.5 Programming Process/Considerations

Follow these steps to obtain data from the ADC**:**

1) Write to the sixteen bits (ADE [13:0]) on the Bank0-R41~R42 (ADER1~2) register to define the characteristics of P50~P57 and P71~P75 (digital I/O, analog channels, or voltage reference pin)

2) Write to the Bank 0-R3E/ADCON register to configure the AD module**:**
   a) Select the ADC input channel (ADIS[4:0))
   b) Define the AD conversion clock rate (CKR [2:0])
   c) Select the VREFS input source of the ADC
   d) Set the ADPD bit to “**1**” to begin sampling

3) Set the ADWK bit, if the Wake-up function is employed

4) Set the ADIE bit, if the Interrupt function is employed

5) Write “ENI” instruction, if the Interrupt function is employed

6) Set the ADRUN bit to “**1**”

7) Write “SLEP” instruction or Polling

8) Wait for either Wake-up or for the ADRUN bit to be cleared (“**0**” value), whereby Status flag (ADSF) is set to “**1**,” or ADC interrupt occurs.

9) Read the ADDL and ADDH conversion data registers. If the ADC input channel changes at this time, the ADDL and ADDH values can be cleared to “**0**.”

10) Clear the status flag (ADSF)

11) For the next conversion, go to Step 1 or Step 2 as required. At least two T_{AD} are required before the next acquisition starts. On the other hand, the timing setting ADRUN = 1 must be later than the timing setting ADPD=1, and the difference between the two timing is also two T_{AD}.

NOTE

In order to obtain accurate values, it is necessary to avoid any data transition on the I/O pins during AD conversion

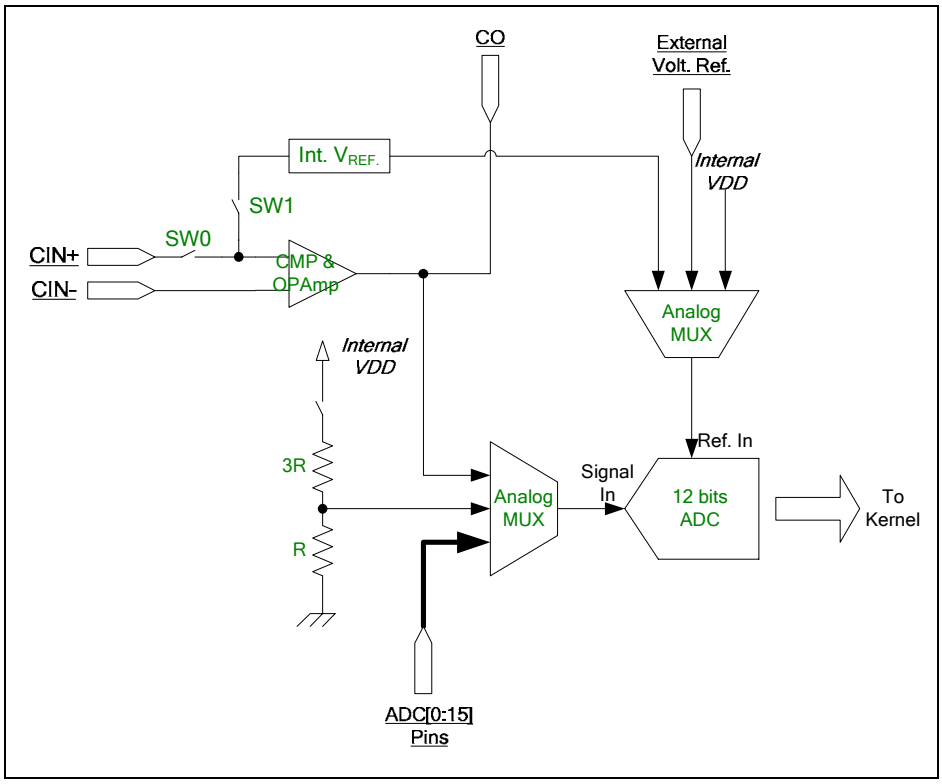


Figure 6-8 ADC, CMP OPAmp, and VDD Detection Block Diagram.

6.7 Timer

There is one timer in the real chip. Timer 1 is an 8-bit up-counter.

R_BANK	Addr.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bank 0	0x24	TC1CR1	TC1S	TC1RC	TC1SS1	-	TC1FF	TC1OMS	TC1IS1	TC1IS0
			R/W	R/W	R/W	-	R	R/W	R/W	R/W
Bank 0	0x25	TC1CR2	TC1M2	TC1M1	TC1M0	TC1SS0	TC1CK3	TC1CK2	TC1CK1	TC1CK0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 0	0x26	TC1DA	TC1DA7	TC1DA6	TC1DA5	TC1DA4	TC1DA3	TC1DA2	TC1DA1	TC1DA0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 0	0x27	TC1DB	TC1DB7	TC1DB6	TC1DB5	TC1DB4	TC1DB3	TC1DB2	TC1DB1	TC1DB0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 0	0x16	ISR2	-	-	-	-	-	-	-	TC1DIF
			-	-	-	-	-	-	-	F
Bank 0	0x1C	IMR2	-	-	-	-	-	-	-	TC1DIE
			-	-	-	-	-	-	-	R/W

6.7.1 Timer/Counter Mode

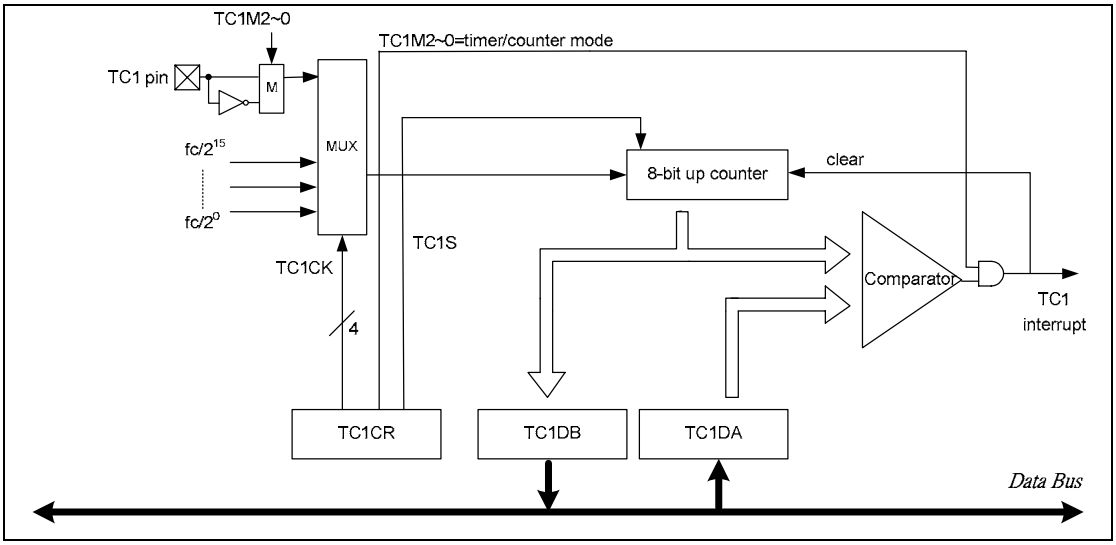


Figure 6-9a Timer/Counter Mode Block Diagram

In the Timer/Counter mode, counting-up is performed by using internal clock or TC3 pin. When the contents of up-counter match the TC1DA, the interrupt is then generated and the counter is cleared. Counting-up resumes after the counter is cleared. The current contents of up-counter are loaded into TC1DB by setting TC1RC to "**1**".

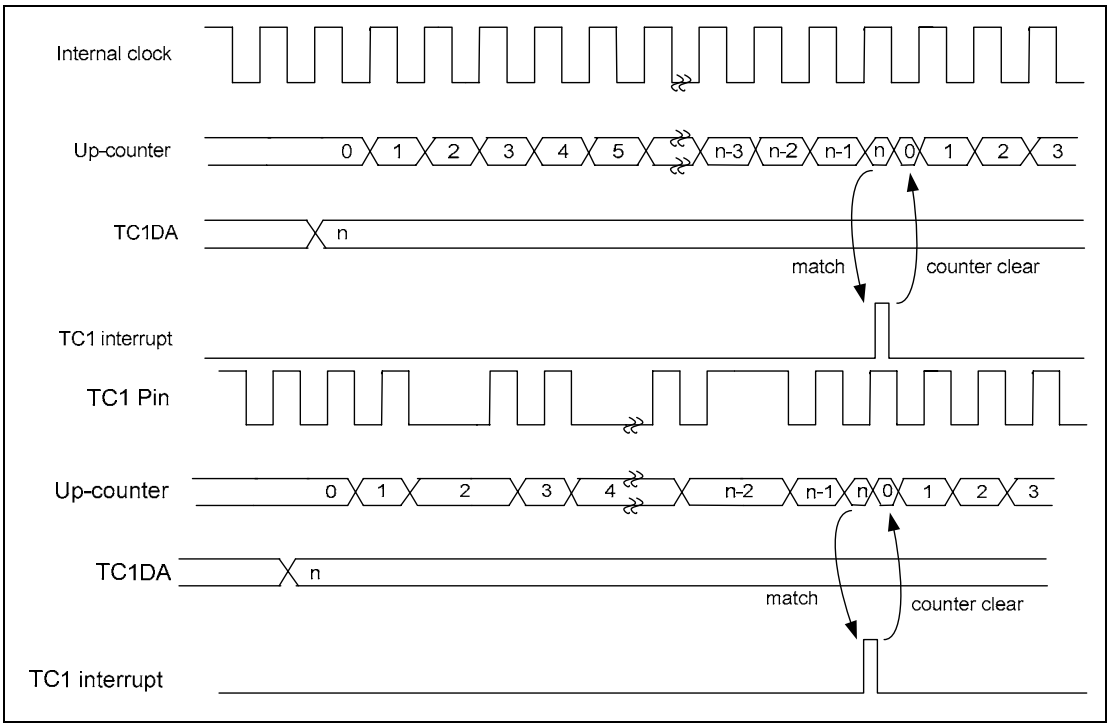


Figure 6-9b Timer/Counter Mode Waveform

6.7.2 Window Mode

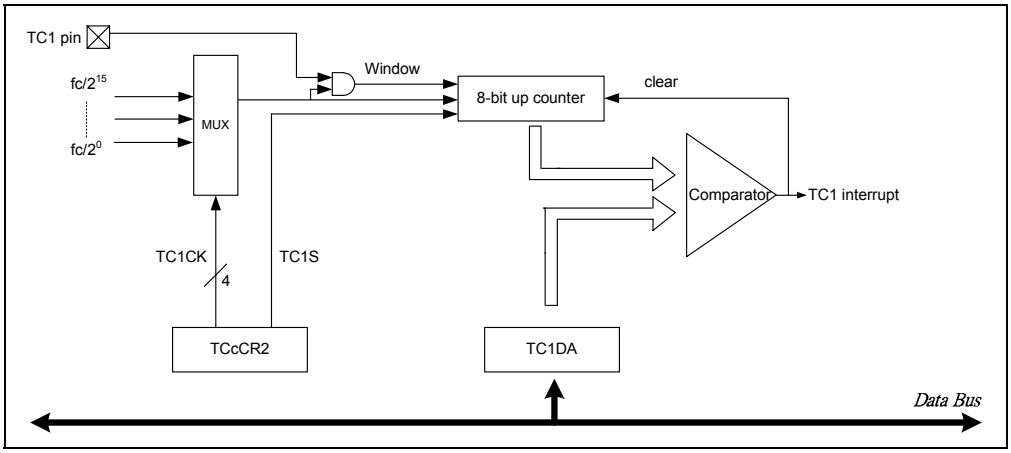


Figure 6-10a Window Mode Block Diagram

In Window mode, counting-up is performed on rising edge of the pulse that is Logical AND of an internal clock and the TC1 pin (Window pulse). When the contents of up-counter match the TC1DA, interrupt is generated and the counter is cleared. The frequency (Window pulse) must be slower than the selected internal clock.

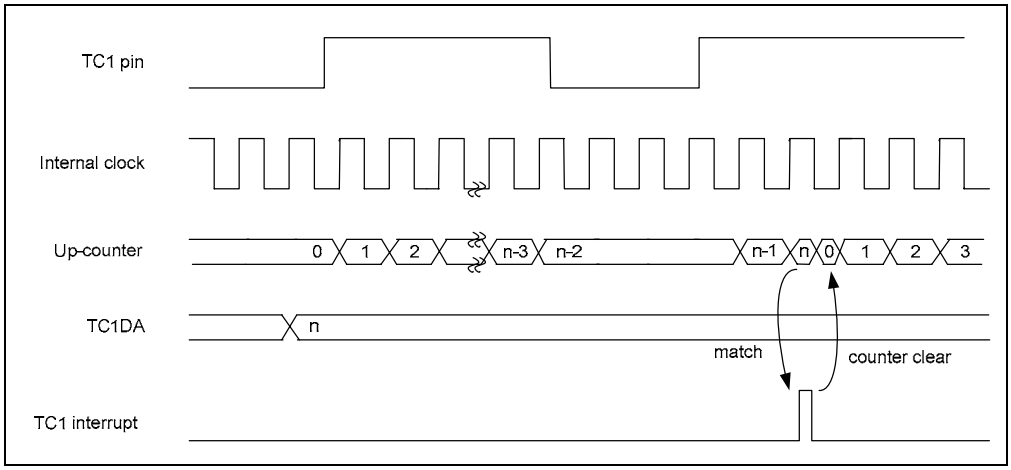


Figure 6-10b Window Mode Waveform

6.7.3 Capture Mode

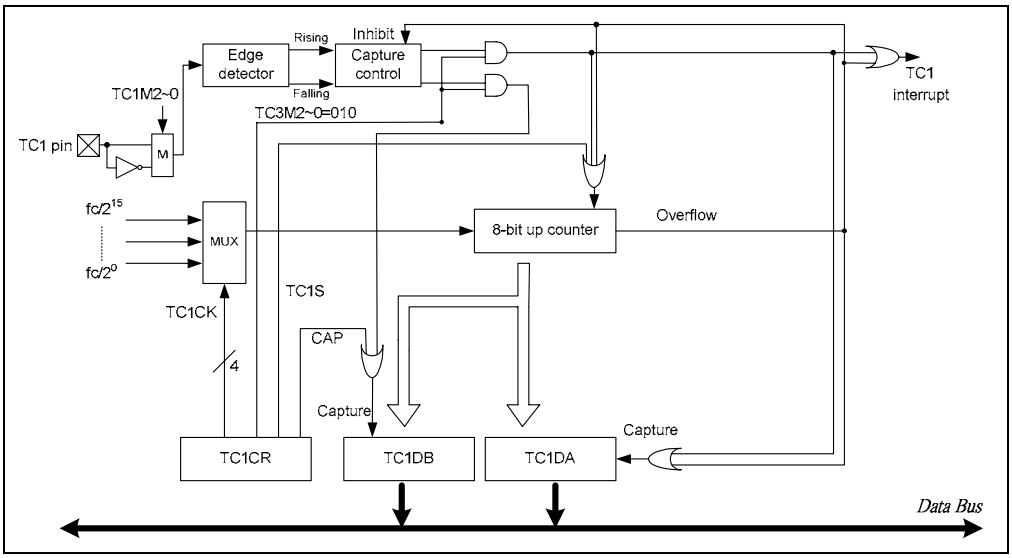


Figure 6-11a Capture Mode Block Diagram

In Capture mode, the pulse width, period, and duty of the TC1 input pin are measured in this mode, and can be used to decode the remote control signal. The counter is free running by the internal clock. On the rising (falling) edge of TC1 pin, the contents of counter is loaded into TC1DA, then the counter is cleared and interrupt is generated. On the falling (rising) edge of TC13 pin, the contents of counter are loaded into TC1DB, while the counter is still counting. Once the next rising edge of TC1 pin triggers, the contents of counter are loaded into TC1DA, the counter is cleared, and interrupt is generated again. If overflow before the edge is detected, the FFH is loaded into TC1DA and overflow interrupt is generated. During interrupt processing, it can be determined whether or not there is an overflow by checking whether or not the TC1DA value is FFH. After an interrupt (capture to TC1DA or overflow detection) is generated, capture and overflow detection are halted until TC1DA is read out.

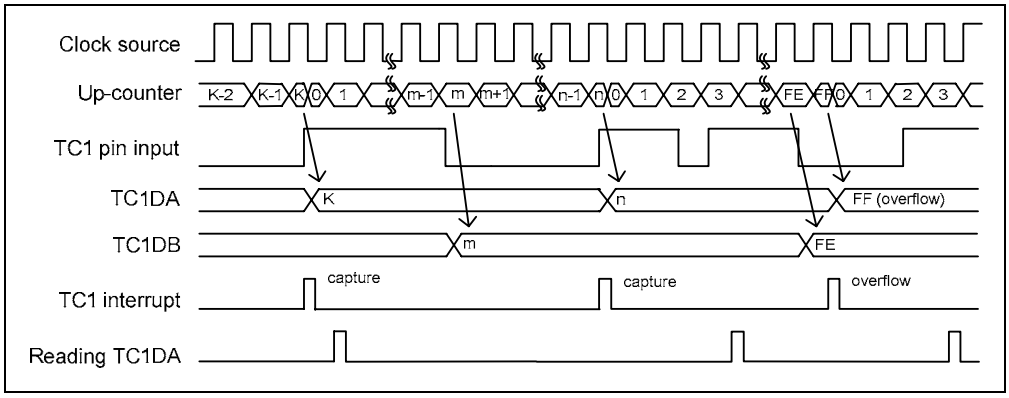


Figure 6-11b Capture Mode Waveform

6.7.4 Programmable Divider Output (PDO) Mode and Pulse Width Modulation (PWM) Mode

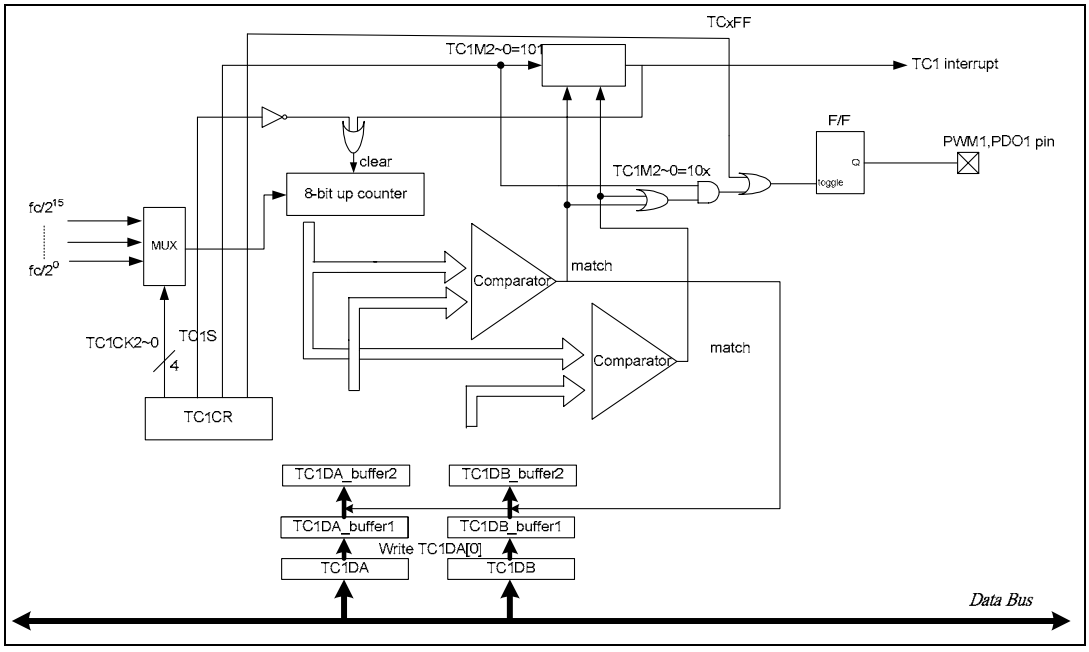


Figure 6-12a PDO / PWM Mode Block Diagram

■ Programmable Divider Output (PDO)

In Programmable Divider Output (PDO) mode, counting-up is performed using internal clock. The contents of TC1DA are compared with the contents of the up-counter. The F/F output is toggled and the counter is cleared each time a match is found. The F/F output is inverted and output to PDO pin. This mode can generate 50% duty pulse output. The PDO pin is initialized to "**0**" during reset. A TC1 interrupt is generated each time the PDO output is toggled.

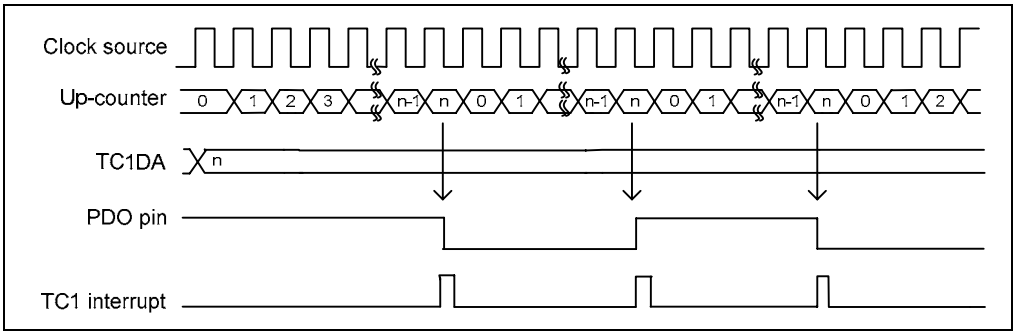


Figure 6-12b PDO Mode Waveform

■ **Pulse Width Modulation (PWM)**

In Pulse Width Modulation (PWM) Output mode, counting up is performed using the internal clock with prescaler. The Duty of PWM1 is controlled by TC1DB, and the period of PWM1 is controlled by TC1DA. The pulse at the PWM1 pin is held to high level as long as TC1S=1 or TIMERX matches TC1DA, while the pulse is held to low level as long as Timer x matches TC1DB. Once TC1FF is set to "**1**", the PWM3 signal is inverted. A TC1 interrupt is generated and defined by TC1IS. On the other hand, the TC1DA and TC1DB can be written anytime, but the data of TC13DA and TC1DB are latched only at writing TC1DA [0]. Therefore, the new duty and new period of PWM appear at the PMW pin at the last period–match.

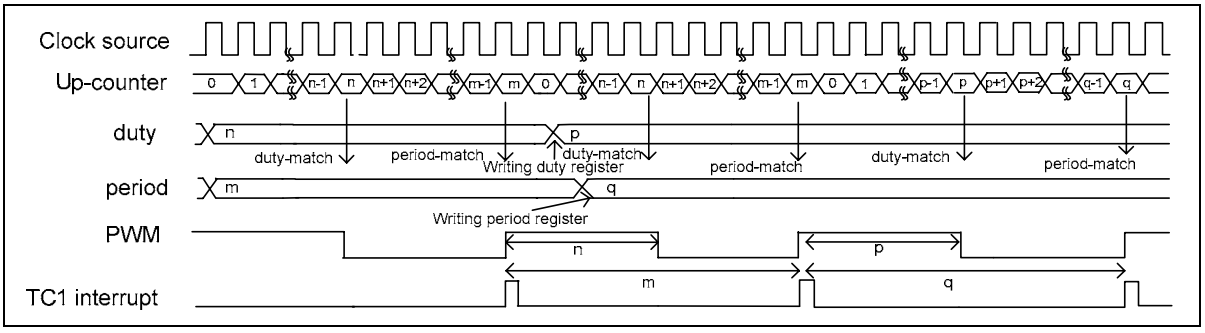


Figure 6-12c PWM mode waveform

6.7.5 Buzzer Mode

The TC1 pin outputs the clock after dividing the frequency.

6.8 PWM Module

6.8.1 Overview

In PWM mode, PWMX and /PWMX produce up to 16-bit resolution PWM output (see the functional block diagram below). A PWM output consists of a time period and a duty cycle, and it keeps the output high. The PWM baud rate is the inverse of the time period. Figure 6-13b (*PWM Output Timing*) depicts the relationships between a time period and a duty cycle.

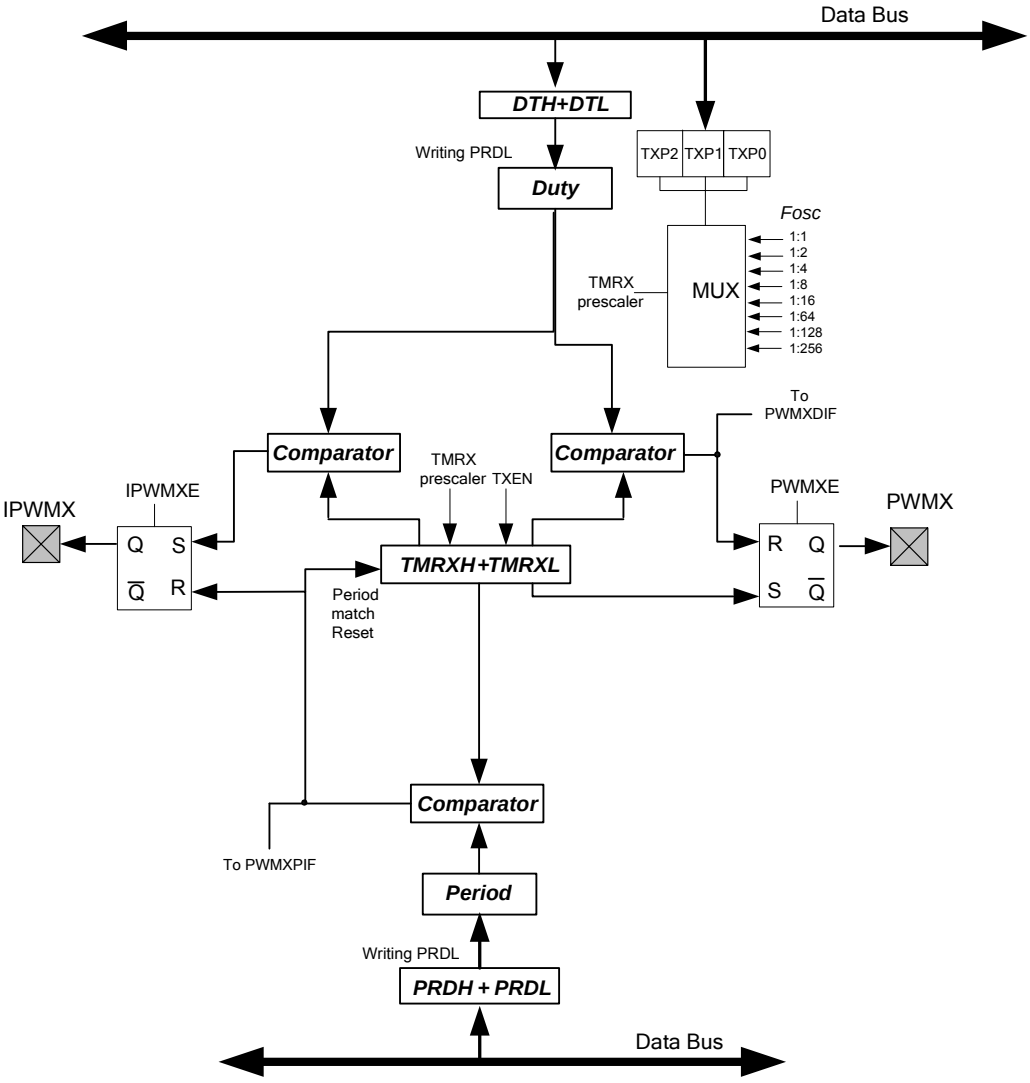


Figure 6-13a PWM Functional Block Diagram

PWM and /PWM (inverted PWM) can be used individually or used as dual PWM. When used individually, the definitions of active level between PWM and /PWM are somewhat different.

For example, setting the period and duty cycle (period > duty) as PWMXE=1/0 and IPWMXE=0/1, and finally setting TXEN = 1. The following figure shows the PWM output timing.

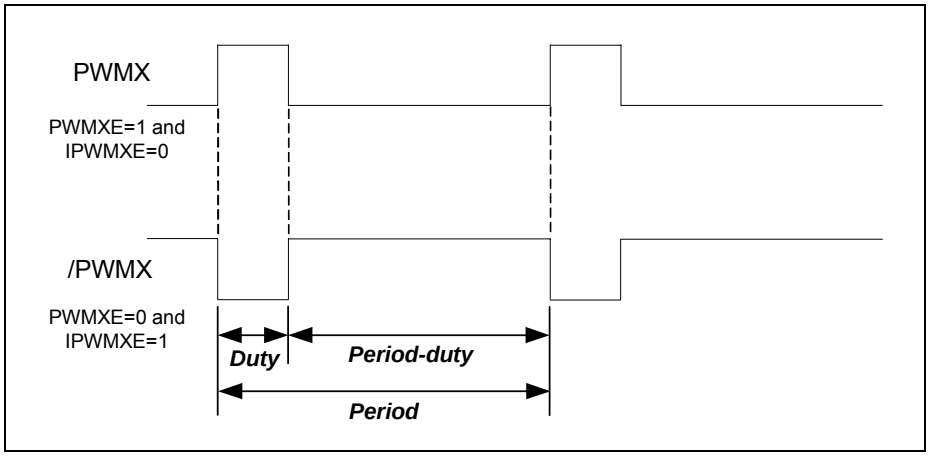


Figure 6-13b PWM Output Timing (PWMXA=0 and /PWMXA=0)

6.8.2 Control Register

R_Bank	Addr.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bank 0	0x17	ISR3	-	-	PWMCPSF	PWMCDSF	PWMBPSF	PWMBDSF	PWMAPSF	PWMADSF
			-	-	F	F	F	F	F	F
Bank 0	0x1D	IMR3	-	-	PWMCPIE	PWMCDIE	PWMBPIE	PWMBDIE	PWMAPIE	PWMADIE
			-	-	R/W	R/W	R/W	R/W	R/W	R/W
Bank 1	0x17	PWMACR	PWMAE	IPWMAE	-	-	TAEN	TAP2	TAP1	TAP0
			R/W	R/W	-	-	R/W	R/W	R/W	R/W
Bank 1	0x18	PRDAL	PRDA7	PRDA6	PRDA5	PRDA4	PRDA3	PRDA2	PRDA1	PRDA0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 1	0x19	PRDAH	PRDA15	PRDA14	PRDA13	PRDA12	PRDA11	PRDA10	PRDA9	PRDA8
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 1	0x1A	DTAL	DTA7	DTA6	DTA5	DTA4	DTA3	DTA2	DTA1	DTA0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 1	0x1B	DTAH	DTA15	DTA14	DTA13	DTA12	DTA11	DTA10	DTA9	DTA8
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 1	0x1C	TMRAL	TMRA7	TMRA6	TMRA5	TMRA4	TMRA3	TMRA2	TMRA1	TMRA0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 1	0x1D	TMRAH	TMRA15	TMRA14	TMRA13	TMRA12	TMRA11	TMRA10	TMRA9	TMRA8
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 1	0x1E	PWMBCR	PWMBE	IPWMBE	-	-	TBEN	TBP2	TBP1	TBP0
			R/W	R/W	-	-	R/W	R/W	R/W	R/W
Bank 1	0x1F	PRDBL	PRDB7	PRDB6	PRDB5	PRDB4	PRDB3	PRDB2	PRDB1	PRDB0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

(Continuation)

R_Bank	Addr.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bank 1	0x20	PRDBH	PRDB15	PRDB14	PRDB13	PRDB12	PRDB11	PRDB10	PRDB9	PRDB8
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 1	0x21	DTBL	DTB7	DTB6	DTB5	DTB4	DTB3	DTB2	DTB1	DTB0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 1	0x22	DTBH	DTB15	DTB14	DTB13	DTB12	DTB11	DTB10	DTB9	DTB8
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 1	0x23	TMRBL	TMRB7	TMRB6	TMRB5	TMRB4	TMRB3	TMRB2	TMRB1	TMRB0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 1	0x24	TMRBH	TMRB15	TMRB14	TMRB13	TMRB12	TMRB11	TMRB10	TMRB9	TMRB8
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 1	0x25	PWMCCR	PWMCE	IPWMCE	-	-	TCEN	TCP2	TCP1	TCP0
			R/W	R/W	-	-	R/W	R/W	R/W	R/W
Bank 1	0x26	PRDCL	PRDC7	PRDC6	PRDC5	PRDC4	PRDC3	PRDC2	PRDC1	PRDC0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 1	0x27	PRDCH	PRDC15	PRDC14	PRDC13	PRDC12	PRDC11	PRDC10	PRDC9	PRDC8
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 1	0x28	DTCL	DTC7	DTC6	DTC5	DTC4	DTC3	DTC2	DTC1	DTC0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 1	0x29	DTCH	DTC15	DTC14	DTC13	DTC12	DTC11	DTC10	DTC9	DTC8
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 1	0x2A	TMRCL	TMRC7	TMRC6	TMRC5	TMRC4	TMRC3	TMRC2	TMRC1	TMRC0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 1	0x2B	TMRCH	TMRC15	TMRC14	TMRC13	TMRC12	TMRC11	TMRC10	TMRC9	TMRC8
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

6.8.3 Increment Timer Counter (TMRX: TMRAH/TMRAL, TMRBH/TMRBL, TMRCH/TMRCL, or TMRDH/TMRDL)

TMRX are 16-bit clock counters with programmable prescalers. They are designed for the PWM module as baud rate clock generators. TMR can be read only. If employed, they can be turned off for power saving by setting the TAEN bit [BANK1-R1A <3>], TBEN bit [BANK1-R21<3>], TCEN bit [BANK1-R28<3>], or TDEN bit [BANK1-R2F <3>] to "**0**."

TMRA, TMRB, TMRC, and TMRD are internal designs and cannot be read.

6.8.4 PWM Time Period (PRDX: PRDAL/H, PRDBL/H, PRDCL/H, or PRDDL/H)

The PWM time period is 16-bit resolution and is defined by writing to the PRDX register. When TMRX is equal to PRDX, the following events occur on the next increment cycle**:**

- TMRX is cleared.
- The PWMX pin is set to "**1**"
- The PWMXIF pin is set to "**1**"

NOTE

*The PWM output cannot be set if the duty cycle is "**0**".*

The following formula describes how to calculate the PWM time period**:**

$$Period = (PRDX + 1) \times \left(\frac{1}{F_{OSC}}\right) \times \frac{CLKS}{2} \times (TMRX \ \ prescale\ value)$$

Example: PRDX = 49; Fosc = 4 MHz; TMRX (0, 0, 0) = 1 **:** 1,
CLKS bit of the Code Option Register = 0 (two oscillator periods);
Then-

$$Period = (49 + 1) \times \left(\frac{1}{4M}\right) \times \frac{2}{2} \times 1 = 12.5\mu s$$

6.8.5 PWM Duty Cycle (DTX: DTAH/DTAL, DTBH/DTBL, DTCH/DTCL, or DTDH/DTDL)

The PWM duty cycle is defined by writing to the DTX register, and is latched from DTX to DLX while TMRX is cleared. When DLX is equal to TMRX, the PWMX pin is cleared. DTX can be loaded anytime. However, it cannot be latched into DLX until the current value of DLX is equal to TMRX.

The following formula describes how to calculate the PWM duty cycle**:**

$$Duty\ cycle = (DTX) \times \left(\frac{1}{F_{OSC}}\right) \times \frac{CLKS}{2} \times (TMRX \ \ prescale\ value)$$

Example: DTX = 10; Fosc = 4 MHz; TMRX (0, 0, 0) = 1 : 1,
CLKS bit of the Code Option Register = 0 (two oscillator periods);
Then-

$$Duty\ cycle = (10) \times \left(\frac{1}{4M}\right) \times \frac{2}{2} \times 1 = 2.5\mu s$$

6.8.6 Comparator X

Changing the output status while matching occurs will simultaneously set the TMRXIF flag.

6.8.7 PWM Programming Process/Steps

1) Load the PWM duty cycle to DT

2) Load the PWM time period to PRD

3) Load the PWM dead time cycle (only for dual PWM function)

4) Enable the interrupt function by writing Bank 0-R1D, if required.

5) Load a desired value for the timer prescaler

6) Set active level of duty of PWM

7) Enable PWMX function, i.e., enable PWMXE control bit (if using dual PWM function enable also the PWMXE control bit)

8) Finally enable the TMRX function, i.e., enable TXEN control bit.

If the application needs to change the PWM duty, period and dead time cycle at run time, refer to the following programming steps**:**

1) Load the new duty and dead time cycle (if using dual PWM function) at any time.

2) Load the new period cycle. You must take note of the order of loading the period cycle. As the low byte of PWM period cycle is assigned a value, the new PWM cycle is loaded into the circuit. The circuit will automatically update the new duty, period, and dead time cycle to generate the new PWM waveform at the next PWM cycle.

6.9 Comparator

The MCU has four comparators comprising of two analog inputs and one output. All of the comparators can be set as OP. The comparator can be utilized to wake up the MCU from Sleep mode. The comparator circuit diagram is depicted in the following figure.

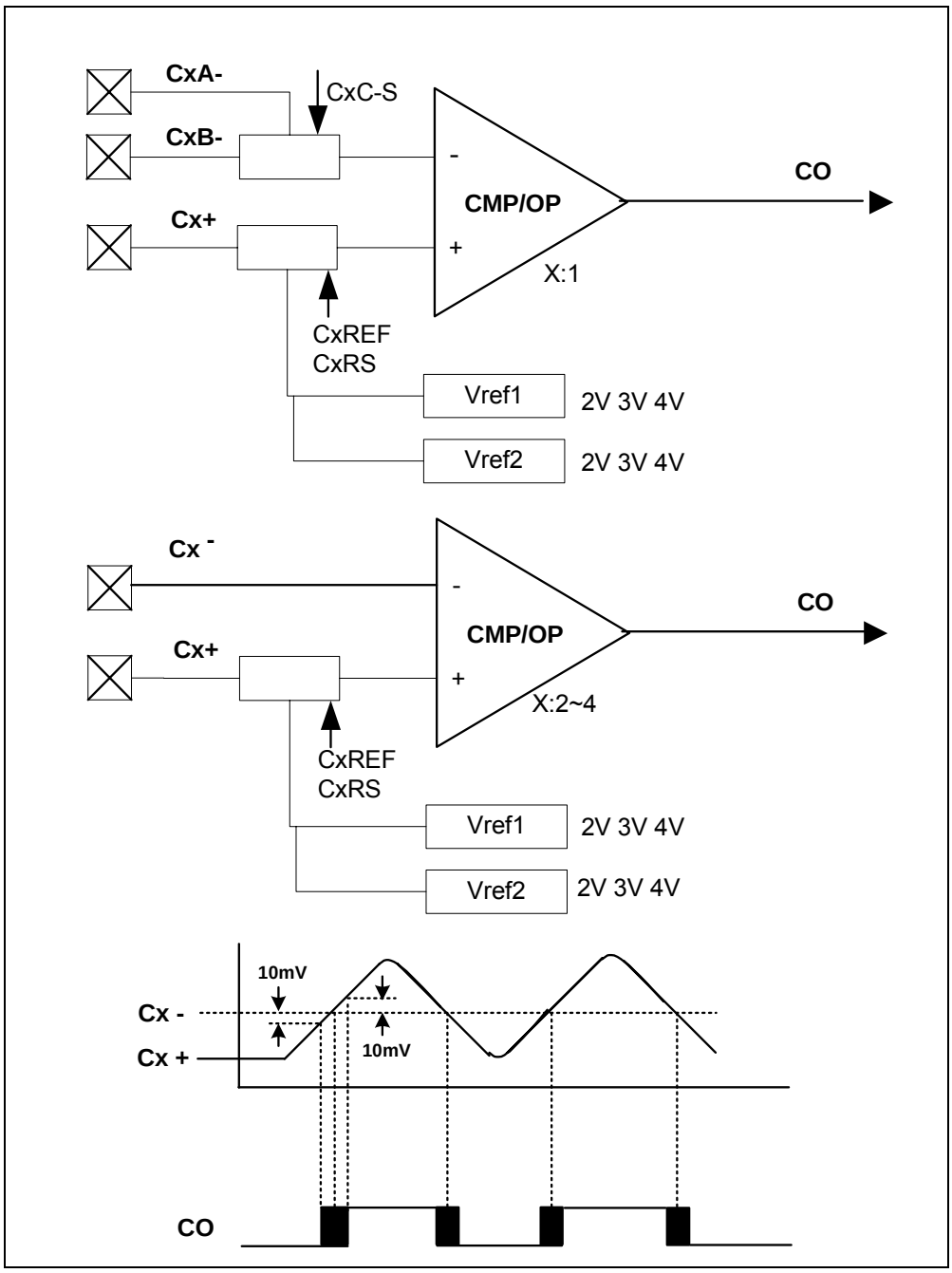


Figure 6-14b Comparator Circuit and Operating Mode

6.9.1 External Reference Signal

The analog signal presented at Cin– is compared to the signal at Cin+, and the digital output (CO) of the comparator has to be adjusted accordingly by taking the following notes into considerations:

NOTE

- *The reference signal must be between Vss and Vdd.*
- *The non-inverting end of Comparator 2 can be connected to the internal reference and the corresponding pin can be set as comparator I/O or general I/O.*
- *The non-inverting end of Comparator 2 can be connected to Vref1.*
- *There are three reference voltage levels for Vref1, i.e., 2V, 3V, and 4V.*
- *The falling edge of CO2 can turn-off the PWMx only or both PWMx and /PWMx, when the PWMxA and IPWMxA are in turned-on state.*
  Example: (falling edge of CO1 → PWMA, or both PWMA and /PWMA)

6.9.2 Comparator Outputs

- The compared result is stored in the CMPOUT2.
- The function of Pin CO2 is defined by programming the Register <C2S [1:0]>.

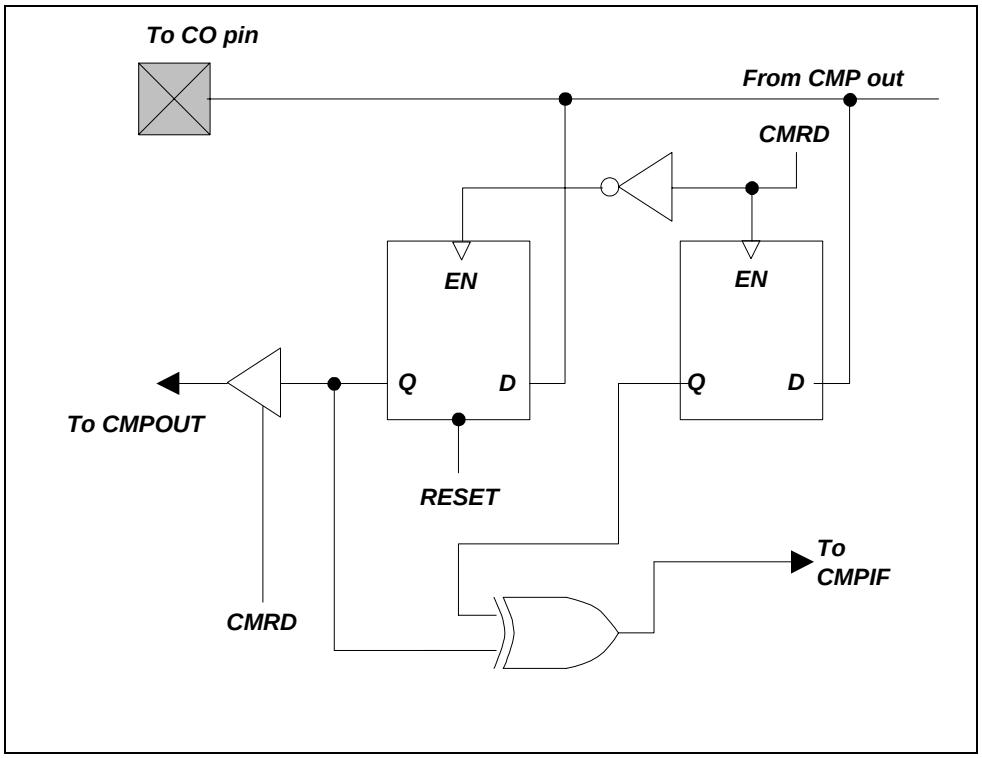


Figure 6-15 Comparator Output Configuration

6.9.3 Programming the Related Registers

R_Bank	Addr.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bank 0	0x10	WUCR2	CMP2WK	-	-	-	-	-	-	-
			R/W	-	-	-	-	-	-	-
Bank 0	0x15	SFR1	CMP2SF	-	-	-	-	-	-	-
			R/W	-	-	-	-	-	-	-
Bank 0	0x1B	IMR1	CMP2IE	-	-	-	-	-	-	-
			R/W	-	-	-	-	-	-	-
Bank 0	0x3B	CMP2CR	C2RS	CP2OUT	C2S1	C2S0	-	-	-	SDPWMB
			R/W	R/W	R/W	R/W	-	-	-	R/W

6.9.4 Comparator Interrupt

- CMP2IE must be enabled for the “ENI” instruction to take effect.
- Interrupt is triggered whenever a change occurs on the comparator output pin.
- The actual change on the pin can be determined by reading the Bit CP2OUT.
- The comparator interrupt flag CMP2IF, can only be cleared by software.

6.9.5 Wake-up from Sleep Mode

- The comparator and the interrupt remain active in Sleep mode when CMP2IE=1 and CMPWK=1.
- If a comparator output changes state, the interrupt will wake up the device from Sleep mode.
- The power consumption should be taken into consideration for the benefit of energy conservation.
- If the function is unemployed during Sleep mode, turn off the comparator before entering into sleep mode.

6.10 I²C Function

R_Bank	Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bank 0	0x30	I2CCR1	Strobe/Pend	IMS	ISS	STOP	SAR_EMPTY	ACK	FULL	EMPTY
			R/W	R/W	R/W	R	R	R	R	R
Bank 0	0x31	I2CCR2	I2CBF	GCEN		BBF	I2CTS1	I2CTS0	I2CCS	I2CEN
			R	R/W		R	R/W	R/W	R/W	R/W
Bank 0	0x32	I2CSA	SA6	SA5	SA4	SA3	SA2	SA1	SA0	IRW
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 0	0x33	I2CDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 0	0x34	I2CDAL	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 0	0x35	I2CDAH	-	-	-	-	-	-	DA9	DA8
			-	-	-	-	-	-	R/W	R/W
Bank 0	0x18	SFR4	-	-	-	-	-	I2CSTPIF	I2CRSF	I2CTSF
			-	-	-	-	-	R/W	R/W	R/W
Bank 0	0x1E	IMR4						I2CSTPIE	I2CRIE	I2CTIE
								R/W	R/W	R/W

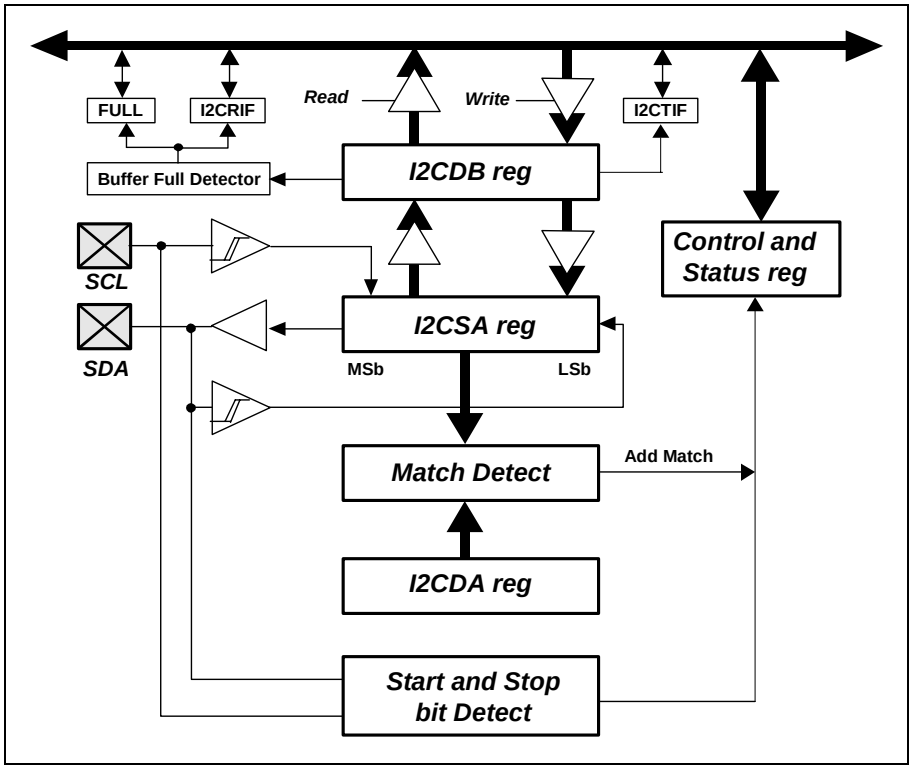


Figure 6-16a 1^{2}C Block Diagram

The EM78P374N supports a bidirectional, 2-wire bus, 7/10-bit addressing and data transmission protocol. A device that sends data onto the bus is defined as Transmitter, while a device receiving data is defined as a Receiver. The bus has to be controlled by a master device which generates the Serial Clock (SCL), controls the bus access, and generates the Start and Stop conditions. Both Master and Slave can operate as Transmitter or Receiver, but the Master device determines which mode is activated.

Both Serial Data (SDA) and SCL are bi-directional lines, connected to a positive supply voltage via a pull-up resistor. When the bus is free, both lines are high. The output stage of devices connected to the bus must have an open-drain or open-collector to perform the wired-AND function. Data on the I^{2}C-bus can be transferred at the rates of up to 100kbit/s in Standard-mode or up to 400kbit/s in Fast-mode.

The data on the SDA line must be stable during HIGH period of the clock. The High or Low state of the data line can only change when the clock signal on the SCL line is Low.

The I^{2}C interrupt occurs as describe below**:**

Condition	Master/Slave	Transmit Address	Transmit Data	Stop
Master Transmitter (transmits to Slave-Receiver)	Master	Transmit interrupt	Transmit interrupt	Stop interrupt
	Slave	Receive interrupt	Receive interrupt	Stop interrupt
Master Receiver (read Slave-Transmitter)	Master	Transmit interrupt	Receive interrupt	Stop interrupt
	Slave	Transmit interrupt	Transmit interrupt	Stop interrupt

Within the procedure of the I^2C bus, unique situations could arise which are defined as START (S) and STOP (P) conditions.

A High to Low transition on the SDA line while SCL is High is one such unique case. This condition indicates a START condition.

A Low to High transition on the SDA line while SCL is High defines a STOP condition.

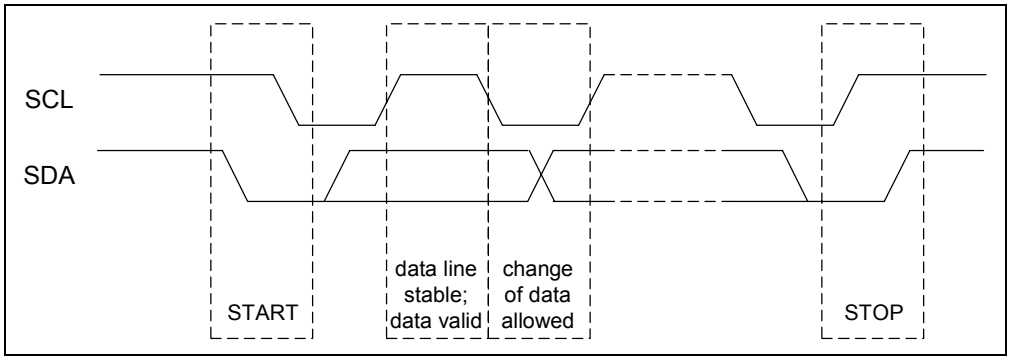


Figure 6-16b I2C Transfer Condition

6.10.1 7-Bit Slave Address

The Master-transmitter transmits to the Slave-receiver. The transfer direction is not changed.

The Master reads the Slave immediately after the first byte. At the moment of the first acknowledgement, the Master-transmitter becomes a Master-receiver and the Slave-Receiver becomes a Slave-transmitter. This first acknowledgement is still generated by the Slave. The STOP condition is generated by the Master, which has previously sent a Not-Acknowledge (A). The difference between Master-transmitter and Master-receiver is only in the R//W bit. If the R//W bit is "**0**," the Master device is the Transmitter. Otherwise; the Master device is the Receiver (R//W bit is "**1**"). The Master-Transmitter is illustrated in the following Figure 6-17a, and that of Master-Receiver is shown in Figure 6-17b.

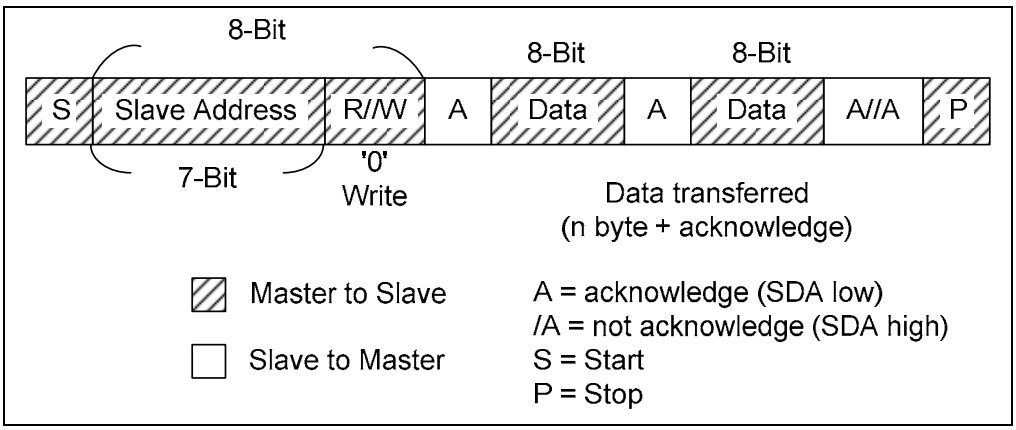


Figure 6-17a Master-Transmitter transmits to Slave-Receiver with 7-Bit Slave Address

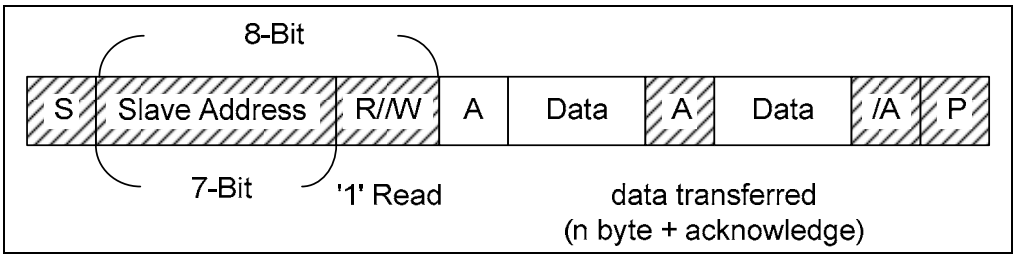


Figure 6-17b Master-Receiver reads from Slave-Transmitter with 7-Bit Slave Address

6.10.2 10-Bit Slave Address

In 10-Bit slave address mode, using 10 Bits for addressing exploits the reserved combination 11110XX for the first 7 bits of the first byte following a START(S) or repeated START (Sr) condition. The first 7 bits of the first byte are the combination 11110XX of which the last two bits (XX) are the two most-significant bits of the 10-bit address. If the R//W bit is "**0**", the second byte after acknowledgement would be the eight address bits of the 10-bit Slave address. Otherwise; the second byte would just be the next transmitted data from a Slave to Master device. The first bytes 11110XX are transmitted using the Slave address register (I2CSA), and the second bytes XXXXXXXX are transmitted using the data buffer (I2CDB).

The following will explain the possible data transfer formats for 10-bit Slave address mode**:**

■ **Master-Transmitter Transmits to Slave-Receiver with a 10-bit Slave Address**

When the Slave receives the first byte after START bit from Master, each Slave device will compare the 7 bits of the first byte (11110XX) with their own address and the 8th bit (R//W). If the R//W bit is "**0**" the Slave will return the Acknowledge (A1). It is possible that more than one Slave devices will return the Acknowledge (A1). Then all Slave devices will continue to compare the second address (XXXXXXXX). If a Slave device finds a match, that particular Slave device will be the only one to return an Acknowledge (A2).

The matched Slave device will remain addressed by the Master until it receives the STOP condition or a repeated START condition followed by a different Slave address.

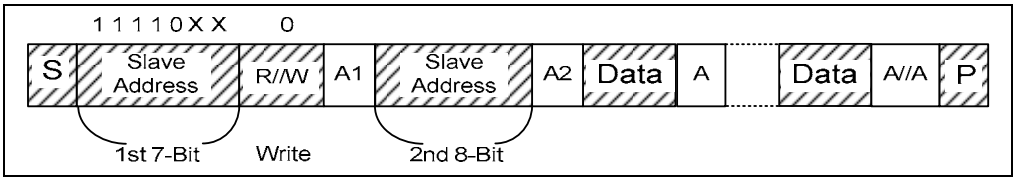


Figure 6-18b Master-Transmitter transmits to Slave-Receiver with a 10-Bit Slave Address

■ Master-Receiver Reads Slave-Transmitter with a 10-bit Slave Address

Up to, and including Acknowledge Bit A2, the procedure is the same as that described above for Master-Transmitter addressing a Slave-Receiver. After the Acknowledge A2, a repeated START condition (Sr) condition takes place, followed by seven bits Slave address (11110XX), but the 8th bit R//W is "**1**." The addressed Slave device will then return the Acknowledge A3. If the repeated START (Sr) condition occurs and the seven bits of first byte (11110XX) are received by Slave device, all the Slave devices will compare with their own address and test the 8th R//W. However, none of the Slave devices can return an acknowledgement because R//W=1.

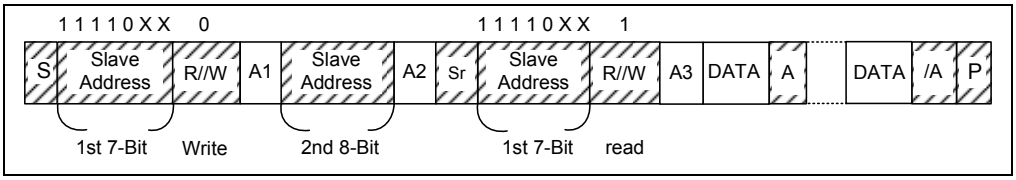


Figure 6-18b Master-Receiver reads Slave-Transmitter with a 10-Bit Slave Address

■ Master Transmits and Receives Data to and from the Same Slave Device with 10-Bit Addresses

The initial operation of this data transfer format is the same as explained in the above paragraph on "*Master-Transmitter transmits to Slave-Receiver with a 10-bit Slave Address.*" Then the Master device starts to transmit the data to the Slave device. When the Slave device receives the Acknowledge or None-Acknowledge that is followed by repeat START (Sr), the above operation under "*Master-Receiver reads Slave- Transmitter with a 10-Bit Slave Address*" is repeatedly performed.

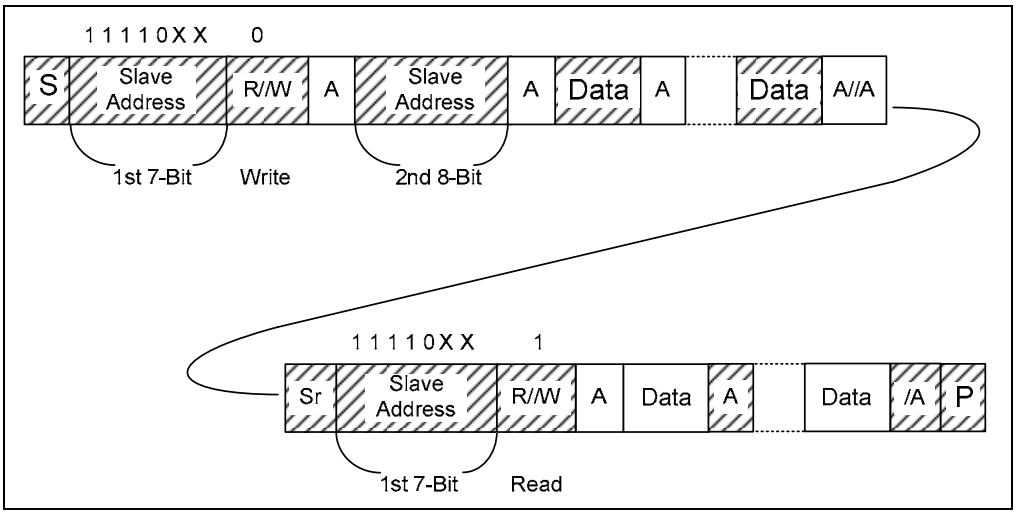


Figure 6-18c Master Addresses a Slave with 10-Bit Address transmits and receives Data with the Same Slave Device

■ Master Device Transmits Data to Two or More Slave Devices with 10 and 7 Bits Slave Address

For 10-bit address, the initial operation of this data transfer format is the same as explained in the above paragraph on "*Master-Transmitter Transmits to Slave-Receiver with a 10-bit Slave Address,*" which describes how to transmit data to Slave device. After the Master device completes the initial transmittal, and wants to continue transmitting data to another device, the Master needs to address each of the new Slave devices by repeating the initial operation mentioned above. If the Master device wants to transmit the data in 7-bit and 10-bit Slave address modes successively, this could be done after the START or repeat START conditions as illustrated in the following figures.

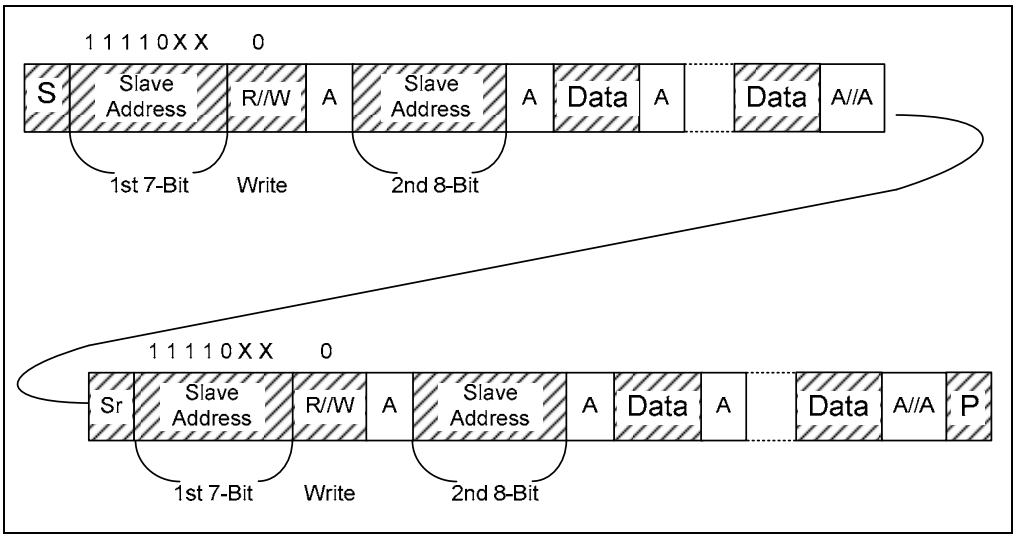


Figure 6-18d Master transmitting to more than One Slave Devices with 10-Bit Slave Address

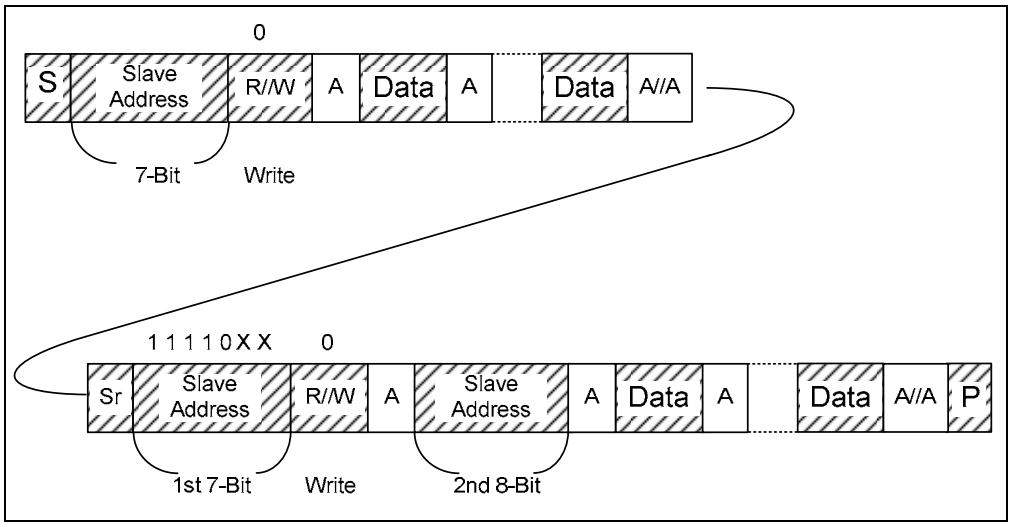


Figure 6-18e Master successively transmitting to 7-Bit and 10-Bit Slave Address

6.10.3 Master Mode 1^2C Transmit

In transmitting (receiving) serial data, the I^2C is carried on as follows**:**

1) Set I2CTS1~0, I2CCS, and ISS bits to select I^2C transmit clock source.

2) Set I2CEN and IMS bits to enable the I^2C Master function.

3) Write Slave address into the I2CSA register and IRW bit to select read or write.

4) Set strobe bit to start transmitting and then check I2CTSF (I2CTSF) bit.

5) Write 1^{st} data into the I2CDB register, set strobe bit, and check I2CTSF (I2CRSF) bit.

6) Write 2^{nd} data into the I2CDB register, set strobe bit, STOP bit, and check I2CTSF (I2CRSF) bit.

6.10.4 Slave Mode 1^2C Transmit

In receiving (transmitting) serial data, the I^2C is carried on as follows**:**

1) Set I2CTS1~0, I2CCS, and ISS bits to select I^2C transmit clock source.

2) Set I2CEN and IMS bits to enable I^2C Slave function.

3) Write device address into the I2CDA register.

4) Check I2CRSF (I2CTSF) bit, read I2CDB register (address), and then clear Pend bit.

5) Check I2CRSF (I2CTSF) bit, read I2CDB register (1st data), and then clear Pend bit.

6) Check I2CRSF (I2CTSF) bit, read I2CDB register (2nd data), and then clear Pend bit.

7) Check I2CSTPSF bit, end transmission.

6.11 LVD (Low Voltage Detector)

Under unstable power source condition, such as external power noise interference or EMS test condition, a violent power vibration could occur. At the time, the VDD could become unstable as it could be operating below working voltage. When the system supply voltage (VDD) is below the operating voltage, the IC kernel will automatically keep all register status.

6.11.1 Low Voltage Reset (LVR)

The detailed LVR operation mode is as follows:

LVR1	LVR0	VDD Reset Level	VDD Release Level
0	0	4.0V *	4.2V
0	1	3.5V **	3.7V
1	0	2.7V ***	2.9V
1	1	NA (Power-on Reset)	

* *If VDD < 4.0V and is kept for 5 µs, the IC will be reset.*
** *If VDD < 3.5V and is kept for 5 µs, the IC will be reset.*
*** *If VDD < 2.7V and is kept for 5 µs, the IC will be reset.*

6.11.2 Low Voltage Detect

■ **Registers for LVD Circuit**

R_Bank	Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bank 1	0X49	**LVDCR**	**LVDEN**	**LVD2**	**LVD1**	**LVD0**	**/LVD**	-	-	-
Bank 0	0X10	**WUCR2**	-	-	**LVDWK**	-	-	-	-	-
Bank 0	0x1B	**IMR1**	-	-	**LVDIE**	-	-	-	-	-
Bank 0	0x15	**SFR1**	-	-	**LVDSF**	-	-	-	-	-

■ **Corresponding Bits for LVD**

LVDEN	LVDS1, LVDS0	LVD Voltage Interrupt Level	LVDB
1	11	VDD <2.2V	0
		VDD >2.2V	1
1	10	VDD <3.3V	0
		VDD >3.3V	1
1	01	VDD <4.0V	0
		VDD >4.0V	1
1	00	VDD <4.5V	0
		VDD >4.5V	1
0	XX	NA	1

■ LVD Programming Process

Follow the steps below to obtain data from the LVD**:**

1) Write to the two bits (LVDS1 ~ LVDS0) on the Bank1-R49 register to define the LVD level (see Section 6.1.96 for details).
2) Set the LVDWK bit if the Wake-up function is in use.
3) Set the LVDIE bit if the interrupt function is in use.
4) Write "ENI" instruction if the interrupt function is in use.
5) Set LVDEN bit to "**1**."
6) Write "SLEP" instruction or poll /LVD bit.
7) Clear the interrupt flag bit (LVDSF) when Low Voltage is detected.

NOTE

- *When the LVDEN bit is set to enable the LVD module, the current consumption will increase to 10 μA.*
- *During the Sleep mode, the LVD module continues to operate. If the device voltage drop slowly and crosses the detect point, the LVDSF bit will be set and the device will wake-up from Sleep mode.*
- *When the system resets, the LVD flag will be cleared.*

Figure below shows the LVD module detection point in an external voltage condition.

■ When VDD drops but remains above VLVD, the LVDSF remains at "**0**".

■ When VDD drops but above V_{LVD}, LVDSF remains at "**0**". When VDD drops below V_{LVD}, LVDSF is set to "**1**." If global ENI is enabled, the LVDSF is also set to "**1**", and the next instruction will branch to interrupt vector.
After the VDD rises above V_{LVD} again, the LVDSF will be set to "**1**" again. When the global ENI is enabled, the next instruction will be executed in the interrupt vector. Then the LVD interrupt flag is cleared to "**0**" by software.

■ When VDD drops below V_{RESET} in less than 1μs, the system will keep all the registers status, and the system halts but with the oscillation remaining active.
When VDD drops below V_{RESET} but in more than 1 μs, a system reset occurs (refer to Section 6.1.15 for more details).

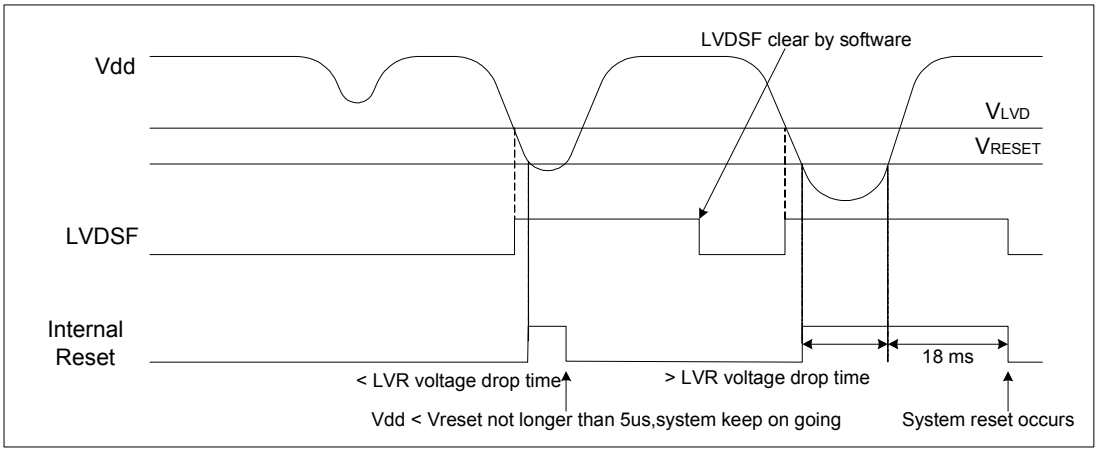


Figure 6-19 LVD Waveform Characteristics showing Detection Point in an External Voltage Condition

6.12 Oscillator

6.12.1 Oscillator Modes

The MCU can be operated in six different oscillator modes (Fm), such as:

- High XTAL oscillator Mode 2 (HXT2)
- High XTAL oscillator Mode 1 (HXT1)
- XTAL oscillator mode (XT)
- Low XTAL oscillator mode (LXT)
- Internal RC oscillator mode (IRC)

User can select one of the modes by programming the Option pin. There are three types of the clock source which is used for Fs. Fs can be determined by Fss1 and Fss0 options. The maximum operating frequency of crystal/resonator on the different VDDs, are listed in the table below.

- **Summary of Maximum Operating Speeds**

Conditions	VDD	Fxt Max. (MHz)
Two clocks	1.8	4
	3.0	8
	5.0	20

6.12.2 Crystal Oscillator/Ceramic Resonators (XTAL)

The EM78P374N can be driven by an external clock signal through the OSCI pin as shown in the figure at right.

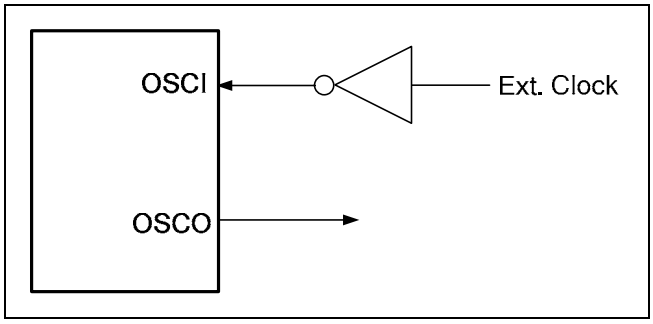


Figure 6-20a External Clock Input Circuit

In most applications, Pin OSCI and Pin OSCO can be connected with a crystal or ceramic resonator to generate oscillation as depicted in the right figures. The same applies to LXT mode or HXT mode.

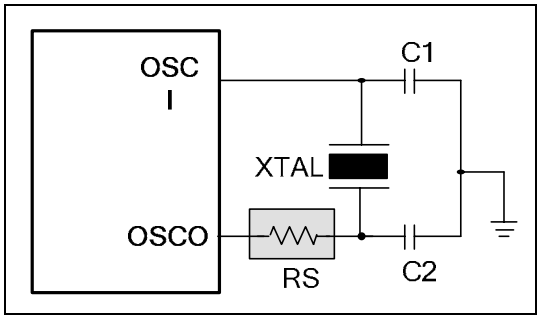


Figure 6-20c Crystal/Resonator Circuit

The following table provides the recommended values of C1 and C2. Since each resonator has its own attributes, you should refer to its specification for the appropriate values of C1 and C2. The serial resistor, RS; may be necessary for AT strip cut crystal or low frequency mode.

■ **Capacitor Selection Guide for Crystal Oscillator or Ceramic Resonator**

Oscillator Type	Frequency Mode	Frequency	C1 (pF)	C2 (pF)
Main-oscillator (Ceramic Resonators)	LXT (100K ~ 1 MHz)	100kHz	60pF	60pF
		200kHz	60pF	60pF
		455kHz	40pF	40pF
		1.0 MHz	30pF	30pF
	HXT2 (1M ~ 6 MHz)	1.0 MHz	30pF	30pF
		2.0 MHz	30pF	30pF
		4.0 MHz	20pF	20pF
Main-oscillator (Crystal Oscillator)	LXT (100K ~ 1 MHz)	100kHz	60pF	60pF
		200kHz	60pF	60pF
		455kHz	40pF	40pF
		1.0 MHz	30pF	30pF
	XT (1M ~ 6 MHz)	1.0 MHz	30pF	30pF
		2.0 MHz	30pF	30pF
		4.0 MHz	20pF	20pF
		6.0 MHz	30pF	30pF
	HXT2 (6M ~ 12 MHz)	6.0 MHz	30pF	30pF
		8.0 MHz	20pF	20pF
		12.0 MHz	30pF	30pF
	HXT1 (12M ~ 20 MHz)	12.0 MHz	30pF	30pF
		16.0 MHz	20pF	20pF
		20.0 MHz	15pF	15pF

6.12.3 Internal RC Oscillator Mode

The EM78P374N offers a versatile Internal RC mode with a default frequency value of 4 MHz. Internal RC oscillator mode has other frequencies (16 MHz, 8 MHz, 4 MHz, and 1 MHz) that can be set with Code Option**:** RCM1 and RCM0. All these four main frequencies can be calibrated by programming the Code Option bits**:** C5~C0. Table below shows a typical drift rate of the calibration.

■ **Internal RC Drift Rate (Ta=25°C, VDD=5V±5%, VSS=0V)**

Internal RC Frequency	Drift Rate			
	Temperature (-40°C ~ +85°C)	Voltage (2.5V ~ 5.5V)	Process	Total
1 MHz	±2%	±1%	±1%	±4%
4 MHz	±2%	±1%	±1%	±4%
8 MHz	±2%	±1%	±1%	±4%
16 MHz	±2%	±1%	±1%	±4%

NOTE

These are theoretical values provided for reference only. Actual values may vary depending on the actual process.

6.13 Power-on Considerations

Any microcontroller is not guaranteed to start to operate properly before the power supply stabilizes to a steady state. The EM78P374N is equipped with a built-in Power-on Voltage Detector (POVD) with a detecting level of 2.0V. Power will work well if Vdd rises fast enough (50 ms or less). However, under critical applications, extra devices may still be required to assist in solving the power-up problems.

6.14 External Power-on Reset Circuit

The circuit shown in next figure implements an external RC to generate the reset pulse. The pulse width (time constant) should be kept long enough for Vdd to achieve minimum operating voltage. Apply this circuit when the power supply has a slow rising time. Since the current leakage from the /RESET pin is ± 5 μA, it is recommended that R should not be greater than 40 KΩ in order for the /RESET pin voltage to remain at below 0.2V. The diode (D) acts as a short circuit at the moment of power down. The capacitor (C) will discharge rapidly and fully. The current-limited resistor (Rin) will prevent high current or ESD (electrostatic discharge) from flowing to Pin /RESET.

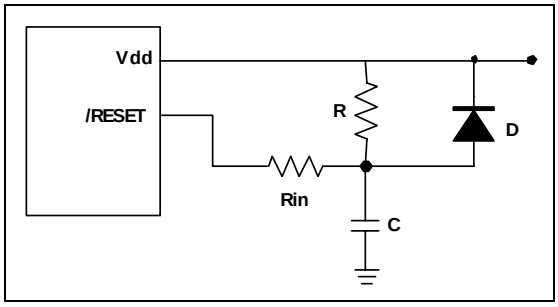


Figure 6-21 External Power-up Reset Circuit

6.15 Residue-Voltage Protection

When the battery is replaced, device power (Vdd) is taken off but residue-voltage remains. The residue-voltage may trip below Vdd minimum, but not to zero. This condition may cause a poor power-on reset. The following figures show how to perform and accomplish a proper residue-voltage protection circuit.

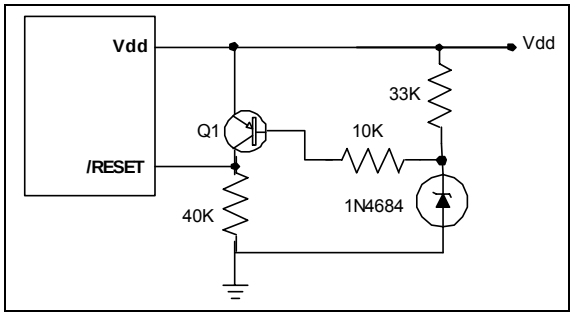


Figure 6-22a Circuit 1 for Residue Voltage Protection

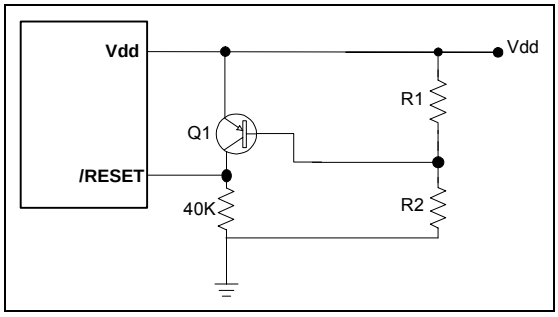


Figure 6-22b Circuit 2 for Residue Voltage Protection

6.16 Code Option

6.16.1 Code Option Register (Word 0)

Word 0															
Bit	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mnemonic	-	-	-	-	HLFS	HLP	LVR1	LVR0	RESETEN	ENWDT	NRHL	NRE	PR2	PR1	PR0
1	-	-	-	-	Normal	High	High	High	P67	Disable	32/fc	Enable	Disable		
0	-	-	-	-	Green	Low	Low	Low	/RST	Enable	8/fc	Disable	Enable		
Default	0	1	0	0	1	0	1	1	1	1	1	1	Disable		

Bit 14: Not used. Set to "**0**" all the time.

Bit 13: Not used. Set to "**1**" all the time.

Bits 12 ~ 11: Not used. Set to "**0**" all the time.

Bit 10 (HLFS): Reset to Normal or Green Mode Select bit

0: CPU is defined as Green mode when a Reset occurs.

1: CPU is defined as Normal mode when a Reset occurs (default).

Bit 9: Power consumption selection

0: Low power consumption

1: Normal power consumption (default)

Bits 8 ~ 7 (LVR1 ~ LVR0): Low Voltage Reset Enable bits

LVR1	LVR0	VDD Reset Level	VDD Release Level
0	0	4.0V *	4.2V
0	1	3.5V **	3.7V
1	0	2.7V ***	2.9V
1	1	NA (Power-on Reset)	

* *If VDD < 4.0V and is kept for about 5 µs, the IC will be reset.*
** *If VDD < 3.5V and is kept for about 5 µs, the IC will be reset.*
*** *If VDD < 2.7V and is kept for about 5 µs, the IC will be reset.*

Bit 6 (RESETEN): P67//RST pin select bit

0: Enable, /RST pin

1: Disable, P67 pin (default)

Bit 5 (ENWDT): WDT enable bit

Bit 4 (NRHL): Noise rejection high/low pulse define bit

NOTE

In Low XTAL oscillator (LXT) mode, the noise rejection high/low pulses are always 8/Fm.

Bit 3 (NRE): Noise Rejection Enable bit

0: Disable

1: Enable (default)

> **NOTE**
> *In Green, Idle, and Sleep modes, the noise rejection circuit is always disabled.*

6.16.2 Code Option 1 (Word 1)

Word 1															
Bit	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Mnemonic	**-**	**FSS0**	**C5**	**C4**	**C3**	**C2**	**C1**	**C0**	**RCM1**	**RCM0**	**-**	**OSC2**	**OSC1**	**OSC0**	**RCOUT**
1	-	16kHz	High	High	High	High	High	High	High	High	-	High	High	High	High
0	-	32kHz	Low	Low	Low	Low	Low	Low	Low	Low	-	Low	Low	Low	Low
Default	1	1	1	1	1	1	1	1	1	1	0	0	1	1	1

Bit 14: Not used. Set to "**1**" all the time.

Bit 13 (FSS0): Sub-frequency selection

0: 32kHz

1: 16kHz (default)

Bits 12 ~ 7 (C5 ~ C0):IRC trim bits. These are automatically set by the writer.

Bits 6 ~ 5 (RCM1 ~ RCM0): IRC frequency selection bits

RCM1	RCM0	Frequency (MHz)
0	0	1
0	1	8
1	0	16
1	1	4 (default)

Bits 3 ~ 1 (OSC2 ~ OSC0): Oscillator modes selection bits

Mode	OSC2	OSC1	OSC0
HXT1 (High XTAL1 Oscillator mode) Frequency range: 12 ~ 20 MHz	1	1	1
HXT2 (High XTAL2 Oscillator mode) Frequency range: 6 ~ 12 MHz	1	1	0
XT (XTAL Oscillator mode) Frequency range: 1 ~ 6MHz	1	0	1
LXT1 (Low XTAL1 Oscillator mode) Frequency range: 100kHz ~ 1 MHz	1	0	0
IRC (Internal RC Oscillator mode) OSCI pin acts as I/O **(default)**	0	1	1
IRC (Internal RC Oscillator mode) OSCI pin acts RCOUT	0	1	0

Bit 0 (RCOUT): System Clock Output Enable bit in IRC mode

0: OSCI pin output instruction cycle time in open drain

1: OSCI output instruction cycle time (default)

6.16.3 Code Option 2 (Word 2)

Word 2															
Bit	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Mnemonic	**-**	**-**	**-**	**SC3**	**SC2**	**SC1**	**SC0**	**-**	**IRCIRS**	**-**	**I2COPT**	**-**	**-**	**-**	**-**
1	-	-	-	High	High	High	High	-	Regulator	-	High	-	-	-	-
0	-	-	-	Low	Low	Low	Low	-	Bandgap	-	Low	-	-	-	-
Default	0	0	0	1	1	1	1	1	1	1	1	0	0	0	1

Bit 14: Not used. Set to "**0**" all the time.

Bits 13 ~ 12: Not used. Set to "**0**" all the time.

Bits 11 ~ 8 (SC3 ~ SC0): Trim bits of sub-frequency IRC. These are automatically set by the writer.

Bit 7: Not used. Set to "**1**" all the time.

Bit 6 (IRCIRS): IRC internal reference selection

0: Bandgap

1: IRC regulator (default)

Bit 5: Not used. Set to "**1**" all the time.

Bit 4 (I2COPT): I^2C optional bit. It is used to switch the pin I^2C function position

0: I^2C Pins (SCL/SDA) are P72, P73 in the pin assignment figure

1: I^2C Pins (SCL/SDA) are P61, P62 in the pin assignment figure (Default)

Bits 3 ~ 1: Not used. Set to "**0**" all the time.

Bit 0: Not used. Set to "**1**" all the time.

6.16.4 Code Option 3 (Word 3)

Word 3															
Bit	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Mnemonic	**EFTIM**	**-**	**-**	**ADFM**	**-**	**-**	**-**	**-**	**-**	**ID5**	**ID4**	**ID3**	**ID2**	**ID1**	**ID0**
1	Light	-	-	High	-	-	-	-	-	Customer ID					
0	Heavy	-	-	Low	-	-	-	-	-						
Default	1	1	1	0	1	1	0	0	0						

Bit 14 (EFTIM): Low Pass Filter (**0:** Heavy, **1:** Light)

0: Less than 10 MHz- pass (heavy LPS)

1: Less than 25 MHz- pass (light LPS, default)

Bits 13 ~ 12: Not used. Set to "**1**" all the time.

Bit 11 (ADFM): These bits control the AD data buffer format (ADDH and ADDL). Refer to the following table.

ADFM			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
12 bits	0	ADDH	-	-	-	-	ADD11	ADD10	ADD9	ADD8
		ADDL	ADD7	ADD6	ADD5	ADD4	ADD3	ADD2	ADD1	ADD0
	1	ADDH	ADD11	ADD10	ADD9	ADD8	ADD7	ADD6	ADD5	ADD4
		ADDL	-	-	-	-	ADD3	ADD2	ADD1	ADD0

Bits 10~9: Not used. Set to "**1**" all the time.

Bits 8~6: Not used. Set to "**0**" all the time.

Bits 5~0: Customer ID

6.16.5 Code Option F (Word F)

Word F															
Bit	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mnemonic	-	-	-	-	-	-	PR11	PR10	PR9	PR8	PR7	PR6	PR5	PR4	PR3
1	-	-	-	-	-	-	High	High	High	High	High	High	High	High	High
0	-	-	-	-	-	-	Low	Low	Low	Low	Low	Low	Low	Low	Low
Default	-	-	-	-	-	-	1	1	1	1	1	1	1	1	1

Bits 14 ~ 9: Not used. Set to "**0**" all the time.

Bits 8 ~ 0: Protect bits

6.17 Instruction Set

Each instruction in the instruction set is a 15-bit word divided into an OP code and one or more operands. Normally, all instructions are executed within one single instruction cycle (one instruction consists of 2 oscillator periods), unless the program counter is changed by instruction "MOV R2,A", "ADD R2,A", or by instructions of arithmetic or logic operation on R2 (e.g., "SUB R2,A", "BS(C) R2,6", "CLR R2", etc.). In this case, the execution takes two instruction cycles.

If for some reasons, the specification of the instruction cycle is not suitable for certain applications, try to modify the instruction as follows**:**

A) Change one instruction cycle to consist of four oscillator periods.

B) "JMP", "CALL", "RET", "RETL", "RETI", or the conditional skip ("JBS", "JBC", "JZ", "JZA", "DJZ", "DJZA") commands which were tested to be true, are executed within two instruction cycles. The instructions that are written to the program counter also take two instruction cycles.

Case A is selected by the Code Option bit, called CLK. One instruction cycle consists of two oscillator clocks if CLK is low and four oscillator clocks if CLK is high.

Additionally, the Instruction Set also offers the following features**:**

1) Every bit of any register can be set, cleared, or tested directly.

2) The I/O register can be regarded as general register. That is, the same instruction can operate on I/O register.

The symbol "R" represents a register designator that specifies which one of the registers (including operational registers and general purpose registers) is to be utilized by the instruction. "**b**" represents a bit field designator that selects the value for the bit which is located in the register "**R**", and affects operation. "**k**" represents an 8 or 10-bit constant or literal value.

■ Instruction Set Table:

In the following Instruction Set table, the following symbols are used**:**

"**R**" *represents a register designator that specifies which one of the registers (including operational registers and general purpose registers) is to be utilized by the instruction.*

"**b**" *represents a bit field designator that selects the value for the bit which is located in the register "**R**", and affects the operation.*

"**k**" *represents an 8 or 10-bit constant or literal value.*

Binary Instruction	HEX	Mnemonic	Operation	Status Affected
000 0000 0000 0000	0000	NOP	No operation	None
000 0000 0000 0001	0001	DAA	Decimal Adjust A	C
000 0000 0000 0011	0003	SLEP	0 → WDT, Stop oscillator	T,P
000 0000 0000 0100	0004	WDTC	0 → WDT	T,P
000 0000 0001 0000	0010	ENI	Enable Interrupt	None
000 0000 0001 0001	0011	DISI	Disable Interrupt	None
000 0000 0001 0010	0012	RET	[Top of Stack] → PC	None
000 0000 0001 0011	0013	RETI	[Top of Stack] → PC, Enable Interrupt	None
000 0001 rrrr rrrr	01rr	MOV R,A	A → R	None
000 0010 0000 0000	0200	CLRA	0 → A	Z
000 0011 rrrr rrrr	03rr	CLR R	0 → R	Z
000 0100 rrrr rrrr	04rr	SUB A,R	R-A → A	Z, C, DC
000 0101 rrrr rrrr	05rr	SUB R,A	R-A → R	Z, C, DC
000 0110 rrrr rrrr	06rr	DECA R	R-1 → A	Z
000 0111 rrrr rrrr	07rr	DEC R	R-1 → R	Z
000 1000 rrrr rrrr	08rr	OR A,R	A ∨ R → A	Z

(Continuation)

Binary Instruction	HEX	Mnemonic	Operation	Status Affected
000 1001 rrrr rrrr	09rr	OR R,A	A ∨ R → R	Z
000 1010 rrrr rrrr	0Arr	AND A,R	A & R → A	Z
000 1011 rrrr rrrr	0Brr	AND R,A	A & R → R	Z
000 1100 rrrr rrrr	0Crr	XOR A,R	A ⊕ R → A	Z
000 1101 rrrr rrrr	0Drr	XOR R,A	A ⊕ R → R	Z
000 1110 rrrr rrrr	0Err	ADD A,R	A + R → A	Z, C, DC
000 1111 rrrr rrrr	0Frr	ADD R,A	A + R → R	Z, C, DC
001 0000 rrrr rrrr	10rr	MOV A,R	R → A	Z
001 0001 rrrr rrrr	11rr	MOV R,R	R → R	Z
001 0010 rrrr rrrr	12rr	COMA R	/R → A	Z
001 0011 rrrr rrrr	13rr	COM R	/R → R	Z
001 0100 rrrr rrrr	14rr	INCA R	R+1 → A	Z
001 0101 rrrr rrrr	15rr	INC R	R+1 → R	Z
001 0110 rrrr rrrr	16rr	DJZA R	R-1 → A, skip if zero	None
001 0111 rrrr rrrr	17rr	DJZ R	R-1 → R, skip if zero	None
001 1000 rrrr rrrr	18rr	RRCA R	R(n) → A(n-1), R(0) → C, C → A(7)	C
001 1001 rrrr rrrr	19rr	RRC R	R(n) → R(n-1), R(0) → C, C → R(7)	C
001 1010 rrrr rrrr	1Arr	RLCA R	R(n) → A(n+1), R(7) → C, C → A(0)	C
001 1011 rrrr rrrr	1Brr	RLC R	R(n) → R(n+1), R(7) → C, C → R(0)	C
001 1100 rrrr rrrr	1Crr	SWAPA R	R(0-3) → A(4-7), R(4-7) → A(0-3)	None
001 1101 rrrr rrrr	1Drr	SWAP R	R(0-3) ↔ R(4-7)	None
001 1110 rrrr rrrr	1Err	JZA R	R+1 → A, skip if zero	None
001 1111 rrrr rrrr	1Frr	JZ R	R+1 → R, skip if zero	None
010 0bbb rrrr rrrr	2xrr	BC R,b	0 → R(b)	None
010 1bbb rrrr rrrr	2xrr	BS R,b	1 → R(b)	None
011 0bbb rrrr rrrr	3xrr	JBC R,b	if R(b)=0, skip	None
011 1bbb rrrr rrrr	3xrr	JBS R,b	if R(b)=1, skip	None
100 kkkk kkkk kkkk	4kkk	CALL k	PC+1 → [SP], (Page, k) → PC	None

(Continuation)

Binary Instruction	HEX	Mnemonic	Operation	Status Affected
101 kkkk kkkk kkkk	5kkk	JMP k	(Page, k) → PC	None
110 0000 kkkk kkkk	60kk	MOV A,k	k → A	None
110 0100 kkkk kkkk	64kk	OR A,k	A ∨ k → A	Z
110 1000 kkkk kkkk	68kk	AND A,k	A & k → A	Z
110 1100 kkkk kkkk	6Ckk	XOR A,k	A ⊕ k → A	Z
111 0000 kkkk kkkk	70kk	RETL k	k → A, [Top of Stack] → PC	None
111 0100 kkkk kkkk	74kk	SUB A,k	k-A → A	Z, C, DC
111 1100 kkkk kkkk	7Ckk	ADD A,k	k+A → A	Z, C, DC
111 1010 0000 kkkk	7A0k	SBANK k	K→R1(4)	None
111 1010 0100 kkkk	7A4k	GBANK k	K→R1(0)	None
111 1010 1000 kkkk kkk kkkk kkkk kkkk	7A8k kkkk	LCALL k	Next instruction: k kkkk kkkk kkkk PC+1→[SP], k→PC	None
111 1010 1100 kkkk kkk kkkk kkkk kkkk	7ACk kkkk	LJMP k	Next instruction: k kkkk kkkk kkkk K→PC	None
111 1011 rrrr rrrr	7Brr	TBRD R	ROM[(TABPTR)] → R	None

7 Absolute Maximum Ratings

Items	Rating		
Temperature under bias	-40°C	to	85°C
Storage temperature	-65°C	to	150°C
Input voltage	Vss-0.3V	to	Vdd+0.5V
Output voltage	Vss-0.3V	to	Vdd+0.5V
Working Voltage	2.1V	to	5.5V
Working Frequency	DC	to	20 MHz

8 DC Electrical Characteristics

■ **Ta=25°C, VDD=5.0V, VSS=0V**

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Fxt	XTAL: VDD to 3V	Two cycles with two clocks	DC	8	-	MHz
	XTAL: VDD to 5V		DC	16	-	MHz
	ERIC: VDD to 5V	R: 2.2 MΩ	F±30%	32.7	F±30%	kHz
	IRC: VDD to 5V	4 MHz, 1 MHz, 8 MHz, 16 MHz	-	F	-	Hz
IIL	Input Leakage Current for input pins	VIN = VDD, VSS	-1	0	1	μA
IRCE	Internal RC Oscillator error per stage	-	-	±1	-	%
IRC1	IRC: VDD to 5V	RCM0:RCM1=1:1	-	4	-	MHz
IRC2	IRC: VDD to 5V	RCM0:RCM1=1:0	-	8	-	MHz
IRC3	IRC: VDD to 5V	RCM0:RCM1=0:1	-	16	-	MHz
IRC4	IRC: VDD to 5V	RCM0:RCM1=0:0	-	1	-	MHz
VIHRC	Input High Threshold Voltage (Schmitt trigger)	OSCI in RC mode	3.9	4	4.1	V
IERC1	Sink current	VI from low to high, VI=5V	21	22	23	mA
VILRC	Input Low Threshold Voltage (Schmitt trigger)	OSCI in RC mode	1.7	1.8	1.9	V
IERC2	Sink current	VI from high to low, VI=2V	16	17	18	mA
IIL	Input Leakage Current for input pins	VIN = VDD, VSS	-1	0	1	μA
VIH1	Input High Voltage (Schmitt trigger)	Ports 5, 6, 7,	0.7Vdd	-	Vdd+0.3V	V
VIL1	Input Low Voltage (Schmitt trigger)	Ports 5, 6, 7	-0.3V	-	0.3Vdd	V
VIHT1	Input High Threshold Voltage (Schmitt trigger)	/RESET	0.7Vdd	-	Vdd+0.3V	V
VILT1	Input Low Threshold Voltage (Schmitt trigger)	/RESET	-0.3V	-	0.3Vdd	V
VIHT2	Input High Threshold Voltage (Schmitt trigger)	TCC, INT	0.7Vdd	-	Vdd+0.3V	V
VILT2	Input Low Threshold Voltage (Schmitt trigger)	TCC, INT	-0.3V	-	0.3Vdd	V
VIHX1	Clock Input High Voltage	OSCI in crystal mode	2.9	3.0	3.1	V
VILX1	Clock Input Low Voltage	OSCI in crystal mode	1.7	1.8	1.9	V
IOH1	Output High Voltage (Ports 5, 6, 7)	VOH = VDD-0.1VDD	-	-4.8	-	mA
IOH2	Output High Voltage (high drvie) (Ports 5, 6, 7)	VOH = VDD-0.1VDD	-	-7.9	-	mA
IOL1	Output Low Voltage (Ports 5, 6, 7)	VOL = GND+0.1VDD	-	14	-	mA
IOL2	Output Low Voltage (P67)	VOL = GND+0.1VDD	-	16	-	mA
IOL3	Output Low Voltage (high sink) (Ports 5, 6, 7)	VOL = GND + 0.1VDD	-	27	-	mA
IOL4	Output Low Voltage (high sink) (P67)	VOL = GND + 0.1VDD	-	39	-	mA

(Continuation)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
LVR1	Low voltage reset level	Ta= 25°C	2.41	2.7	2.99	V
		Ta= -40~85°C	2.14	2.7	3.25	V
LVR2	Low voltage reset level	Ta= 25°C	3.1	3.5	3.92	V
		Ta= -40~85°C	2.73	3.5	4.25	V
LVR3	Low voltage reset level	Ta= 25°C	3.56	4.0	4.43	V
		Ta= -40~85°C	3.16	4.0	4.81	V
IPH	Pull-high current	Pull-high active, input pin at VSS	-	-62	-	μA
IPL	Pull-low current	Pull-low active, input pin at Vdd	-	40	-	μA
ISB1	Power down current (Sleep mode)	/RESET= 'High', Fm and Fs off All input and I/O pins at VDD, Output pin floating. WDT disabled	-	1.2	-	μA
ISB2	Power down current (Sleep mode)	/RESET= 'High', Fm and Fs off. All input and I/O pins at VDD, Output pin floating. WDT enabled	-	10.8	-	μA
ISB3	Power down current (Idle mode)	/RESET= 'High', Fm off. Fs=32kHz (IRC type), Output pin floating, WDT enabled	-	10.8	-	μA
ICC1	Operating supply current (Green mode)	/RESET= 'High', Fm off Fs=16kHz (IRC type), Output pin floating, WDT enabled	-	22.8	-	μA
ICC2	Operating supply current (Green mode)	/RESET= 'High', Fm off Fs=32kHz (IRC type), Output pin floating, WDT enabled	-	30	-	μA
ICC3	Operating supply current (Normal mode)	/RESET= 'High', Fm=4MHz (Crystal type), Fs on, Output pin floating, WDT enabled	-	1.44	-	mA
ICC4	Operating supply current (Normal mode)	/RESET= 'High', Fm=4MHz (IRC type), Fs on, Output pin floating, WDT enabled	-	1.32	-	mA
ICC5	Operating supply current (Normal mode)	/RESET= 'High', Fm=10MHz (Crystal type), Fs on, Output pin floating, WDT enabled	-	2.8	-	mA
ICC6	Operating supply current (Normal mode)	/RESET= 'High', Fm=16MHz (IRC type), Fs on, Output pin floating, WDT enabled	-	3.84	-	mA
ICC7	Operating supply current (Normal mode)	/RESET= 'High', Fm=16MHz (Crystal type), Fs on, Output pin floating, WDT enabled	-	4.4	-	mA

NOTE

- *The DC Characteristics parameters are theoretical values only and have not been tested or verified.*
- *Data under the "Min.", "Typ.", and "Max." columns are based on theoretical results at 25℃. These data are for design reference only and have not been tested or verified.*

8.1 AD Converter Characteristics

■ **Vdd=2.5V to 5.5V, Vss=0V, Ta= 25°C**

Symbol		Parameter	Condition	Min.	Typ.	Max.	Unit
V_{AREF}		Analog reference voltage	V_{AREF} - V_{ASS} ≥ 2.5V	2.5	–	Vdd	V
V_{ASS}				Vss	–	Vss	V
VAI		Analog input voltage	–	V_{ASS}	–	V_{AREF}	V
IAI1	Ivdd	Analog supply current	VDD=V_{AREF}=5.5V, V_{ASS} = 0.0V Fin = 100kHz (V reference from Vdd)	–	-	1400	μA
	Ivref			–	–	10	μA
IAI2	Ivdd	Analog supply current	VDD=V_{AREF}=5.5V, V_{ASS} = 0.0V Fin = 100kHz (V reference from VREF)	–	–	900	μA
	IVref			–	–	500	μA
RN		Resolution	–	–	12	-	Bits
INL		Integral Nonlinearity	V_{AREF}= Vdd=5.0V Ta=25°C	–	–	±4	LSB
DNL		Differential nonlinear error	V_{AREF}= Vdd=5.0V Ta=25°C	–	–	±1	LSB
GE		Gain Error	V_{AREF}= Vdd=5.0V Ta=25°C	–	–	±8	LSB
OE		Offset error	V_{AREF}= Vdd=5.0V Ta=25°C	–	–	±4	LSB
ZAI		Recommended impedance of analog voltage source	–	–	–	10	KΩ
TAD		ADC clock duration	VDD=3~5.5V, V_{ASS} = 0.0V, Ta=25°C	0.5	-	–	μs
			VDD=2.5~3V, V_{ASS} = 0.0V, Ta=25°C	2	-	-	μs
Tsh		Sample and Hold Time	VDD=3~5.5V, V_{ASS} = 0.0V, Ta=25°C	4	-	–	μs
			VDD=2.5~3V, V_{ASS} = 0.0V, Ta=25°C	16	-	-	μs
TCN		AD conversion time	VDD=2.5~5.5V, V_{ASS} = 0.0V, Ta=25°C	-	Tsh+12 TAD	–	s
PSRR		Power supply rejection ratio	V_{AREF}= 2.5V, VREF=Vdd, Vdd=2.5V ~ 5.5V, Vin=0V ~ 2.5V	–	–	2	LSB
$A_{1/4VDD}$		Accuracy for 1/4 VDD			±3		%

8.2 Comparator Characteristics

■ **Vdd = 5.0V, Vss=0V, Ta = 25°C**

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
VOS	Input offset voltage	–	–	2	–	mV
Vcm	Input common-mode voltage range	–	GND	–	VDD	V
ICO	Supply current of comparator	Co=0V, Ta= -40~85°C	–	150	–	µA
TRS	Response time	VREF=1.0V, VRL=5V, RL=5.1k, CL=15p*	–	2.5	–	µs
TLRS	Large signal response time	VREF=2.5V, VRL = 5V, RL = 5.1k**	–	500	–	ns
IOL	Output sink current	Vi(-) = 1V, Vi(+) = 0V, Vo = GND+0.5V***	–	12	–	mA
VSAT	Saturation voltage	Vi(-)=1V, Vi(+)=0V, IOL <= 4mA***	–	0.2	0.4	V

* *These parameters are hypothetical (not tested) and provided for design reference use only.*

** *The response time specified is a 0V~VDD input step with 1/2VDD overdrive.*

*** *The driving ability is decided by digital output block.*

8.3 OP Characteristics

■ **Vdd = 5.0V, Vss=0V, Ta= 25°C**

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
VOS	Input offset voltage	Vip=0.5V, 4.5V	–	2	–	mV
SR	Slew rate	Ta= -40~85°C	–	1.5	–	V/µs
IVR	Input voltage range	–	0	–	5	V
OVS	Output voltage swing	Vip=0V, I_L=1.0mA Ta= -40~85°C	–	200	–	mV
		Vip=5V, I_L=1.0mA Ta= -40~85°C	–	4.7	–	V
IOP	Supply current of OP	Ta= -40~85°C	–	400	–	µA
PSRR	Power supply rejection ratio	Ta= -40~85°C	–	75	–	dB
CMRR	Common mode reject ratio	$0V \leqq V_{CM} \leqq V_{DD}$	–	90	–	dB
GBP	Gain bandwidth product	RL=1Meg, CL=100p	–	2.6	–	MHz

8.4 VREF 2V/3V/4V Characteristics

■ **Vdd = 5.0V, Vss=0V, Ta=-40 to 85°C**

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
VDD	Power Supply	–	2.1	–	5.5	V
I_{VDD}	DC Supply Current	No load	–	–	250	μA
A_{Vref}	Accuracy for Vref	Vref=2V, 3V, 4V	–	±1	±1.75	%
Warm up time	Time ready for voltage reference	VDD = VDD_{min} - 5.5V Cload = 19.2pf Rload = 15.36KΩ	–	30	50	μs
VDD_{min}	Minimum Power Supply	–	–	Vref + 0.2*	–	V

* **VDD_{min}:** *Can also work at Vref+0.1V, but has a poor PSRR*

9 AC Electrical Characteristics

■ **Ta=25°C, VDD=5V ± 5%, VSS=0V**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Dclk	Input CLK duty cycle	–	45	50	55	%
Tins	Instruction cycle time	Crystal type	125	–	DC	ns
Tpor*	Delay time after Power-on-Reset release	16kHz	–	16 ± 3%*	–	ms
Trstrl	Delay time after /Reset, WDT, and LVR release	Crystal type HLFS=1	–	WSTO**+510/Fm	–	μs
		IRC type HLFS=1	–	WSTO** + 8/Fm	–	μs
		HLFS=0	–	WSTO** + 8/Fs	–	μs
Trsth1	Hold time after /RESET pin reset	–	–	1 μs	–	μs
Trsth2	Hold time after LVR pin reset	–	–	1 μs	–	μs
Twdt*	Watchdog timer time-out	16kHz	–	16 ± 3%*	–	ms
Tset	Input pin setup time	–	–	0	–	ns
Thold	Input pin hold time	–	15	20	25	ns
Tdelay	Output pin delay time	Cload=20pF Rload=1MΩ	–	20	–	ns

* ***Tpor and Twdt*** *are 16 ± 10% ms at FSS0=1 (16kHz), Ta=-40°~85°C, and VDD=2.1~5.5V*

** **WSTO:** *Waiting time from Start-to-Oscillation*

NOTE

- *The above parameters are theoretical values only and have not been tested or verified.*
- *Data under the "Min.", "Typ." and "Max." columns are based on theoretical results at 25°C. These data are for design reference only and have not been tested or verified.*

APPENDIX

A Package Type

OTP MCU	Package Type	Pin Count	Package Size
EM78P374NSS24	SSOP	24	150 mil
EM78P374NSO24	SOP	24	300 mil
EM78P374NK24	Skinny DIP	24	300 mil
EM78P374NSS20	SSOP	20	209 mil
EM78P374NSO20	SOP	20	300 mil
EM78P374ND20	PDIP	20	300 mil
EM78P374NSO18	SOP	18	300 mil
EM78P374ND18	PDIP	18	300 mil

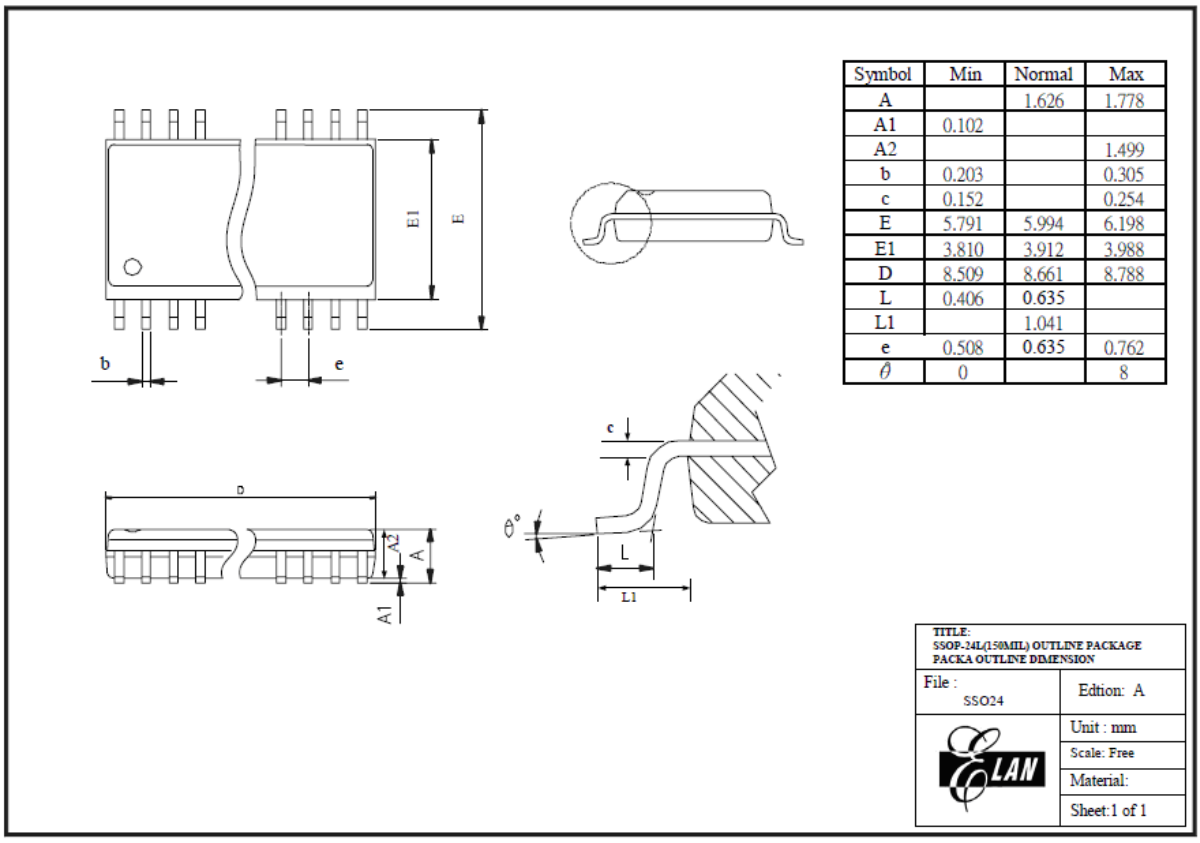
These are Green products which do not contain hazardous substances and comply with the third edition of Sony SS-00259 standard.

Pb content is less than 100ppm and complies with Sony specifications.

Part No.	EM78P374NxJ/xS
Electroplate type	Pure Tin
Ingredient (%)	Sn: 100%
Melting point (°C)	232°C
Electrical resistivity (μΩ-cm)	11.4
Hardness (hv)	8~10
Elongation (%)	>50%

B Packaging Configuration

B.1 EM78P374NSS24 150 mil



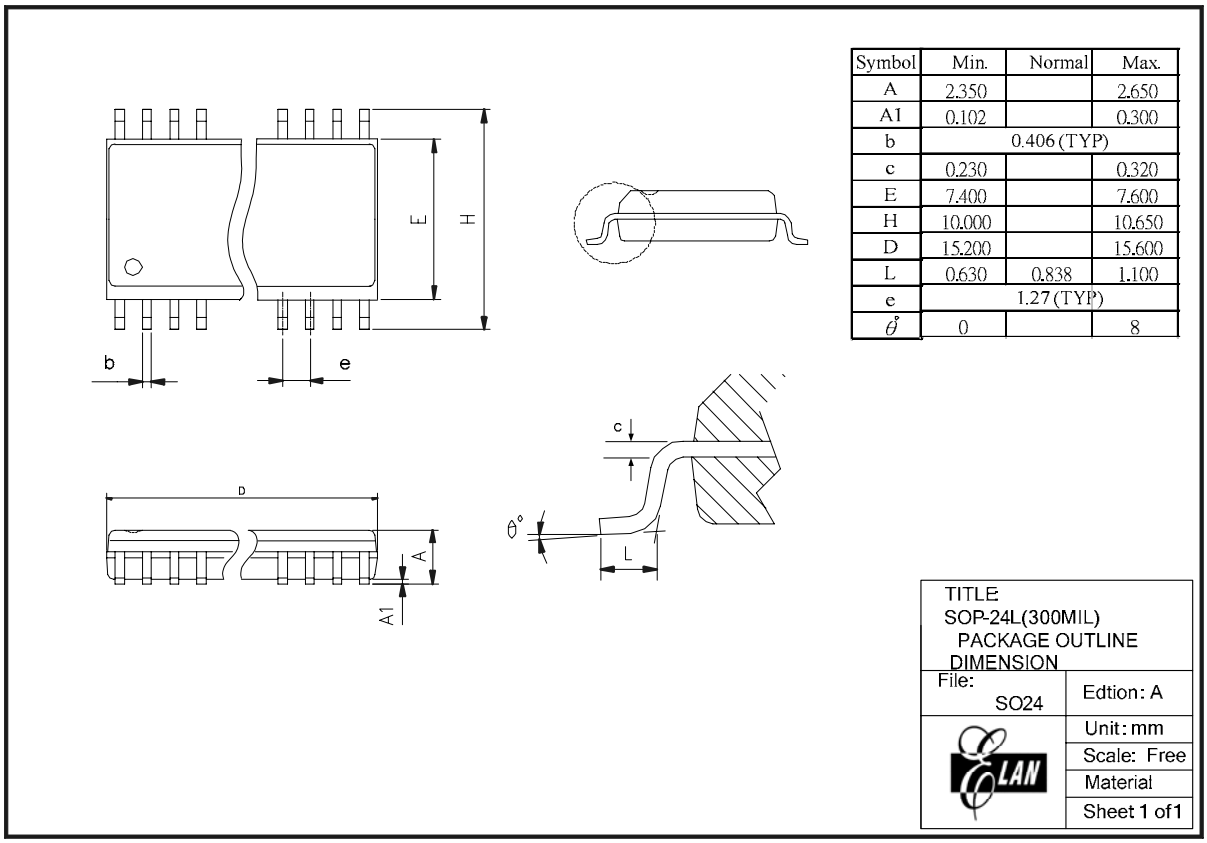
Symbol	Min	Normal	Max
A		1.626	1.778
A1	0.102		
A2			1.499
b	0.203		0.305
c	0.152		0.254
E	5.791	5.994	6.198
E1	3.810	3.912	3.988
D	8.509	8.661	8.788
L	0.406	0.635	
L1		1.041	
e	0.508	0.635	0.762
θ	0		8

TITLE:
SSOP-24L(150MIL) OUTLINE PACKAGE
PACKA OUTLINE DIMENSION

File : SSO24	Edtion: A
	Unit : mm
	Scale: Free
	Material:
	Sheet:1 of 1

Figure B-1 EM78P374N 24-Pin SSOP Package Type

B.2 EM78P374NSO24 300 mil



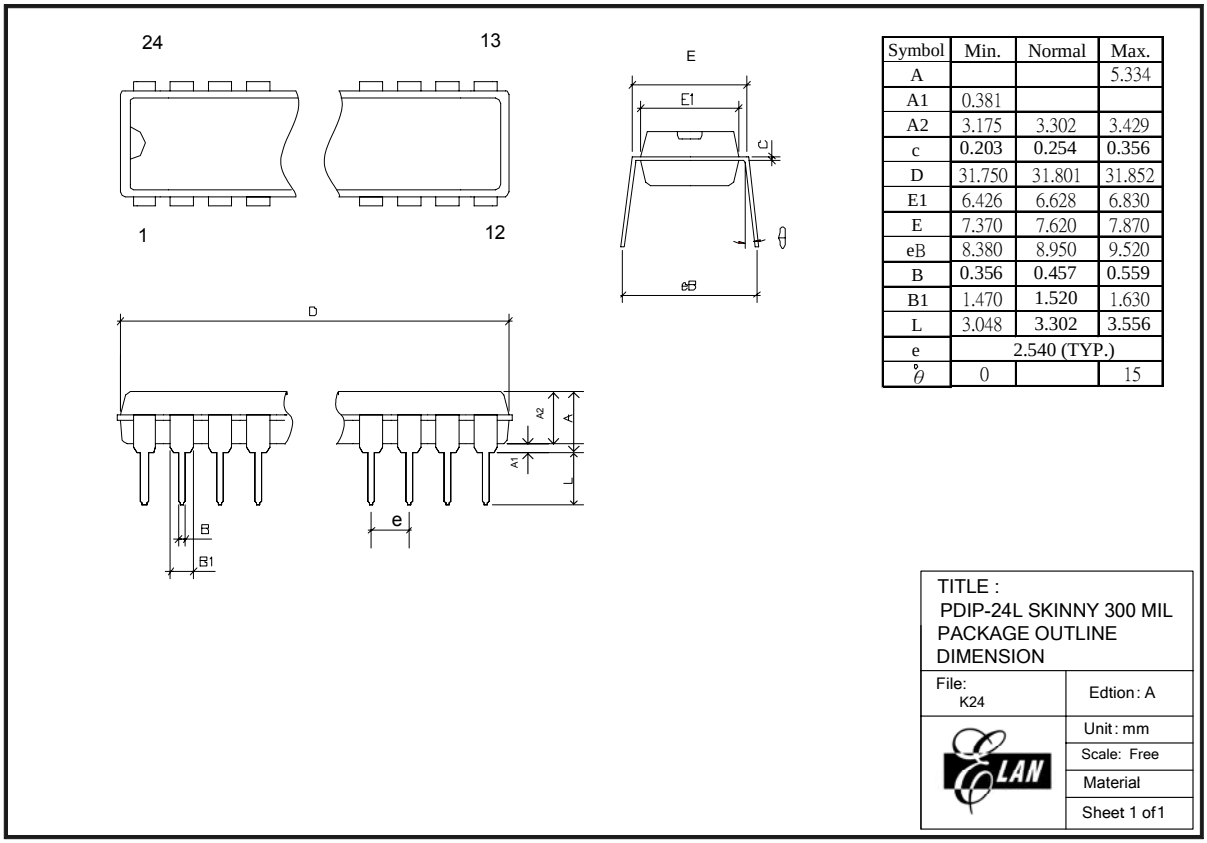
Symbol	Min.	Normal	Max.
A	2.350		2.650
A1	0.102		0.300
b	0.406 (TYP)		
c	0.230		0.320
E	7.400		7.600
H	10.000		10.650
D	15.200		15.600
L	0.630	0.838	1.100
e	1.27 (TYP)		
θ°	0		8

TITLE
SOP-24L(300MIL)
PACKAGE OUTLINE
DIMENSION

File: SO24	Edtion: A
	Unit: mm
	Scale: Free
	Material
	Sheet 1 of1

Figure B-2 EM78P372N 24-Pin SOP Package Type

B.3 EM78P374NK24 300 mil



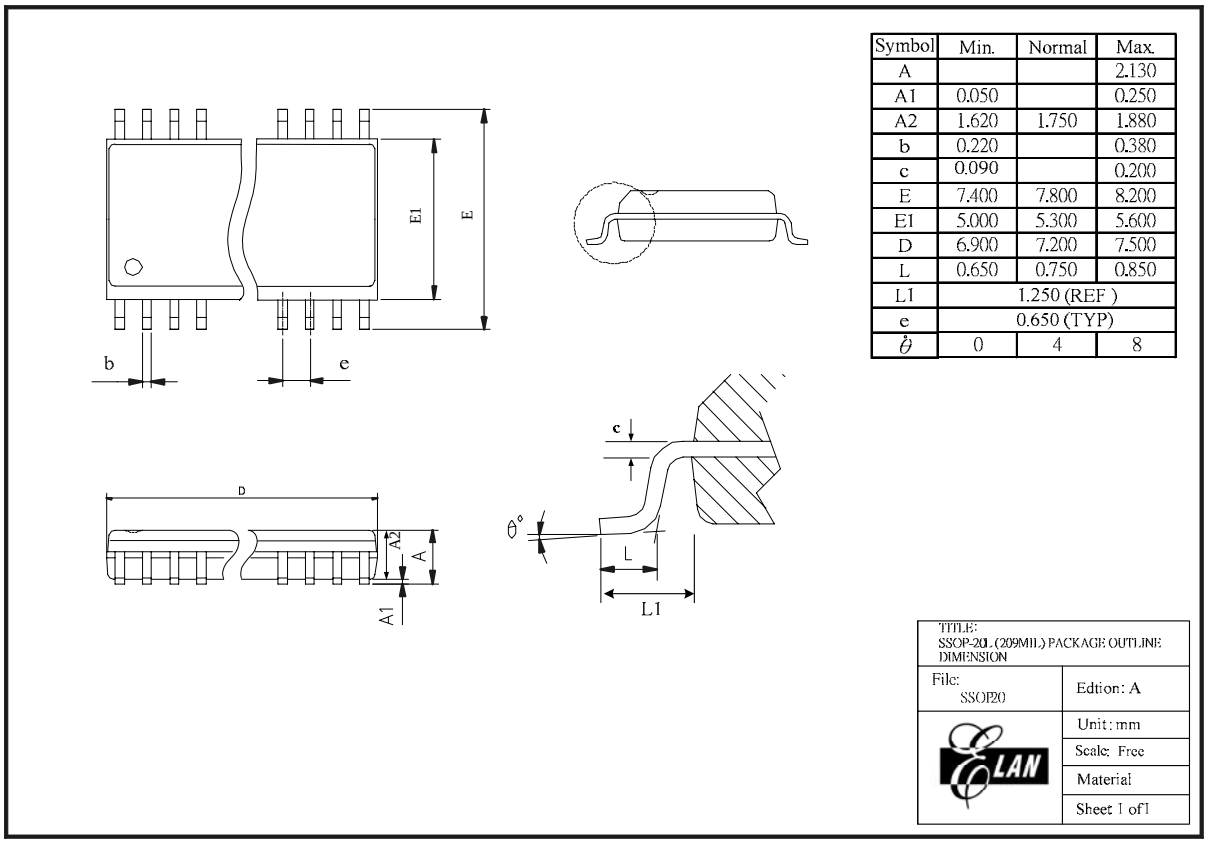
Symbol	Min.	Normal	Max.
A			5.334
A1	0.381		
A2	3.175	3.302	3.429
c	0.203	0.254	0.356
D	31.750	31.801	31.852
E1	6.426	6.628	6.830
E	7.370	7.620	7.870
eB	8.380	8.950	9.520
B	0.356	0.457	0.559
B1	1.470	1.520	1.630
L	3.048	3.302	3.556
e	2.540 (TYP.)		
θ°	0		15

TITLE :
PDIP-24L SKINNY 300 MIL
PACKAGE OUTLINE
DIMENSION

File: K24	Edtion : A
	Unit : mm
	Scale: Free
	Material
	Sheet 1 of1

Figure B-3 EM78P374N 24-Pin Skinny DIP Package Type

B.4 EM78P374NSS20 209 mil

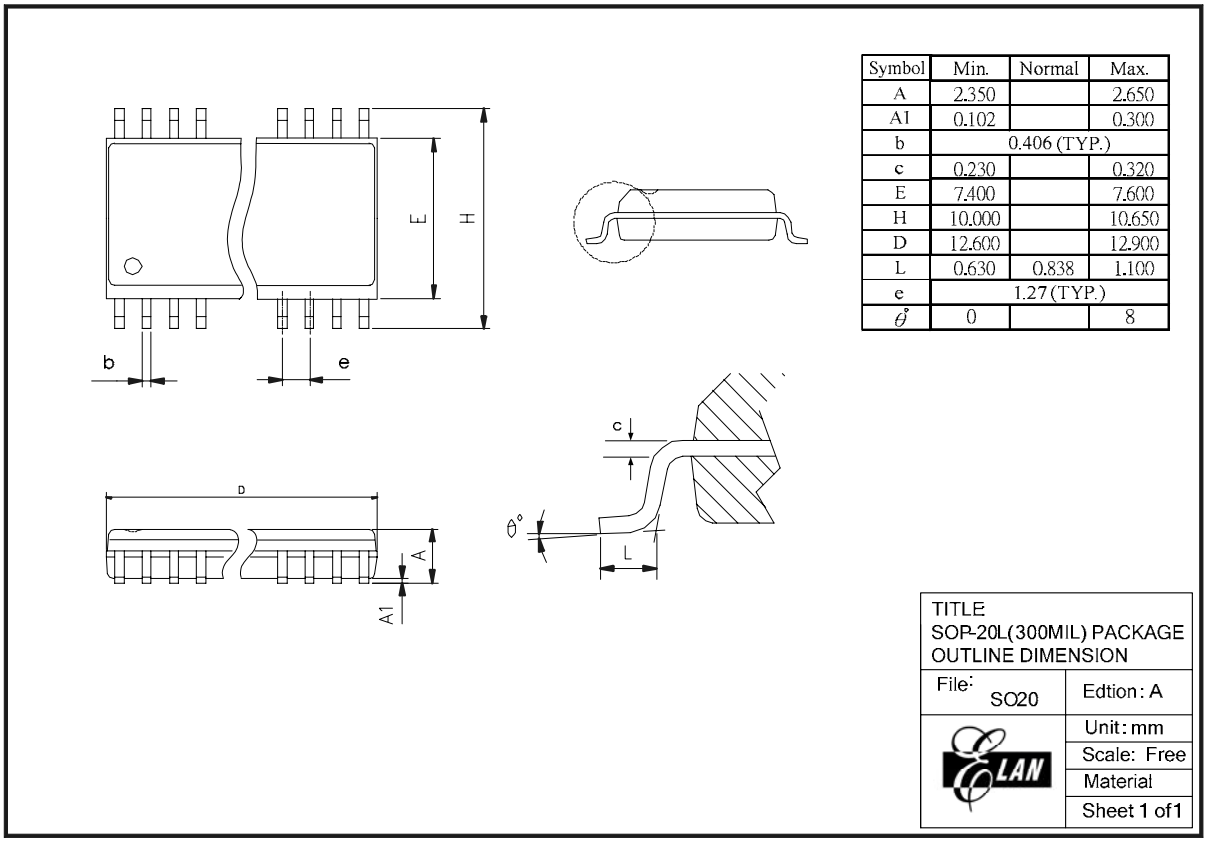


Symbol	Min.	Normal	Max.
A			2.130
A1	0.050		0.250
A2	1.620	1.750	1.880
b	0.220		0.380
c	0.090		0.200
E	7.400	7.800	8.200
E1	5.000	5.300	5.600
D	6.900	7.200	7.500
L	0.650	0.750	0.850
L1	1.250 (REF)		
e	0.650 (TYP)		
θ	0	4	8

TITLE: SSOP-20L (209MIL) PACKAGE OUTLINE DIMENSION	
File: SSOP20	Edtion: A
	Unit: mm
	Scale: Free
	Material
	Sheet 1 of1

Figure B-4 EM78P374N 20-Pin SSOP Package Type

B.5 EM78P374NSO20 300 mil

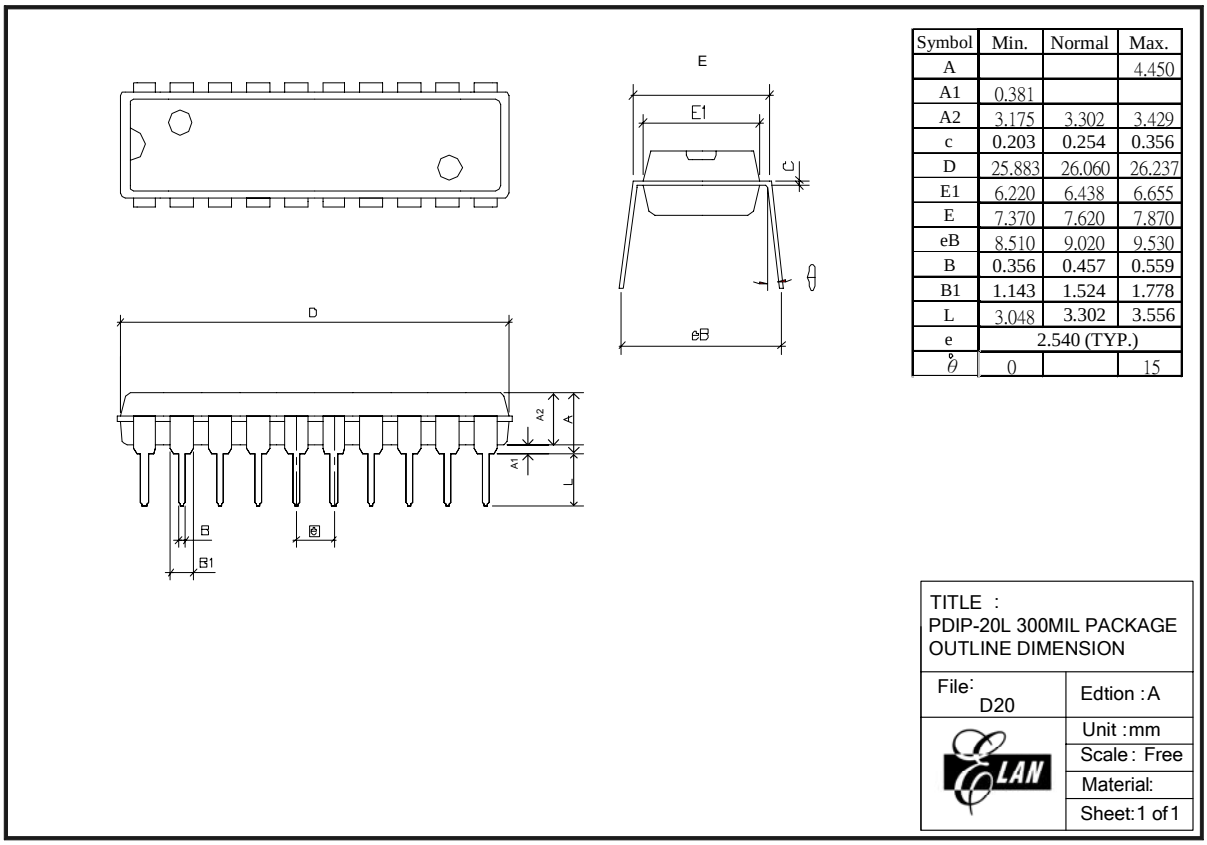


Symbol	Min.	Normal	Max.
A	2.350		2.650
A1	0.102		0.300
b		0.406 (TYP.)	
c	0.230		0.320
E	7.400		7.600
H	10.000		10.650
D	12.600		12.900
L	0.630	0.838	1.100
e		1.27 (TYP.)	
θ°	0		8

TITLE SOP-20L(300MIL) PACKAGE OUTLINE DIMENSION	
File: SO20	Edtion: A
	Unit: mm
	Scale: Free
	Material
	Sheet 1 of1

Figure B-5 EM78P374N 20-Pin SOP Package Type

B.6 EM78P374ND20 300 mil



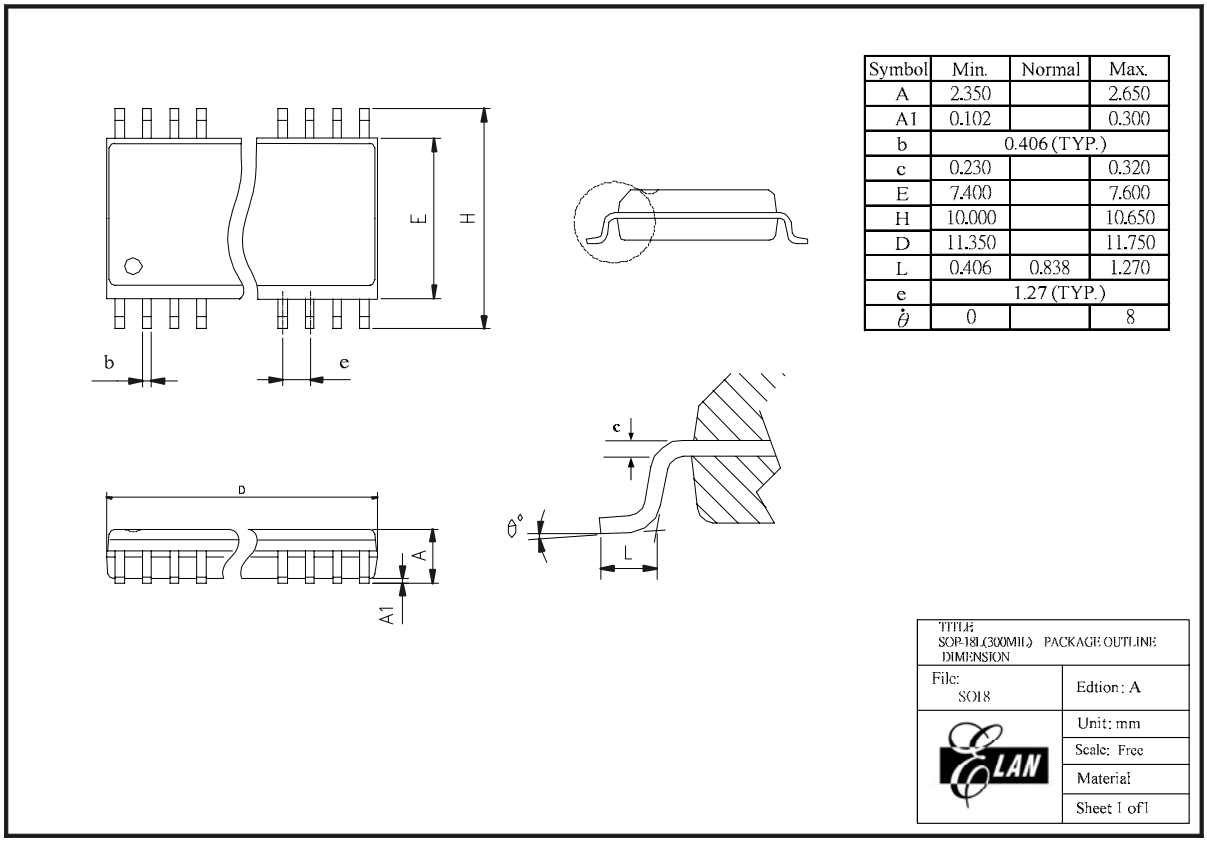
Symbol	Min.	Normal	Max.
A			4.450
A1	0.381		
A2	3.175	3.302	3.429
c	0.203	0.254	0.356
D	25.883	26.060	26.237
E1	6.220	6.438	6.655
E	7.370	7.620	7.870
eB	8.510	9.020	9.530
B	0.356	0.457	0.559
B1	1.143	1.524	1.778
L	3.048	3.302	3.556
e	2.540 (TYP.)		
θ	0		15

TITLE :
PDIP-20L 300MIL PACKAGE OUTLINE DIMENSION

File: D20 | Edtion : A
Unit : mm
Scale : Free
Material:
Sheet: 1 of 1

Figure B-6 EM78P374N 20-Pin PDIP Package Type

B.7 EM78P374NSO18 300 mil

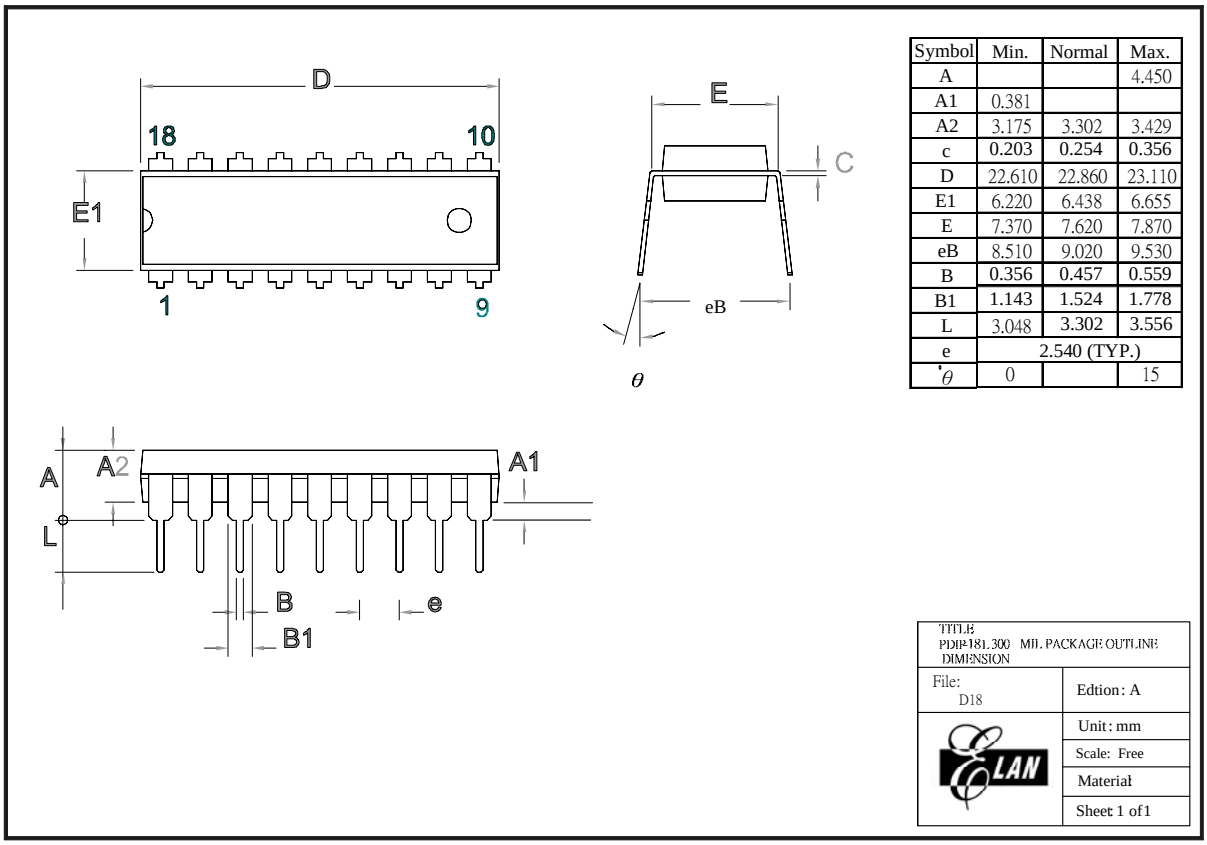


Symbol	Min.	Normal	Max.
A	2.350		2.650
A1	0.102		0.300
b	0.406 (TYP.)		
c	0.230		0.320
E	7.400		7.600
H	10.000		10.650
D	11.350		11.750
L	0.406	0.838	1.270
e	1.27 (TYP.)		
θ	0		8

TITLE: SOP-18L(300MIL) PACKAGE OUTLINE DIMENSION	
File: SO18	Edtion: A
	Unit: mm
	Scale: Free
	Material
	Sheet 1 of1

Figure B-7 EM78P374N 18-Pin SOP Package Type

B.8 EM78P374ND18



Symbol	Min.	Normal	Max.
A			4.450
A1	0.381		
A2	3.175	3.302	3.429
c	0.203	0.254	0.356
D	22.610	22.860	23.110
E1	6.220	6.438	6.655
E	7.370	7.620	7.870
eB	8.510	9.020	9.530
B	0.356	0.457	0.559
B1	1.143	1.524	1.778
L	3.048	3.302	3.556
e	2.540 (TYP.)		
θ	0		15

TITLE
PDIP-18L 300 MIL PACKAGE OUTLINE DIMENSION

File: D18 | Edtion: A

Unit: mm

Scale: Free

Material

Sheet 1 of1

Figure B-8 EM78P374N 18-Pin PDIP Package Type

C Quality Assurance and Reliability

Test Category	Test Conditions	Remarks
Solderability	Solder temperature=245 ± 5°C, for 5 seconds up to the stopper using a rosin-type flux	–
Pre-condition	Step 1: TCT, 65°C (15 min)~150°C (15 min), 10 cycles	For SMD IC (such as SOP, QFP, SOJ, etc)
	Step 2: Bake at 125°C, TD (durance)=24 hrs	
	Step 3: Soak at 30°C / 60% , TD (durance)=192 hrs	
	Step 4: IR flow 3 cycles (Pkg thickness ≥ 2.5 mm or Pkg volume ≥ 350 mm^3 – 225 ± 5°C) (Pkg thickness ≤ 2.5 mm or Pkg volume ≤ 350 mm^3 – 240 ± 5°C)	
Temperature cycle test	-65° (15 min)~150°C (15 min), 200 cycles	–
Pressure cooker test	TA =121°C, RH=100%, pressure=2 atm, TD (durance) = 96 hrs	–
High temperature / High humidity test	TA=85°C , RH=85% , TD (durance)=168 , 500 hrs	–
High-temperature storage life	TA=150°C, TD (durance)=500, 1000 hrs	–
High-temperature operating life	TA=125°C, VCC=Max. operating voltage, TD (durance) =168, 500, 1000 hrs	–
Latch-up	TA=25°C, VCC=Max. operating voltage, 800mA/40V	–
ESD (HBM)	TA=25°C, ≥ | ± 4KV |	IP_ND,OP_ND,IO_ND IP_NS,OP_NS,IO_NS IP_PD,OP_PD,IO_PD, IP_PS,OP_PS,IO_PS, VDD-VSS(+),VDD_VSS (-)mode
ESD (MM)	TA=25°C, ≥ | ± 400V |	

C.1 Address Trap Detect

The Address Trap Detect is one of the MCU embedded fail-safe functions that detects MCU malfunction caused by noise or the like. Whenever the MCU attempts to fetch an instruction from a certain section of ROM, an internal recovery circuit is auto started. If a noise-caused address error is detected, the MCU will repeat execution of the program until the noise is eliminated. The MCU will then continue to execute the next program.