EM78P468NB/P470N

8-Bit Microcontroller

Product Specification

DOC. VERSION 1.2

ELAN MICROELECTRONICS CORP.

November 2012

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APPENDIX

Specification Revision History

Doc. Version	Revision Description	Date
1.0	Initial Release Version	2010/10/11
1.1	1. Modified the contents of the Features 2. Modified the contents of the Pin Description 3. Modified the form of each register in the Function Description 4. Added an LVR function description 5. Modfiied the contents of the Code Option Register 6. Modified the contents of the Instruction Set Table	2011/07/05
1.2	1. Modified the 44-pin package type name 2. Deleted the EM78P468NBQ64A package type on the Features section and other related sections, as well as on the Appendix section.	2012/11/30

1 General Description

The EM78P468NB/P470N is an 8-bit microprocessor designed and developed with low-power and high-speed CMOS technology. It is integrated with Watchdog Timer (WDT), Data RAM, ROM, programmable real time clock counter, internal/external interrupt, power-down mode, LCD driver, infrared transmitter function, and tri-state I/O. The microprocessor is equipped with an on-chip 4K×13-bit Electrical One Time Programmable Read Only Memory (OTP-ROM) and provides multi-protection bits to prevent intrusion of user's OTP memory code. Seven Code option bits are available for user requirements. Special 13 bits customer ID options are provided as well.

With its enhanced OTP-ROM feature, the EM78P468NB/P470N provides a convenient way of developing and verifying user programs. Moreover, this OTP device offers the advantages of easy and effective program updates with development and programming tools. User can take advantage of ELAN's Writer to easily program his development codes.

2 Features

- CPU Configuration:
  - 4K×13 bits on-chip OTP-ROM
  - 144 bytes general purpose register
  - 128 bytes on-chip data RAM
  - 272 bytes SRAM
  - 8 level stacks for subroutine nesting
  - Four programmable Level Voltage Reset (LVR) :4.0V, 3.5V, 2.7V, 1.7V(POR)
- I/O Port Configuration:
  - Typically, 12 bidirectional tri-state I/O ports
  - 16 bidirectional tri-state I/O ports shared with LCD segment output pin
  - Up to 28 bidirectional tri-state I/O ports
- Operating Voltage and Temperature Range:
  - Commercial**:** 2.1V ~ 5.5V (at 0°C ~ +70°C)
  - Industrial**:** 2.3V ~ 5.5V (at -40°C ~ +85°C)
- Operating Mode:
  - Normal Mode**:** The CPU operates on main oscillator frequency (Fm)
  - Green Mode**:** The CPU operates on sub-oscillator frequency (Fs) and the main oscillator (Fm) is stopped
  - Idle Mode**:** CPU is idle, LCD display remains working
  - Sleep Mode**:** The whole chip stops working
  - Input port wake-up function (Port 6, Port 8). Works under Idle and Sleep modes.
  - Operation speed: DC ~ 10 MHz clock input
  - Dual clock operation
- Oscillation Mode:
  - High frequency oscillator can be selected from among Crystal, RC, or PLL (phase lock loop)
  - Low frequency oscillator can select between Crystal and RC modes
- Peripheral Configuration:
  - 8-bit real time clock/counter (TCC)
  - One infrared transmitter / PWM generator
  - Four sets of 8-bit auto reload count-down timers which can be used as interrupt sources**:**
    - ◊ Counter 1**:** Independent count-down timer
    - ◊ Counter 2**:** High Pulse Width Timer (HPWT) and Low Pulse Width Timer (LPWT) shared with IR function.
    - ◊ Programmable free running on-chip Watchdog Timer (WDT). This function operates under Normal, Green, and Idle modes.
- Eight Interrupt Sources: Three External and Five Internal:
  - Internal interrupt source**:** TCC; Counters 1, 2; and High/Low pulse width timer.
  - External interrupt source**:** INT0, INT1, and Pin change wake-up (Port 6 and Port 8)
- LCD Circuit:
  - Common driver pins: 4
  - Segment driver pins: 32
  - LCD Bias: 1/3, 1/2 bias
  - LCD Duty: 1/4, 1/3, 1/2 duty
- Package Type:
  - Dice form: 59 pins
  - QFP 64-pin: EM78P468NBQ64 (14mm×20mm)
  - LQFP 64-pin: EM78P468NBL64 (7mm×7mm)
  - LQFP 44-pin: EM78P470NL44 (10mm×10mm)
  - QFP 44-pin: EM78P470NQ44 (10mm×10mm)

Note: *These are all Green Products which do not contain hazardous substances.*

3 Pin Assignment

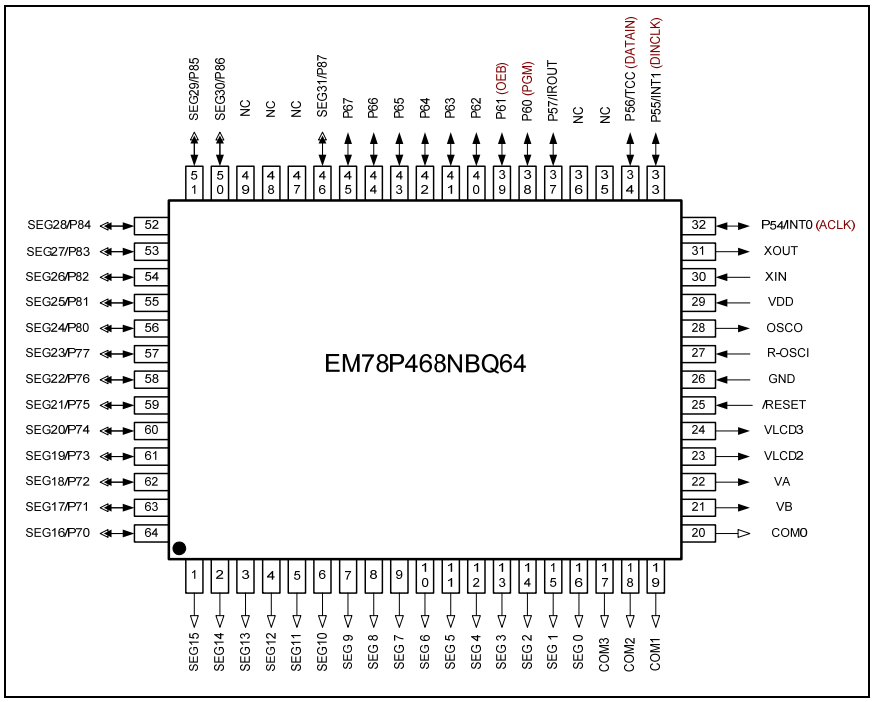


Figure 3-1 64-Pin QFP EM78P468NBQ64 Pin Assignment

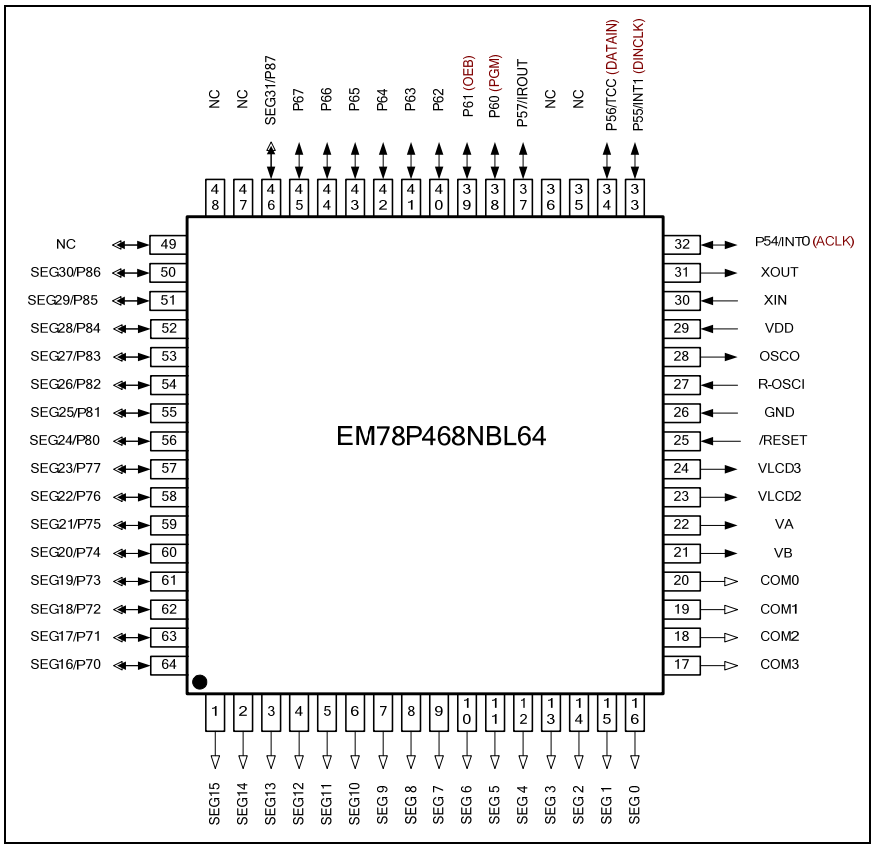


Figure 3-2 64-Pin LQFP EM78P468NBL64 Pin Assignment

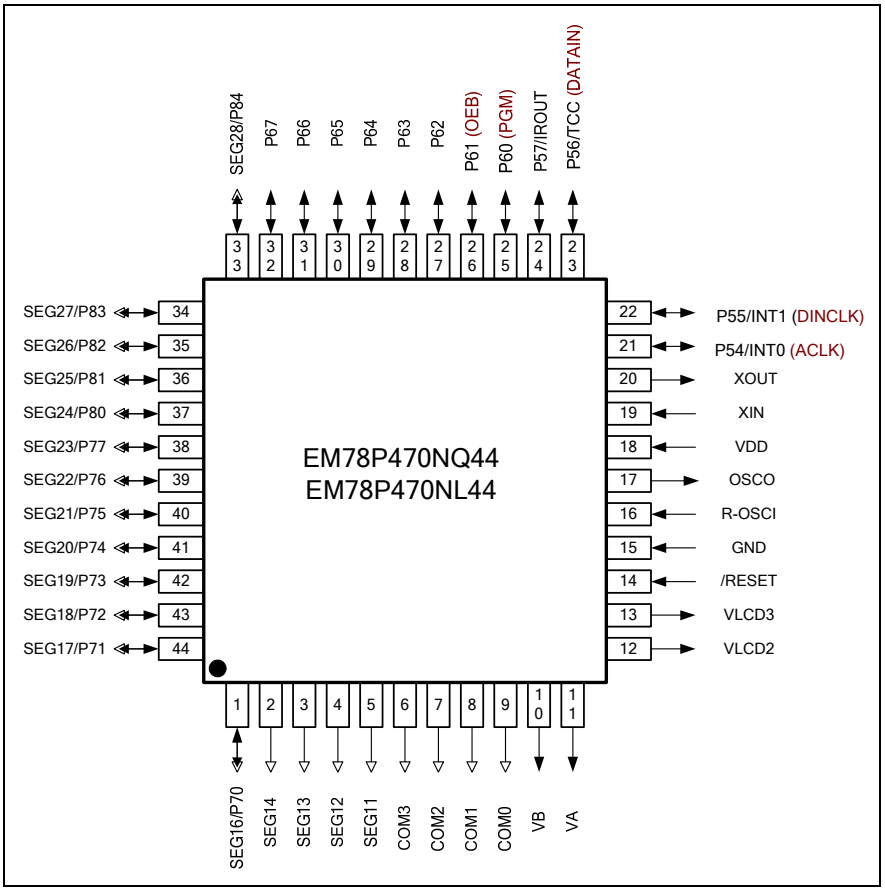
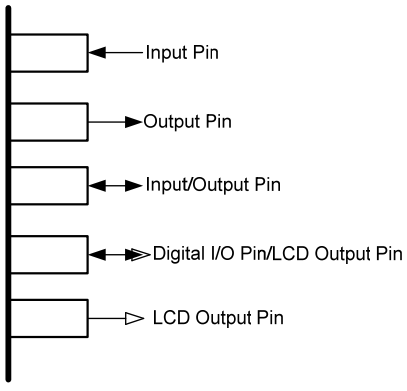


Figure 3-3 44-Pin QFP EM78470NQ44 / LQFP EM78P470NL44 Pin Assignment

Legend: The arrowheads shown on each pin in the above figures stand for the following types of function:



4 Pin Description

4.1 Pin Description

Symbol	Function	Input Type	Output Type	Description
P54/INT0 (ACLK)	P54	ST	CMOS	Bidirectional I/O pin
	INT0	ST	–	External interrupt pin. INT0 interrupt source can be set to falling or rising edge by IOC71 register Bit 7 (INT_EDGE). Wakes up from Sleep mode and Idle mode when the pin status changes.
	(ACLK)	ST	–	ACLK pin for Writer programming
P55/INT1 (DINCK)	P55	ST	CMOS	Bidirectional I/O pin
	INT1	ST	–	External interrupt pin. Interrupt source is a falling edge signal. Wakes up from Sleep mode and Idle mode when the pin status changes.
	(DINCK)	ST	–	DINCK pin for Writer programming
P56/TCC (DATAIN)	P56	ST	CMOS	Bidirectional I/O pin. This pin works in Normal/ Green/Idle mode.
	TCC	ST	–	External input pin of TCC
	(DATAIN)	ST	–	DATAIN pin for Writer programming
P57/IROUT	P57	ST	CMOS	Bidirectional I/O pin. This pin is capable of sinking 20mA/5V.
	IROUT	ST	–	IR/PWM mode output pin
P60 (OEB)	P60	ST	CMOS	Programmable pull-high, pull-down and open-drain. All pins wake up from Sleep and Idle modes when the pin status changes.
	(OEB)	ST	–	OEB pin for Writer programming
P61 (PGM)	P61	ST	CMOS	Programmable pull-high, pull-down and open-drain. All pins wake up from Sleep and Idle modes when the pin status changes
	(PGM)	ST	–	PGM pin for Writer programming
P62	P62	ST	CMOS	Bidirectional I/O pin with programmable pull-high, pull-down and open-drain. All pins wake up from Sleep and Idle modes when the pin status changes
P63	P63	ST	CMOS	Bidirectional I/O pin with programmable pull-high, pull-down and open-drain. All pins wake up from Sleep and Idle modes when the pin status changes

Symbol	Function	Input Type	Output Type	Description
P64	P64	ST	CMOS	Bidirectional I/O pin with programmable pull-high, pull-down and open-drain. All pins wake up from Sleep and Idle modes when the pin status changes
P65	P65	ST	CMOS	Bidirectional I/O pin with programmable pull-high, pull-down and open-drain. All pins wake up from Sleep and Idle modes when the pin status changes
P66	P66	ST	CMOS	Bidirectional I/O pin with programmable pull-high, pull-down and open-drain. All pins wake up from Sleep and Idle modes when the pin status changes
P67	P67	ST	CMOS	Bidirectional I/O pin with programmable pull-high, pull-down and open-drain. All pins wake up from Sleep and Idle modes when the pin status changes
COM3~0	COM3~0	–	AN	LCD common output pin
SEG0~15	SEG0~15	–	AN	LCD segment output pin
SEG16/P70	SEG16	–	AN	LCD segment output pin
	P70	ST	CMOS	Bidirectional I/O pin . All pins wake up from Sleep and Idle modes when the pin status changes
SEG17/P71	SEG17	–	AN	LCD segment output pin
	P71	ST	CMOS	Bidirectional I/O pin . All pins wake up from Sleep and Idle modes when the pin status changes
SEG18/P72	SEG18	–	AN	LCD segment output pin
	P73	ST	CMOS	Bidirectional I/O pin . All pins wake up from Sleep and Idle modes when the pin status changes
SEG19/P73	SEG19	–	AN	LCD segment output pin
	P73	ST	CMOS	Bidirectional I/O pin . All pins wake up from Sleep and Idle modes when the pin status changes
SEG20/P74	SEG20	–	AN	LCD segment output pin
	P74	ST	CMOS	Bidirectional I/O pin . All pins wake up from Sleep and Idle modes when the pin status changes
SEG21/P75	SEG21	–	AN	LCD segment output pin
	P75	ST	CMOS	Bidirectional I/O pin . All pins wake up from Sleep and Idle modes when the pin status changes

Symbol	Function	Input Type	Output Type	Description
SEG22/P76	SEG22	–	AN	LCD segment output pin
	P76	ST	CMOS	Bidirectional I/O pin . All pins wake up from Sleep and Idle modes when the pin status changes
SEG23/P77	SEG23	–	AN	LCD segment output pin
	P77	ST	CMOS	Bidirectional I/O pin . All pins wake up from Sleep and Idle modes when the pin status changes
SEG24/P80	SEG24	–	AN	LCD segment output pin
	P80	ST	CMOS	Bidirectional I/O pin with programmable pull-high. All pins wake up from Sleep and Idle modes when the pin status changes
SEG25/P81	SEG25	–	AN	LCD segment output pin
	P81	ST	CMOS	Bidirectional I/O pin with programmable pull-high. All pins wake up from Sleep and Idle modes when the pin status changes
SEG26/P82	SEG26	–	AN	LCD segment output pin
	P82	ST	CMOS	Bidirectional I/O pin with programmable pull-high. All pins wake up from Sleep and Idle modes when the pin status changes
SEG27/P83	SEG27	–	AN	LCD segment output pin
	P83	ST	CMOS	Bidirectional I/O pin with programmable pull-high. All pins wake up from Sleep and Idle modes when the pin status changes
SEG28/P84	SEG28	–	AN	LCD segment output pin
	P84	ST	CMOS	Bidirectional I/O pin with programmable pull-high. All pins wake up from Sleep and Idle modes when the pin status changes
SEG29/P85	SEG29	–	AN	LCD segment output pin
	P85	ST	CMOS	Bidirectional I/O pin with programmable pull-high. All pins wake up from Sleep and Idle modes when the pin status changes
SEG30/P86	SEG30	–	AN	LCD segment output pin
	P86	ST	CMOS	Bidirectional I/O pin with programmable pull-high. All pins wake up from Sleep and Idle modes when the pin status changes
SEG31/P87	SEG31	–	AN	LCD segment output pin
	P87	ST	CMOS	Bidirectional I/O pin with programmable pull-high. All pins wake up from Sleep and Idle modes when the pin status changes

Symbol	Function	Input Type	Output Type	Description
VB	VB	–	AN	Connects capacitors for LCD bias voltage
VA	VA	–	AN	Connects capacitors for LCD bias voltage
VLCD2	VLCD2	–	AN	One of LCD bias voltage
VLCD3	VLCD3	–	AN	One of LCD bias voltage
/RESET (VPP)	/RESET	ST	–	General-purpose Input only Low active. If it remains at logic low, the device will reset. /RESET pin for writer programming
	VPP	ST	–	Vpp pin for Writer programming
R-OSCI	R-OSCI	AN	–	In Crystal mode: crystal input In RC mode: resistor pull high In PLL mode: connect a 0.01μF capacitance to GND Connect a 0.01 μF capacitor to GND and code option selects PLL mode when high oscillator is not used.
OSCO	OSCO	–	XTAL	In Crystal mode: crystal input In RC mode: instruction clock output
Xin	Xin	XTAL	–	In Crystal mode: Input pin for sub-oscillator. Connect to a 32.768kHz crystal.
Xout	Xout	–	XTAL	In Crystal mode: Connect to a 32.768kHz crystal. In RC mode: instruction clock output
NC	NC	–	–	No connection
VDD	VDD	Power	–	Power
GND	GND	Power	–	Ground

Legend: *ST: Schmitt Trigger input* *CMOS: CMOS output*
AN: analog pin *XTAL: oscillation pin for crystal / resonator*

Pin Status with Enabled Functions

Pin Function	I/O Status		Pin Control		
	I/O Direction	Pin Change WK/Int.	Pull High	Pull Low	O.D.
General Input	Input	S/W	S/W	S/W	S/W
General Output	Output	Disable	S/W	S/W	S/W
TCC	Input	Disable	S/W	S/W	S/W
LCD Driver	Input	Disable	Disable	Disable	S/W
TC-OUT	Output	Disable	Init: Enable	S/W	S/W
Reset	Input	Disable	S/W	S/W	S/W
EX_INT	Input	Disable	S/W	S/W	S/W
OSCI	Input	Disable	Disable	Disable	S/W
OSCO	Input	Disable	Disable	Disable	S/W

NOTE

Disable: *→ It is always disabled*

Enable: *→ It is always enabled*

S/W: *→ It can be controlled by register. The initial status is disabled.*

1. If the pin is not working as general I/O, it is a must to disable the Pin Change Wake-up/Interrupt function.

2. Priority: Digital function output > digital function input > general I/O

5 Block Diagram

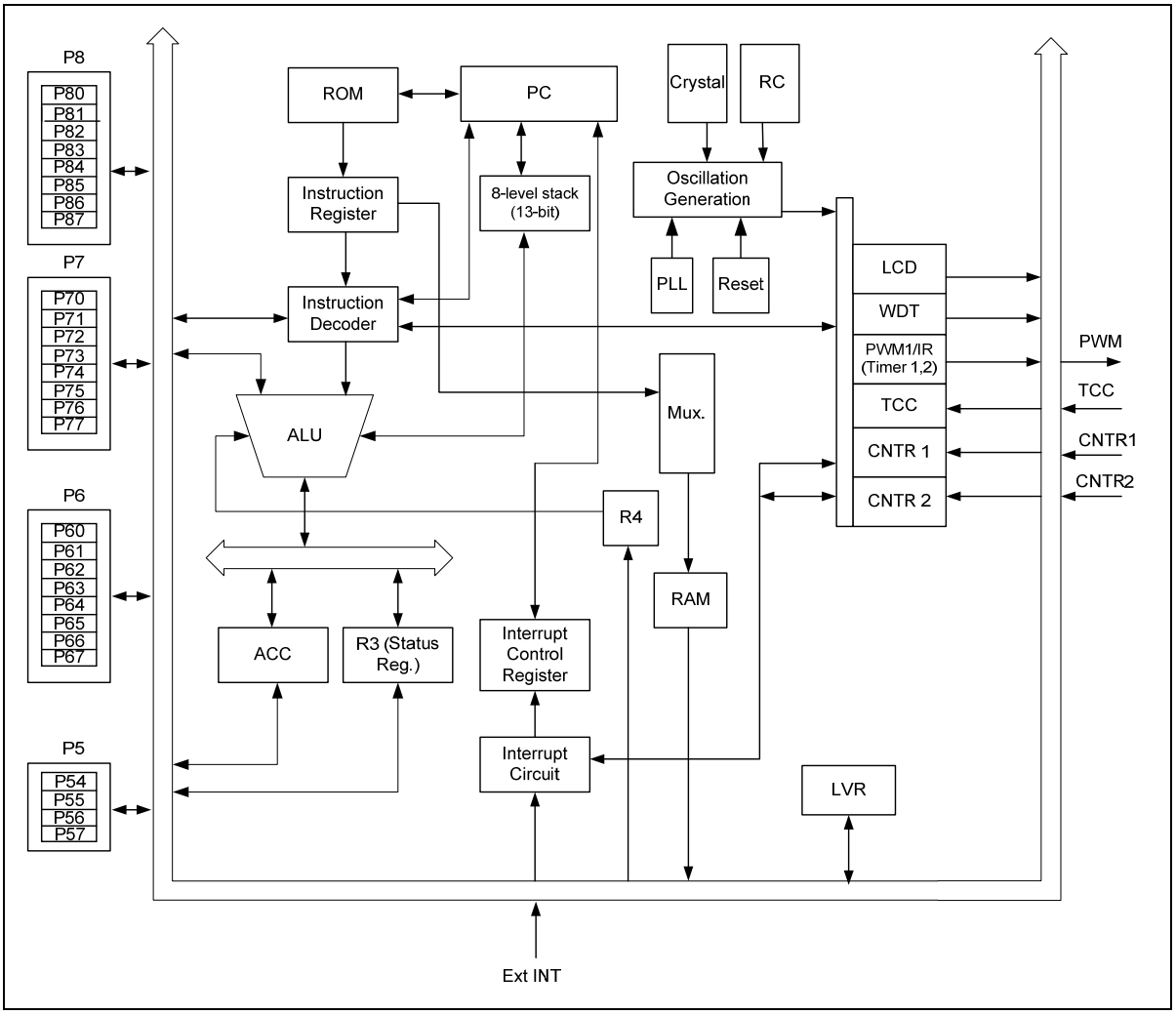


Figure 5-1 System Block Diagram

6 Functional Description

6.1 Operational Registers

6.1.1 R0/IAR (Indirect Addressing Register – Address: 00h)

R0 is not a physically implemented register. Its major function is to perform as an indirect address pointer. Any instruction that uses R0 as a register, actually accesses the data pointed by the RAM Select Register (R4).

6.1.2 R1/TCC (Timer Clock Counter – Address: 01h)

The Timer Clock Counter is incremented by an external signal edge applied to TCC, or by the instruction cycle clock. It is written and read by the program as any other register.

6.1.3 R2/PC (Program Counter – Address: 02h)

- The R2 structure is depicted in Figure 6-1 shown below.

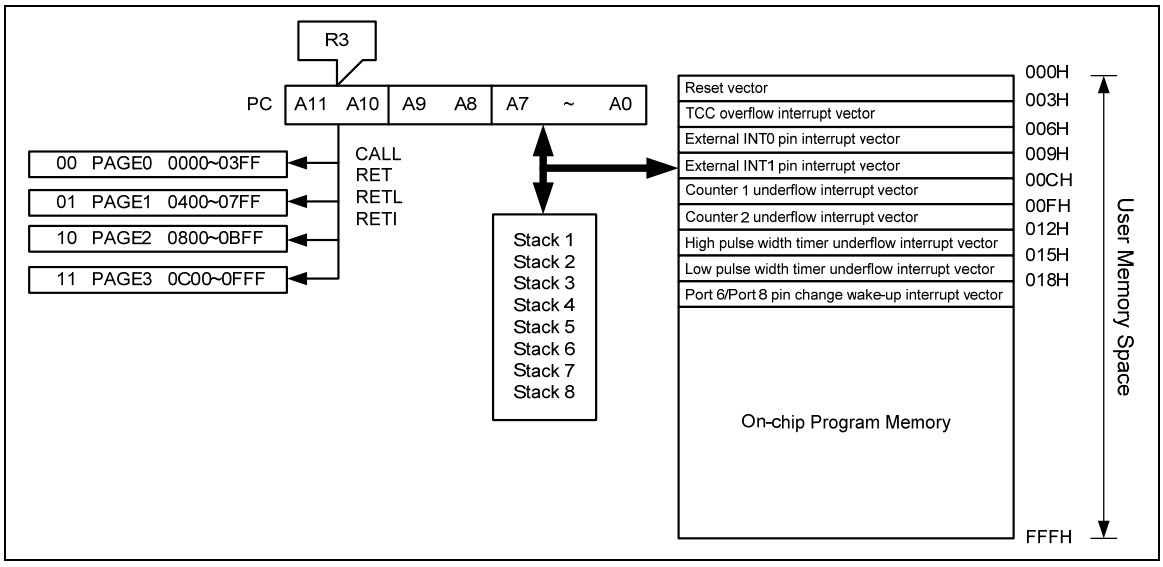


Figure 6-1 Program Counter Organization

- The configuration structure generates 4K×13 bits on-chip ROM addresses to the relative programming instruction codes.
- The contents of R2 are all set to "**0**"s when a Reset condition occurs.
- "JMP" instruction allows direct loading of the lower 10 program counter bits. Thus, "JMP" allows the PC to jump to any location within a page.
- "CALL" instruction loads the lower 10 bits of the PC, and PC+1 are pushed onto the stack. Thus, the subroutine entry address can be located anywhere within a page.

- "RET" ("RETL k", "RETI") instruction loads the program counter with the contents of the top-level stack.
- "ADD R2, A" allows a relative address to be added to the current PC, and the ninth and above bits of the PC will increase progressively.
- "MOV R2, A" allows loading of an address from the "A" register to the lower 8 bits of the PC, and the ninth and tenth bits (A8 ~ A9) of the PC remain unchanged.
- The most significant bits (A10~A11) are loaded with the contents of PS0~PS1 into the Status Register (R3) upon execution of a "JMP" or "CALL" instruction.

6.1.3.1 Data Memory Configuration

ADDRESS	SBANK0	SBANK1	IOCPAGE0	IOCPAGE1
00	R0			
01	R1 (TCC)			
02	R2 (PC)			
03	R3 (Status & ROM page)			
04	R4 (RAM selection)			
05	R5 (Port 5 & IOC page)	R5 (TBRDH)	IOC50 (Port 5 IO control)	IOC51 (unused)
06	R6 (Port 6)	R6 (TBRDL)	IOC60 (Port 6 IO control)	IOC61 (Wake-up register)
07	R7 (Port 7)		IOC 70 (Port 7 IO control)	IOC71 (TCC control)
08	R8 (Port 8)		IOC80 (Port 8 IO control)	IOC81 (WDT control)
09	R9 (LCD control)		IOC90 (RAM Address)	IOC91 (CNT1/2 control)
0A	RA (LCD contrast & addr.)		IOCA0 (RAM Data)	IOCA1 (H/L pulse time control)
0B	RB (LCD data)		IOCB0 (CNT1 preset)	IOCB1 (Port 6 pull-high)
0C	RC (Counter enable reg.)		IOCC0 (CNT2 preset)	IOCC1 (Port 6 open-drain)
0D	RD (System Clock control)		IOCD0 (High pulse timer preset)	IOCD1 (Port 8 pull-high)
0E	RE (IR control)		IOCE0 (Low pulse timer preset)	IOCE1 (Port 6 pull down)
0F	RF (Interrupt status)		IOCF0 (interrupt mask)	IOCF1 (unused)
10 | 1F	16 byte common register			
20 | 3F	Bank 0 32 byte common register	Bank 1 32 byte common register	Bank 2 32 byte common register	Bank 3 32 byte common register

Figure 6-2 Data Memory Configuration

6.1.4 R3/SR (Status Register)

(Address: 03h)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	PS1	PS0	T	P	Z	DC	C
	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7: Unused bit

Bits 6 ~ 5 (PS1 ~ PS0): Page select bits

PS1	PS0	ROM Page (Address)
0	0	Page 0 (000H ~ 3FFH)
0	1	Page 1 (400H ~ 7FFH)
1	0	Page 2 (800H ~ BFFH)
1	1	Page 3 (C00H ~ FFFH)

PS0~PS1 are used to select a ROM page. You can use the “PAGE” instruction (e.g., “PAGE 1”) or set PS1~PS0 bits to change the ROM page. When executing a "JMP", "CALL", or other instructions which causes the program counter to be changed (e.g., “MOV R2, A”), the PS0~PS1 are loaded into the 11th and 12th bits of the program counter where it selects one of the available program memory pages. Note that “RET” (“RETL”, “RETI”) instruction does not change the PS0~PS1 bits. That is, the return will always be to the page from where the subroutine was called, regardless of the current setting of PS0~PS1 bits.

Bit 4 (T): Time-out bit. Set to “**1**” by the "SLEP" and "WDTC" commands or during power up and reset to “**0**” by WDT timeout.

Event	T	P	Remark
WDT wake-up from Sleep mode	0	0	–
WDT time out (not Sleep mode)	0	1	–
/RESET wake-up from Sleep	1	0	–
Power up	1	1	–
Low pulse on /RESET	1	1	×: don't care

Bit 3 (P): Power down bit. Set to “**1**” during power on or by a "WDTC" command and reset to “**0**” by a "SLEP" command.

Bit 2 (Z): Zero flag

Bit 1 (DC): Auxiliary carry flag

Bit 0 (C): Carry flag

6.1.5 R4/RSR (RAM Select Register)

(Address: 04h)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RBS1	RBS0	RSR5	RSR4	RSR3	RSR2	RSR1	RSR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7 ~ 6 (RBS1 ~ RBS0): Determine which bank among the four banks, is activated (see the data memory configuration in Figure 6-2. Use the "BANK" instruction (e.g., "Bank 1") to change banks.

Bits 5 ~ 0 (RSR5 ~ RSR0): Used to select up to 64 registers (Address: 00~3F) under indirect addressing mode. If no indirect addressing is used, the RSR is used as an 8-bit general purpose read/writer register.

6.1.6 SBANK0 R5/Port 5 (Port 5 I/O Data and Page of Register Selection)

(Address: 05h)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P57	P56	P55	P54	-	-	-	IOCPAGE
R/W	R/W	R/W	R/W	-	-	-	R/W

Bits 7 ~ 4 (P57 ~ P54):4-bit I/O registers of Port 5. Use the IOC50 register to define each bit either as input or output.

Bits 3 ~ 1: Unused bits

Bit 0 (IOCPAGE): Switch Registers IOC5 ~ IOCF to another page

IOCPAGE = **"0":** Page 0 (Registers IOC 50 to IOC F0) selected

IOCPAGE = **"1":** Page 1 (Registers IOC 51 to IOC F1) selected

6.1.7 SBANK0 R6/Port 6 (Port 6 I/O Data Register)

(Address: 06h)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P67	P66	P65	P64	P63	P62	P61	P60
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7 ~ 0 (P67 ~ P60): 8-bit I/O registers of Port 6. Use the IOC60 register to define each bit either as input or output.

6.1.8 SBANK0 R7/Port 7 (Port 7 I/O Data Register)

(Address: 07h)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P77	P76	P75	P74	P73	P72	P71	P70
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7 ~ 0 (P77 ~ P70): 8-bit I/O registers of Port 7. Use the IOC70 register to define each bit either as input or output.

6.1.9 SBANK0 R8/Port 8 (Port 8 I/O Data Register)

(Address: 08h)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P87	P86	P85	P84	P83	P82	P81	P80
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7 ~ 0 (P87 ~ P80): 8-bit I/O registers of Port 8. Use IOC80 register to define each bit either as input or output.

6.1.10 SBANK0 R9/LCDCR (LCD Control Register)

(Address: 09h)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BS	DS1	DS0	LCDEN	-	LCDTYPE	LCDF1	LCDF0
R/W	R/W	R/W	R/W	-	R/W	R/W	R/W

Bit 7 (BS): LCD bias select bit

BS = **"0":** 1/2 bias

BS = **"1":** 1/3 bias

Bit 6 ~ 5 (DS1 ~ DS0): LCD duty select

DS1	DS0	LCD Duty
0	0	1/2 duty
0	1	1/3 duty
1	×	1/4 duty

Bit 4 (LCDEN): LCD enable bit

LCDEN = **"0":** LCD circuit disabled. All common/segment outputs are set to ground (GND) level.

LCDEN = **"1":** LCD circuit enabled

Bit 3: Unused bit

Bit 2 (LCDTYPE): LCD drive waveform type select bit

LCDTYPE = **"0":** A type waveform

LCDTYPE = **"1":** B type waveform

Bits 1 ~ 0 (LCDF1 ~ LCDF0): LCD frame frequency control bits

LCDF1	LCDF0	LCD Frame Frequency (e.g., Fs=32.768kHz)		
		1/2 Duty	1/3 Duty	1/4 Duty
0	0	Fs/(256×2)=64.0	Fs/(172×3)=63.5	Fs/(128×4)=64.0
0	1	Fs/(280×2)=58.5	Fs/(188×3)=58.0	Fs/(140×4)=58.5
1	0	Fs/(304×2)=53.9	Fs/(204×3)=53.5	Fs/(152×4)=53.9
1	1	Fs/(232×2)=70.6	Fs/(156×3)=70.0	Fs/(116×4)=70.6

Fs: *sub-oscillator frequency*

6.1.11 SBANK0 RA/LCD_ADDR (LCD Address)

(Address: 0Ah)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	LCD_A4	LCD_A3	LCD_A2	LCD_A1	LCD_A0
-	-	-	R/W	R/W	R/W	R/W	R/W

Bits 7 ~ 5: Unused bits

Bits 4 ~ 0 (LCDA4 ~ LCDA0): LCD RAM addresses

RA (LCD Address)	RB (LCD Data Buffer)					Segment
	Bits 7 ~4	Bit 3 (LCD_D3)	Bit 2 (LCD_D2)	Bit 1 (LCD_D1)	Bit 0 (LCD_D0)	
00H	–	–	–	–	–	**SEG0**
01H	–	–	–	–	–	**SEG1**
02H	–	–	–	–	–	**SEG2**
|			|			|
1DH	–	–	–	–	–	**SEG29**
1EH	–	–	–	–	–	**SEG30**
1FH	–	–	–	–	–	**SEG31**
Common	×	**COM3**	**COM2**	**COM1**	**COM0**	

6.1.12 SBANK0 RB/LCD_DB (LCD Data Buffer)

(Address: 0Bh)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	LCD_D3	LCD_D2	LCD_D1	LCD_D0
-	-	-	-	R/W	R/W	R/W	R/W

Bits 7 ~ 4: Unused bits

Bits 3 ~ 0 (LCD_D3 ~ LCD_D0): LCD RAM data transfer register

6.1.13 SBANK0 RC/CNTER (Counter Enable Register)

(Address: 0Ch)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	LPWTEN	HPWTEN	CNT2EN	CNT1EN
-	-	-	-	R/W	R/W	R/W	R/W

Bits 7 ~ 4: Unused bits

Bit 3 (LPWTEN): Low pulse width timer enable bit

LPWTEN = **"0":** Disable LPWT. Stop counting operation.

LPWTEN = **"1":** Enable LPWT. Start counting operation.

Bit 2 (HPWTEN): High pulse width timer enable bit

HPWTEN = **"0":** Disable HPWT. Stop counting operation.

HPWTEN = **"1":** Enable HPWT. Start counting operation.

Bit 1 (CNT2EN): Counter 2 enable bit

CNT2EN = **"0":** Disable Counter 2. Stop counting operation.

CNT2EN = **"1":** Enable Counter 2. Start counting operation.

Bit 0 (CNT1EN): Counter 1 enable bit

CNT1EN = **"0":** Disable Counter 1. Stop counting operation.

CNT1EN = **"1":** Enable Counter 1. Start counting operation.

6.1.14 SBANK0 RD/SBPCR (System, Booster and PLL Control Register)

(Address: 0Dh)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SBANK	CLK2	CLK1	CLK0	IDLE	BF1	BF0	CPUS
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7 (SBANK): Special Register 0x05 ~ 0x06 bank select bit

0: SBANK 0

1: SBANK 1

Bits 6 ~ 4 (CLK2 ~ CLK0): Main clock select bits for PLL mode (code option select)

CLK2	CLK1	CLK0	Main Clock	Example Fs=32.768K
0	0	0	Fs×130	4.26 MHz
0	0	1	Fs×65	2.13 MHz
0	1	0	Fs×65/2	1.065 MHz
0	1	1	Fs×65/4	532kHz
1	×	×	Fs×244	8 MHz

Bit 3 (IDLE): Idle mode enable bit. This bit determines the intended mode of the SLEP instruction.

Idle = **"0"**+SLEP instruction → Sleep mode

Idle = **"1"**+SLEP instruction → Idle mode

NOTE

NOP *instruction must be added after SLEP instruction.*

Example: *Idle mode: Idle bit = "1" +SLEP instruction + NOP instruction*

Sleep mode: Idle bit = "0" +SLEP instruction + NOP instruction

Bits 2, 1 (BF1, BF0): LCD booster frequency select bits to adjust VLCD 2, 3 driving.

BF1	BF0	Booster Frequency
0	0	Fs
0	1	Fs/4
1	0	Fs/8
1	1	Fs/16

Bit 0 (CPUS): CPU oscillator source select. When CPUS=0, the CPU oscillator selects the Sub-oscillator and the Main oscillator is stopped.

CPUS = **"0":** Sub-oscillator (Fs) is selected

CPUS = **"1":** Main oscillator (Fm) is selected

■ CPU Operation Mode

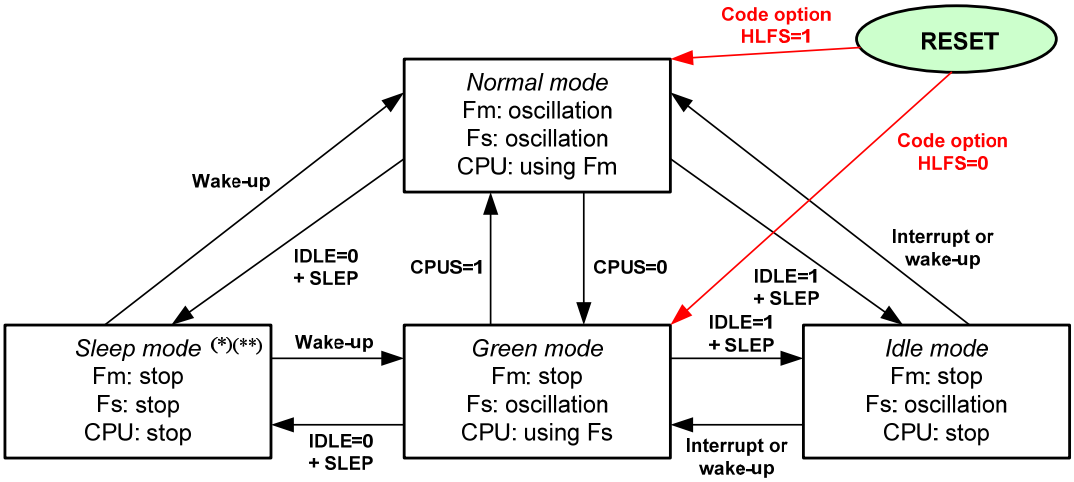


Figure 6-3 CPU Operation Mode

Note

(*) *If the watchdog function is enabled before going into sleep mode, some circuits like the timer (its clock source is Fs) must stop counting.*

If the watchdog function is enabled before going into sleep mode, some circuits like timer (its clock source is the external pin) can still count and its interrupt flag can be active at matching condition as corresponding interrupt is enabled. But the CPU cannot be waken-up by this event.

(**)

Switching Operation Mode at Sleep → Normal, Green → Normal:

If the clock source of timer is Fm, the timer/counter must stop counting at sleep or green mode. Then, the timer can continue to count until the clock source is stable at normal mode. That clock source is stable means the CPU starts to work at normal mode.

Switching Operation Mode at Sleep → Green:

If the clock source of timer is Fs, the timer must stop counting at sleep mode. Then, the timer can continue to count until the clock source is stable at green mode. That clock source is stable means the CPU starts to work at green mode.

Switching Operation Mode at Sleep → Normal:

If the clock source of the timer is Fs, the timer must stop counting at sleep mode. Then, the timer can continue to count until clock source is stable at normal mode. That clock source is stable means the CPU starts to work at normal mode.

Fmain	Fsub	Power-on LVR	Pin-Reset WDT	
			N / G / I	S
IRC	IRC	16ms + WSTO + 8*1/Fmain	WSTO + 8*1/Fmain	WSTO + 8*1/Fmain
	XT	16ms + WSTO + 510*1/Fsub	WSTO + 8*1/Fmain	WSTO + 510*1/Fsub
XT	IRC	16ms + WSTO + 510*1/Fmain	WSTO + 510*1/Fmain	WSTO + 510*1/Fmain
	XT	16ms + WSTO + 510*1/Fsub	WSTO + 510*1/Fmain	WSTO + 510*1/Fsub

Fmain	Fsub	G → N	I → N	S → N
IRC	IRC	WSTO + 8*1/Fmain	WSTO + 8*1/Fmain	WSTO + 8*1/Fmain
	XT	WSTO + 8*1/Fmain	WSTO + 8*1/Fmain	WSTO + 510*1/Fsub
XT	IRC	WSTO + 510*1/Fmain	WSTO + 510*1/Fmain	WSTO + 510*1/Fmain
	XT	WSTO + 510*1/Fmain	WSTO + 510*1/Fmain	WSTO + 510*1/Fsub

Fmain	Fsub	I → G	S → G
IRC	IRC	WSTO + 8*1/Fsub	WSTO + 8*1/Fsub
	XT	WSTO + 8*1/Fsub	WSTO + 510*1/Fsub
XT	IRC	WSTO + 8*1/Fsub	WSTO + 8*1/Fsub
	XT	WSTO + 8*1/Fsub	WSTO + 510*1/Fsub

WSTO: *Waiting Time from Start-to-Oscillation*

N: *Normal mode* ***G:*** *Green mode* ***I:*** *Idle mode* ***S:*** *Sleep mode*

6.1.15 SBANK0 RE/IRCR (IR Control Register)

(Address: 0Eh)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IRE	HF	LGP	-	IROUTE	TCCE	EINT1	EINT0
R/W	R/W	R/W	-	R/W	R/W	R/W	R/W

Bit 7 (IRE): Infrared Remote Enable bit

IRE = **"0":** Disable the IR/PWM function. The state of P5.7/IROUT pin is determined by Bit 7 of IOC 50 if it is used as IROUT.

IRE = **"1":** Enable IR or PWM function.

Bit 6 (HF): High carry frequency

HF = **"0":** For PWM application, disable the H/W modulator function. The IROUT waveform is generated according to high-pulse and low-pulse time as determined by the respective high pulse and low pulse width timers. Counter 2 is an independent auto reload timer.

HF = **"1":** For IR application mode, enable the H/W modulator function. The low time section of the generated pulse is modulated with the Fcarrier frequency. The Fcarrier frequency is provided by Counter 2.

Bit 5 (LGP): IROUT for low pulse width timer

LGP = **"0":** Both high-pulse width timer register and low-pulse width timer are valid.

LGP = **"1":** The high-pulse width timer register is ignored. So the IROUT waveform is dependent on the low-pulse width timer register only.

Bit 4: Unused bit

Bit 3 (IROUTE): Defines the function of the P57/IROUT pin

IROUTE = **"0":** Defined as bidirectional general I/O pin

IROUTE = **"1":** Defined as IR or PWM output pin. The P57 control bit (Bit 7 of IOC50) must be set to **"0."**

Bit 2 (TCCE): Defines the function of the P56/TCC pin.

TCCE = **"0":** Defined as bidirectional general I/O pin

TCCE = **"1":** Defined as external input pin of TCC. The P56 control bit (Bit 6 of IOC50) must be set to **"1."**

Bit 1 (EINT1): Defines the function of the P55/INT1 pin.

EINT1 = **"0":** Defined as bidirectional general I/O pin.

EINT1 = **"1":** Define as external interrupt pin of INT1. The P55 control bit (Bit 5 of IOC50) must be set to **"1."**

Bit 0 (EINT0): Defines the function of the P54/INT0 pin.

EINT0 = **"0":** Defined as bidirectional general I/O pin.

EINT0 = **"1":** Defined as external interrupt pin of INT0. The P54 control bit (Bit 4 of IOC50) must be set to **"1."**

6.1.16 SBANK0 RF/ISR (Interrupt Status Register)

(Address: 0Fh)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ICIF	LPWTF	HPWTF	CNT2F	CNT1F	INT1F	INT0F	TCIF
F	F	F	F	F	F	F	F

These bits are set to "**1**" when interrupt occurs respectively.

Bit 7 (ICIF): Port 6 and Port 8 input status change interrupt flag. Set when Port 6 and Port 8 input status changes.

Bit 6 (LPWTF): Interrupt flag of the internal low-pulse width timer underflows.

Bit 5 (HPWTF): Interrupt flag of the internal high-pulse width timer underflows.

Bit 4 (CNT2F): Interrupt flag of the internal Counter 2 underflows.

Bit 3 (CNT1F): Interrupt flag of the internal Counter 1 underflows.

Bit 2 (INT1F): External INT1 pin interrupt flag

Bit 1 (INT0F): External INT0 pin interrupt flag

Bit 0 (TCIF): TCC timer overflow interrupt flag. Set when TCC timer overflows.

6.1.17 SBANK1 R5/TBRDH (TBRD High Address)

(Address: 05h)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
HLB	-	-	-	RBit11	RBit10	RBit9	RBit8
R/W	-	-	-	R/W	R/W	R/W	R/W

Bit 7 (HLB): Take MLB or LSB at machine code

HLB = **"0":** low 8 bits machine code

HLB = **"1":** low 5 bits machine code

Bits 6 ~ 4: Not used

Bits 3 ~ 0 (RBit11 ~ RBit8): program ROM high address.

6.1.18 SBANK1 R6/TBRDL (TBRD Low Address)

(Address: 06h)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RBit7	RBit6	RBit5	RBit4	RBit3	RBit2	RBit1	RBit0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7 ~ 0 (RBit7~RBit0): Program ROM low address.

6.1.19 General Purpose Register (Address: 10h~3Fh; R10~R3F)

R10~R1F and R20~R3F (Banks 0~3) are general purpose registers.

6.2 Special Purpose Register

6.2.1 A (Accumulator)

Internal data transfer operation, or instruction operand holding usually involves the temporary storage function of the Accumulator, which is not an addressable register.

6.2.2 IOC Page 0 (IOC50 ~ IOCF0, Bit 0 of R5 = "0")

6.2.2.1 IOC50/P5CR (Port 5 I/O and Ports 7, 8 for LCD Segment Control Register)

(Address: 05h, Bit 0 of R5 = "0")

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IOC57	IOC56	IOC55	IOC54	P8HS	P8LS	P7HS	P7LS
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7 ~ 4 (IOC57 ~ 54): Port 5 I/O direction control register

IOC5x = **"0":** Set the relative P5x I/O pins as output

IOC5x = **"1":** Set the relative P5x I/O pin into high impedance (input pin)

Bit 3 (P8HS): Switch to high nibble I/O of Port 8 or to LCD segment output while sharing pins with SEGxx/P8x pins.

P8HS = **"0":** Select high nibble of Port 8 as normal P84~P87

P8HS = **"1":** Select LCD segment output as SEG 28~SEG 31 output

Bit 2 (P8LS): Switch to low nibble I/O of Port 8 or to LCD segment output while sharing pins with SEGxx/P8.x pins.

P8LS = **"0":** Select low nibble of Port 8 as normal P80~P83

P8LS = **"1":** Select LCD Segment output as SEG 24~SEG 27 output

Bit 1 (P7HS): Switch to high nibble I/O of Port 7 or to LCD segment output while sharing pins with SEGxx/P7x pins.

P7HS = **"0":** Select high nibble of Port 7 as normal P74~P77

P7HS = **"1":** Select LCD Segment output as SEG 20~SEG 23 output

Bit 0 (P7LS): Switch to low nibble I/O of Port 7 or to LCD segment output while sharing pins with SEGxx/P7x pins.

P7LS = **"0":** Select low nibble of Port 7 as normal P70~P73

P7LS = **"1":** Select LCD segment output as SEG 16~SEG 19 output

6.2.2.2 IOC60/P6CR (Port 6 I/O Control Register)

(Address: 06h, Bit 0 of R5 = "0")

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IOC67	IOC66	IOC65	IOC64	IOC63	IOC62	IOC61	IOC60
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7 ~ 4 (IOC67 ~ IOC60): Port 6 I/O direction control register

IOC6x = "0": Set the relative Port 6x I/O pins as output

IOC6x = "1": Set the relative Port 6x I/O pin into high impedance (input pin)

6.2.2.3 IOC70/P7CR (Port 7 I/O Control Register)

(Address: 07h, Bit 0 of R5 = "0")

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IOC77	IOC76	IOC75	IOC74	IOC73	IOC72	IOC71	IOC70
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7 ~ 0 (IOC77 ~ IOC70): Port 7 I/O direction control register

IOC7x = "0": Set the relative Port 7x I/O pins as output

IOC7x = "1": Set the relative Port 7x I/O pin into high impedance (input pin)

6.2.2.4 IOC80/P8CR (Port 8 I/O Control Register)

(Address: 08h, Bit 0 of R5 = "0")

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IOC87	IOC86	IOC85	IOC84	IOC83	IOC82	IOC81	IOC80
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7 ~ 0 (IOC 87 ~ IOC 80): Port 8 I/O direction control register

IOC8x = "0": Set the relative Port 8x I/O pins as output

IOC8x = "1": Set the relative Port 8x I/O pin into high impedance (input pin)

6.2.2.5 IOC90/RAM_ADDR (128 Bytes RAM Address)

(Address: 09h, Bit 0 of R5 = "0")

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	RAM_A6	RAM_A5	RAM_A4	RAM_A3	RAM_A2	RAM_A1	RAM_A0
0	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7: Unused bit, must be fixed to "**0**".

Bits 6 ~ 0 (RAM_A6 ~ RAM_A0): 128 bytes RAM address

6.2.2.6 IOCA0/RAM_DB (128 Bytes RAM Data Buffer)

(Address: 0Ah, Bit 0 of R5 = "0")

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RAM_D7	RAM_D6	RAM_D5	RAM_D4	RAM_D3	RAM_D2	RAM_D1	RAM_D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7 ~ 0 (RAM_D7 ~RAM_D0): 128 bytes RAM data transfer register

6.2.2.7 IOCB0/CNT1PR (Counter 1 Preset Register)

(Address: 0Bh, Bit 0 of R5 = "0")

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7 ~ Bit 0: These are Counter 1 buffers which can be read and written to. Counter 1 is an 8-bit down-count timer with 8-bit prescaler used to preset the counter and read the preset value. The prescaler is set by the IOC91 register. After an interrupt, the preset value will be auto-reloaded.

6.2.2.8 IOCC0/CNT2PR (Counter 2 Preset Register)

(Address: 0Ch, Bit 0 of R5 = "0")

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7 ~ Bit 0: These are Counter 2 buffers which can be read and written to. Counter 2 is an 8-bit down-count timer with 8-bit prescaler used to preset the counter and read the preset value. The prescaler is set by IOC91 register. After an interrupt, the preset value will be auto-reloaded.

When IR output is enabled, this control register can obtain carrier frequency output. If the Counter 2 clock source is equal to F_T, then-

$$\text{Carrier frequency (Fcarrier)} = \frac{F_T}{2 * (\text{preset\_value} + 1) * \text{prescaler}}$$

6.2.2.9 IOCD0/HPWTPR (High-Pulse Width Timer Preset Register)

(Address: 0Dh, Bit 0 of R5 = "0")

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7 ~ Bit 0: These are high-pulse width timer buffers which can be read and written to. High-pulse width timer preset register is an 8-bit down-counter with 8-bit prescaler used as IOCD0 to preset the counter and read the preset value. The prescaler is set by the IOCA1 register. After an interrupt, the preset value will be auto-reloaded.

For PWM or IR application, this control register is set as high pulse width. If the high-pulse width timer clock source is F_T, then –

$$\text{High pulse time} = \frac{\text{prescaler} * (\text{preset\_value} + 1)}{F_T}$$

6.2.2.10 IOCE0/LPWTPR (Low-Pulse Width Timer Preset Register)

(Address: 0Eh, Bit 0 of R5 = "0")

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7 ~ Bit 0: All are low-pulse width timer buffer that can be read and written to. Low-pulse width timer preset is an eight-bit down-counter with 8-bit prescaler that is used as IOCE0 to preset the counter and read preset value. The prescaler is set by IOCA1 register. After an interrupt, it will auto-reload the preset value.

For PWM or IR application, this control register is set as low pulse width. If the low-pulse width timer clock source is F_T, then –

$$\text{Low pulse time} = \frac{\text{prescaler} * (\text{preset\_value} + 1)}{F_T}$$

6.2.2.11 IOCF0/IMR (Interrupt Mask Register)

(Address: 0Fh, Bit 0 of R5 = "0")

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ICIE	LPWTE	HPWTE	CNT2E	CNT1E	INT1E	INT0E	TCIE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7 ~ Bit 0: Interrupt enable bit. Enable the respective interrupt source.

"0": Disable interrupt

"1": Enable interrupt

IOCF0 register is readable and writable.

6.2.3 IOC Page 1 (IOC61 ~ IOCE1, Bit 0 of R5 = "1")

6.2.3.1 IOC61/WUCR (Wake-up and Sink Current of P5.7/IROUT Control Register)

(Address: 06h, Bit 0 of R5 = "1")

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IROCS	0	0	0	/WUE8H	/WUE8L	/WUE6H	/WUE6L
R/W	-	-	-	R/W	R/W	R/W	R/W

Bit 7 (IROCS): IROUT/Port 57 output sink current setting

IROCS	P57/IROUT Sink Current Setting	
	VDD=5V	VDD=3V
"0"	10 mA	6 mA
"1"	20 mA	12 mA

Bits 6, 5, 4: Unused bits, must be fixed to "**0**"

Bit 3 (/WUE8H): "0"/"1"→ Enable/disable Pins P84~P87 to change wake-up function

Bit 2 (/WUE8L): "0"/"1"→ Enable/disable Pins P80~P83 to change wake-up function

Bit 1 (/WUE6H): "0"/"1"→ Enable/disable Pins P64~P67 to change wake-up function

Bit 0 (/WUE6L): "0"/"1"→ Enable/disable Pins P60~P63 to change wake-up function

NOTE

Do not set Port 6 and Port 8 as input floating when wake-up function is enabled.
"Enable" is the default status of the wake-up function.

6.2.3.2 IOC71/TCCCR (TCC Control Register)

(Address: 07h, Bit 0 of R5 = "1")

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INT_EDGE	INT	TS	TE	PSRE	TCCP2	TCCP1	TCCP0
R/W	F	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7 (INT_EDGE): Interrupt edge select bit

INT_EDGE = **"0":** Interrupt on the rising edge of P54/INT0 pin

INT_EDGE = **"1":** Interrupt on the falling edge of P54/INT0 pin

Bit 6 (INT): INT enable flag. This bit is read only.

INT = **"0":** Interrupt masked by DISI or hardware interrupt

INT = **"1":** Interrupt enabled by ENI/RETI instructions

Bit 5 (TS): TCC signal source

TS = **"0":** Internal instruction cycle clock

TS = **"1":** Transition on TCC pin, TCC period > internal instruction clock period

Bit 4 (TE): TCC signal edge

TE = **"0":** Incremented by TCC pin rising edge

TE = **"1":** Incremented by TCC pin falling edge

Bits 3 ~ 0 (PSRE, TCCP2 ~ TCCP0): TCC prescaler bits

PSRE	TCCP2	TCCP1	TCCP0	TCC Rate
0	×	×	×	1:1
1	0	0	0	1:2
1	0	0	1	1:4
1	0	1	0	1:8
1	0	1	1	1:16
1	1	0	0	1:32
1	1	0	1	1:64
1	1	1	0	1:128
1	1	1	1	1:256

6.2.3.3 IOC81/WDTCR (WDT Control Register)

(Address: 08h, Bit 0 of R5 = "1")

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	WDTE	WDTP2	WDTP1	WDTP0
-	-	-	-	R/W	R/W	R/W	R/W

Bits 7 ~ 4: Unused bits

Bit 3 (WDTE): Watchdog timer enable. This control bit is used to enable the Watchdog timer

WDTE = **"0":** Disable WDT function

WDTE = **"1":** Enable WDT function

Bits 2 ~ 0 (WDTP2 ~ WDTP0): Watchdog Timer prescaler bits. The WDT clock source is sub-oscillation frequency.

WDTP2	WDTP1	WDTP0	WDT Rate
0	0	0	1:1
0	0	1	1:2
0	1	0	1:4
0	1	1	1:8
1	0	0	1:16
1	0	1	1:32
1	1	0	1:64
1	1	1	1:128

6.2.3.4 IOC91/CNT12CR (Counters 1 and 2 Control Register)

(Address: 09h, Bit 0 of R5 = "1")

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CNT2S	CNT2P2	CNT2P1	CNT2P0	CNT1S	CNT1P2	CNT1P1	CNT1P0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7 (CNT2S): Counter 2 clock source select

CNT2S = **"0":** Fs (Fs: sub-oscillator clock)

CNT2S = **"1":** Fm (Fm: main-oscillator clock)

Bits 6 ~ 4 (CNT2P2 ~ CNT2P0): Counter 2 prescaler select bits

CNT2P2	CNT2P1	CNT1P0	Counter 2 Scale
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

Bit 3 (CNT1S): Counter 1 clock source select bit

CNT1S = **"0":** Fs (Fs: sub-oscillator clock)

CNT1S = **"1":** Fm (Fm: main-oscillator clock)

Bits 2 ~ 0 (CNT1P2 ~ CNT1P0): Counter 1 prescaler select bits

CNT1P2	CNT1P1	CNT1P0	Counter 1 Scale
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

6.2.3.5 IOCA1/HLPWTCR (High/Low Pulse Width Timer Control Register)

(Address: 0Ah, Bit 0 of R5 = "1")

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LPWTS	LPWTP2	LPWTP1	LPWTP0	HPWTS	HPWTP2	HPWTP1	HPWTP0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7 (LPWTS): Low-pulse width timer clock source select bit

LPWTS = **"0":** Fs (Fs: sub-oscillator clock)

LPWTS = **"1":** Fm (Fm: main-oscillator clock)

Bits 6 ~ 4 (LPWTP2~ LPWTP0): Low-pulse width timer prescaler select bits

LPWTP2	LPWTP1	LPWTP0	Low-Pulse Width Timer Scale
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

Bit 3 (HPWTS): High-pulse width timer clock source select bit

HPWTS = **"0":** Fs (Fs: sub-oscillator clock)

HPWTS = **"1":** Fm (Fm: main-oscillator clock)

Bits 2 ~ 0 (HPWTP2 ~ HPWTP0): High-pulse width timer prescaler select bits

HPWTP2	HPWTP1	HPWTP0	High-Pulse Width Timer Scale
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

6.2.3.6 IOCB1/P6PH (Port 6 Pull-high Control Register)

(Address: 0Bh, Bit 0 of R5 = "1")

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PH67	PH66	PH65	PH64	PH63	PH62	PH61	PH60
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7 ~ Bit 0 (PH67 ~ PH60): Port 6 pull high function enable bits

PH6x = **"0":** Disable P6x pin internal pull-high resistor function

PH6x = **"1":** Enable P6x pin internal pull-high resistor function

6.2.3.7 IOCC1/P6OD (Port 6 Open Drain Control Register)

(Address: 0Ch, Bit 0 of R5 = "1")

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OP67	OP66	OP65	OP64	OP63	OP62	OP61	OP60
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7 ~ Bit 0 (OP67 ~ OP60): Port 6 open drain function enable bits

OD6x = **"0":** Disable P6x pin open drain function

OD6x = **"1":** Enable P6x pin open drain function

6.2.3.8 IOCD1/P8PH (Port 8 Pull High Control Register)

(Address: 0Dh, Bit 0 of R5 = "1")

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PH87	PH86	PH85	PH84	PH83	PH82	PH81	PH80
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7 ~ Bit 0 (PH87 ~ PH80): Port 8 pull-high function enable bits

PH8x = **"0":** Disable P8x pin internal pull-high resistor function

PH8x = **"1":** Enable P8x pin pull-high resistor function

6.2.3.9 IOCE1/P6PL (Port 6 Pull Low Control Register)

(Address: 0Eh, Bit 0 of R5 = "1")

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PL67	PL66	PL65	PL64	PL63	PL62	PL61	PL60
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7 ~ Bit 0 (PL67 ~ PL60): Port 6 pull low function enable bits

PL6x = **"0":** Disable P6x pin internal pull-low resistor function

PL6x = **"1":** Enable P6x pin internal pull-low resistor function

6.3 TCC and WDT Prescaler

Two 8-bit counters are available as prescalers for the TCC (Time Clock Counter) and WDT (Watchdog Timer). The TCCP2~TCCP0 bits of the IOC71 register are used to determine the ratio of the TCC prescaler. Likewise, the WDTP2~WDTP0 bits of the IOC81 register are used to determine the WDT prescaler. The TCC prescaler (TCCP2 ~TCCP0) is cleared by the instructions each time they are written into TCC, while the WDT prescaler is cleared by the "WDTC" and "SLEP" instructions. Figures 6-4(a) and 6-4(b) depict the functional block diagrams of TCC and WDT respectively.

R1 (TCC) is an 8-bit timer/counter. The TCC clock source is selected from either internal instruction clock or external signal input (edge selectable from the TCC control register). If the TCC signal source is from the internal instruction clock, the TCC will be incremented by "1" at every instruction cycle (without prescaler). If the TCC signal source is from an external clock input, the TCC will be incremented by "1" at every falling edge or rising edge of the TCC pin.

The Watchdog Timer (WDT) is a free running on-chip sub-oscillator. The WDT will keep on running even after the oscillator driver has been turned off. During Normal mode, Green mode or Idle mode operation, a WDT time-out (if enabled) will cause the device to reset. The WDT can be enabled or disabled any time during Normal mode and Green mode by software programming (see WDTE bit of IOC81 register in Section 6.4.3). The WDT time-out period is calculated using the following formula:

WDT Time-out Period = (prescaler × 256 / (Fs/2)).

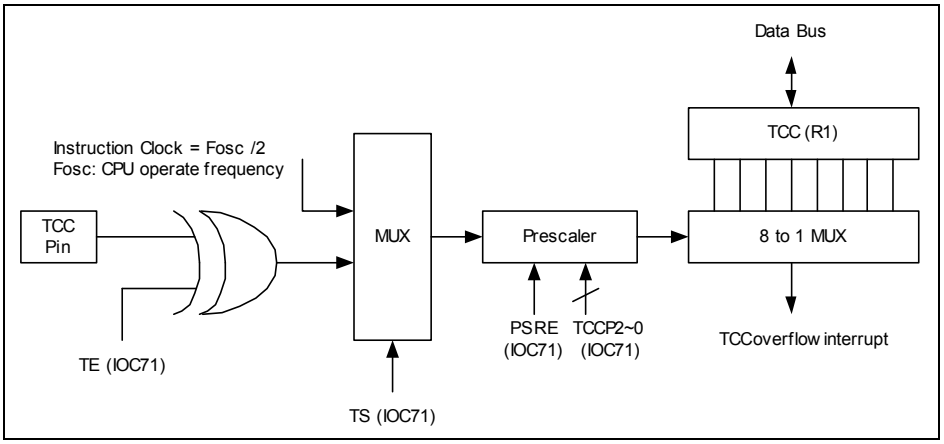


Figure 6-4(a) TCC Functional Block Diagram

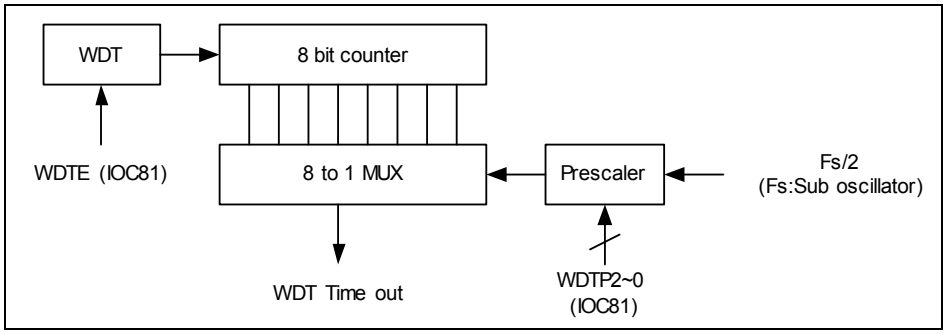
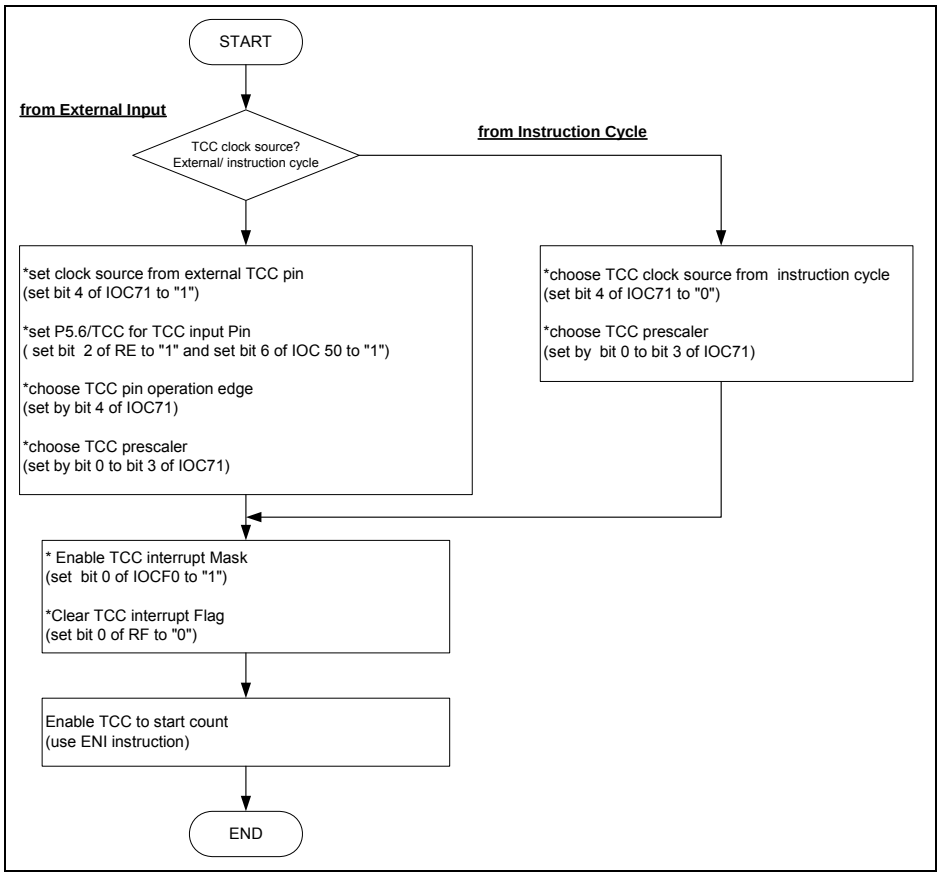
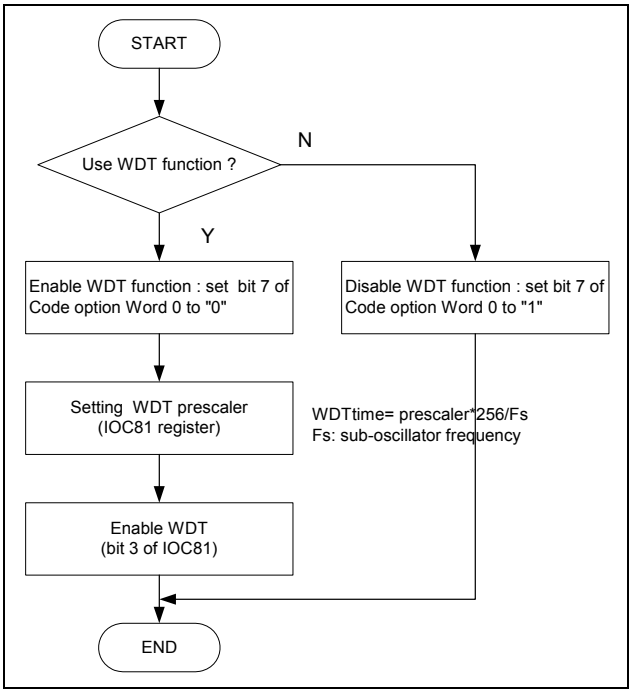


Figure 6-4(b) WDT Functional Block Diagram

6.3.1 TCC Setting Flowchart

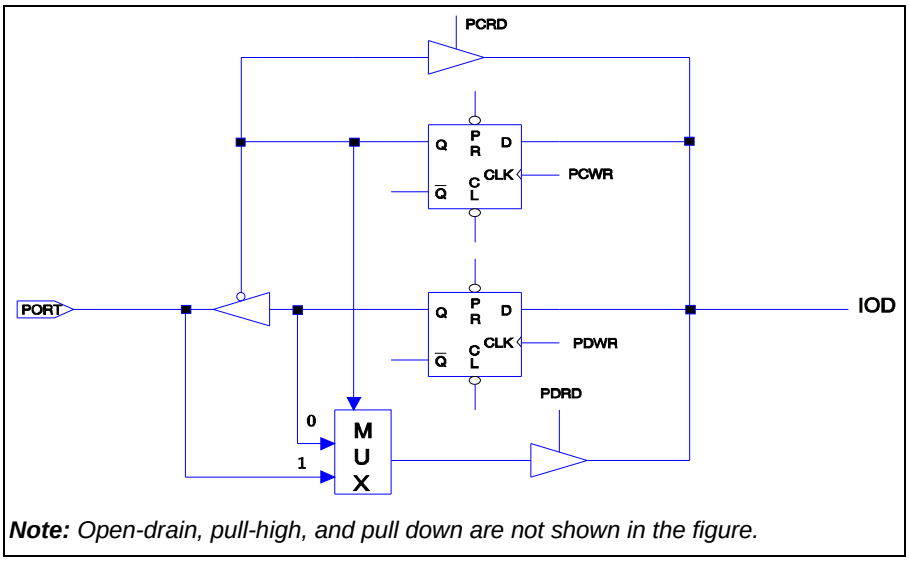


6.3.2 WDT Setting Flowchart



6.4 I/O Ports

The I/O registers (Port 5, Port 6, Port 7, and Port 8), are bidirectional tri-state I/O ports. Port 6 and Port 8 are pulled-high internally by software while Port 6 is pulled-low internally by software. Furthermore, Port 6 also has its open-drain output through software. Port 6 and Port 8 features an input status changed interrupt (or wake-up) function and are pulled-high by software. Each I/O pin can be defined as "input" or "output" pin by the I/O control register (IOC50 ~ IOC80). The I/O registers and I/O control registers are both readable and writable. The I/O interface circuits are as shown in the following Figure 6-5.



Note: *Open-drain, pull-high, and pull down are not shown in the figure.*

Figure 6-5 I/O Port and I/O Control Register Circuit for Port 5 ~ 8

6.5 Reset and Wake-up

A reset can be activated by

- POR (Power-on Reset)
- WDT timeout. (if enabled)
- LVR (if enabled)
- /RESET pin goes to low

Note that the reset circuit is always enabled. It will reset the CPU at 1.9V. Once a reset occurs, the following functions are performed:

- The oscillator is running, or will be started
- The program counter (R2/PC) is set to all "**0**"
- All I/O port pins are configured as input mode (high-impedance state)
- The TCC/Watchdog timer and prescaler are cleared
- When power is on, the Bits 5 and 6 of R3 and the upper two bits of R4 are cleared.
- Bits of the IOC71 register are set to all "**1**," except for Bit 6 (INT flag)

■ For other registers, see the following table.

6.5.1 Summary of Registers Initialized Values

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x05	IOC50 (P5CR)	Bit Name	IOC57	IOC56	IOC55	IOC54	P8HS	P8LS	P7HS	P7LS
		Power-on	1	1	1	1	0	0	0	0
		/RESET and WDT	1	1	1	1	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x06	IOC60 (P6CR)	Bit Name	IOC67	IOC66	IOC65	IOC64	IOC63	IOC62	IOC61	IOC60
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x07	IOC70 (P7CR)	Bit Name	IOC77	IOC76	IOC75	IOC74	IOC73	IOC72	IOC71	IOC70
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x08	IOC80 (P8CR)	Bit Name	IOC87	IOC86	IOC85	IOC84	IOC83	IOC82	IOC81	IOC80
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x09	IOC90 (RAM_ADDR)	Bit Name	0	RAM_A6	RAM_A5	RAM_A4	RAM_A3	RAM_A2	RAM_A1	RAM_A0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x0A	IOCA0 (RAM_DB)	Bit Name	RAM_D7	RAM_D6	RAM_D5	RAM_D4	RAM_D3	RAM_D2	RAM_D1	RAM_D0
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P

(Continuation)

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0B	IOCB0 (CNT1PR)	Bit Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x0C	IOCC0 (CNT2PR)	Bit Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x0D	IOCD0 (HPWTPR)	Bit Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x0E	IOCE0 (LPWTPR)	Bit Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x0F	IOCF0 (IMR)	Bit Name	ICIE	LPWTE	HPWTE	CNT2E	CNT1E	INT1E	INT0E	TCIE
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x06	IOC61 (WUCR)	Bit Name	IROCS	0	0	0	/WUE8H	/WUE8L	/WUE6H	/WUE6L
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P

(Continuation)

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x07	IOC71 (TCCCR)	Bit Name	INT_EDGE	INT	TS	TE	PSRE	TCCP2	TCCP1	TCCP0
		Power-on	1	0	1	1	1	1	1	1
		/RESET & WDT	1	0	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x08	IOC81 (WDTCR)	Bit Name	X	X	X	X	WDTE	WDTP2	WDTP1	WDTP0
		Power-on	0	0	0	0	0	1	1	1
		/RESET & WDT	0	0	0	0	0	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x09	IOC91 (CNT12CR)	Bit Name	CNT2S	CNT2P2	CNT2P1	CNT2P0	CNT1S	CNT1P2	CNT1P1	CNT1P0
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x0A	IOCA1 (HLPWTCR)	Bit Name	LPWTS	LPWTP2	LPWTP1	LPWTP0	HPWTS	HPWTP2	HPWTP1	HPWTP0
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x0B	IOCB1 (P6PH)	Bit Name	PH67	PH66	PH65	PH64	PH63	PH62	PH61	PH60
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x0C	IOCC1 (P6OD)	Bit Name	OP67	OP66	OP65	OP64	OP63	OP62	OP61	OP60
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x0D	IOCD1 (P8PH)	Bit Name	PH87	PH86	PH85	PH84	PH83	PH82	PH81	PH80
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P

(Continuation)

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0E	IOCE1 (P6PL)	Bit Name	PL67	PL66	PL65	PL64	PL63	PL62	PL61	PL60
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x00	R0 (IAR)	Bit Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Power-on	U	U	U	U	U	U	U	U
		/RESET & WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x01	R1 (TCC)	Bit Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x02	R2 (PC)	Bit Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	Jump to Address 0x0018 or continue to execute next instruction							
0x03	R3 (SR)	Bit Name	X	PS1	PS0	T	P	Z	DC	C
		Power-on	0	0	0	1	1	U	U	U
		/RESET & WDT	0	0	0	t	t	P	P	P
		Wake-up from Pin Change	P	P	P	t	t	P	P	P
0x04	R4 (RSR)	Bit Name	RBS1	RBS0	RSR5	RSR4	RSR3	RSR2	RSR1	RSR0
		Power-on	0	0	U	U	U	U	U	U
		/RESET & WDT	0	0	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x05	SBANK0 R5 (Port 5)	Bit Name	P57	P56	P55	P54	X	X	X	IOCPAGE
		Power-on	1	1	1	1	0	0	0	0
		/RESET & WDT	1	1	1	1	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P

(Continuation)

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x06	SBANK0 R6 (Port 6)	Bit Name	P67	P66	P65	P64	P63	P62	P61	P60
		Power-on	1	1	1	1	1	1	1	1
		/RESET & WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x07	SBANK0 R7 (Port 7)	Bit Name	P77	P76	P75	P74	P73	P72	P71	P70
		Power-on	1	1	1	1	1	1	1	1
		/RESET & WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x08	SBANK0 R8 (Port 8)	Bit Name	P87	P86	P85	P84	P83	P82	P81	P80
		Power-on	1	1	1	1	1	1	1	1
		/RESET & WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x09	SBANK0 R9 (LCDCR)	Bit Name	BS	DS1	DS0	LCDEN	X	LCDTYPE	LCDF1	LCDF0
		Power-on	1	1	0	0	0	0	0	0
		/RESET & WDT	1	1	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x0A	SBANK0 RA (LCD_ADDR)	Bit Name	X	X	X	LCD_A4	LCD_A3	LCD_A2	LCD_A1	LCD_A0
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x0B	SBANK0 RB (LCD_DB)	Bit Name	X	X	X	X	LCD_D3	LCD_D2	LCD_D1	LCD_D0
		Power-on	0	0	0	0	U	U	U	U
		/RESET & WDT	0	0	0	0	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x0C	SBANK0 RC (CNTER)	Bit Name	X	X	X	X	LPWTEN	HPWTEN	CNT2EN	CNT1EN
		Power-on	0	1	0	0	0	0	0	0
		/RESET & WDT	0	1	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	0	P	P	P	P	P

(Continuation)

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0D	SBANK0 RD (SBPCR)	Bit Name	SBANK	CLK2	CLK1	CLK0	IDLE	BF1	BF0	CPUS
		Power-on	0	0	0	0	1	0	0	*1
		/RESET & WDT	0	0	0	0	1	0	0	*1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x0E	SBANK0 RE (IRCR)	Bit Name	IRE	HF	LGP	X	IROUTE	TCCE	EINT1	EINT0
		Power-on	0	0	0	U	0	0	0	0
		/RESET & WDT	0	0	0	U	0	0	0	0
		Wake-up from Pin Change	P	P	P	U	P	P	P	P
0x0F	SBANK0 RF (ISR)	Bit Name	ICIF	LPWTF	HPWTF	CNT2F	CNT1F	INT1F	INT0F	TCIF
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	N	P	P	P	P	P	P	P
0x05	SBANK1 R5 (TBRDH)	Bit Name	HLB	0	0	0	RBit11	RBit10	RBit9	RBit8
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x06	SBANK1 R6 (TBRDL)	Bit Name	RBit7	RBit6	RBit5	RBit4	RBi3	RBit2	RBit1	RBit0
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x10 ~ 0x3F	R10~R3F	Bit Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Power-on	U	U	U	U	U	U	U	U
		/RESET & WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P

Legend: **"x"** = *Not used* **"P"** = *Previous value before reset*
"–" = *Not defined* **"t"** = *Check R3 register explanation*
"u" = *Unknown or don't care* "**N**" = *Monitors interrupt operation status*

6.5.2 Summary of Wake-up and Interrupt Modes

All categories in Wake-up signals Interrupt modes are as follows:

Wake-up Signal	Sleep Mode	Idle Mode	Green Mode	Normal Mode
TCC time out IOCF0 Bit 0=1	×	×	Interrupt	Interrupt
INT0 pin IOCF0 Bit 1=1	Wake-up + interrupt + next instruction	Wake-up + interrupt + next instruction	Interrupt	Interrupt
INT1 pin IOCF0 Bit 2=1	Wake-up + interrupt + next instruction	Wake-up + interrupt + next instruction	Interrupt	Interrupt
Counter 1 IOCF0 Bit 3=1	×	Wake-up + interrupt + next instruction	Interrupt	Interrupt
Counter 2 IOCF0 Bit 4=1	×	Wake-up + interrupt + next instruction	Interrupt	Interrupt
High-pulse timer IOCF0 Bit 5=1	×	Wake-up + interrupt + next instruction	Interrupt	Interrupt
Low-pulse timer IOCF0 Bit 6=1	×	Wake-up + interrupt + next instruction	Interrupt	Interrupt
Port 6, Port 8 (input status change wake-up) Bit 7 of IOCF0 = “0”	Wake-up + next instruction	Wake-up + next instruction	×	×
Port 6, Port 8 (input status change wake-up) Bit 7 of IOCF0 = “1”	Wake-up + interrupt + next instruction	Wake-up + interrupt + next instruction	×	×
WDT time out	×	RESET	RESET	RESET
Low Voltage Reset	RESET	RESET	RESET	RESET

6.6 LVR (Low Voltage Reset)

6.6.1 Low Voltage Reset

LVR pin setting. The detailed operation mode is as follows:

LVR1	LVR0	VDD Reset Level	VDD Release Level
0	0	4.0V	4.2V
0	1	3.5V	3.7V
1	0	2.7V	2.9V
1	1	NA (Power-on Reset)	

If VDD < 2.7V and it is kept at 5 μs, the IC will be reset.

If VDD < 3.5V and it is kept at 5 μs, the IC will be reset.

If VDD < 4.0V and it is kept at 5 μs, the IC will be reset.

6.7 Oscillator

6.7.1 Oscillator Modes

The EM78P468NB/P470N operates in three different oscillator modes:

a) Main oscillator (R-OSCI, OSCO), such as RC oscillator with external resistor and internal capacitor mode (ERIC).

b) Crystal oscillator mode

c) PLL operation mode (R-OSCI connected to Ground through a 0.01μF capacitor). User can select which mode to use by programming FMMD1 and FMMD0 in the Code Options Register (see Section 6.13). The sub-oscillator can operate in Crystal mode and ERIC mode. The tables below show how these three modes are defined.

■ Oscillator Modes as defined by FSMD, FMMD1, and FMMD0:

FSMD	FMMD1	FMMD0	Main Clock	Sub-clock
0	0	0	RC type (ERIC)	RC type (ERIC)
0	0	1	Crystal type	RC type (ERIC)
0	1	×	PLL type	RC type (ERIC)
1	0	0	RC type (ERIC)	Crystal type
1	0	1	Crystal type	Crystal type
1	1	×	PLL type	Crystal type

■ Summary of maximum operating speeds:

VDD	Fxt Max. (MHz)
2.3	4
3.0	8
5.0	10

6.7.2 Phase Lock Loop (PLL Mode)

When operating in PLL mode, the high frequency is determined by the sub-oscillator. You can use the RD register (see Section 6.1.14) to change the high oscillator frequency. The relation between high frequency (Fm) and sub-oscillator is as shown in the following figure.

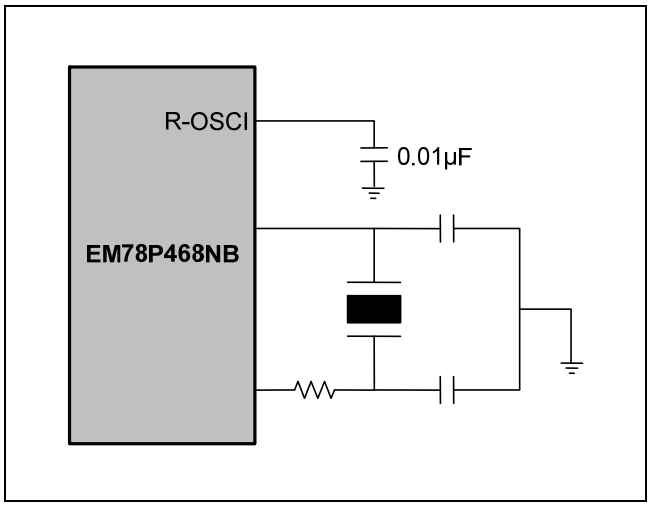


Figure 6-6 PLL Mode Circuit Diagram

6.7.3 Crystal Oscillator/Ceramic Resonators (Crystal)

The EM78P468NB/P470N can be driven by an external clock signal through the R-OSCI pin as shown in Figure 6-7(a) below.

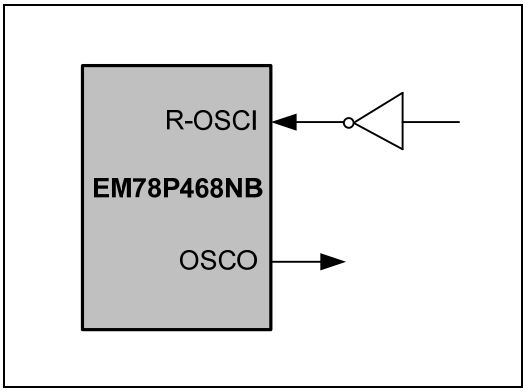


Figure 6-7(a) External Clock Input Circuit Diagram

In most applications, the R-OSCI pin and the OSCO pin are connected with a crystal or ceramic resonator to generate oscillation. The following figure depicts such circuit.

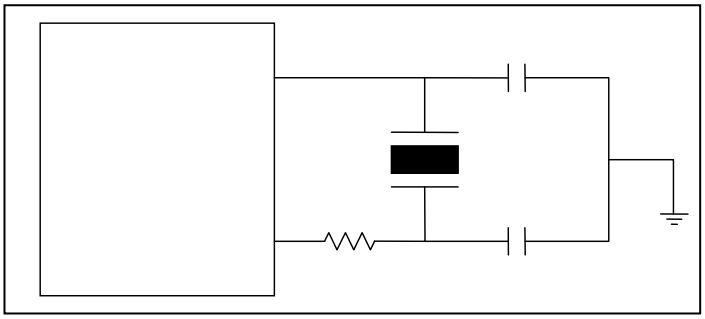


Figure 6-7(b) Crystal/Resonator Circuit Diagram

The following table provides the recommended values of C1 and C2. Since each resonator has its own attribute, user should refer to its specification for appropriate values of C1 and C2. RS, a serial resistor, may be necessary for AT strip cut crystal or low frequency mode.

- Capacitor Selection Guide for Crystal Oscillator or Ceramic Resonators

Oscillator Source	Oscillator Type	Frequency	C1 (pF)	C2 (pF)
Main Oscillator	Ceramic Resonators	455kHz	100~150	100~150
		2.0 MHz	20~40	20~40
		4.0 MHz	10~30	10~30
	Crystal Oscillator	455kHz	20~40	20~150
		1.0 MHz	15~30	15~30
		2.0 MHz	15	15
		4.0 MHz	15	15
Sub-Oscillator	Crystal Oscillator	32.768kHz	25	25

6.7.4 RC Oscillator Mode with Internal Capacitor

If both precision and cost are taken into consideration, this microcontroller also offers a special oscillation mode, which has an on-chip internal capacitor and an external resistor connected to VDD. The internal capacitor functions as temperature compensator. In order to obtain more accurate frequency, a precise resistor is recommended.

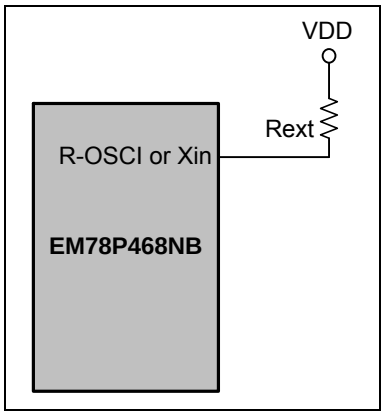


Figure 6-8 Internal C Oscillator Mode Circuit

- RC Oscillator Frequencies

Pin	Rext	Average Fosc 5V, 25℃	Average Fosc 3V, 25℃
R-OSCI	51k	2.2221 MHz	2.1972 MHz
	100k	1.1345 MHz	1.1203 MHz
	300k	381.36kHz	374.77kHz
Xin	2.2M	32.768kHz	32.768kHz

NOTE

1) Data measured from QFP packages with frequency drift of about ± 30%.
2) Values are provided for design reference only.

6.8 Power-on Considerations

Any microcontroller (as with EM78P468NB/P470N) is not warranted to start operating properly before the power supply stabilizes in a steady state. This microcontroller has an on-chip Power-on Reset (POR) with detection level range of 1.9V to 2.1V. The circuitry eliminates the extra external reset circuit but will work well only if the VDD rises fast enough (50 ms or less). However, under critical applications, extra devices are still required to assist in solving power-on problems.

6.8.1 External Power-on Reset Circuit

The circuits shown below implements an external RC to generate reset pulse. The pulse width (time constant) should be kept long enough to allow the VDD to reach minimum operation voltage. This circuit is used when the power supply has a slow rise time. Since current leakage from the /RESET pin is ± 5μA, it is recommended that R should not be greater than 40KΩ in order for the voltage at Pin /RESET to remain below 0.2V. The diode (D) acts as a short circuit at power-down. The Capacitor, C, will discharge rapidly and fully. The current-limited resistor Rin, will prevent high current discharge or ESD (electrostatic discharge) from flowing into Pin /RESET.

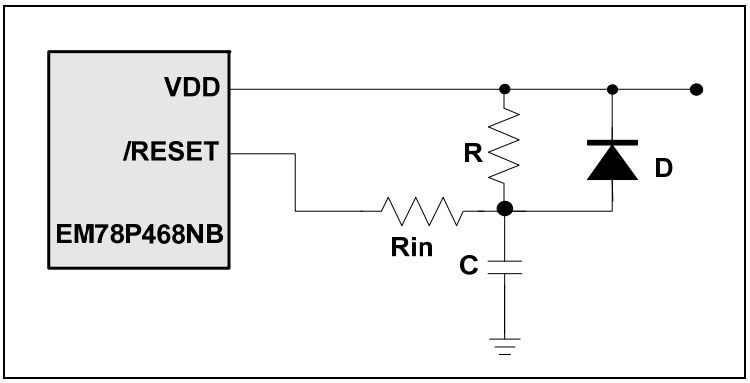


Figure 6-9 External Power-on Reset Circuit

6.8.2 Residue-Voltage Protection

When battery is replaced, device power (VDD) is disconnected but residue-voltage remains. The residue-voltage may trips below minimum VDD, but above zero. This condition may cause poor power-on reset. The following figures show how to build a proper protection circuit against residue-voltage.

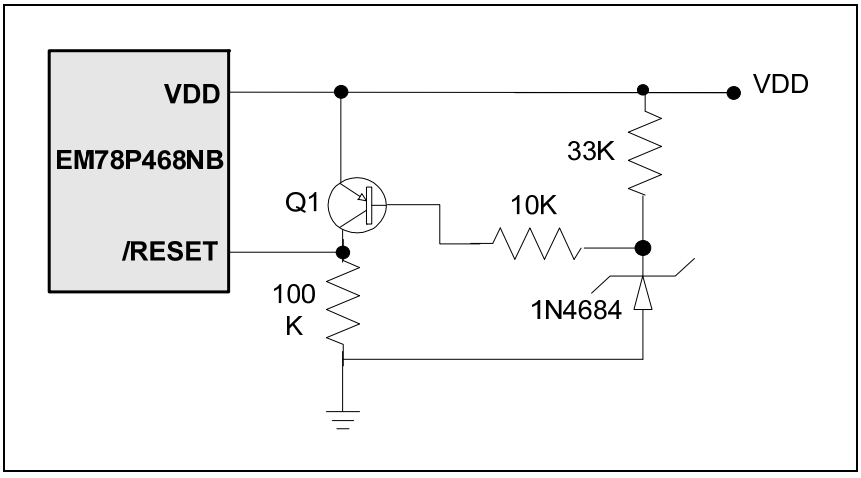


Figure 6-10(a) Residue-Voltage Protection Circuit 1

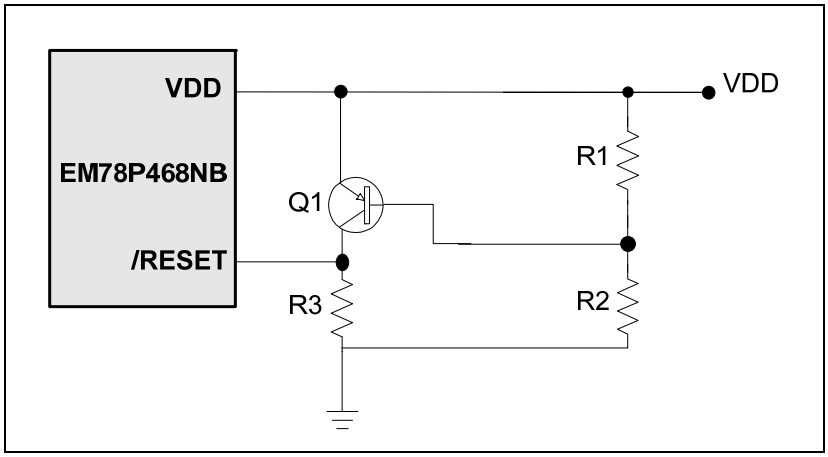


Figure 6-10(b) Residue Voltage Protection Circuit 2

6.9 Interrupt

The EM78P468NB/P470N has eight interrupt sources as listed below:

- TCC overflow interrupt
- External interrupt P54/INT0 pin
- External interrupt P55/INT1 pin
- Counter 1 underflow interrupt
- Counter 2 underflow interrupt
- High-pulse width timer underflow interrupt
- Low-pulse width timer underflow interrupt
- Port 6, Port 8 input status change wake-up

This IC has internal interrupts which are falling edge triggered or as follows:

- TCC timer overflow interrupt
- Four 8-bit down counter/timer underflow interrupt

If these interrupt sources change signal from high to low, the RF register will generate a **"1"** flag to the corresponding register if the IOCF0 register is enabled.

RF is the interrupt status register that records the interrupt request in the relative flags/bits. IOCF0 is the interrupt mask register. The global interrupt is enabled by ENI instruction and disabled by DISI instruction. When one of the interrupts (when enabled) is generated, it will cause the next instruction to be fetched from Address 0003H~0018H according to the interrupt source.

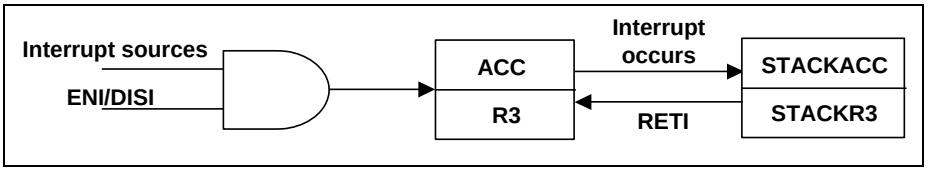


Figure 6-11 Interrupt Back-up Diagram

With this microcontroller, each individual interrupt source has its own interrupt vector as depicted in the table below. Before the interrupt subroutine is executed, the contents of the ACC and the R3 registers are initially saved by the hardware. After the interrupt service routine is completed, the ACC and R3 registers are restored. The existing interrupt service routine does not allow other interrupt service routine to be executed. Hence, if other interrupts occur while an existing interrupt service routine is being executed; the hardware will save the later interrupts. Only after the existing interrupt service routine is completed that the next interrupt service routine is executed.

- Interrupt Vector

Interrupt Vector	Interrupt Status
0003H	TCC overflow interrupt.
0006H	External interrupt P54/INT0 pin
0009H	External interrupt P55/INT1 pin
000CH	Counter 1 underflow interrupt
000FH	Counter 2 underflow interrupt
0012H	High-pulse width timer underflow interrupt
0015H	Low-pulse width timer underflow interrupt
0018H	Port 6, Port 8 input status change wake up

6.10 LCD Driver

The EM78P468NB/P470N can drive an LCD of up to 32 segments and 4 commons that drive a total of 4×32 dots. The LCD block is made up of an LCD driver, display RAM, segment output pins, common output pins, and LCD operating power supply pins. This circuit works on Normal mode, Green mode, and Idle mode. The LCD duty; bias; the number of segment; the number of common, and frame frequency are determined through the LCD control register.

The basic structure contains a timing controller that uses a subsystem clock to generate the proper timing for different duty and display accesses. The R9 register is a command register for the LCD driver which includes LCD enable/disable, bias (1/2 and 1/3), duty (1/2, 1/3, 1/4), and LCD frame frequency control. The Register RA is an LCD contrast and LCD RAM address control register. The Register RB is an LCD RAM data buffer. LCD booster circuit can change the operation frequency to improve VLCD2 and VLCD3 drive capability. The control register is described in the following sections.

6.10.1 R9/LCDCR (LCD Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BS	DS1	DS0	LCDEN	–	LCDTYPE	LCDF1	LCDF0
R/W	R/W	R/W	R/W	-	R/W	R/W	R/W

Bit 7 (BS): LCD bias select bit, "**0**" **:** 1/2 bias

"**1**" **:** 1/3 bias

Bits 6 ~ 5 (DS1 ~ DS0): LCD duty select

DS1	DS0	LCD Duty
0	0	1/2 duty
0	1	1/3 duty
1	×	1/4 duty

Bit 4 (LCDEN): LCD enable bit

LCDEN = **"0":** Disable the LCD circuit

LCDEN = **"1":** Enable the LCD circuit

When the LCD function is disabled, all common/segment outputs are set to ground (GND) level.

Bit 3: Not used

Bit 2 (LCDTYPE): LCD drive waveform type select bit

LCDTYPE = "0": "A" type waveform

LCDTYPE = "1": "B" type waveform

Bits 1 ~ 0 (LCDF1 ~ LCDF0): LCD frame frequency control bits:

LCDF1	LCDF0	LCD Frame Frequency (e.g., Fs=32.768kHz)		
		1/2 Duty	1/3 Duty	1/4 Duty
0	0	Fs/(256×2)=64.0	Fs/(172×3)=63.5	Fs/(128×4)=64.0
0	1	Fs/(280×2)=58.5	Fs/(188×3)=58.0	Fs/(140×4)=58.5
1	0	Fs/(304×2)=53.9	Fs/(204×3)=53.5	Fs/(152×4)=53.9
1	1	Fs/(232×2)=70.6	Fs/(156×3)=70.0	Fs/(116×4)=70.6

Note: Fs: *sub-oscillator frequency*

6.10.2 RA/LCD_ADDR (LCD Address)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	LCD_A4	LCD_A3	LCD_A2	LCD_A1	LCD_A0
-	-	-	R/W	R/W	R/W	R/W	R/W

Bits 7 ~ 5: Not used, fixed to "**0**"

Bits 4 ~ 0 (LCDA4 ~ LCDA0): LCD RAM address

RA (LCD Address)	RB (LCD Data Buffer)					Segment
	Bits 7 ~4	Bit 3 (LCD_D3)	Bit 2 (LCD_D2)	Bit 1 (LCD_D1)	Bit 0 (LCD_D0)	
00H	–	–	–	–	–	SEG0
01H	–	–	–	–	–	SEG1
02H	–	–	–	–	–	SEG2
¦	¦					¦
1DH	–	–	–	–	–	SEG29
1EH	–	–	–	–	–	SEG30
1FH	–	–	–	–	–	SEG31
Common	X	COM3	COM2	COM1	COM0	-

6.10.3 RB/LCD_DB (LCD Data Buffer)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
–	–	–	–	LCD_D 3	LCD_D 2	LCD_D 1	LCD_D 0
-	-	-	-	R/W	R/W	R/W	R/W

Bits 7 ~ 4: Not used

Bits 3 ~ 0 (LCD_D3 ~ LCD_D0): LCD RAM data transfer registers

6.10.4 RD/SBPCR (System, Booster and PLL Control Registers)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SBANK	CLK2	CLK1	CLK0	IDLE	BF1	BF0	CPUS
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 2 ~ 1 (BF1 ~ BF0): LCD booster frequency select bits

BF1	BF0	Booster Frequency
0	0	Fs
0	1	Fs/4
1	0	Fs/8
1	1	Fs/16

- LCD function Initial setting flowchart

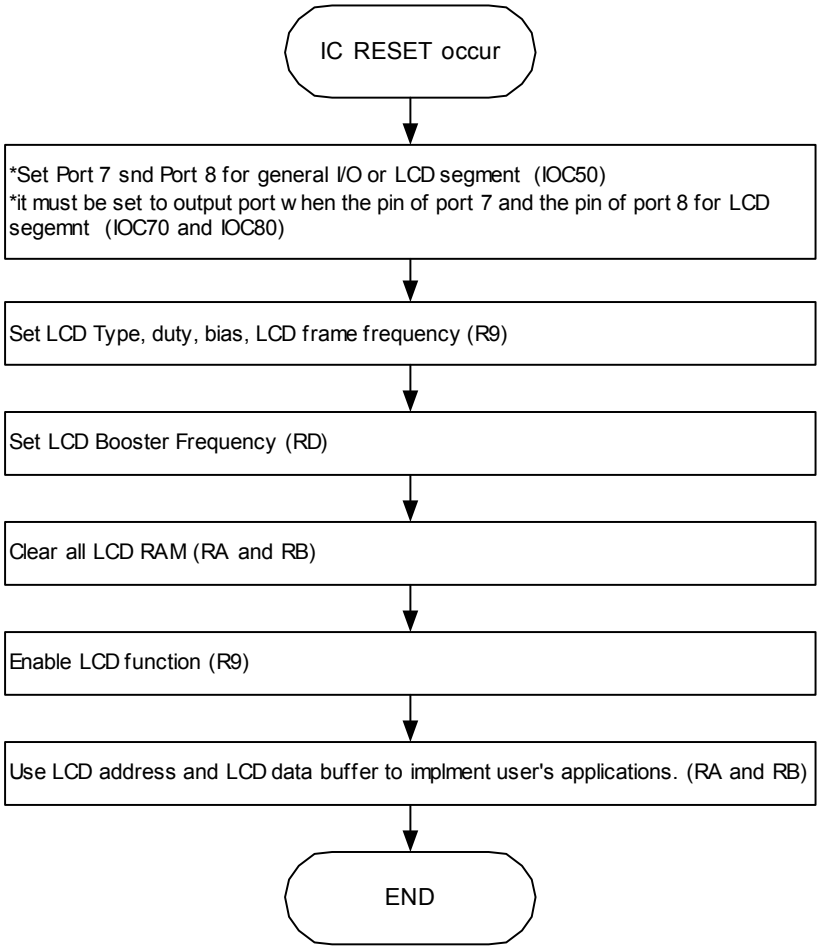


Figure 6-12(a) LCD Function Initial Setting Flowchart

- Booster circuit connection for LCD voltage

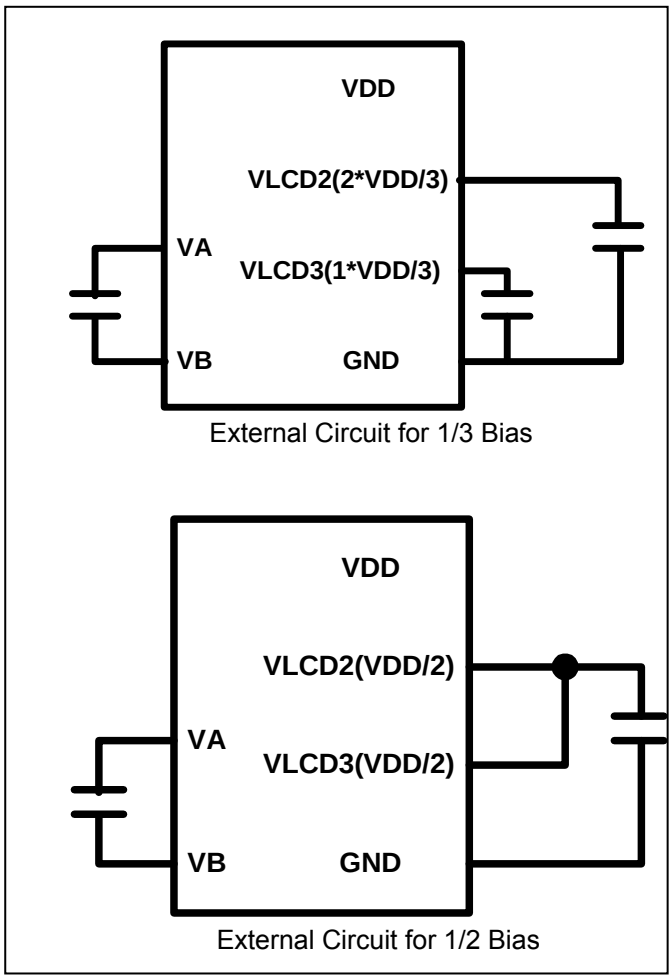


Figure 6-12(b) Charge Bump Circuit Connection (Cext=0.1μf)

■ LCD Waveforms for 1/2 Bias

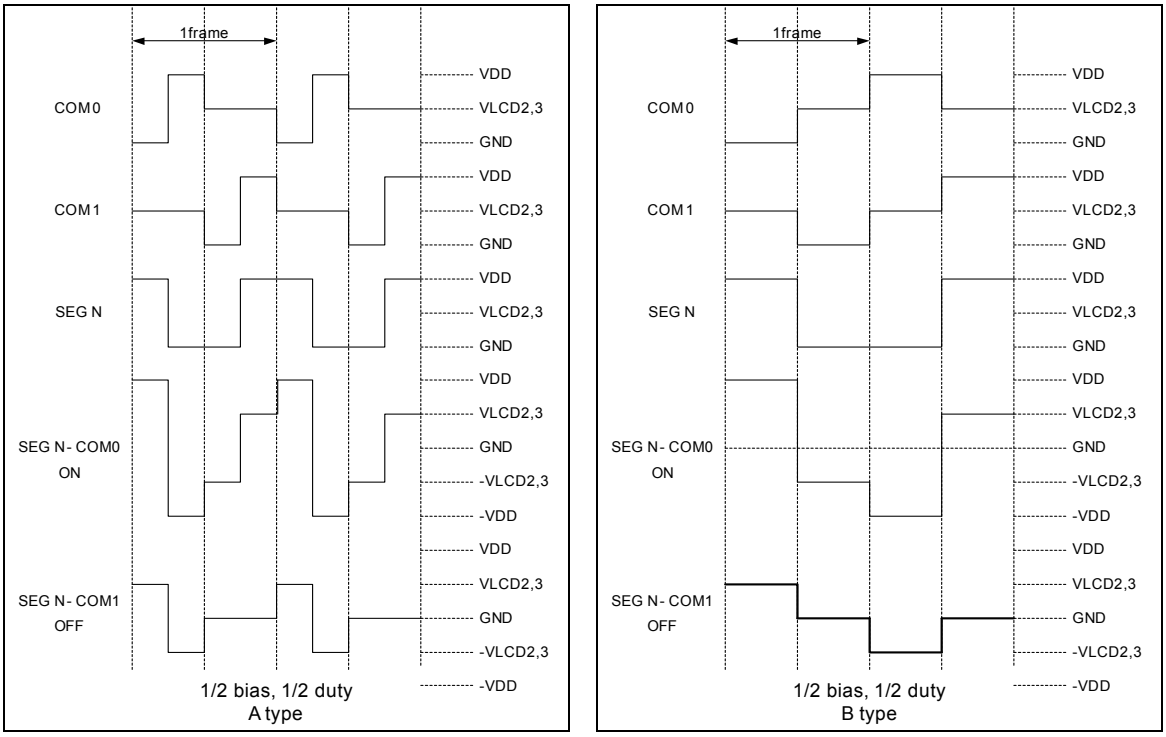


Figure 6-12(c) LCD Waveform for 1/2 Bias, 1/2 Duty

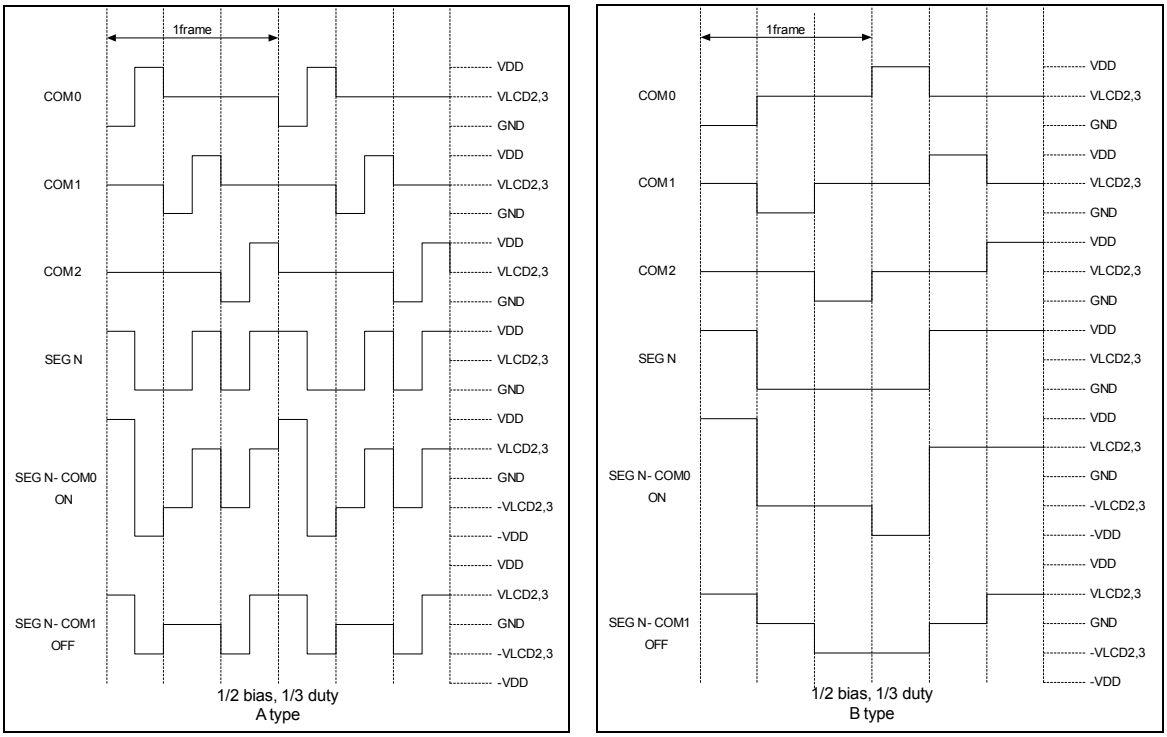


Figure 6-12(d) LCD Waveform for 1/2 Bias, 1/3 Duty

■ LCD Waveforms for 1/3 Bias

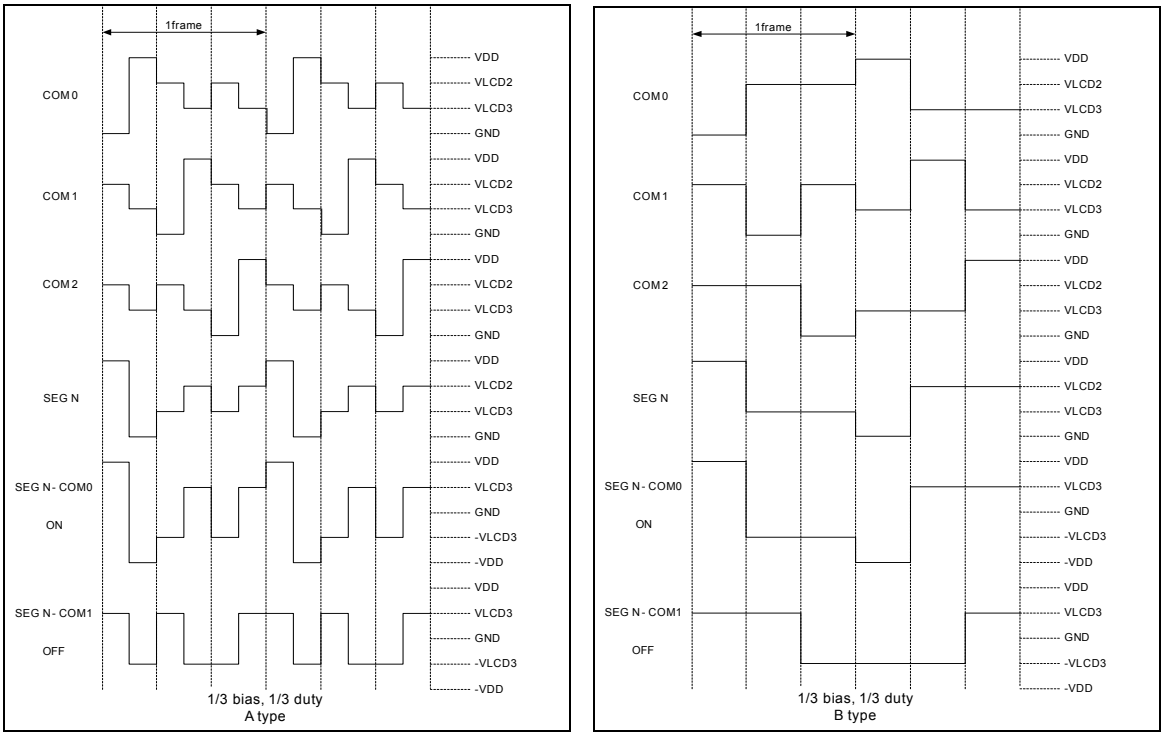


Figure 6-12(e) LCD Waveform for 1/3 Bias, 1/3 Duty

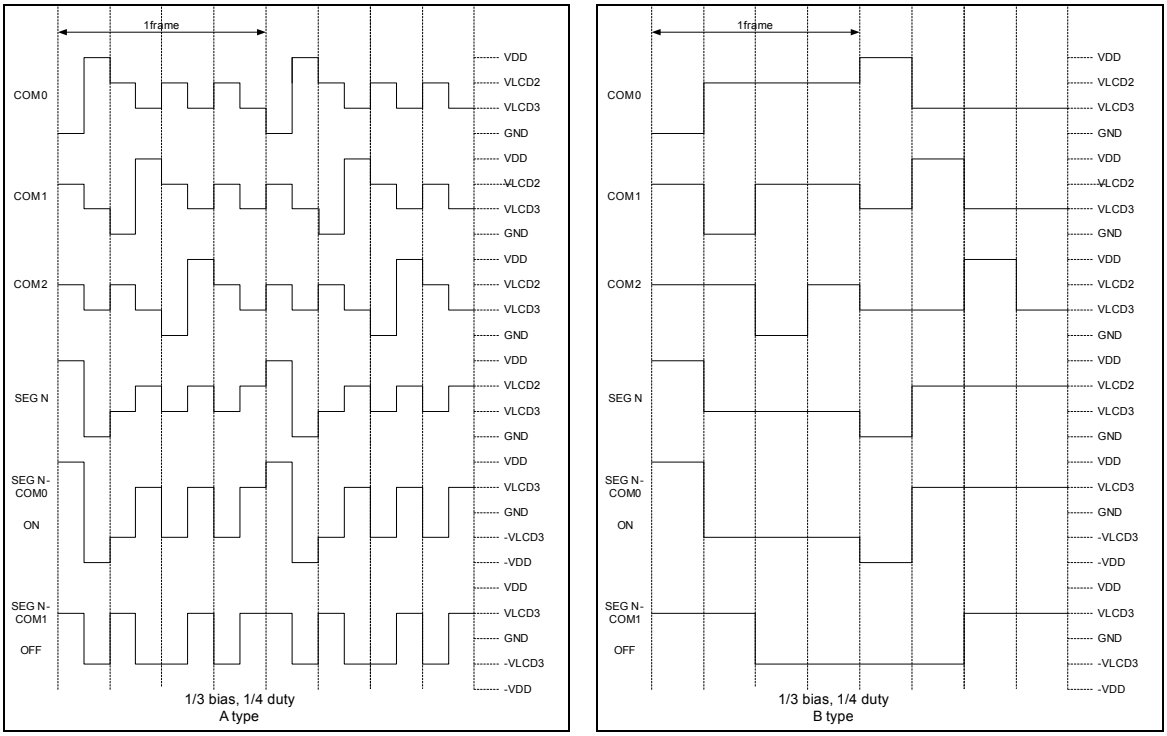


Figure 6-12(f) LCD Waveform for 1/3 Bias, 1/4 Duty

6.11 Infrared Remote Control Application/PWM Waveform Generation

This microcontroller can output infrared carrier under user-friendly or PWM standard waveform. The IR and PWM waveform generated functions include an 8-bit down count timer/counter, high-pulse width timer, low-pulse width timer, and IR control register. The IR system block diagram is shown below. The IROUT pin waveform is determined by IR control register (RE), IOC90 (Counters 1 and 2 control register), IOCA0 (high-pulse width timer, low-pulse width timer control register), IOCC0 (Counter 2 preset), IOCD0 (high-pulse width timer preset register), and IOCE0 (low-pulse width timer preset register). Details on Fcarrier, high-pulse time, and low pulse time are explained below.

If Counter 2 clock source is FT (this clock source can be set by IOC91), then -

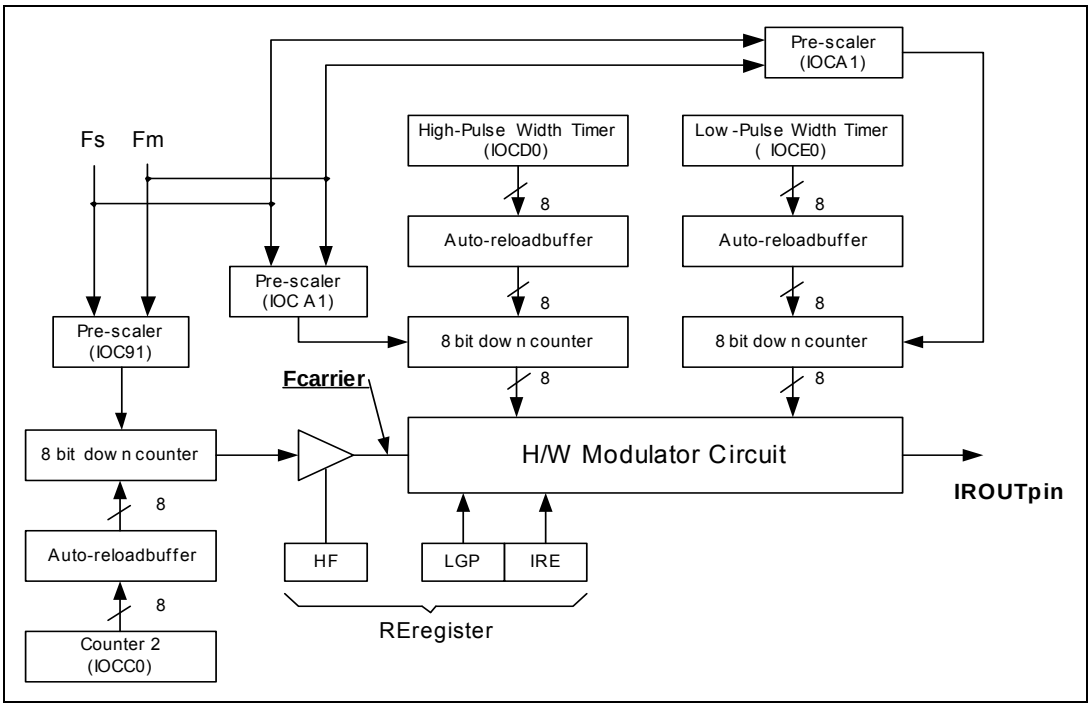
$$F_{carrier} = \frac{F_T}{2 \times (1 + decimal\ \ of\ \ Counter\ \ 2\ \ preset\ \ value\ \ (IOCC\ 0)) \times prescaler}$$

If the high-pulse width timer clock source is FT (this clock source can be set by IOCA1), then-

$$T_{high\ \ pulse\ \ time} = \frac{prescaler\ \ \times (1 + decimal\ \ of\ \ high\ \ pulse\ \ width\ \ timer\ \ value\ \ (IOCD\ 0))}{F_T}$$

If the low-pulse width timer clock source is FT (this clock source can be set by IOCA1);

$$T_{low\ \ pulse\ \ time} = \frac{prescaler\ \ \times (1 + decimal\ \ of\ \ low\ \ pulse\ \ width\ \ timer\ \ value\ \ (IOCE\ 0))}{F_T}$$



Note: ***Fm:*** *main oscillator frequency* ***Fs:*** *sub-oscillator frequency*

Figure 6-13 IR/PWM System Block Diagram

6.11.1 IROUT Output Waveforms

The IROUT output waveform is further explained in the following figures:

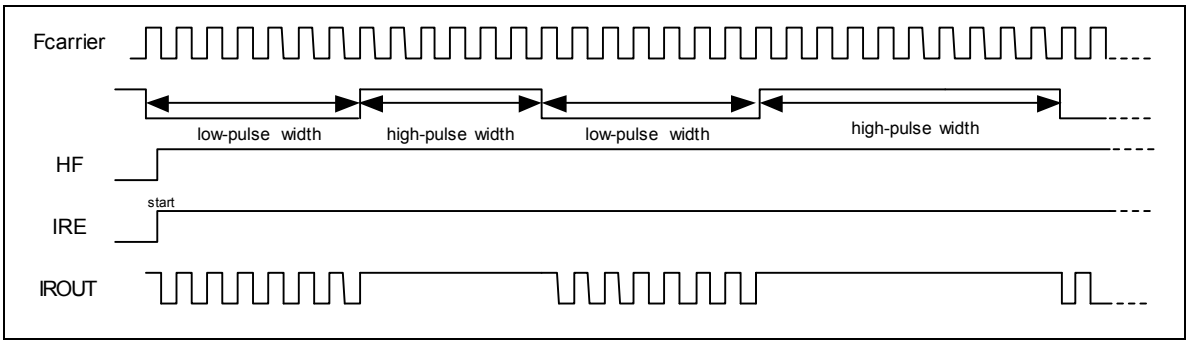


Figure 6-14(a) LGP=0, IROUT Pin Output Waveform

LGP=0, HF=1, the IROUT waveform can modulate Fcarrier waveform when in low-pulse width time.

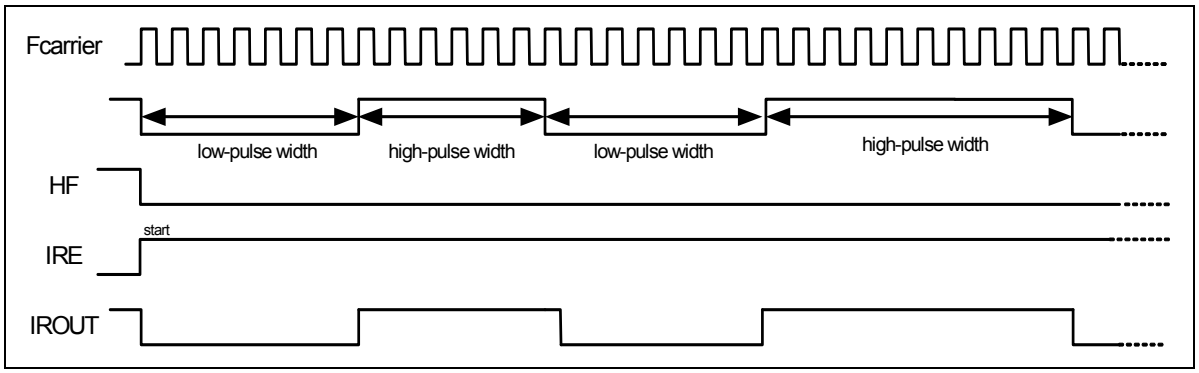


Figure 6-14(b) LGP=0, IROUT Pin Output Waveform

LGP=0, HF=0, the IROUT waveform cannot modulate Fcarrier waveform when in low-pulse width time. So IROUT waveform is determined by high-pulse time and low-pulse time. This mode generates standard PWM waveform.

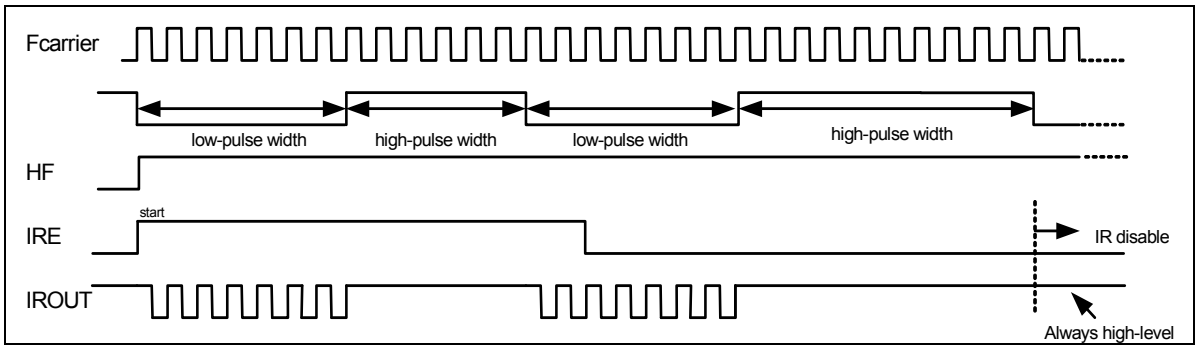


Figure 6-14(c) LGP=0, IROUT Pin Output Waveform

LGP=0, HF=1, the IROUT waveform can modulate Fcarrier waveform when in low-pulse width time. When IRE goes from high to low, the output waveform of IROUT will keep on transmitting until high-pulse width timer interrupt occurs.

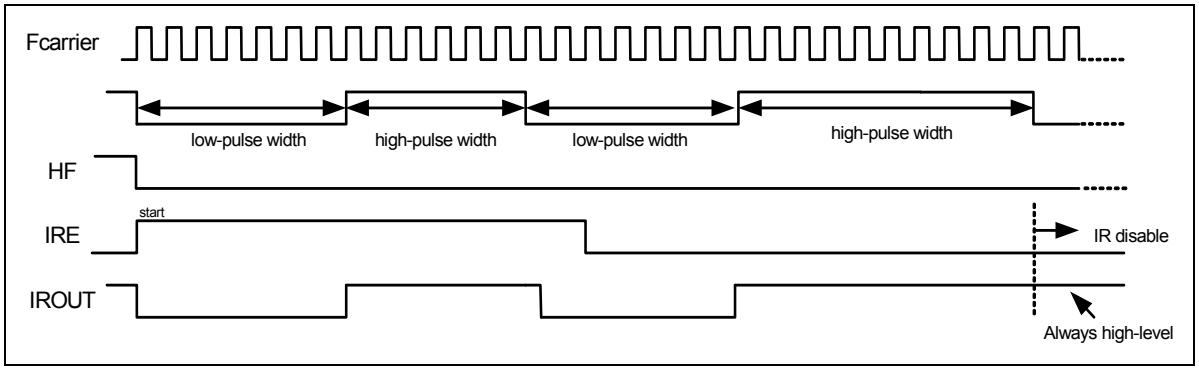


Figure 6-14(d) LGP=0, IROUT Pin Output Waveform

LGP=0, HF=0, the IROUT waveform cannot modulate Fcarrier waveform when in low-pulse width time. So IROUT waveform is determined by high-pulse time and low-pulse time. This mode produces standard PWM waveform. When IRE goes from high to low, the output waveform of IROUT will keep on transmitting until high-pulse width timer interrupt occurs.

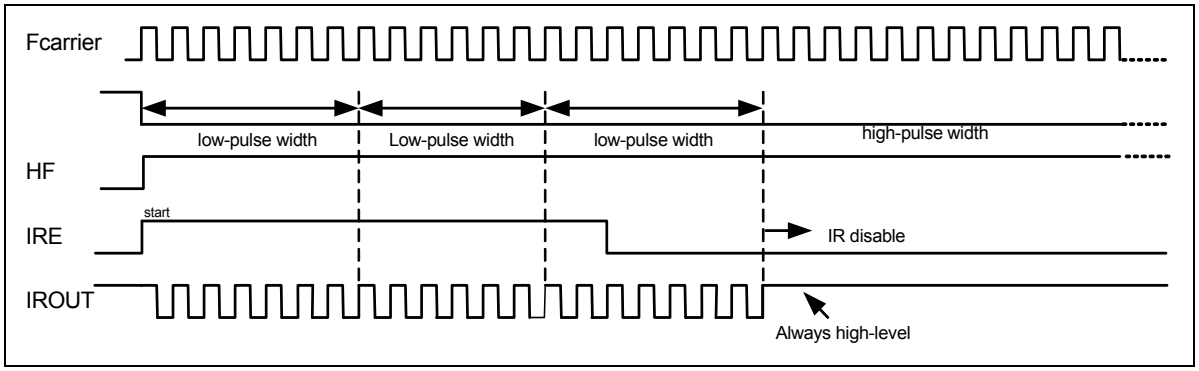


Figure 6-14(e) LGP=1, IROUT Pin Output Waveform

LGP=1, when this bit is set to high level, the high-pulse width timer is ignored. So IROUT waveform output from low-pulse width timer is established.

6.11.2 IR/PWM Function Enable Flowchart

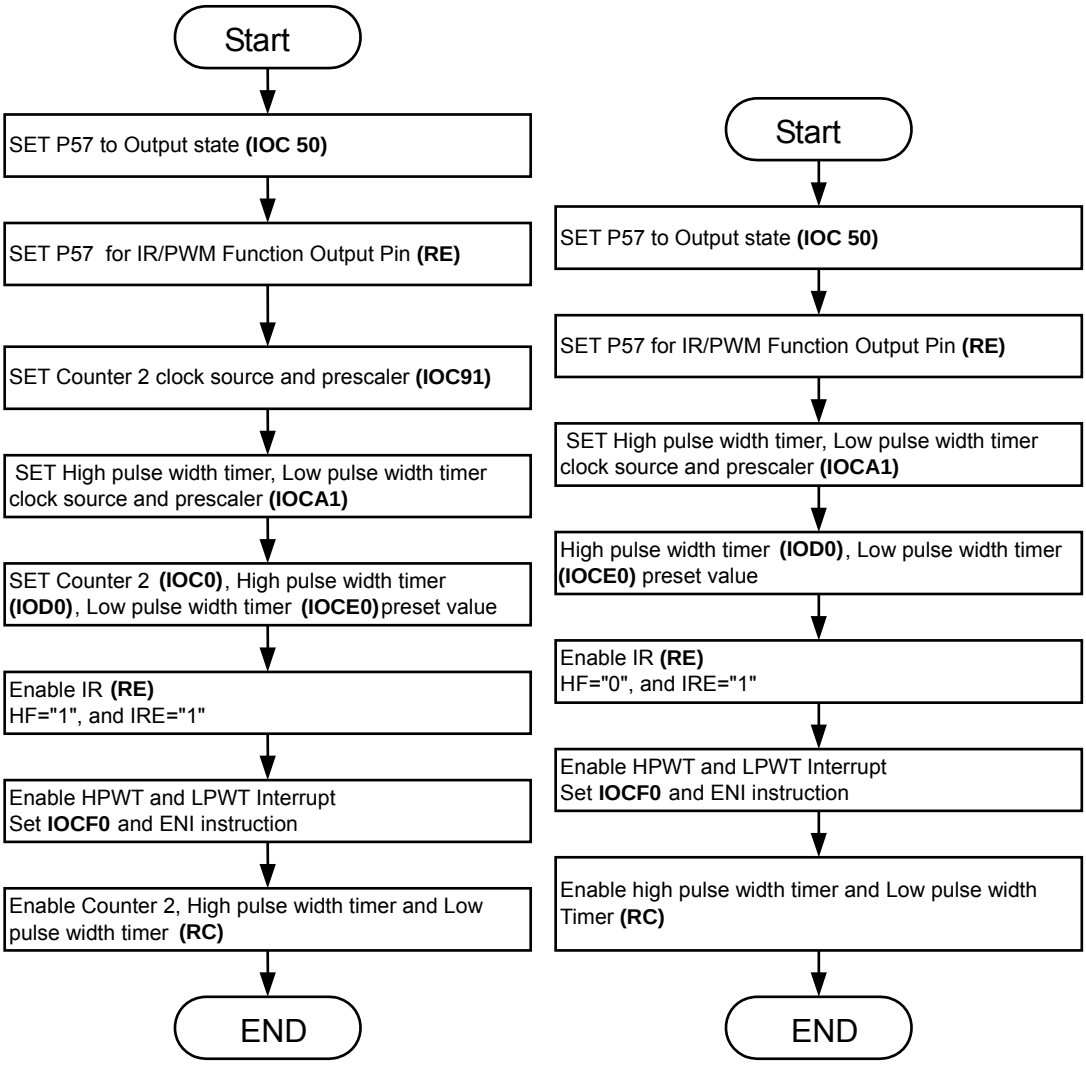


Figure 6-15 IR/PWM Function Enable Flowchart

6.12 Code Options

The EM78P468NB/P470N has one Code Option word that is not part of the normal program memory. The option bits cannot be accessed during normal program execution.

Their respective Code Option Register and Customer ID Register arrangement distribution are as follows:

Word 0	Word 1	Word 2
Bit 12~Bit 0	Customer ID	Bit 12~Bit 0

Word 0 and Word 2 of code options are for IC function setting. Word 1 is for customer ID code application. The following are the settings for OTP IC programming.

6.12.1 Code Option Register (Word 0)

	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit	Bit 1	Bit 0
Mnemonic	–	XTAL1	XTAL0	-	HLFS	ENWDTB	FSMD	FMMD1	FMMD0	HLP	PR2	PR1	PR0
1	–	High	High	-	High	Disable	High	High	High	Enable	Disable		
0	–	Low	Low	-	Low	Enable	Low	Low	Low	Disable	Enable		
Default	1	1	1	0	1	1	1	1	1	1	1	1	1

Bit 12: Unused bit

Bits 11~10 (XTAL1 ~ XTAL0): Crystal range setting for main oscillator:

XTAL1	XTAL0	Crystal Range
0	0	Reserved
0	1	6 MHz~10 MHz (XXT_EN)
1	0	1 MHz~6 MHz (MXT_EN)
1	1	100kHz~1 MHz (LXT_EN)

Bit 9: Unused bit, default "0"

Bit 8 (HLFS): Main or sub-oscillator select bit

HLFS = **"0":** CPU is set to select sub-oscillator when reset occurs.

HLFS = **"1":** CPU is set to select main-oscillator when reset occurs.

Bit 7 (ENWDTB): Watchdog timer enable/disable bit

ENWDTB = **"0":** Enable watchdog timer

ENWDTB = **"1":** Disable watchdog timer

Bit 6 (FSMD): Sub-oscillator type selection

Bits 5 ~ 4 (FMMD1 ~ FMMD0): Main Oscillator Type Selection

FSMD	FMMD1	FMMD0	Main Oscillator Type	Sub Oscillator Type
0	0	0	RC type	RC type
0	0	1	Crystal type	RC type
0	1	×	PLL type	RC type
1	0	0	RC type	Crystal type
1	0	1	Crystal type	Crystal type
1	1	×	PLL type	Crystal type

Bit 3 (HLP): Power consumption selection. If the system used to run in Green mode, it must be set to low power consumption to help support the energy saving. It is recommended that low power consumption mode is selected.

HLP = **"0":** Low power consumption mode

HLP = **"1":** High power consumption mode

Bits 2 ~ 0 (PR2 ~ PR0): Protect bit

PR2~PR0 are protect bits. Each protect status is as follows:

PR2	PR1	PR0	Protect
0	0	0	Enable
1	1	1	Disable

6.12.2 Code Option Register (Word 1)

	Bit 12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Mnemonic	ID12	ID11	ID11	ID9	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
1	High	High	High	High	High	High	High	High	High	High	High	High	High
0	Low	Low	Low	Low	Low	Low	Low	Low	Low	Low	Low	Low	Low
Default	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits 12 ~ 0 (ID12 ~ ID0): Customer ID

6.12.3 Code Option Register (Word 2)

	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mnemonic	-	-	-	-	-	-	-	-	-	-	-	LVR1	LVR0
1	High	High	High	High	High	High	High	High	High	High	High	High	High
0	Low	Low	Low	Low	Low	Low	Low	Low	Low	Low	Low	Low	Low
Default	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits 12 ~ 2: unused bits

Bits 1 ~ 0 (LVR1 ~ LVR0): Low voltage reset level selection.

LVR1	LVR0	VDD Reset Level	VDD Release Level
0	0	4.0V	4.2V
0	1	3.5V	3.7V
1	0	2.7V	2.9V
1	1	NA (Power-on Reset)	

6.13 Instruction Set

Each instruction in the Instruction Set is a 13-bit word divided into an OP code and one or more operands. Normally, all instructions are executed within one single instruction cycle (one instruction consists of 2 oscillator periods), unless the program counter is changed by Instructions "MOV R2,A", "ADD R2,A", or by instructions of arithmetic or logic operation on R2 (e.g., "SUB R2,A", "BS(C) R2,6", "CLR R2", ····). In this case, the execution takes two instruction cycles.

If for some reasons, the specification of the instruction cycle is not suitable for certain applications, try modifying the instruction as follows:

Execute within two instruction cycles the "JMP", "CALL", "RET", "RETL", and "RETI" instructions, or the conditional skip instructions ("JBS", "JBC", "JZ", "JZA", "DJZ", "DJZA") which were tested to be true. Also execute within two instruction cycles the instructions that are written to the program counter.

Additionally, the instruction set offers the following features:

1) Every bit of any register can be set, cleared, or tested directly.

2) The I/O register can be regarded as general register. That is, the same instruction can operate on I/O register.

6.13.1 Instruction Set Table

The following symbols are used with the Instruction Set table:

R = *Register designator that specifies which one of the registers (including operation and general purpose registers) is to be utilized by the instruction.*

b = *Bit field designator that selects the value for the bit located in the register R and which affects the operation.*

k = *8 or 10-bit constant or literal value*

Mnemonic			Operation	Status Affected
NOP			No Operation	None
DAA			Decimal Adjust A	C
SLEP			0 → WDT, Stop oscillator	T, P
WDTC			0 → WDT	T, P
IOW	R		A → IOCR	None*
ENI			Enable Interrupt	None
DISI			Disable Interrupt	None
RET			[Top of Stack] → PC	None
RETI			[Top of Stack] → PC, Enable Interrupt	None
IOR	R		IOCR → A	None*
MOV	R,	A	A → R	None
CLRA			0 → A	Z
CLR	R		0 → R	Z
SUB	A,	R	R-A → A	Z,C,DC
SUB	R,	A	R-A → R	Z,C,DC

(Continuation)

Mnemonic			Operation	Status Affected
DECA	R		R-1 → A	Z
DEC	R		R-1 → R	Z
OR	A,	R	A ∨ R → A	Z
OR	R,	A	A ∨ R → R	Z
AND	A,	R	A & R → A	Z
AND	R,	A	A & R → R	Z
XOR	A,	R	A ⊕ R → A	Z
XOR	R,	A	A ⊕ R → R	Z
ADD	A,	R	A + R → A	Z, C, DC
ADD	R,	A	A + R → R	Z, C, DC
MOV	A,	R	R → A	Z
MOV	R,	R	R → R	Z
COMA	R		/R → A	Z
COM	R		/R → R	Z
INCA	R		R+1 → A	Z
INC	R		R+1 → R	Z
DJZA	R		R-1 → A, skip if zero	None
DJZ	R		R-1 → R, skip if zero	None
RRCA	R		R(n) → A(n-1), R(0) → C, C → A(7)	C
RRC	R		R(n) → R(n-1), R(0) → C, C → R(7)	C
RLCA	R		R(n) → A(n+1), R(7) → C, C → A(0)	C
RLC	R		R(n) → R(n+1), R(7) → (C), C → (R(0)	C
SWAPA	R		R(0-3) → (A(4-7), R(4-7) → (A(0-3)	None
SWAP	R		R(0-3) → (R(4-7)	None
JZA	R		R+1 → A, skip if zero	None
JZ	R		R+1 → R, skip if zero	None
BC	R,	b	0→ (R(b)	None
BS	R,	b	1→ (R(b)	None
JBC	R,	b	if R(b)=0, skip	None
JBS	R,	b	if R(b)=1, skip	None

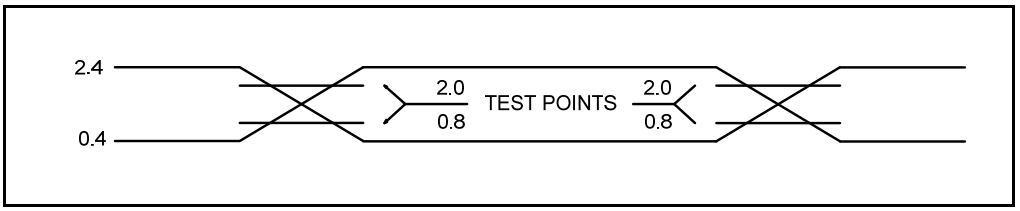
(Continuation)

Mnemonic			Operation	Status Affected
CALL	k		PC+1 → [SP], (Page, k) → (PC)	None
JMP	k		(Page, k) → (PC)	None
MOV	A,	k	k → A	None
OR	A,	k	A v k → A	Z
AND	A,	k	A & k → A	Z
XOR	A,	k	A ⊕ k → A	Z
RETL	k		k → A, [Top of Stack] → PC	None
SUB	A,	k	k-A → A	Z, C, DC
ADD	A,	k	k+A → A	Z, C, DC
PAGE	k		K->R3(5:6)	None
BANK	k		K->R4(7:6)	None
TBRD	R		If SBANK1 R5 Bit 7=0, machine code(7:0) → R Else machine code(12:8) → R(4:0), R(7:5)=(0,0,0)	None

* *This instruction is applicable to IOC50~IOF0 and IOC61~IOCE1.*

7 Timing Diagram

7.1 AC Test Input/Output Waveform



Note: *AC Testing: Input are driven at 2.4V for logic "**1**," and 0.4V for logic "**0**"*

Timing measurements are made at 2.0V for logic "1," and 0.8V for logic "0"

Figure 7-1(a) AC Test Timing Diagram

7.2 Reset Timing (CLK = "0")

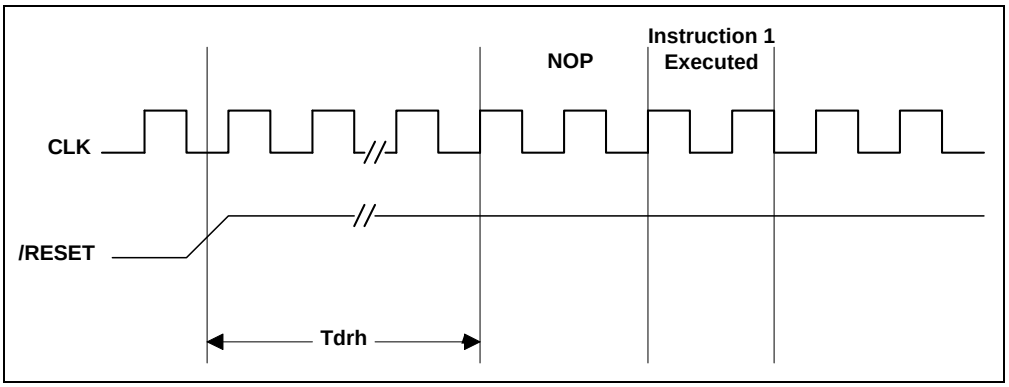
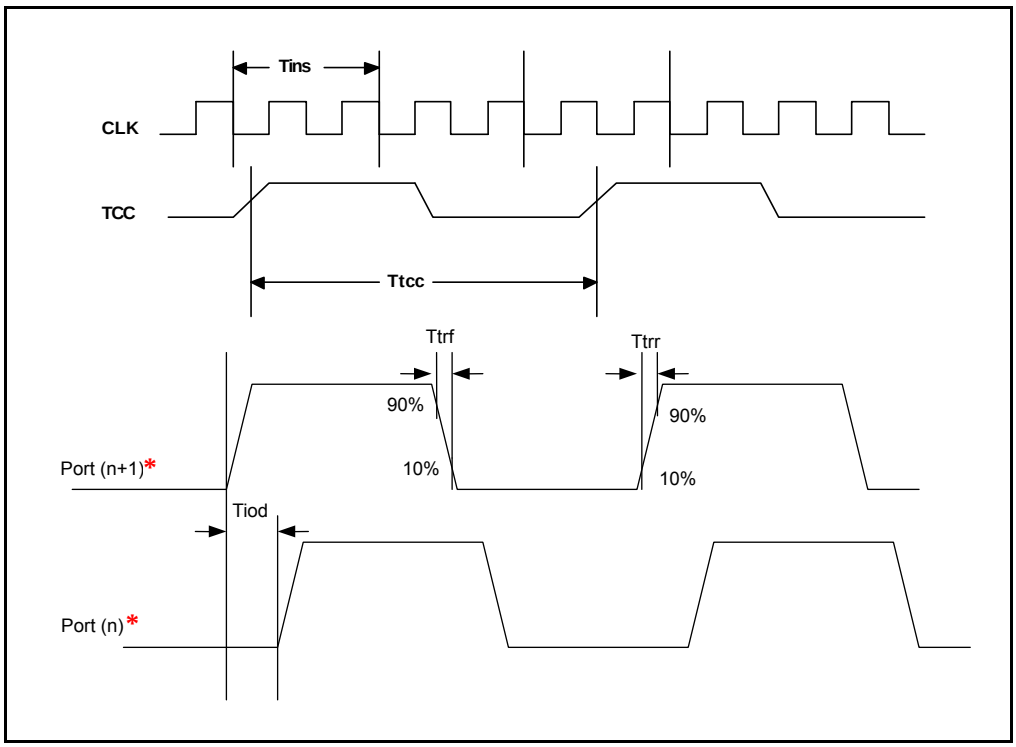


Figure 7-1(b) Reset Timing Diagram

7.3 TCC Input Timing (CLKS = “0”)



***n** = 0 , 2 , 4 , 6*

Figure 7-1(c) TCC Input Timing Diagram

8 Absolute Maximum Ratings

Items	Symbol	Condition	Rating		Unit
			Min.	Max.	
Supply voltage	VDD	–	GND-0.3	+7.0	V
Input voltage	V_I	Port 5 ~ Port 8	GND-0.3	VDD+0.3	V
Output voltage	V_O	Port 5 ~ Port 8	GND-0.3	VDD+0.3	V
Operation temperature	T_{OPR}	–	-40	85	℃
Storage temperature	T_{STG}	–	-65	150	℃
Power consumption	P_D	–	–	500	mW
Operating Frequency	–	–	32.768K	10M	Hz

9 Electrical Characteristics

9.1 DC Electrical Characteristics

- Ta= -40°C ~85 °C, VDD= 5.0V, GND= 0V

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
FXT	Crystal: VDD to 5V	Two cycles with two clocks	32.768	8M	10M	kHz
Fs	Sub-oscillator	Two cycles with two clocks	–	32.768	–	kHz
ERIC	External R, Internal C for Sub-oscillator	R: 300KΩ, internal capacitance	270	384	500	kHz
	External R, Internal C for Sub-oscillator	R: 2.2MΩ, internal capacitance	22.9	32.768	42.6	kHz
IIL	Input Leakage Current for Input pins	VIN = VDD, GND	-1	0	1	μA
VIH1	Input High Threshold Voltage (Schmitt Trigger)	Ports 5, 6, 7, 8	2.0	–	–	V
VIL1	Input High Threshold Voltage (Schmitt Trigger)	Ports 5, 6, 7, 8	–	–	0.8	V
VIHT1	Input High Threshold Voltage (Schmitt Trigger)	/RESET	2.0	–	–	V
VILT1	Input Low Threshold Voltage (Schmitt Trigger)	/RESET	–	–	0.8	V
VIHT2	Input High Threshold Voltage (Schmitt Trigger)	TCC, INT0, INT1	2.0	–	–	V
VILT2	Input Low Threshold Voltage (Schmitt Trigger)	TCC, INT0, INT1	–	–	0.8	V
IOH1	Output High Voltage (Ports 5~8)	VOH = 2.4V, IROCS="0"	-10	–	–	mA
IOL1	Output Low Voltage (Ports 5~8)	VOL = 0.4V, IROCS="0"	–	–	10	mA
IOH2	Output high Voltage (P5.7/IROUT Pin)	VOH = 2.4V, IROCS="1"	-20	–	–	mA
IOL2	Output Low Voltage (P5.7/IR OUT Pin)	VOL = 0.4V, IROCS="1"	–	–	20	mA
IPH	Pull-High Current	Pull-high active, input pin at GND	-55	-75	-95	μA
IPL	Pull-Low Current	Pull-low active, input pin at VDD	55	75	95	μA
ISB	Sleep Mode Current	All input and I/O pins at VDD, Output pin floating, WDT disabled	–	0.5	1.5	μA
ICC1	Idle Mode Current	/RESET= 'High', CPU OFF, Sub-oscillator clock (32.768kHz) ON, output pin floating, LCD enabled, no load	–	14	18	μA

(Continuation)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
ICC2	Green Mode Current	/RESET= 'High', CPU ON, Sub-oscillator clock (32.768kHz), Output pin floating, WDT enabled, LCD enabled	–	22	30	μA
ICC3	Normal Mode	/RESET= 'High', Fosc=4 MHz (Crystal type, CLKS="0"), Output pin floating	–	2.2	3	mA
ICC4	Normal Mode	/RESET= 'High', Fosc=10 MHz (Crystal type, CLKS="0"), Output pin floating	–	3.1	4	mA

■ Ta= -40°C ~85 °C, VDD= 3.0V, GND= 0V

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
FXT	Crystal: VDD to 5V	Two cycles with two clocks	32.768	8M	10M	kHz
Fs	Sub-Oscillator	Two cycles with two clocks	–	32.768	–	kHz
ERIC	External R, Internal C for Sub-Oscillator	R: 300KΩ, internal capacitance	270	384	500	kHz
	External R, Internal C for Sub-Oscillator	R: 2.2MΩ, internal capacitance	22.9	32.768	42.6	kHz
IIL	Input Leakage Current for Input Pins	VIN = VDD, GND	-1	0	1	μA
VIH1	Input High Threshold Voltage (Schmitt Trigger)	Ports 5, 6, 7, 8	1.8	–	–	V
VIL1	Input High Threshold Voltage (Schmitt Trigger)	Ports 5, 6, 7, 8	–	–	0.6	V
VIHT1	Input High Threshold Voltage (Schmitt Trigger)	/RESET	1.8	–	–	V
VILT1	Input Low Threshold Voltage (Schmitt Trigger)	/RESET	–	–	0.6	V
VIHT2	Input High Threshold Voltage (Schmitt Trigger)	TCC, INT0, INT1	1.8	–	–	V
VILT2	Input Low Threshold Voltage (Schmitt Trigger)	TCC, INT0, INT1	–	–	0.6	V
IOH1	Output High Voltage (Ports 5~8)	VOH = 2.4V, IROCS=”0”	-1.8	–	–	mA
IOL1	Output Low Voltage (Ports 5~8)	VOL = 0.4V, IROCS=”0”	–	–	6	mA

(Continuation)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
IOH1	Output high voltage (P5.7/IROUT Pin)	VOH = 2.4V, IROCS="1"	-3.5	–	–	mA
IOL2	Output Low Voltage (P5.7/IR OUT Pin)	VOL = 0.4V, IROCS="1"	–	–	12	mA
IPH	Pull-High Current	Pull-high active, input pin at GND	-16	-23	-30	μA
IPL	Pull-Low Current	Pull-low active, input pin at VDD	16	23	30	μA
ISB	Sleep Mode Current	All input and I/O pins at VDD, Output pin floating, WDT disabled	–	0.1	1	μA
ICC1	Idle Mode Current	/RESET= 'High', CPU OFF, Sub-oscillator clock (32.768kHz) ON, output pin floating, LCD enabled, no load	–	4	8	μA
ICC2	Green Mode Current	/RESET= 'High', CPU ON, Sub-oscillator clock (32.768kHz), Output pin floating, WDT enabled, LCD enabled	–	10	20	μA
ICC3	Normal Mode	/RESET= 'High', Fosc=4MHz (Crystal type, CLKS="0"), Output pin floating	–	0.73	1.2	mA

9.2 AC Electrical Characteristics

■ Ta=- 40°C ~ 85 °C, VDD=5V±5%, GND=0V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Dclk	Input CLK duty cycle	–	45	50	55	%
Tins	Instruction cycle time (CLKS="0")	Crystal type	100	–	DC	ns
		RC type	500	–	DC	ns
Ttcc	TCC input period	–	(Tins+20)/N*	–	–	ns
Tdrh	Device reset hold time	Ta = 25°C	11.3	16.2	21.6	ms
Trst	/RESET pulse width	Ta = 25°C	2000	–	–	ns
Twdt	Watchdog timer period	Ta = 25°C	11.3	16.2	21.6	ms
Tset	Input pin setup time	–	–	0	–	ns
Thold	Input pin hold time	–	–	20	–	ns
Tdelay	Output pin delay time	Cload=20pF	–	50	–	ns

* **N** = Selected prescaler ratio

APPENDIX

A Package Type

Name	Package Type	Pin Count	Package Size
EM78P468NBH	Dice	59	–
EM78P468NBQ64	QFP	64	14 mm × 20 mm
EM78P468NBL64	LQFP	64	7 mm × 7 mm
EM78P470NL44	LQFP	44	10 mm × 10 mm
EM78P470NQ44	QFP	44	10 mm × 10 mm

A.1 Green Products Compliance

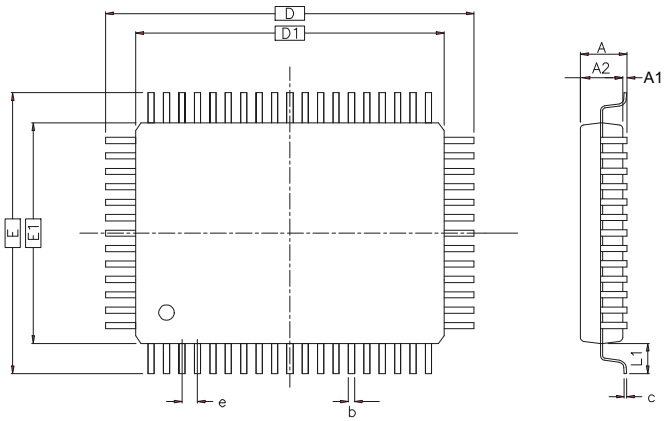
These MCUs are bona-fide Green products which do not contain hazardous substances. They complied with the third edition of Sony SS-00259 standard.

The Pb contents are less the 100ppm and complied with Sony specifications.

Part No.	EM78P468NxS/xJ
Electroplate type	Pure Tin
Ingredient (%)	Sn: 100%
Melting point (°C)	232°C
Electrical resistivity (μΩ cm)	11.4
Hardness (hv)	8~10
Elongation (%)	>50%

B Package Information

B.1 QFP – 64

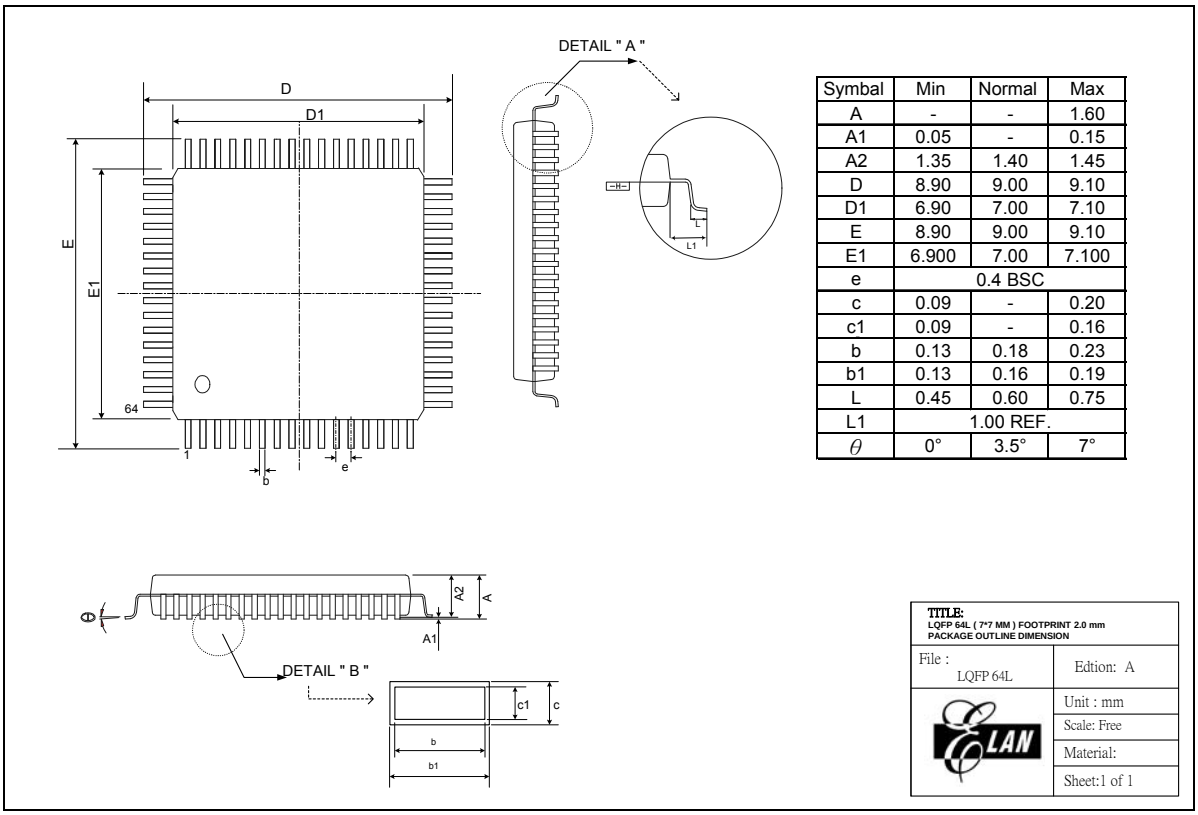


Symbal	Min	Normal	Max
A	—	—	3.40
A1	0.25	—	—
A2	2.55	2.72	3.05
D		25.00 BASIC	
D1		20.00 BASIC	
E		19.00 BASIC	
E1		14.00 BASIC	
θ	0°	3.5	7°
c	0.11	0.15	0.23
L	1.15	1.3	1.45
L1		2.50 REF	
b	0.35	0.4	0.50
e		1.00 BSC	

TITLE: QFP-64 L(14*20 MM) FOOTPRINT 5.0mm PACKAGE OUTLINE DIMENSION	
File : QFP 64L	Edtion: A
	Unit : mm
	Scale: Free
	Material:
	Sheet:1 of 1

Figure B-1 EM78P468NBQ64 64-Pin QFP Package Type

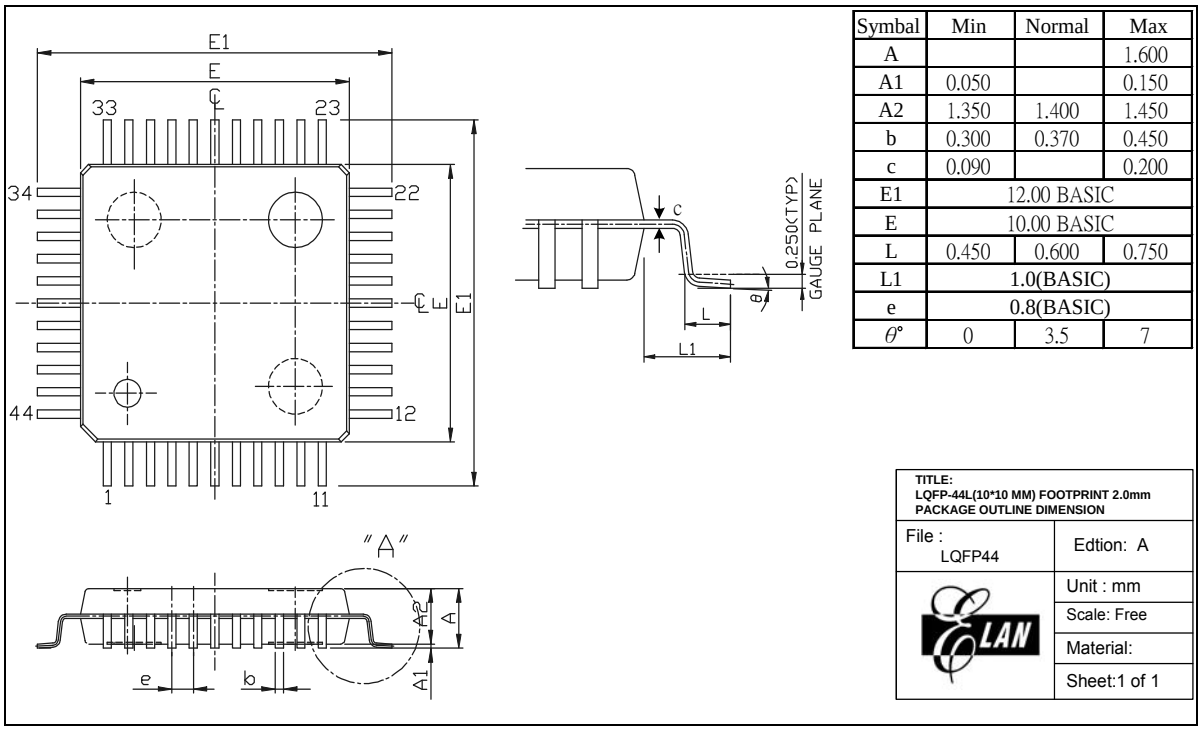
B.2 LQFP – 64



Symbal	Min	Normal	Max
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
D	8.90	9.00	9.10
D1	6.90	7.00	7.10
E	8.90	9.00	9.10
E1	6.900	7.00	7.100
e	0.4 BSC		
c	0.09	-	0.20
c1	0.09	-	0.16
b	0.13	0.18	0.23
b1	0.13	0.16	0.19
L	0.45	0.60	0.75
L1	1.00 REF.		
θ	0°	3.5°	7°

Figure B-3 EM78P468NBL64 64-Pin LQFP Package Type

B.3 LQFP – 44



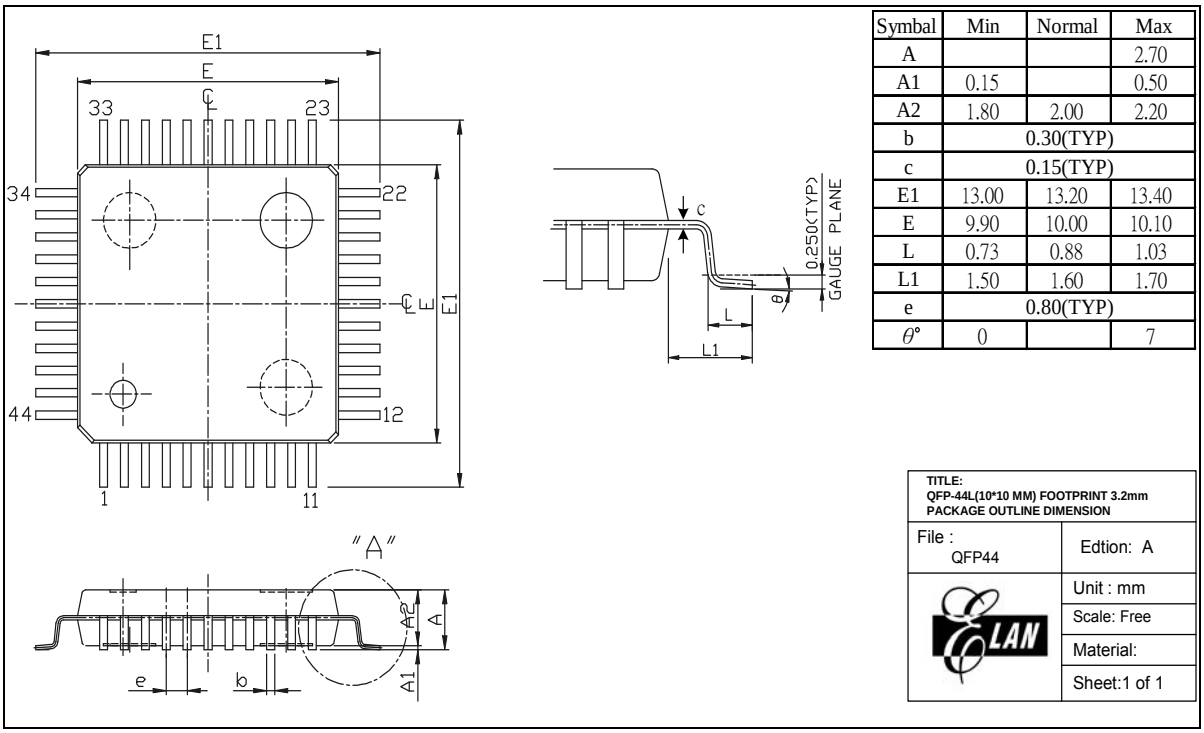
Symbal	Min	Normal	Max
A			1.600
A1	0.050		0.150
A2	1.350	1.400	1.450
b	0.300	0.370	0.450
c	0.090		0.200
E1	12.00 BASIC		
E	10.00 BASIC		
L	0.450	0.600	0.750
L1	1.0(BASIC)		
e	0.8(BASIC)		
θ°	0	3.5	7

TITLE:
LQFP-44L(10*10 MM) FOOTPRINT 2.0mm
PACKAGE OUTLINE DIMENSION

File : LQFP44	Edtion: A
	Unit : mm
	Scale: Free
	Material:
	Sheet:1 of 1

Figure B-4 EM78P470NL44 44-Pin LQFP Package Type

B.4 QFP – 44



Symbal	Min	Normal	Max
A			2.70
A1	0.15		0.50
A2	1.80	2.00	2.20
b		0.30(TYP)	
c		0.15(TYP)	
E1	13.00	13.20	13.40
E	9.90	10.00	10.10
L	0.73	0.88	1.03
L1	1.50	1.60	1.70
e		0.80(TYP)	
θ°	0		7

TITLE:
QFP-44L(10*10 MM) FOOTPRINT 3.2mm
PACKAGE OUTLINE DIMENSION

File : QFP44	Edtion: A
	Unit : mm
	Scale: Free
	Material:
	Sheet:1 of 1

Figure B-5 EM78P470NQ44 44-Pin QFP Package Type