EM78P516N

8-Bit Microcontroller

Product Specification

DOC. VERSION 1.0

ELAN MICROELECTRONICS CORP.

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APPENDIX

Specification Revision History

Doc. Version	Revision Description	Date
1.0	Initial version	2015/04/09

1 General Description

The EM78P516N is an 8-bit microprocessor designed and developed with low-power and high-speed CMOS technology. Integrated onto a single chip are on-chip Watchdog Timer (WDT), Data RAM, ROM, Programmable Real Time Clock Counter, Internal/External Interrupt, Power-down mode, LCD driver, Infrared Transmitter function, and tri-state I/O. The series has an on-chip 6K×13-bit Electrical One Time Programmable Read Only Memory (OTP-ROM). The EM78P516N provides multi-protection bits to prevent intrusion of user's OTP memory code. Seven Code option bits are available to meet user's requirements. Special 13 bits customer ID options are provided as well.

With its enhanced OTP-ROM feature, the EM78P516N provides a convenient way of developing and verifying user's programs. Moreover, this OTP device offers the advantages of easy and effective program updates, using development and programming tools. Users can avail of the ELAN Writer to easily program their development code.

2 Features

- CPU Configuration
  - 6K×13 bits on-chip OTP-ROM
  - 144 bytes general purpose register
  - 128 bytes on-chip data RAM
  - 272 bytes SRAM
    144 bytes general purpose register
    128 bytes on-chip data RAM
  - 8-level stacks for subroutine nesting
  - Power-on voltage detector provided (1.7±0.1V) for EM78P516N
- I/O Port Configuration
  - Typically, 12 bidirectional tri-state I/O ports.
  - 16 bidirectional tri-state I/O ports shared with LCD segment output pin.
  - Up to 28 bidirectional tri-state I/O ports
  - Four programmable high-sink/drive I/O ports: P5, P6, P7, P8
- Operating Voltage and Temperature Range:

  EM78P516N
  - Commercial: 2.1V ~ 5.5V. (at 0°C ~+70°C)
  - Industrial: 2.3V ~ 5.5V. (at -40°C ~+85°C)
- Operating Mode:
  - Normal mode: The CPU is operated on main oscillator frequency (Fm)
  - Green mode: The CPU is operated on sub-oscillator frequency (Fs) and main oscillator (Fm) is stopped
  - Idle mode: CPU idle, LCD display remains working
  - Sleep mode: The whole chip stops working
    - Input port wake-up function (Port 6, Port 8). Works on Idle and Sleep mode.
    - Operation speed: DC ~ 10 MHz clock input
    - Dual clock operation
- Oscillation Mode
  - High frequency oscillator can select among Crystal, RC, or PLL (phase lock loop)
  - Low frequency oscillator can select between Crystal or RC mode
- Peripheral Configuration
  - 8-bit real Time Clock/Counter (TCC)
  - One infrared transmitter/PWM generator function
  - Four sets of 8 bits auto reload down-counting timer can be used as interrupt sources
    - Counter 1: independent down-counting timer
    - Counter 2, High Pulse Width Timer (HPWT), and Low Pulse Width Timer (LPWT) shared with IR function.
    - Programmable free running on-chip Watchdog Timer (WDT). This function can operate in Normal, Green and Idle mode.
    - 15-channels Analog-to-Digital Converter with 12bit resolution +1 internal reference for Vref and 1/2Vdd (power detector)
- Eight Interrupt Sources: Three External and Five Internal
  - Internal interrupt source: TCC; Counters 1 and 2 High/Low pulse width timer
  - External interrupt source : INT0, INT1 and Pin change wake-up (Port 6 and Port 8)
- LCD Circuit
  - Common driver pins: 4
  - Segment driver pins: 32
  - LCD Bias: 1/3, 1/2 bias
  - LCD Duty: 1/4, 1/3, 1/2 duty
- Package Type:
  - Dice form: 59 pins
  - QFP-64 pin: EM78P516NQ64 (Body 14mm×20mm)
  - LQFP-64 pin: EM78P516NL64 (Body 7mm×7mm)
  - LQFP-44 pin: EM78P516NL44 (Body 10mm×10mm)
  - QFP-44 pin: EM78P516NQ44 (Body 10mm×10mm)
  - QFP-64 pin: EM78P516NQ64B (Body 14mm×14mm)
  - LQFP-48 pin: EM78P516NL48 (Body 7mm×7mm)

  Note: *These are Green products which do not contain hazardous substances*

3 Pin Assignment

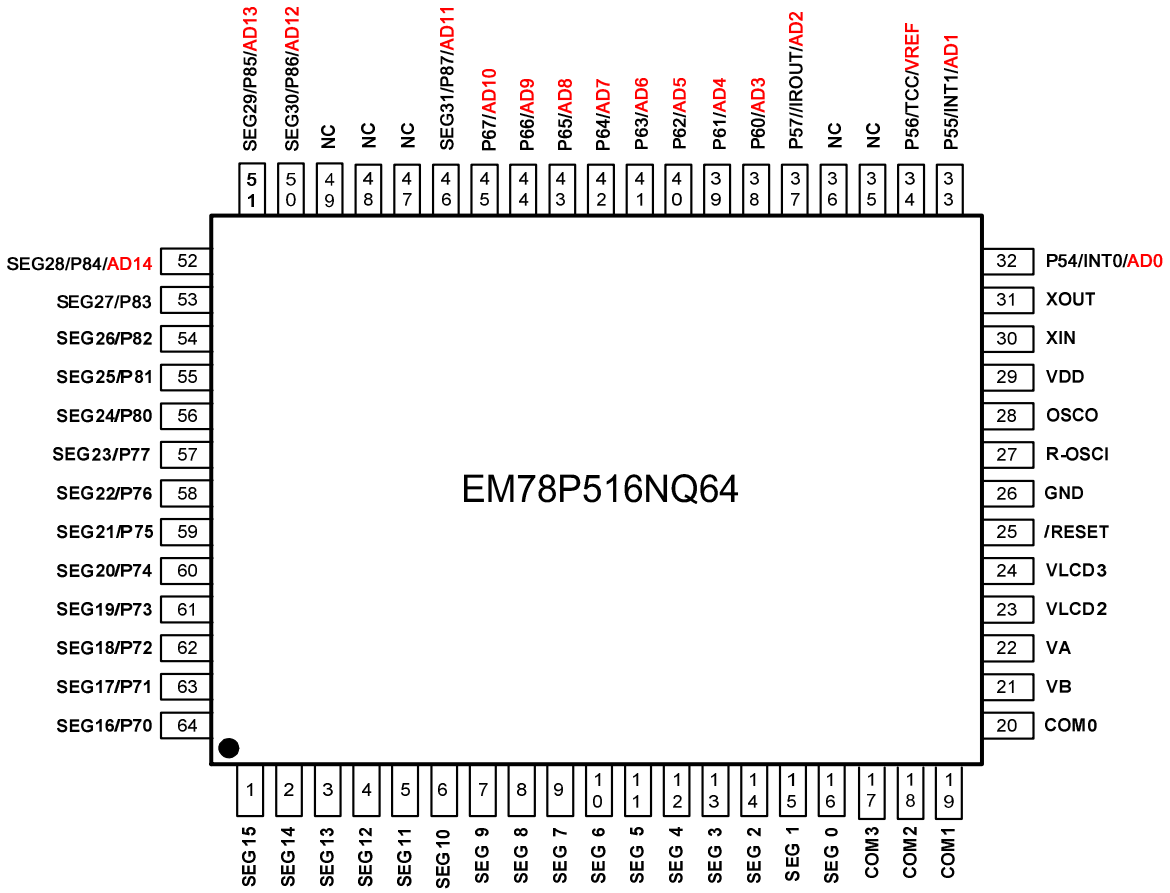


Figure 3-1 64-pin QFP EM78P516NQ64 Pin Assignment

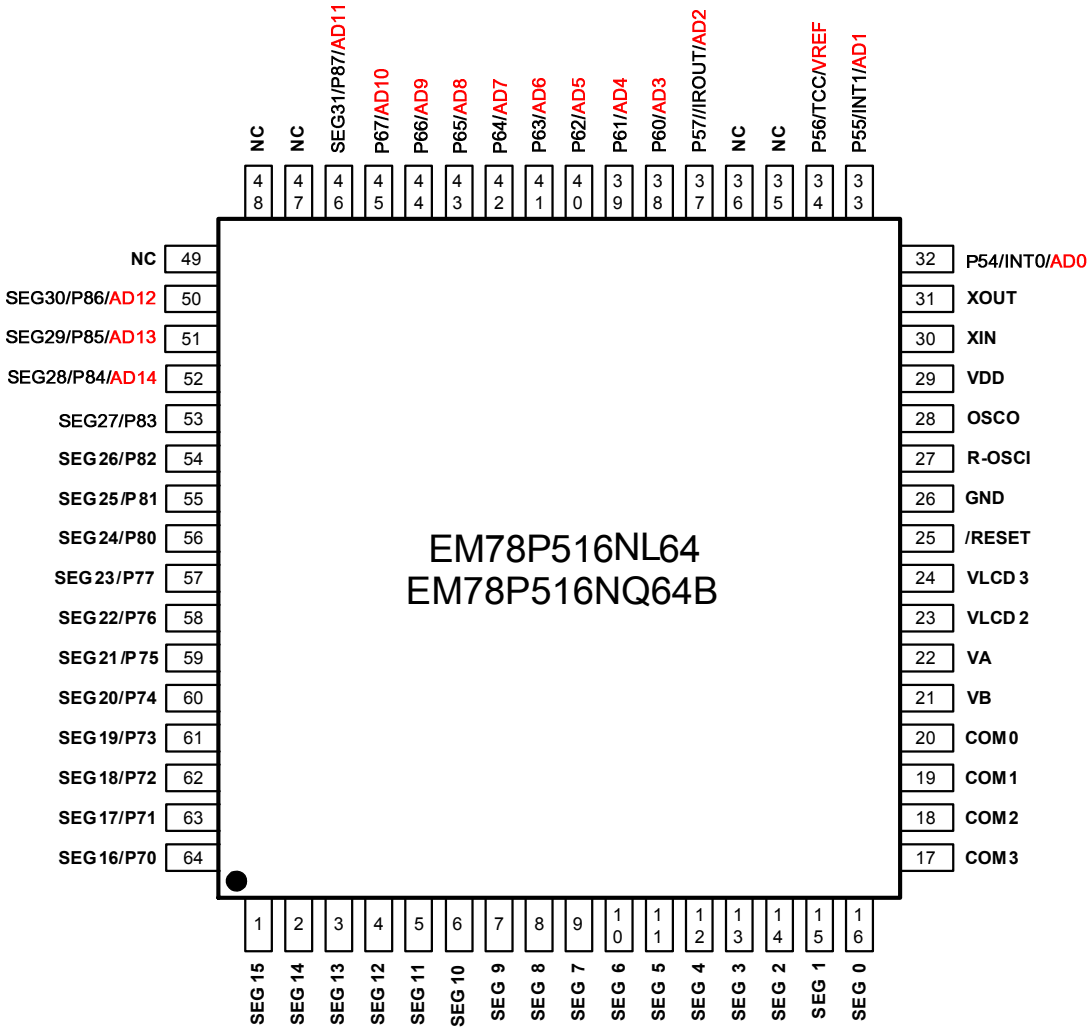


Figure 3-2 64-Pin LQFP/QFP EM78P516NL64/EM78P516NQ64B Pin Assignment

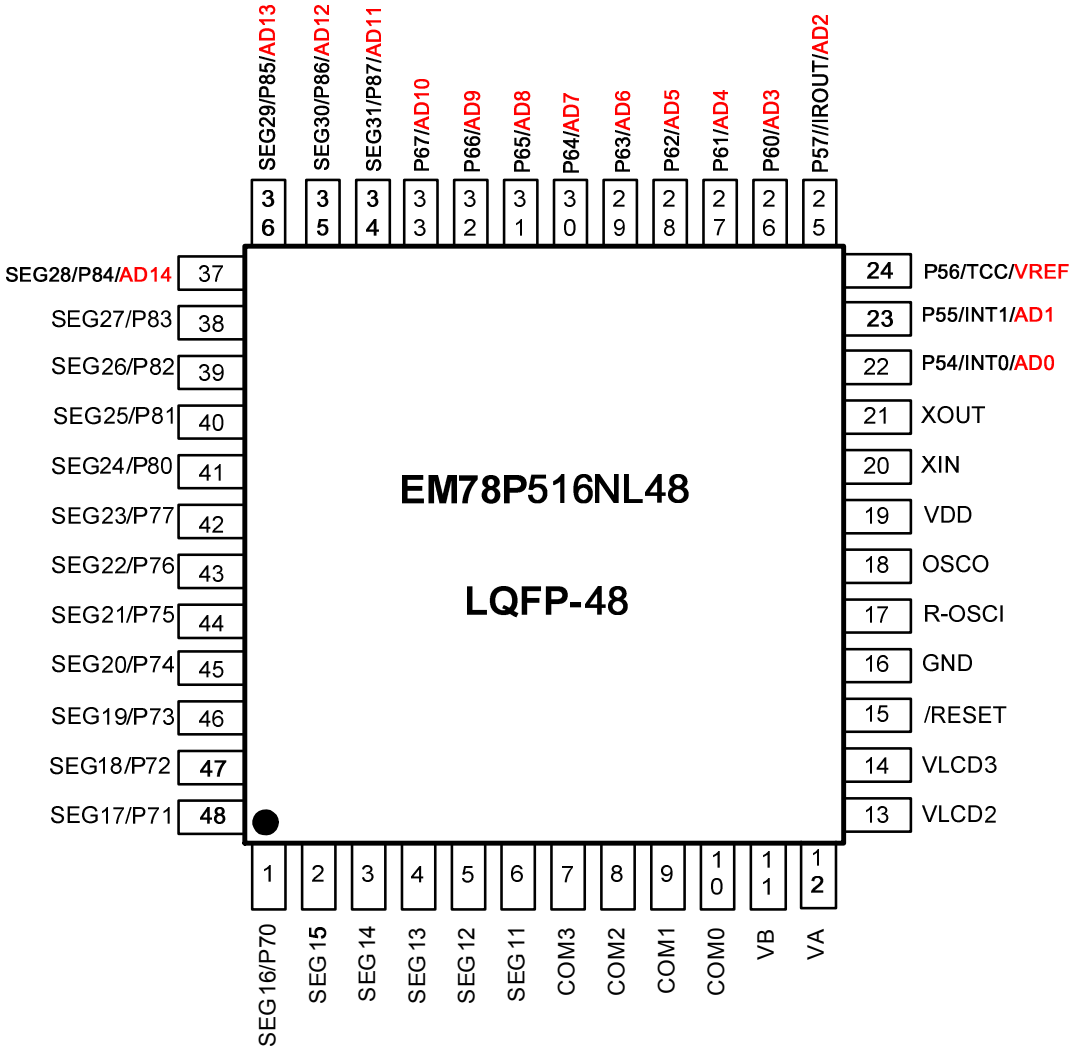


Figure 3-3 48-Pin LQFP/QFP EM78P516NL48 Pin Assignment

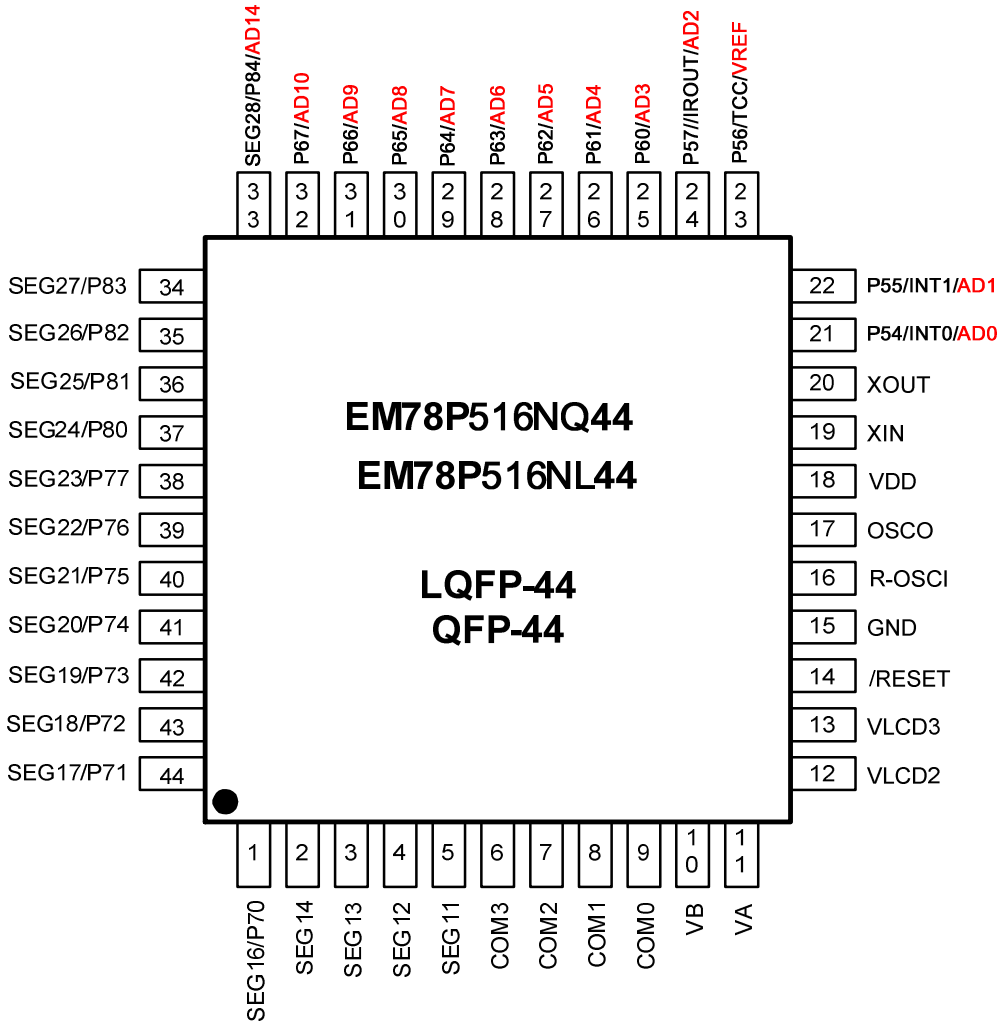


Figure 3-4 44-Pin LQFP/QFP EM78P516NQ44/EM78P516NL44 Pin Assignment

4 Pin Description

Symbol	Function	Input Type	Output Type	Description
P54/INT0 (ACLK)	P54	ST	CMOS	Bidirectional I/O pin
	INT0	ST	–	External interrupt pin. The INT0 interrupt source can be set to falling or rising edge by IOC71 Register Bit 7 (INT_EDGE). Wakes up from Sleep mode and Idle mode when the pin status changes.
	(ACLK)	ST	–	ACLK pin for Writer programming
P55/INT1 (DINCK)	P55	ST	CMOS	Bidirectional I/O pin
	INT1	ST	–	External interrupt pin The Interrupt source is a falling edge signal. Wakes up from Sleep mode and Idle mode when the pin status changes.
	(DINCK)	ST	–	DINCK pin for Writer programming
P56/TCC (DATAIN)	P56	ST	CMOS	Bidirectional I/O pin. This pin works in Normal/ Green/Idle mode.
	TCC	ST	–	TCC External input pin
	(DATAIN)	ST	–	DATAIN pin for Writer programming
P57/IROUT	P57	ST	CMOS	Bidirectional I/O pin. This pin is capable of sinking 20 mA / 5V.
	IROUT	ST	–	IR/PWM mode output pin
P60 (PGMB)	P60	ST	CMOS	Programmable pull-high, pull-down and open-drain. All pins wake up from Sleep and Idle modes when the pin status changes.
	(PGMB)	ST	–	PGMB pin for Writer programming
P61 (OEB)	P61	ST	CMOS	Programmable pull-high, pull-down and open-drain. All pins wake up from Sleep and Idle modes when the pin status changes.
	(OEB)	ST	–	OEB pin for Writer programming
P62	P62	ST	CMOS	Bidirectional I/O pin with programmable pull-high, pull-down and open-drain. All pins wake up from Sleep and Idle modes when the pin status changes.
P63	P63	ST	CMOS	Bidirectional I/O pin with programmable pull-high, pull-down and open-drain. All pins wake up from Sleep and Idle modes when the pin status changes.

Symbol	Function	Input Type	Output Type	Description
P64	P64	ST	CMOS	Bidirectional I/O pin with programmable pull-high, pull-down and open-drain. All pins wake up from Sleep and Idle modes when the pin status changes.
P65	P65	ST	CMOS	Bidirectional I/O pin with programmable pull-high, pull-down and open-drain. All pins wake up from Sleep and Idle modes when the pin status changes.
P66	P66	ST	CMOS	Bidirectional I/O pin with programmable pull-high, pull-down and open-drain. All pins wake up from Sleep and Idle modes when the pin status changes.
P67	P67	ST	CMOS	Bidirectional I/O pin with programmable pull-high, pull-down and open-drain. All pins wake up from Sleep and Idle modes when the pin status changes.
COM3~0	COM3~0	–	AN	LCD common output pin
SEG0~15	SEG0~15	–	AN	LCD segment output pin
SEG16/P70	SEG16	–	AN	LCD segment output pin
	P70	ST	CMOS	Bidirectional I/O pin. All pins wake up from Sleep and Idle modes when the pin status changes.
SEG17/P71	SEG17	–	AN	LCD segment output pin
	P71	ST	CMOS	Bidirectional I/O pin. All pins wake up from Sleep and Idle modes when the pin status changes.
SEG18/P72	SEG18	–	AN	LCD segment output pin
	P73	ST	CMOS	Bidirectional I/O pin. All pins wake up from Sleep and Idle modes when the pin status changes.
SEG19/P73	SEG19	–	AN	LCD segment output pin
	P73	ST	CMOS	Bidirectional I/O pin. All pins wake up from Sleep and Idle modes when the pin status changes.
SEG20/P74	SEG20	–	AN	LCD segment output pin
	P74	ST	CMOS	Bidirectional I/O pin. All pins wake up from Sleep and Idle modes when the pin status changes.
SEG21/P75	SEG21	–	AN	LCD segment output pin
	P75	ST	CMOS	Bidirectional I/O pin. All pins wake up from Sleep and Idle modes when the pin status changes.

Symbol	Function	Input Type	Output Type	Description
SEG22/P76	SEG22	–	AN	LCD segment output pin
	P76	ST	CMOS	Bidirectional I/O pin. All pins wake up from Sleep and Idle modes when the pin status changes.
SEG23/P77	SEG23	–	AN	LCD segment output pin
	P77	ST	CMOS	Bidirectional I/O pin. All pins wake up from Sleep and Idle modes when the pin status changes.
SEG24/P80	SEG24	–	AN	LCD segment output pin
	P80	ST	CMOS	Bidirectional I/O pin with programmable pull-high. All pins wake up from Sleep and Idle modes when the pin status changes.
SEG25/P81	SEG25	–	AN	LCD segment output pin
	P81	ST	CMOS	Bidirectional I/O pin with programmable pull-high. All pins wake up from Sleep and Idle modes when the pin status changes.
SEG26/P82	SEG26	–	AN	LCD segment output pin
	P82	ST	CMOS	Bidirectional I/O pin with programmable pull-high. All pins wake up from Sleep and Idle modes when the pin status changes.
SEG27/P83	SEG27	–	AN	LCD segment output pin
	P83	ST	CMOS	Bidirectional I/O pin with programmable pull-high. All pins wake up from Sleep and Idle modes when the pin status changes.
SEG28/P84	SEG28	–	AN	LCD segment output pin
	P84	ST	CMOS	Bidirectional I/O pin with programmable pull-high. All pins wake up from Sleep and Idle modes when the pin status changes.
SEG29/P85	SEG29	–	AN	LCD segment output pin
	P85	ST	CMOS	Bidirectional I/O pin with programmable pull-high. All pins wake up from Sleep and Idle modes when the pin status changes.
SEG30/P86	SEG30	–	AN	LCD segment output pin
	P86	ST	CMOS	Bidirectional I/O pin with programmable pull-high. All pins wake up from Sleep and Idle modes when the pin status changes.
SEG31/P87	SEG31	–	AN	LCD segment output pin
	P87	ST	CMOS	Bidirectional I/O pin with programmable pull-high. All pins wake up from Sleep and Idle modes when the pin status changes.

Symbol	Function	Input Type	Output Type	Description
VB	VB	–	AN	Connects capacitors for LCD bias voltage
VA	VA	–	AN	Connects capacitors for LCD bias voltage
VLCD2	VLCD2	–	AN	One of LCD bias voltage
VLCD3	VLCD3	–	AN	One of LCD bias voltage
/RESET (VPP)	/RESET	ST	–	General-purpose Input only Low active. If it remains at logic low, the device will reset. /RESET pin for writer programming
	VPP	ST	–	Vpp pin for Writer programming
R-OSCI	R-OSCI	AN	–	In Crystal mode: crystal input In RC mode: resistor pull high In PLL mode: connect a 0.01µF capacitance to GND Connect a 0.01 µF capacitor to GND and code option selects PLL mode when high oscillator is not used.
OSCO	OSCO	–	XTAL	In Crystal mode: crystal input In RC mode: instruction clock output
Xin	Xin	XTAL	–	In Crystal mode: Input pin for sub-oscillator. Connect to a 32.768kHz crystal.
Xout	Xout	–	XTAL	In Crystal mode: Connect to a 32.768kHz crystal. In RC mode: instruction clock output
NC	NC	–	–	No connection
VDD	VDD	Power	–	Power
GND	GND	Power	–	Ground

***Legend*: ST:** *Schmitt Trigger input* **CMOS:** *CMOS output*
AN: *analog pin* **XTAL:** *oscillation pin for crystal / resonator*

Pin Status with Enabled Functions

Pin Function	I/O Status		Pin Control		
	I/O Direction	Pin Change WK/Int.	Pull High	Pull Low	O.D.
General Input	Input	S/W	S/W	S/W	S/W
General Output	Output	Disable	S/W	S/W	S/W
TCC	Input	Disable	S/W	S/W	S/W
LCD Driver	Input	Disable	Disable	Disable	S/W
TC-OUT	Output	Disable	Initial: Enable	S/W	S/W
Reset	Input	Disable	S/W	S/W	S/W
EX_INT	Input	Disable	S/W	S/W	S/W
OSCI	Input	Disable	Disable	Disable	S/W
OSCO	Input	Disable	Disable	Disable	S/W

Disable → It is always disabled

Enable → It is always enabled

S/W → It can be controlled by the register, the initial value is disabled.

1. If the pin is not working as general I/O, it is a must to disable the Pin Change Wake-up/Interrupt function.

2. Priority: digital function output > digital function input > general I/O

5 Block Diagram

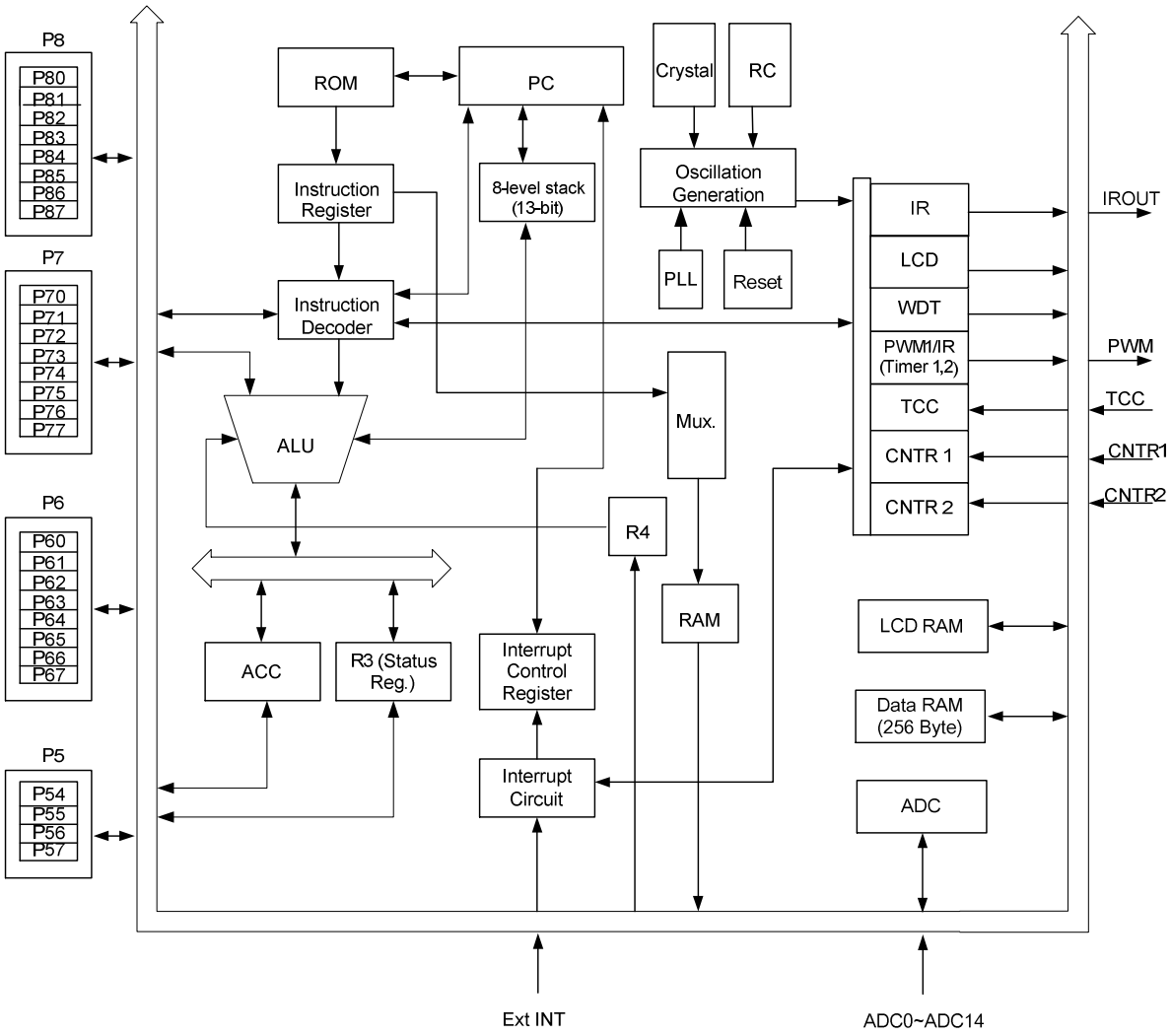


Figure 5 System Block Diagram

6 Functional Description

6.1 Operational Registers

6.1.1 R0, IAR (Indirect Addressing Register)

(Address: 00h)

R0 is not a physically implemented register. Its major function is to perform as an indirect address pointer. Any instruction using R0 as a register, actually accesses the data pointed by the RAM Select Register (R4).

6.1.2 R1, TCC (Timer Clock Counter)

(Address: 01h)

The Timer Clock Counter is incremented by an external signal edge applied to TCC, or by the instruction cycle clock. It is written and read by the program as any other register.

6.1.3 R2, PC (Program Counter)

(Address: 02h)

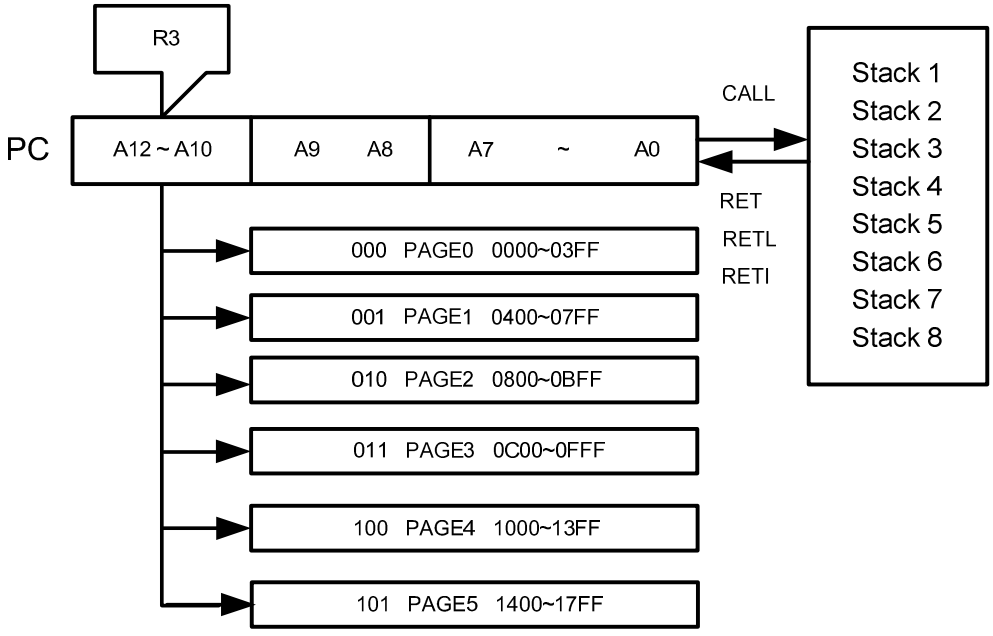


Figure 6-1 Program Counter Organization

- The structure of R2 is depicted in Figure 6-1, *Program Counter Organization*.
- The configuration structure generates 6K×13 bits on-chip ROM addresses to the relative programming instruction codes.
- The contents of R2 are all set to "0"s when a Reset condition occurs.

- "JMP" instruction allows direct loading of the lower 10 program counter bits. Thus, "JMP" allows the PC to jump to any location within a page.
- "CALL" instruction loads the lower 10 bits of the PC, and PC+1 are pushed onto the stack. Thus, the subroutine entry address can be located anywhere within a page.
- "RET" ("RETL k", "RETI") instruction loads the program counter with the contents at the top of the stack.
- "ADD R2, A" allows a relative address to be added to the current PC, and the ninth and above bits of the PC will increment progressively.
- "MOV R2, A" allows loading of an address from the "A" register to the lower 8 bits of the PC, and the ninth and tenth bits (A8 ~ A9) of the PC will remain unchanged.
- The most significant bits (A10~A12) will be loaded with the content of PS0~PS1 in the Status register (R3) upon execution of a "JMP" or "CALL" instruction.

Address	Bank 0 Registers	Bank 1 Registers	IOC Page 0 Registers. (R5 Bit 0 → 0)	IOC Page 1 Registers (R5 Bit 0 → 1)
00	**R0** (Indirect Addressing Register)			
01	**R1** (Time Clock Counter)			
02	**R2** (Program Counter)			
03	**R3** (Status Register and ROM page)			
04	**R4** (RAM Select Register)			
05	**R5** (Port 5 and IOC page)	**R5** (P5HDSCR)	**IOC50** (I/O Port Control Register)	
06	**R6** (Port 6)	**R6** (P6HDSCR)	**IOC60** (I/O Port Control Register)	**IOC61** (Wake up register)
07	**R7** (Port 7)	**R7** (P78HDSCR)	**IOC70** (I/O Port Control Register)	**IOC71** (TCC control register)
08	**R8** (Port 8)	**R8** (ADC input select register 1)	**IOC80**(I/O Port Control Register)	**IOC81** (WDT control register)
09	**R9** (LCD Control Register)	**R9** (ADC input select register 2)	**IOC90** (128 byte RAM address)	**IOC91** (Counter 1,2 control)
0A	**RA** (LCD contrast and Address)	**RA** (ADC control register)	**IOCA0** (128 byte RAM data buffer)	**IOCA1** (High/Low pulse timer control)
0B	**RB** (LCD data buffer)	**RB** (ADC input channel selection register)	**IOCB0** (Counter 1 preset)	**IOCB1** (Port 6 pull-high control)
0C	**RC** (Counter Enable Register)	**RC** (Low byte of ADC Data)	**IOCC0** (Counter 2 preset)	**IOCC1** (Port 6 open drain control)
0D	**RD** (System clock Control Register)	**RD** (High byte of ADC Data)	**IOCD0** (High-pulse timer preset)	**IOCD1** (Port 8 pull-high control)
0E	**RE** (IR Control Register)	**RE** (Interrupt Mask Register 2)	**IOCE0** (Low-pulse timer preset)	**IOCE1** (Port 6 pull-low control)
0F	**RF** (Interrupt Status Register 1)	**RF** (Interrupt Status Register 2)	**IOCF0** (Interrupt Mask Register1)	
10 : 1F	General Registers			
20 : 3F	**Bank 0**	**Bank 1**	**Bank 2**	**Bank 3**

Figure 6-2 Data Memory Configuration

6.1.4 R3, SR (Status Register)

(Address: 03h)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PS2	PS1	PS0	T	P	Z	DC	C
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7 ~ 5 (PS2 ~ 0): Page Select bits

PS2	PS1	PS0	Program memory page (Address)
0	0	0	Page 0
0	0	1	Page 1
0	1	0	Page 2
0	1	1	Page 3
1	0	0	Page 4
1	0	1	Page 5
1	1	0	Page 5
1	1	1	Page 5

PS0~PS2 are used to select a ROM page. User can use the PAGE instruction (e.g. PAGE 1) or set PS2~PS0 bits to change the ROM page. When executing a "JMP", "CALL", or other instructions which causes the program counter to be changed (e.g. MOV R2, A), PS2~PS0 are loaded into the 11th and 12th bits of the program counter where it selects one of the available program memory pages. Note that RET (RETL, RETI) instruction does not change the PS2~PS0 bits. That is, the return will always be to the page from where the subroutine was called, regardless of the current setting of PS2~PS0 bits.

Bit 4 (T): Time-out bit. Set to “1” by the "SLEP" and "WDTC" commands or during power up and reset to “0” by WDT timeout.

Event	T	P	Remark
WDT wake up from sleep mode	0	0	–
WDT time out (not sleep mode)	0	1	–
/RESET wake up from sleep	1	0	–
Power up	1	1	–
Low pulse on /RESET	1	1	×: don't care

Bit 3 (P): Power down bit. Set to “1” during power on or by a "WDTC" command and reset to “0” by a "SLEP" command.

Bit 2 (Z): Zero flag

Bit 1 (DC): Auxiliary Carry flag

Bit 0 (C): Carry flag

6.1.5 R4, RSR (RAM Select Register)

(Address: 04h)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RBS1	RBS0	RSR5	RSR4	RSR3	RSR2	RSR1	RSR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7 ~ 6 (RBS1 ~ RBS0): determine which bank is activated among the four banks. See the data memory configuration in Figure 6-2. Use the Bank Instruction (e.g. Bank 1) to change banks.

Bank 1	Bank 0	Special Register Bank	RAM Bank
0	0	Bank 0	Bank 0
0	1	Bank 1	Bank 1
1	0	Bank 0	Bank 2
1	1	Bank 0	Bank 3

Bits 5 ~ 0 (RSR5 ~ RSR0): used to select up to 64 registers (Address: 00~3F) in indirect addressing mode. If no indirect addressing is used, the RSR can be used as an 8-bit general purpose read/writer register.

6.1.6 Bank 0 R5, Port 5 (Port 5 I/O Data and Page of Register Select

(Address: 05h)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
R57	R56	R55	R54	–	–	–	IOCPAGE
R/W	R/W	R/W	R/W	-	-	-	R/W

Bits 7~4: Four bits I/O registers of Port 5

User can use the IOC50 register to define each bit either as input or output.

Bits 3~1: Not used

Bit 0 (IOCPAGE): change IOC5 ~ IOCF to another page

IOCPAGE = "0" : Page 0 (select register of IOC50 to IOC F0)

IOCPAGE = "1" : Page 1 (select register of IOC61 to IOC E1)

6.1.7 Bank 0 R6, Port 6 (Port 6 I/O Data Register)

(Address: 06h)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
R67	R66	R65	R64	R63	R62	R61	R60
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0: 8-bit I/O registers of Port 6

User can use the IOC60 register to define each bit either as input or output.

6.1.8 Bank 0 R7, Port 7 (Port 7 I/O Data Register)

(Address: 07h)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
R77	R76	R75	R74	R73	R72	R71	R70
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0: 8-bit I/O registers of Port 7

User can use the IOC70 register to define each bit either as input or output.

6.1.9 Bank 0 R8, Port 8 (Port 8 I/O Data Register)

(Address: 08h)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
R87	R86	R85	R84	R83	R82	R81	R80
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0: 8-bit I/O registers of Port 8

User can use the IOC80 register to define each bit either as input or output.

6.1.10 Bank 0 R9, LCDCR (LCD Control Register)

(Address: 09h)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BS	DS1	DS0	LCDEN	-	LCDTYPE	LCDF1	LCDF0
R/W	R/W	R/W	R/W	-	R/W	R/W	R/W

Bit 7 (BS): LCD bias select bit

BS = "0": 1/2 bias

BS = "1": 1/3 bias

Bits 6 ~ 5 (DS1 ~ DS0): LCD duty select

DS1	DS0	LCD Duty
0	0	1/2 duty
0	1	1/3 duty
1	×	1/4 duty

Bit 4 (LCDEN): LCD enable bit

LCDEN = "0": LCD circuit disabled. All common/segment outputs are set to ground (GND) level.

LCDEN = "1": LCD circuit enabled.

Bit 3: Not used

Bit 2 (LCDTYPE): LCD drive waveform type select bit

LCDTYPE = "0": A type waveform

LCDTYPE = "1": B type waveform

Bits 1 ~ 0 (LCDF1~LCDF0): LCD frame frequency control bits

LCDF1	LCDF0	LCD Frame Frequency (e.g. Fs=32.768kHz)		
		1/2 Duty	1/3 Duty	1/4 Duty
0	0	Fs/(256×2)=64.0	Fs/(172×3)=63.5	Fs/(128×4)=64.0
0	1	Fs/(280×2)=58.5	Fs/(188×3)=58.0	Fs/(140×4)=58.5
1	0	Fs/(304×2)=53.9	Fs/(204×3)=53.5	Fs/(152×4)=53.9
1	1	Fs/(232×2)=70.6	Fs/(156×3)=70.0	Fs/(116×4)=70.6

Note: *Fs: sub-oscillator frequency*

6.1.11 Bank 0 RA, LCD_ADDR (LCD Address)

(Address: 0Ah)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	LCD_A4	LCD_A3	LCD_A2	LCD_A1	LCD_A0
-	-	-	R/W	R/W	R/W	R/W	R/W

Bits 7~5: Not used, fixed at “0”

Bits 4~0 (LCDA4 ~ LCDA0): LCD RAM addresses

RA (LCD Address)	RB (LCD Data Buffer)					Segment
	Bits 7 ~4	Bit 3 (LCD_D3)	Bit 2 (LCD_D2)	Bit 1 (LCD_D1)	Bit 0 (LCD_D0)	
00H	–	–	–	–	–	SEG0
01H	–	–	–	–	–	SEG1
02H	–	–	–	–	–	SEG2
1DH	–	–	–	–	–	SEG29
1EH	–	–	–	–	–	SEG30
1FH	–	–	–	–	–	SEG31
Common	×	COM3	COM2	COM1	COM0	

6.1.12 Bank 0 RB, LCD_DB (LCD Data Buffer)

(Address: 0Bh)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
–	–	–	–	LCD_D3	LCD_D2	LCD_D1	LCD_D0
-	-	-	-	R/W	R/W	R/W	R/W

Bits 7~4: Not used

Bits 3~0 (LCD_D3 ~ LCD_D0): LCD RAM data transfer register

6.1.13 Bank 0 RC, CNTER (Counter Enable Register)

(Address: 0Ch)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
–	–	–	–	LPWTEN	HPWTEN	CNT2EN	CNT1EN
-	-	-	-	R/W	R/W	R/W	R/W

Bits 7, 5: Not used, must be fixed to “0”

Bits 6, 4: Not used

Bit 3 (LPWTEN): Low pulse width timer enable bit

LPWTEN = "0": Disable LPWT. Stop counting operation.

LPWTEN = "1": Enable LPWT. Start counting operation.

Bit 2 (HPWTEN): High pulse width timer enable bit

HPWTEN = "0": Disable HPWT. Stop counting operation.

HPWTEN = "1": Enable HPWT. Start counting operation.

Bit 1 (CNT2EN): Counter 2 enable bit

CNT2EN = "0": Disable Counter 2. Stop counting operation.

CNT2EN = "1": Enable Counter 2. Start counting operation.

Bit 0 (CNT1EN): Counter 1 enable bit

CNT1EN = "0": Disable Counter 1. Stop counting operation.

CNT1EN = "1": Enable Counter 1. Start counting operation.

6.1.14 Bank 0 RD, SBPCR (System, Booster and PLL Control Register)

(Address: 0Dh)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
–	CLK2	CLK1	CLK0	IDLE	BF1	BF0	CPUS
–	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7: Not used

Bits 6 ~ 4 (CLK2 ~ CLK0): Main clock select bits for PLL mode (Code Option Select)

CLK2	CLK1	CLK0	Main clock	Example Fs=32.768K
0	0	0	Fs×130	4.26 MHz
0	0	1	Fs×65	2.13 MHz
0	1	0	Fs×65/2	1.065 MHz
0	1	1	Fs×65/4	532 kHz
1	×	×	Fs×244	8 MHz

Bit 3 (IDLE): Idle mode enable bit. This bit will determine the intended mode of the SLEP instruction.

Idle = "**0**"+SLEP instruction → Sleep mode

Idle = "**1**"+SLEP instruction → Idle mode

***** *NOP instruction must be added after SLEP instruction.***

Example: ***Idle mode: Idle bit = "1" +SLEP instruction + NOP instruction***

Sleep mode: Idle bit = "0" +SLEP instruction + NOP instruction

Bits 2, 1 (BF1, 0): LCD booster frequency select bit to adjust VLCD 2, 3 driving.

BF1	BF0	Booster Frequency
0	0	Fs
0	1	Fs/4
1	0	Fs/8
1	1	Fs/16

Bit 0 (CPUS): CPU oscillator source select. When CPUS=0, the CPU oscillator select sub-oscillator and the main oscillator is stopped.

CPUS = "0": sub-oscillator (Fs)

CPUS = "1": main oscillator (Fm)

■ CPU Operation Mode

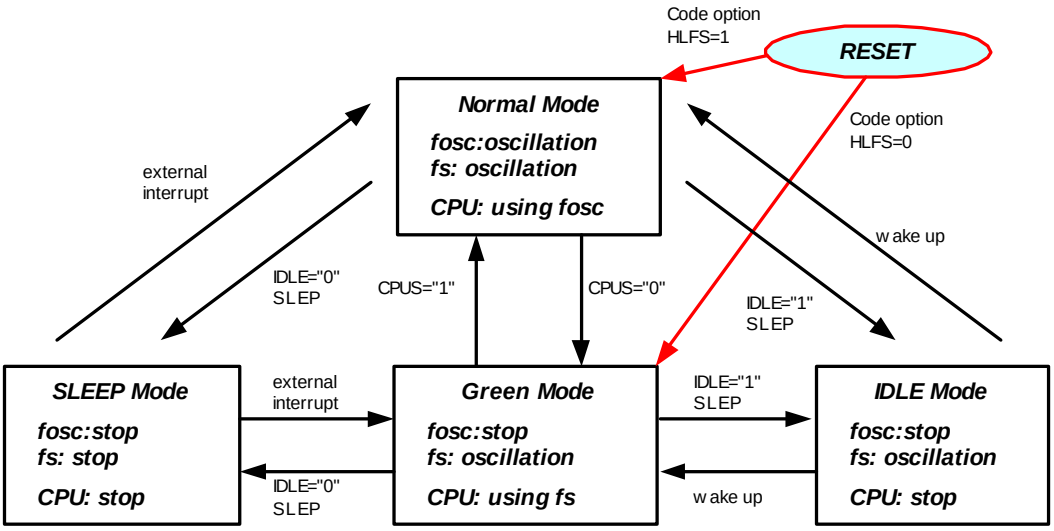


Figure 6-3 CPU Operation Mode

Note

(*) *If the Watchdog function is enabled before going into Sleep mode, some circuits like the Timer (its Clock Source is Fs) must stop counting.*

If the Watchdog function is enabled before going into Sleep mode, some circuits like the Timer (its Clock Source is the external pin) can still count and its interrupt flag can be active at matching condition as corresponding interrupt is enabled. But the CPU cannot be awakened by this event.

(**)

Switching Operation Mode at Sleep → Normal, Green → Normal:

If the Timer Clock Source is Fm, the Timer/Counter must stop counting at Sleep or Green mode. Then, the Timer can continue to count until the Clock Source is stable at Normal mode. That the Clock Source is stable means the CPU starts to work at Normal mode.

Switching Operation Mode at Sleep → Green:

If the Timer Clock Source is Fs, the Timer must stop counting at Sleep mode. Then, the Timer can continue to count until the Clock Source is stable at Green mode. That the Clock Source is stable means the CPU starts to work at Green mode.

Switching Operation Mode at Sleep → Normal:

If the Timer Clock Source is Fs, the Timer must stop counting at Sleep mode. Then, the Timer can continue to count until the Clock Source is stable at Normal mode. That the Clock Source is stable means the CPU starts to work at Normal mode.

Fmain	Fsub	Power-on LVR	Pin-Reset WDT	
			N / G / I	S
RC	RC	18ms+WSTO+15*1/Fsub	18ms+WSTO+15*1/ Fsub	18ms+WSTO+15*1/ Fsub
	XT	18ms+WSTO+15*1/Fsub	18ms+WSTO+15*1/ Fsub	18ms+WSTO+15*1/ Fsub
XT	RC	18ms+WSTO+15*1/Fsub	18ms+WSTO+15*1/ Fsub	18ms+WSTO+15*1/ Fsub
	XT	18ms+WSTO+15*1/Fsub	18ms+WSTO+15*1/Fsub	18ms+WSTO+15*1/Fsub

Fmain	Fsub	G → N	I → N	S → N
RC	RC	WSTO + 11*1/Fmain	WSTO + 15*1/ Fsub	18ms + WSTO + 15*1/ Fsub
	XT	WSTO + 11*1/Fmain	WSTO + 15*1/ Fsub	18ms + WSTO + 15*1/ Fsub
XT	RC	WSTO + 11*1/Fmain	WSTO + 15*1/ Fsub	18ms + WSTO + 15*1/ Fsub
	XT	WSTO + 11*1/Fmain	WSTO + 15*1/ Fsub	18ms + WSTO + 15*1/Fsub

Fmain	Fsub	I → G	S → G
IRC	IRC	WSTO + 15*1/Fsub	18ms + WSTO + 15*1/ Fsub
	XT	WSTO + 15*1/Fsub	18ms + WSTO + 15*1/ Fsub
XT	IRC	WSTO + 15*1/Fsub	18ms + WSTO + 15*1/ Fsub
	XT	WSTO + 15*1/Fsub	18ms + WSTO + 15*1/Fsub

WSTO: *Waiting Time from Start-to-Oscillation*

N: *Normal mode* **G:** *Green mode* **I:** *Idle mode* **S:** *Sleep mode*

6.1.15 Bank 0 RE, IRCR (IR and Port 5 Setting Control Register)

(Address: 0Eh)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IRE	HF	LGP	–	IROUTE	TCCE	EINT1	EINT0
R/W	R/W	R/W	-	R/W	R/W	R/W	R/W

Bit 7 (IRE): Infrared Remote Enable bit

IRE = "0": Disable the IR/PWM function. The state of P57/IROUT/AD2 pin is determined by Bit 7 of IOC 50 if it is for IROUT.

IRE = "1": Enable IR or PWM function

Bit 6 (HF): High carry frequency

HF = "0": For PWM application, disable the H/W modulator function. The IROUT waveform is generated according to high-pulse and low-pulse time as determined by the respective high pulse and low pulse width timers. Counter 2 is an independent auto reload timer.

HF = "1": For IR application mode, enable the H/W modulator function, the low time sections of the generated pulse is modulated with the Fcarrier frequency. The Fcarrier frequency is provided by Counter 2.

Bit 5 (LGP): IROUT for of low pulse width timer

LGP = "0": The high-pulse width timer register and low-pulse width timer is valid.

LGP = "1": The high-pulse width timer register is ignored. So the IROUT waveform is dependent on the low-pulse width timer register only.

Bit 4: Not used

Bit 3 (IROUTE): Define the function of P57/IROUT/AD2 pin

IROUTE = "0": for bidirectional general I/O or AD2 pin

IROUTE = "1": for IR or PWM output pin, the control bit of P57 (Bit 7 of IOC50) must be set to “0”

Bit 2 (TCCE): Define the function of P56/TCC/VREF pin

TCCE = "0": for bidirectional general I/O or VREF pin

TCCE = "1": for external input pin of TCC, the control bit of P56 (Bit 6 of IOC50) must be set to “1”

Bit 1 (EINT1): Define the function of P55/INT1/AD1 pin

EINT1 = "0": for bidirectional general I/O or AD1 pin

EINT1 = "1": for external interrupt pin of INT1, the control bit of P55 (Bit 5 of IOC50) must be set to “1”

Bit 0 (EINT0): Define the function of P54/INT0/AD0 pin

EINT0 = "0": for bidirectional general I/O or AD0 pin

EINT0 = "1": for external interrupt pin of INT0, the control bit of P54 (Bit 4 of IOC50) must be set to “1”

6.1.16 Bank 0 RF, ISR (Interrupt Status Register)

(Address: 0Fh)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ICIF	LPWTF	HPWTF	CNT2F	CNT1F	INT1F	INT0F	TCIF
F	F	F	F	F	F	F	F

These bits are set to “1” when interrupt occurs.

Bit 7 (ICIF): Port 6, Port 8, input status changed interrupt flag. Set when Port 6, Port 8 input changes.

Bit 6 (LPWTF): Interrupt Flag of the internal Low-Pulse Width Timer underflow.

Bit 5 (HPWTF): Interrupt Flag of the internal High-Pulse Width Timer underflow.

Bit 4 (CNT2F): Interrupt Flag of the internal Counter 2 underflow.

Bit 3 (CNT1F): Interrupt Flag of the internal Counter 1 underflow.

Bit 2 (INT1F): External INT1 pin Interrupt Flag

Bit 1 (INT0F): External INT0 pin Interrupt Flag

Bit 0 (TCIF): TCC timer overflow Interrupt Flag. Set when TCC timer overflows.

6.1.17 Bank 1 R5, P5HDSCR (Port 5 High Drive/Sink Control Register)

(Address: 05h)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
H57	H56	H55	H54	-	-	-	-
R/W	R/W	R/W	R/W	R	R	R	R

Bits 7~4 (H57~H54): P57~P54 high drive/sink current control bits

0: Enable high drive/sink

1: Disable high drive/sink

Bits 3~0: Not used, set to "1" all the time.

6.1.18 Bank 1 R6, P6HDSCR (Port 6 High Drive/Sink Control Register)

(Address: 06h)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
H67	H66	H65	H64	H63	H62	H61	H60
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (H67~H60): P67~P60 high drive/sink current control bits

0: Enable high drive/sink

1: Disable high drive/sink

6.1.19 Bank 1 R7, P78HDSCR (Ports 7~8 High Drive/Sink Control Register)

(Address: 07h)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	P8HHDS	P8LHDS	P7HHDS	P7LHDS
R	R	R	R	R/W	R/W	R/W	R/W

Bits 7~4: Not used, set to "1" all the time.

Bit 3 (P8HHDS): Control bit used to enable high drive/sink of Port 8 high nibble pin

0: Enable high drive/sink

1: Disable high drive/sink

Bit 2 (P8LHDS): Control bit used to enable high drive/sink of Port 8 low nibble pin

Bit 1 (P7HHDS): Control bit used to enable high drive/sink of Port 7 high nibble pin

Bit 0 (P7LHDS): Control bit used to enable high drive/sink of Port 7 low nibble pin

6.1.20 Bank 1 R8, ADSR1 (ADC Input Select Register 1)

(Address: 08h)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADE7	ADE6	ADE5	ADE4	ADE3	ADE2	ADE1	ADE0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7 (ADE7): AD converter enable bit of P64 pin

0 : Disable AD7, P64 functions as I/O pin

1 : Enable AD7 to function as analog input pin

Bit 6 (ADE6): AD converter enable bit of P63 pin

0 : Disable AD6, P63 functions as I/O pin

1 : Enable AD6 to function as analog input pin

Bit 5 (ADE5): AD converter enable bit of P62 pin

0 : Disable AD5, P62 functions as I/O pin

1 : Enable AD5 to function as analog input pin

Bit 4 (ADE4): AD converter enable bit of P61 pin

0 : Disable AD4, P61 functions as I/O pin

1 : Enable AD4 to function as analog input pin

Bit 3 (ADE3): AD converter enable bit of P60 pin

0 : Disable AD3, P60 functions as I/O pin

1 : Enable AD3 to function as analog input pin

Bit 2 (ADE2): AD converter enable bit of P57 pin

0 : Disable AD2, P57/IROUT functions pin

1 : Enable AD2 to function as analog input pin

Bit 1 (ADE1): AD converter enable bit of P55 pin

0 : Disable AD1, P55/INT1 functions pin

1 : Enable AD1 to function as analog input pin

Bit 0 (ADE0): AD converter enable bit of P54 pin

0 : Disable AD0, P54/INT0 functions pin

1 : Enable AD0 to function as analog input pin

6.1.21 Bank 1 R9, ADSR2 (ADC Input Select Register 2)

(Address: 09h)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	ADE14	ADE13	ADE12	ADE11	ADE10	ADE9	ADE8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7: Not used, set to “0” all the time.

Bit 6 (ADE14): AD converter enable bit of P84 pin

0 : Disable AD14, SEG28/P84 functions pin

1 : Enable AD14 to function as analog input pin

Bit 5 (ADE13): AD converter enable bit of P85 pin

0 : Disable AD13, SEG29/P85 functions pin

1 : Enable AD13 to function as analog input pin

Bit 4 (ADE12): AD converter enable bit of P86 pin

0 : Disable AD12, SEG30/P86 functions pin

1 : Enable AD12 to function as analog input pin

Bit 3 (ADE11): AD converter enable bit of P87 pin

0 : Disable AD11, SEG31/P87 functions pin

1 : Enable AD11 to function as analog input pin

Bit 2 (ADE10): AD converter enable bit of P67 pin

0 : Disable AD10, P67 functions as I/O pin

1 : Enable AD10 to function as analog input pin

Bit 1 (ADE9): AD converter enable bit of P66 pin

0 : Disable AD9, P66 functions as I/O pin

1 : Enable AD9 to function as analog input pin

Bit 0 (ADE8): AD converter enable bit of P65 pin

0 : Disable AD8, P65 functions as I/O pin

1 : Enable AD8 to function as analog input pin

6.1.22 Bank 1 RA, ADCR (ADC Control Register)

(Address: 0Ah)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	CKR1	CKR0	ADRUN	ADP	-	SHS1	SHS0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7: Not used, set to "0" all the time.

Bits 6~5 (CKR1~0): Clock Rate Selection of ADC

System Mode	CKR[2:0]	Clock Rate
Normal Mode	00	F_{Main}/16
	01	F_{Main}/4
	10	F_{Main}/64
	11	F_{Main}/1
Green Mode	xxx	F_{Sub}

Bit 4 (ADRUN): ADC Starts to Run

0 : Reset on completion of the conversion by hardware, this bit cannot be reset by software.

1 : An A/D conversion starts. This bit can be set by software

Bit 3 (ADP): ADC Power

0 : ADC is in power down mode.

1 : ADC is operating normally.

Bit 2: Not used, set to "0" all the time.

Bits 1~0 (SHS1~0): Sample and Hold Timing Selection

SHS[1:0]	Sample and Hold Timing
00	2 x T_{AD}
01	4 x T_{AD}
10	8 x T_{AD}
11	12 x T_{AD}

6.1.23 Bank 1 RB, ADISR (ADC Input Channel and Internal Reference Selection Register)

(Address: 0Bh)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
VREFS	VREF2	VREF1	VREF0	ADIS3	ADIS2	ADIS1	ADIS0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7 (VREFS): The input source of the Vref of the ADC

0: The Vref of the ADC is connected to internal reference voltage (default value), and the P56/TCC/VREF pin carries out the function of P56/TCC.

: The Vref of the ADC is connected to P56/TCC/VREF

Bits 6~4 (VREF2~0): ADC internal reference voltage source

VREF[2:0]	ADC Internal Reference Voltage
000	VDD
001	4.0V ± 1%
010	3.0V ± 1%
011	2.5V ± 1%
1xx	2.0V ± 1%

Bits 3~0 (ADIS3~0): ADC input channel selection bits

ADIS[3:0]	Selected Channel	ADIS[3:0]	Selected Channel
0000	ADC0	1000	ADC8
0001	ADC1	1001	ADC9
0010	ADC2	1010	ADC10
0011	ADC3	1011	ADC11
0100	ADC4	1100	ADC12
0101	ADC5	1101	ADC13
0110	ADC6	1110	ADC14
0111	ADC7	1111	1/2 VDD PowerDet.

6.1.24 Bank 1 RC, ADDL (Low Byte of Analog to Digital Converter Data)

(Address: 0Ch)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADD7	ADD6	ADD5	ADD4	ADD3	ADD2	ADD1	ADD0
R	R	R	R	R	R	R	R

Bits 7~0 (ADD7~0): Low Byte of AD Data Buffer

6.1.25 Bank 1 RD, ADDH (High Byte of Analog to Digital Converter Data)

(Address: 0Dh)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADD11	ADD10	ADD9	ADD8	ADD7	ADD6	ADD5	ADD4
R	R	R	R	R	R	R	R

Bits 7~0 (ADD11~4): High Byte of AD Data Buffer.

6.1.26 Bank 1 RE, IMR2 (Interrupt Mask Register 2)

(Address: 0Eh)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
–	–	–	–	–	–	–	ADIE
–	–	–	–	–	–	–	R/W

Bits 7~1: Not used, set to "0" all the time.

Bit 0 (ADIE): ADSF interrupt enable bit.

0: disable ADSF interrupt

1: enable ADSF interrupt

6.1.27 Bank 1 RF, SF2 (Interrupt Status Register 2)

(Address: 0Fh)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
–	–	–	–	–	–	–	ADIF
	–	–	–	–	–	–	R/W

Bits 7~1: Not used, set to "0" all the time.

Bit 0 (ADIF): Analog to digital conversion interrupt flag. Set when AD conversion is completed, reset by software.

6.1.28 Address: 10h~3Fh; R10~R3F (General Purpose Register)

R10~R31F and R20~R3F (Banks 0~3) are general purpose registers.

6.2 Special Purpose Registers

6.2.1 A (Accumulator)

Internal data transfer operation, or instruction operand holding usually involves the temporary storage function of the Accumulator, which is not an addressable register.

■ Registers of IOC Page 0 (IOC50 ~ IOCF0, Bit 0 of R5 = “0”)

6.2.2 IOC50, P5CR (Port 5 I/O and Ports 7, 8 for LCD Segment Control Register)

(Address: 05h, Bit 0 of R5 = “0”)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IOC57	IOC56	IOC55	IOC54	P8HS	P8LS	P7HS	P7LS
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~4 (IOC57~54): Port 5 I/O direction control register

IOC5x = "0": set the relative P5x I/O pins as output

IOC5x = "1": set the relative P5x I/O pin into high impedance (input pin)

Bit 3 (P8HS): Switch to high nibble I/O of Port 8 or to LCD segment output while sharing pins with SEGxx/P8x pins.

P8HS = "0": select high nibble of Port 8 as normal P84~P87

P8HS = "1": select LCD segment output as SEG 28~SEG 31 output

Bit 2 (P8LS): Switch to low nibble I/O of Port 8 or to LCD segment output while sharing pins with SEGxx/P8x pins

P8LS = "0": select low nibble of Port 8 as normal P80~P83

P8LS = "1": select LCD Segment output as SEG 24~SEG 27 output

Bit 1 (P7HS): Switch to high nibble I/O of Port 7 or to LCD segment output while sharing pins with SEGxx/P7x pins

P7HS = "0": select high nibble of Port 7 as normal P74~P77

P7HS = "1": select LCD Segment output as SEG 20~SEG 23 output

Bit 0 (P7LS): Switch to low nibble I/O of Port 7 or to LCD segment output while sharing pins with SEGxx/P7x pins

P7LS = "0": select low nibble of Port 7 as normal P70~P73

P7LS = "1": select LCD segment output as SEG 16~SEG 19 output

6.2.3 IOC60, P6CR (Port 6 I/O Control Register)

(Address: 06h, Bit 0 of R5 = “0”)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IOC67	IOC66	IOC65	IOC64	IOC63	IOC62	IOC61	IOC60
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7 (IOC67) ~ Bit 0 (IOC60): Port 6 I/O direction control register

IOC6x ="0": set the relative Port 6x I/O pins as output

IOC6x ="1": set the relative Port 6x I/O pin into high impedance (input pin)

6.2.4 IOC70, P7CR (Port 7 I/O Control Register)

(Address: 07h, Bit 0 of R5 = “0”)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IOC77	IOC76	IOC75	IOC74	IOC73	IOC72	IOC71	IOC70
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7 (IOC77) ~ Bit 0 (IOC70): Port 7 I/O direction control register

IOC7x = "0": set the relative Port 7x I/O pins as output

IOC7x = "1": set the relative Port 7x I/O pin into high impedance (input pin)

6.2.5 IOC80, P8CR (Port 8 I/O Control Register)

(Address: 08h, Bit 0 of R5 = “0”)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IOC87	IOC86	IOC85	IOC84	IOC83	IOC82	IOC81	IOC80
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7 (IOC 87) ~ Bit 0 (IOC 80): Port 8 I/O direction control register

IOC8x = "0": set the relative Port 8x I/O pins as output

IOC8x = "1": set the relative Port 8x I/O pin into high impedance (input pin)

6.2.6 IOC90, RAM_ADDR (128 Bytes RAM Address)

(Address: 09h, Bit 0 of R5 = “0”)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	RAM_A6	RAM_A5	RAM_A4	RAM_A3	RAM_A2	RAM_A1	RAM_A0
0	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7: Not used, fixed at “0”

Bits 6~0: 128 bytes RAM address

6.2.7 IOCA0, RAM_DB (128 Bytes RAM Data Buffer)

(Address: 0Ah, Bit 0 of R5 = “0”)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RAM_D7	RAM_D6	RAM_D5	RAM_D4	RAM_D3	RAM_D2	RAM_D1	RAM_D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0: 128 bytes RAM data transfer register

6.2.8 IOCB0, CNT1PR (Counter 1 Preset Register)

(Address: 0Bh, Bit 0 of R5 = “0”)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7 ~ Bit 0: These are Counter 1 buffers which user can read and write. Counter 1 is an 8-bit down-count timer with 8-bit prescaler used to preset the counter and read the preset value. The prescaler is set by the IOC91 register. After an interrupt, it will auto reload the preset value.

6.2.9 IOCC0, CNT2PR (Counter 2 Preset Register)

(Address: 0Ch, Bit 0 of R5 = “0”)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7 ~ Bit 0: These are Counter 2 buffers which user can read and write. Counter 2 is an 8-bit down-count timer with 8-bit prescaler used to preset the counter and read the preset value. The prescaler is set by IOC91 register. After an interrupt, it will reload the preset value.

When IR output is enabled, this control register can obtain carrier frequency output. If the Counter 2 clock source is equal to F_T ,

then

$$\text{Carrier frequency (Fcarrier)} = \frac{F_T}{2 * (\text{preset\_value} + 1) * \text{prescaler}}$$

6.2.10 IOCD0, HPWTPR (High-Pulse Width Timer Preset Register)

(Address: 0Dh, Bit 0 of R5 = "0")

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7 ~ Bit 0: These are high-pulse width timer buffers which user can read and write. High-pulse width timer preset register is an eight-bit down-counter with 8-bit prescaler used as IOCD0 to preset the counter and read the preset value. The prescaler is set by the IOCA1 register. After an interrupt, it will reload the preset value.

For PWM or IR application, this control register is set as high pulse width.

If the high-pulse width timer clock source is F_T ,
then

$$\text{High pulse time} = \frac{\text{prescaler} * (\text{preset\_value} + 1)}{F_T}$$

6.2.11 IOCE0, LPWTPR (Low-Pulse Width Timer Preset Register)

(Address: 0Eh, Bit 0 of R5 = "0")

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7 ~ Bit 0: All are low-pulse width timer buffer that user can read and write. Low-pulse width timer preset is an eight-bit down-counter with 8-bit prescaler that is used as IOCE0 to preset the counter and read preset value. The prescaler is set by IOCA1 register. After an interrupt, it will reload the preset value.

For PWM or IR application, this control register is set as low pulse width.

If the low-pulse width timer clock source is F_T ,
then.

$$\text{Low pulse time} = \frac{\text{prescaler} * (\text{preset\_value} + 1)}{F_T}$$

6.2.12 IOCF0, IMR (Interrupt Mask Register)

(Address: 0Fh, Bit 0 of R5 = "0")

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ICIE	LPWTE	HPWTE	CNT2E	CNT1E	INT1E	INT0E	TCIE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7 ~ Bit 0: interrupt enable bit. Enable the respective interrupt source.

0: disable interrupt

1: enable interrupt

The IOCF0 register is readable and writable.

■ Registers of IOC Page 1 (IOC61 ~ IOCE1, Bit 0 of R5 = “1”)

6.2.13 IOC61, WUCR (Wake-up and Sink Current of P57/IROUT Control Register)

(Address: 06h, Bit 0 of R5 = “1”)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IROCS	-	-	-	/WUE8H	/WUE8L	/WUE6H	/WUE6L
R/W	-	-	-	R/W	R/W	R/W	R/W

Bit 7: IROCS: IROUT/Port 57 output sink current set

IROCS	P57/IROUT Sink Current	
	VDD=5V	VDD=3V
0	10 mA	6 mA
1	20 mA	12 mA

Bits 6, 5, 4: Not used

Bit 3 (/WUE8H): 0/1→ enable/disable P84~P87 pin change wake-up function

Bit 2 (/WUE8L): 0/1 → enable/disable P80~P83 pin change wake-up function

Bit 1 (/WUE6H): 0/1 → enable/disable P64~P67 pin change wake-up function

Bit 0 (/WUE6L): 0/1 → enable/disable P60~P63 pin change wake-up function

*** Port 6 and Port 8 must not be set as input floating when wake-up function is enabled. “Enable” is the initial state of wake-up function.**

6.2.14 IOC71, TCCCR (TCC Control Register)

(Address: 07h, Bit 0 of R5 = “1”)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INT_EDGE	INT	TS	TE	PSRE	TCCP2	TCCP1	TCCP0
R/W	F	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7 (INT_EDGE):

INT_EDGE = "0": Interrupt on the rising edge of P54/INT0 pin

INT_EDGE = "1": Interrupt on the falling edge of P54/INT0 pin

Bit 6 (INT): INT enable flag, this bit is read only

INT = "0": interrupt masked by DISI or hardware interrupt

INT = "1": interrupt enabled by ENI/RETI instructions

Bit 5 (TS): TCC signal source

TS = "0": internal instruction cycle clock

TS = "1": transition on TCC pin, TCC period > internal instruction clock period

Bit 4 (TE): TCC signal edge

TE = "0": incremented by TCC pin rising edge

TE = "1": incremented by TCC pin falling edge

Bits 3~0 (PSRE, TCCP2 ~ TCCP0): TCC prescaler bits

PSRE	TCCP2	TCCP1	TCCP0	TCC Rate
0	×	×	×	1:1
1	0	0	0	1:2
1	0	0	1	1:4
1	0	1	0	1:8
1	0	1	1	1:16
1	1	0	0	1:32
1	1	0	1	1:64
1	1	1	0	1:128
1	1	1	1	1:256

6.2.15 IOC81, WDTCR (WDT Control Register)

(Address: 08h, Bit 0 of R5 = “1”)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
–	–	–	–	WDTE	WDTP2	WDTP1	WDTP0
–	–	–	–	R/W	R/W	R/W	R/W

Bits 7 ~ 4: Not used

Bit 3 (WDTE): Watchdog timer enable. This control bit is used to enable the Watchdog timer,

WDTE = "0": Disable WDT function

WDTE = "1": Enable WDT function

Bits 2 ~ 0 (WDTP2 ~ WDTP0): Watchdog Timer prescaler bits. The WDT clock source is sub-oscillation frequency.

WDTP2	WDTP1	WDTP0	WDT Rate
0	0	0	1:1
0	0	1	1:2
0	1	0	1:4
0	1	1	1:8
1	0	0	1:16
1	0	1	1:32
1	1	0	1:64
1	1	1	1:128

6.2.16 IOC91, CNT12CR (Counters 1, 2 Control Register)

(Address: 09h, Bit 0 of R5 = "1")

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CNT2S	CNT2P2	CNT2P1	CNT2P0	CNT1S	CNT1P2	CNT1P1	CNT1P0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7 (CNT2S): Counter 2 clock source select

"**0**"**:** Fs (Fs: sub-oscillator clock)

"**1**"**:** Fm (Fm: main-oscillator clock)

Bits 6~4 (CNT2P2 ~ CNT2P0): Counter 2 prescaler select bits

CNT2P2	CNT2P1	CNT1P0	Counter 2 Scale
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

Bit 3 (CNT1S): Counter 1 Clock Source Select

"**0**"**:** Fs (Fs: sub-oscillator clock)

"**1**"**:** Fm (Fm: main-oscillator clock)

Bits 2~0 (CNT1P2 ~ CNT1P20): Counter 1 prescaler select bits

CNT1P2	CNT1P1	CNT1P0	Counter 1 Scale
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

6.2.17 IOCA1, HLPWTCR (High/Low Pulse Width Timer Control Register)

(Address: 0Ah, Bit 0 of R5 = "1")

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LPWTS	LPWTP2	LPWTP1	LPWTP0	HPWTS	HPWTP2	HPWTP1	HPWTP0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7 (LPWTS): Low-Pulse Width Timer Clock Source Select

"**0**"**:** Fs (Fs: sub-oscillator clock)

"**1**"**:** Fm (Fm: main-oscillator clock)

Bits 6~4 (LPWTP2~ LPWTP0): Low-Pulse Width Timer Prescaler Select bits

LPWTP2	LPWTP1	LPWTP0	Low-pulse Width Timer Scale
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

Bit 3 (HPWTS): High-Pulse Width Timer Clock Source Select

"**0**"**:** Fs (Fs: sub-oscillator clock)

"**1**"**:** Fm (Fm: main-oscillator clock)

Bits 2~0 (HPWTP2~ HPWTP0): High-Pulse Width Timer Prescaler Select bits

HPWTP2	HPWTP1	HPWTP0	High-pulse Width Timer Scale
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

6.2.18 IOCB1, P6PH (Port 6 Pull-high Control Register)

Address: 0Bh, Bit 0 of R5 = “1”)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PH67	PH66	PH65	PH64	PH63	PH62	PH61	PH60
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7 ~ Bit 0 (PH67 ~ PH60): These are the enable bits of Port 6 pull high function.

PH6x = "0": disable P6x pin internal pull-high resistor function

PH6x = "1": enable P6x pin internal pull-high resistor function

6.2.19 IOCC1, P6OD (Port 6 Open Drain Control Register)

(Address: 0Ch, Bit 0 of R5 = “1”)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OP67	OP66	OP65	OP64	OP63	OP62	OP61	OP60
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7 ~ Bit 0: These are the enable bits of Port 6 open drain function.

OD6x = "0": disable pin P6x open drain function

OD6x = "1": enable pin P6x open drain function

6.2.20 IOCD1, P8PH (Port 8 Pull High Control Register)

(Address: 0Dh, Bit 0 of R5 = "1")

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PH87	PH86	PH85	PH84	PH83	PH82	PH81	PH80
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7 ~ Bit 0: These are the enable bits of Port 8 pull-high function.

PH8x = "0": disable P8x pin internal pull-high resistor function

PH8x = "1": enable P8x pin internal pull-high resistor function

6.2.21 IOCE1, P6PL (Port 6 Pull Low Control Register)

(Address: 0Eh, Bit 0 of R5 = "1")

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PL67	PL66	PL65	PL64	PL63	PL62	PL61	PL60
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7 ~ Bit 0: These are the enable bits of Port 6 pull low function.

PL6x = "0": disable P6x pin internal pull-low resistor function

PL6x = "1": enable P6x pin internal pull-low resistor function

6.3 TCC and WDT Prescaler

Two 8-bit counters are available as prescalers for the TCC (Time Clock Counter) and WDT (Watchdog Timer). The TCCP2~TCCP0 bits of the IOC71 register are used to determine the ratio of the TCC prescaler. Likewise, the WDTP2~WDTP0 bits of the IOC81 register are used to determine the WDT prescaler. The TCC prescaler (TCCP2~TCCP0) is cleared by the instructions each time they are written into TCC, while the WDT prescaler is cleared by the "WDTC" and "SLEP" instructions. Fig.7 depicts the circuit diagram of TCC and WDT.

R1 (TCC) is an 8-bit timer/counter. The clock source of TCC can be selected by internal instruction clock or external signal input (edge selectable from the TCC control register). If the TCC signal source is from the internal instruction clock, the TCC will be incremented by 1 at every instruction cycle (without prescaler). If the TCC signal source is from an external clock input, the TCC will be incremented by 1 at every falling edge or rising edge of the TCC pin.

The Watchdog Timer is free running on sub-oscillator. The WDT will keep on running even after the oscillator driver has been turned off. During Normal mode, Green mode, or Idle mode operation, a WDT time-out (if enabled) will cause the device to reset. The WDT can be enabled or disabled at any time during the Normal mode and Green mode by software programming. Refer to WDTE bit of IOC81 register. The WDT time-out period is equal to (prescaler $\times$ 256 / (Fs/2)).

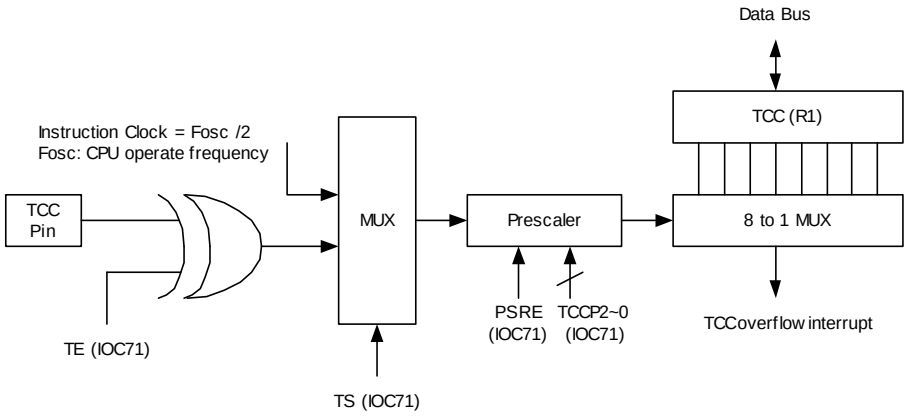


Figure 6-4(a) Block Diagram of TCC

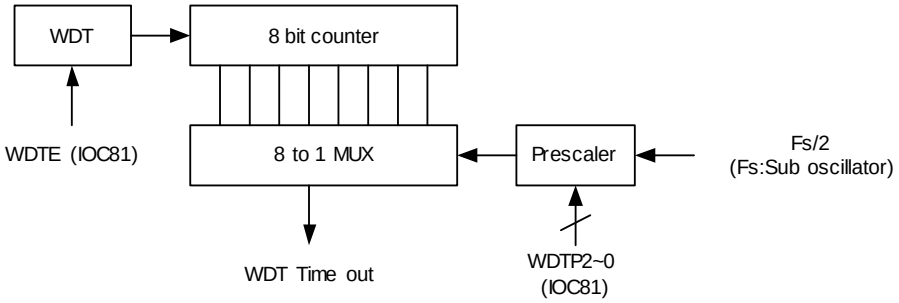
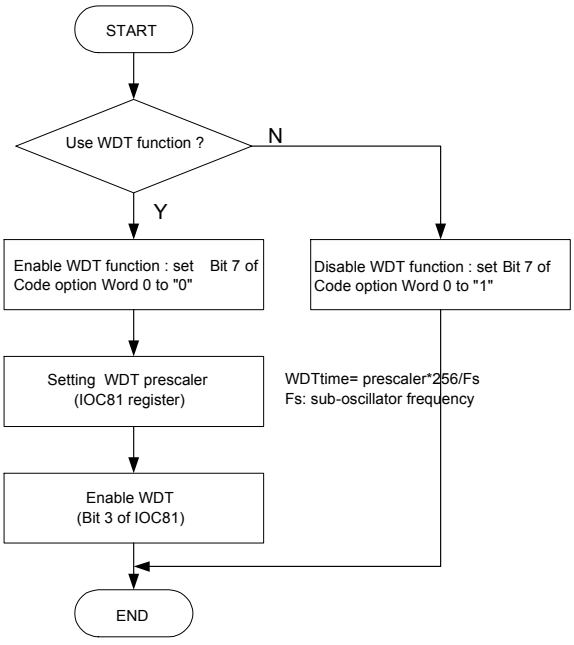
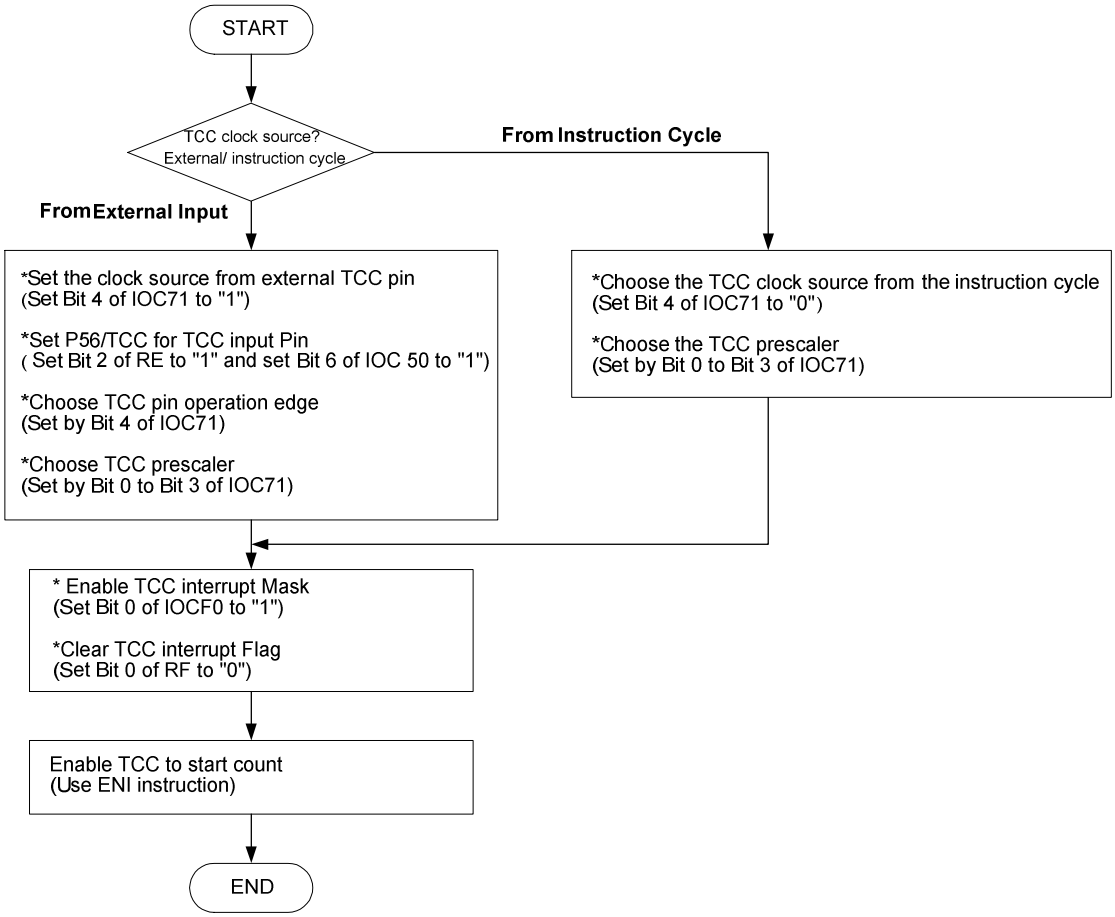


Figure 6-4(b) Block Diagram of WDT

WDT Setting Flowchart

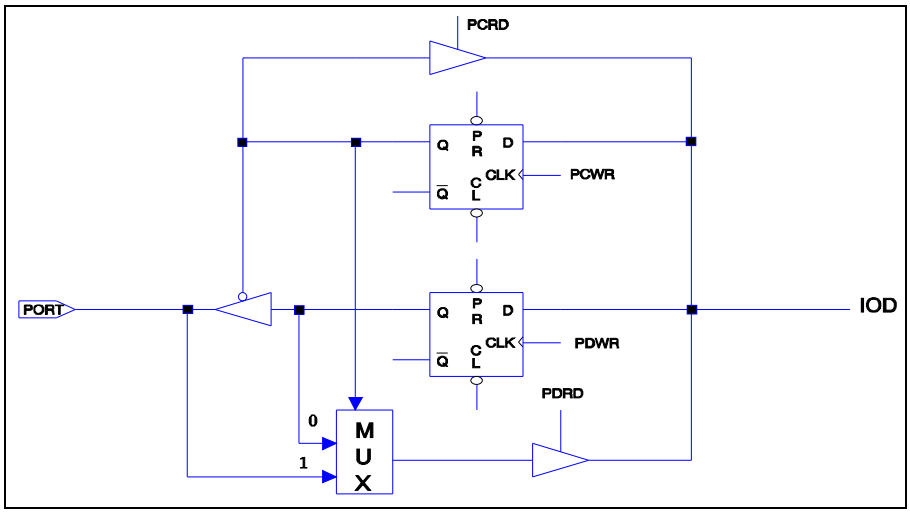


TCC Setting Flowchart



6.4 I/O Ports

The I/O registers, (Port 5, Port 6, Port 7 and Port 8), are bi-directional tri-state I/O ports. Port 6 and Port 8 are pulled-high internally by software; Port 6 is also pulled-low internally by software. Furthermore, Port 6 has its open-drain output also through software. Port 6 and Port 8 features an input status changed interrupt (or wake-up) function and is pulled-high by software. Each I/O pin can be defined as "input" or "output" pin by the I/O control register (IOC50 ~ IOC80). The I/O registers and I/O control registers are both readable and writable. The I/O interface circuits are shown in Figure 6-5.



Note: *Open-drain, pull-high, and pull down are not shown in the figure.*

Figure 6-5 Circuit of I/O Port and I/O Control Register for Port 5 ~ 8

6.5 Reset and Wake-up

A reset can be activated by

- POR (Power-on Reset)
- WDT timeout (if enabled)
- /RESET pin goes to low

Note: *The reset circuit is always enabled. It will reset the CPU at 1.7V.*
Once a reset occurs, the following functions are performed

- The oscillator is running, or will be started
- The program counter (R2/PC) is set to all "0"
- All I/O port pins are configured as input mode (high-impedance state)
- The TCC/Watchdog timer and prescaler are cleared
- When power is on, the Bits 5 and 6 of R3 and the upper two bits of R4 are cleared.
- Bits of the IOC71 register are set to all "1" except for Bit 6 (INT flag)
- For other registers, see Table 2

Table 2 Summary of Registers Initialized Values

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x05	IOC50 (P5CR)	Bit Name	IOC57	IOC56	IOC55	IOC54	P8HS	P8LS	P7HS	P7LS
		Power-on	1	1	1	1	0	0	0	0
		/RESET & WDT	1	1	1	1	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x06	IOC60 (P6CR)	Bit Name	IOC67	IOC66	IOC65	IOC64	IOC63	IOC62	IOC61	IOC60
		Power-on	1	1	1	1	1	1	1	1
		/RESET & WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x07	IOC70 (P7CR)	Bit Name	IOC77	IOC76	IOC75	IOC74	IOC73	IOC72	IOC71	IOC70
		Power-on	1	1	1	1	1	1	1	1
		/RESET & WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x08	IOC80 (P8CR)	Bit Name	IOC87	IOC86	IOC85	IOC84	IOC83	IOC82	IOC81	IOC80
		Power-on	1	1	1	1	1	1	1	1
		/RESET & WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x09	IOC90 (RAM_ADDR)	Bit Name	X	RAM_A6	RAM_A5	RAM_A4	RAM_A3	RAM_A2	RAM_A1	RAM_A0
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x0A	IOCA0 (RAM_DB)	Bit Name	RAM_D7	RAM_D6	RAM_D5	RAM_D4	RAM_D3	RAM_D2	RAM_D1	RAM_D0
		Power-on	U	U	U	U	U	U	U	U
		/RESET & WDT	P	P	P	P	P	P	P	P
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0x0B	IOCB0 (CNT1PR)	Bit Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x0C	IOCC0 (CNT2PR)	Bit Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x0D	IOCD0 (HPWTPR)	Bit Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x0E	IOCE0 (LPWTPR)	Bit Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x0F	IOCF0 (IMR)	Bit Name	ICIE	LPWTE	HPWTE	CNT2E	CNT1E	INT1E	INT0E	TCIE
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x06	IOC61 (WUCR)	Bit Name	IROCS	X	X	X	/WUE8H	/WUE8L	/WUE6H	/WUE6L
		Power-on	0	U	U	U	0	0	0	0
		/RESET & WDT	0	U	U	U	0	0	0	0
		Wake-up from Pin Change	P	U	U	U	P	P	P	P

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x07	IOC71 (TCCCR)	Bit Name	INT_EDGE	INT	TS	TE	PSRE	TCCP2	TCCP1	TCCP0
		Power-on	1	0	1	1	1	1	1	1
		/RESET & WDT	1	0	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x08	IOC81 (WDTCR)	Bit Name	X	X	X	X	WDTE	WDTP2	WDTP1	WDTP0
		Power-on	U	U	U	U	0	1	1	1
		/RESET &WDT	U	U	U	U	0	1	1	1
		Wake-up from Pin Change	U	U	U	U	P	P	P	P
0x09	IOC91 (CNT12CR)	Bit Name	CNT2S	CNT2P2	CNT2P1	CNT2P0	CNT1S	CNT1P2	CNT1P1	CNT1P0
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x0A	IOCA1 (HLPWTCR)	Bit Name	LPWTS	LPWTP2	LPWTP1	LPWTP0	HPWTS	HPWTP2	HPWTP1	HPWTP0
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x0B	IOCB1 (P6PH)	Bit Name	PH67	PH66	PH65	PH64	PH63	PH62	PH61	PH60
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x0C	IOCC1 (P6OD)	Bit Name	OP67	OP66	OP65	OP64	OP63	OP62	OP61	OP60
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x0D	IOCD1 (P8PH)	Bit Name	PH87	PH86	PH85	PH84	PH83	PH82	PH81	PH80
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x0E	IOCE1 (P6PL)	Bit Name	PL67	PL66	PL65	PL64	PL63	PL62	PL61	PL60
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x00	R0 (IAR)	Bit Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Power-on	U	U	U	U	U	U	U	U
		/RESET & WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x01	R1 (TCC)	Bit Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x02	R2 (PC)	Bit Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	Jump to Address 0x0018 or continue to execute next instruction.							
0x03	R3 (SR)	Bit Name	X	PS1	PS0	T	P	Z	DC	C
		Power-on	U	0	0	1	1	U	U	U
		/RESET & WDT	U	0	0	t	t	P	P	P
		Wake-up from Pin Change	U	P	P	t	t	P	P	P
0x04	R4 (RSR)	Bit Name	RBS1	RBS0	RSR5	RSR4	RSR3	RSR2	RSR1	RSR0
		Power-on	0	0	U	U	U	U	U	U
		/RESET & WDT	0	0	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x05	Bank 0 R5 (Port 5)	Bit Name	R57	R56	R55	R54	X	X	X	IOCPAGE
		Power-on	1	1	1	1	U	U	U	0
		/RESET & WDT	1	1	1	1	U	U	U	0
		Wake-up from Pin Change	P	P	P	P	U	U	U	P
0x06	Bank 0 R6 (Port 6)	Bit Name	R67	R66	R65	R64	R63	R62	R61	R60
		Power-on	1	1	1	1	1	1	1	1
		/RESET & WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x7	Bank 0 R7 (Port 7)	Bit Name	R77	R76	R75	R74	R73	R62	R71	R70
		Power-on	1	1	1	1	1	1	1	1
		/RESET & WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x8	Bank 0 R8 (Port 8)	Bit Name	R87	R86	R85	R84	R83	R82	R81	R80
		Power-on	1	1	1	1	1	1	1	1
		/RESET & WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x9	Bank 0 R9 (LCDCR)	Bit Name	BS	DS1	DS0	LCDEN	X	LCDTYPE	LCDF1	LCDF0
		Power-on	1	1	0	0	U	0	0	0
		/RESET & WDT	1	1	0	0	U	0	0	0
		Wake-up from Pin Change	P	P	P	P	U	P	P	P
0xA	Bank 0 RA (LCD_ADDR)	Bit Name	X	X	X	LCD_A4	LCD_A3	LCD_A2	LCD_A1	LCD_A0
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0xB	Bank 0 RB (LCD_DB)	Bit Name	X	X	X	X	LCD_D3	LCD_D2	LCD_D1	LCD_D0
		Power-on	U	U	U	U	U	U	U	U
		/RESET & WDT	U	U	U	U	P	P	P	P
		Wake-up from Pin Change	U	U	U	U	P	P	P	P
0xC	Bank0 RC (CNTER)	Bit Name	X	X	X	X	LPWTEN	HPWTEN	CNT2EN	CNT1EN
		Power-on	0	1	0	0	0	0	0	0
		/RESET & WDT	0	1	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	0	P	P	P	P	P
0xD	Bank 0 RD (SBPCR)	Bit Name	X	CLK2	CLK1	CLK0	IDLE	BF1	BF0	CPUS
		Power-on	U	0	0	0	1	0	0	*1
		/RESET & WDT	U	0	0	0	1	0	0	*1
		Wake-up from Pin Change	U	P	P	P	P	P	P	P
0xE	Bank 0 RE (IRCR)	Bit Name	IRE	HF	LGP	X	IROUTE	TCCE	EINT1	EINT0
		Power-on	0	0	0	U	0	0	0	0
		/RESET & WDT	0	0	0	U	0	0	0	0
		Wake-up from Pin Change	P	P	P	U	P	P	P	P
0xF	Bank 0 RF (ISR)	Bit Name	ICIF	LPWTF	HPWTF	CNT2F	CNT1F	INT1F	INT0F	TCIF
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	N	P	P	P	P	P	P	P
0x5	Bank 1 R5 (P5HDSCR)	Bit Name	H57	H56	H55	H54	-	-	-	-
		Power-On	1	1	1	1	1	1	1	1
		/RESET and WDT	P	P	P	P	1	1	1	1
		Wake-Up from Pin Change	P	P	P	P	1	1	1	1

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x6	Bank 1 R6 (P6HDSCR)	Bit Name	H67	H66	H65	H64	H63	H62	H61	H60
		Power-On	1	1	1	1	1	1	1	1
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0x7	Bank 1 R7 (P78HDSCR)	Bit Name	-	-	-	-	P8HHDS	P8LHDS	P7HHDS	P7LHDS
		Power-On	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	P	P	P	P
		Wake-Up from Pin Change	1	1	1	1	P	P	P	P
0x8	Bank 1 R8 (ADSR1)	Bit Name	ADE7	ADE6	ADE5	ADE4	ADE3	ADE2	ADE1	ADE0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0x9	Bank 1 R9 (ADSR2)	Bit Name	-	ADE14	ADE13	ADE12	ADE11	ADE10	ADE9	ADE8
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	0	P	P	P	P	P	P	P
0xA	Bank 1 RA (ADCR)	Bit Name	-	CKR1	CKR0	ADRUN	ADP	-	SHS1	SHS0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	0	P	P	P	P	0	P	P
0xB	Bank 1 RB (ADISR)	Bit Name	VREFS	VREF2	VREF1	VREF0	ADIS3	ADIS2	ADIS1	ADIS0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0xC	Bank 1 RC (ADDL)	Bit Name	ADD7	ADD6	ADD5	ADD4	ADD3	ADD2	ADD1	ADD0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0xD	Bank 1 RD (ADDH)	Bit Name	ADD11	ADD10	ADD9	ADD8	ADD7	ADD6	ADD5	ADD4
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0xE	Bank 1 RE (IMR2)	Bit Name	-	-	-	-	-	-	-	ADIE
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	0	0	0	0	0	0	0	P
0xF	Bank 1 RF (SF2)	Bit Name	-	-	-	-	-	-	-	ADIF
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	0	0	0	0	0	0	0	P
0x10 ~ 0x3F	R10~R3F	Bit Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Power-on	U	U	U	U	U	U	U	U
		/RESET & WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P

Note: *This bit is equal to the Code Option HLFS bit data*

Legend: ***"x"*** *= not used* ***"P"*** *= previous value before reset*

"–" *= Not defined* ***"t"*** *= check R3 register explanation*

"u" *= unknown or don't care* *"**N**" = Monitors interrupt operation status*

The controller can be awakened from sleep mode and idle mode. The wake-up signals are listed as follows:

Wakeup Signal	Sleep Mode	Idle Mode	Green Mode	Normal Mode 1
TCC time out IOCF Bit 0=1	X	X	Interrupt	Interrupt
INT0 pin IOCF Bit 1=1	Wake-up + interrupt + next instruction	Wake-up + interrupt + next instruction	Interrupt	Interrupt
INT1 pin IOCF Bit 2=1	Wake-up + interrupt + next instruction	Wake-up + interrupt + next instruction	Interrupt	Interrupt
Counter 1 IOCF Bit 3=1	X	Wake-up + interrupt + next instruction	Interrupt	Interrupt
Counter 2 IOCF Bit 4=1	X	Wake-up + interrupt + next instruction	Interrupt	Interrupt
High-pulse timer IOCF Bit 5=1	X	Wake-up + interrupt + next instruction	Interrupt	Interrupt
Low-pulse timer IOCF Bit 6=1	X	Wake-up + interrupt + next instruction	Interrupt	Interrupt
Port6, Port 8 (input status change wake-up)	IOCF Bit 7=0 Wake-up + next instruction IOCF Bit 7=1 Wake-up + interrupt + next instruction	IOCF Bit 7=0 Wake-up + next instruction IOCF Bit 7=1 Wake-up + interrupt + next instruction	X	X
ADC conversion complete Bank1 RF Bit 0=1	Bank1 RE Bit0=1 Wake-up + interrupt + next instruction	Bank1 RE Bit 0=1 Wake-up + interrupt + next instruction	Interrupt	Interrupt
WDT time out	X	RESET	RESET	RESET

6.6 Oscillator

6.6.1 Oscillator Modes

The EM78P516N can operate in three different oscillator modes:

a.) Main oscillator (R-OSCI, OSCO), such as RC oscillator with external resistor and Internal capacitor mode (ERIC)

b.) Crystal oscillator mode

c.) PLL operation mode (R-OSCI connected to 0.01μF capacitor then connected to Ground). User can select which mode by programming FMMD1 and FMMD0 in the Code Options Register. The sub-oscillator can be operated in Crystal mode and ERIC mode. Table 3 below shows how these three modes are defined.

Table 3 Oscillator Modes as defined by FSMD, FMMD1, FMMD0

FSMD	FMMD1	FMMD0	Main Clock	Sub-clock
0	0	0	RC type (ERIC)	RC type (ERIC)
0	0	1	Crystal type	RC type (ERIC)
0	1	×	PLL type	RC type (ERIC)
1	0	0	RC type (ERIC)	Crystal type
1	0	1	Crystal type	Crystal type
1	1	×	PLL type	Crystal type

Table 4 Summary of Maximum Operating Speeds

Conditions	VDD	Fxt Max. (MHz)
Two clocks	2.3	4
	3.0	8
	5.0	10

6.6.2 Phase Lock Loop (PLL Mode)

When operate on PLL mode, the High frequency determined by sub-oscillator. We can choose RD register to change high oscillator frequency. The relation between high frequency (Fm) and sub-oscillator is shown as below table:

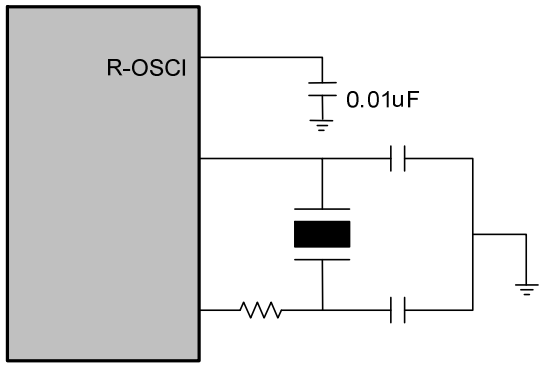


Figure 6-6 PLL Mode Circuit

Bits 6~4 (CLK2~0) of RD: Main clock selection bits for PLL mode (code option select)

CLK2	CLK1	CLK0	Main clock	Example Fs=32.768kHz
0	0	0	Fs × 130	4.26 MHz
0	0	1	Fs × 65	2.13 MHz
0	1	0	Fs × 65/2	1.065 MHz
0	1	1	Fs × 65/4	532kHz
1	×	×	Fs × 244	8 MHz

6.6.3 Crystal Oscillator/Ceramic Resonators (Crystal)

This LSI can be driven by an external clock signal through the R-OSCI pin as shown in Figure 6-7 below. In most applications, the R-OSCI pin and the OSCO pin can be connected with a crystal or ceramic resonator to generate oscillation. Fig. 6-8 depicts such circuit. Table 5 provides the recommended values of C1 and C2. Since each resonator has its own attribute, user should refer to its specification for appropriate values of C1 and C2. RS, a serial resistor, may be necessary for AT strip cut crystal or low frequency mode.

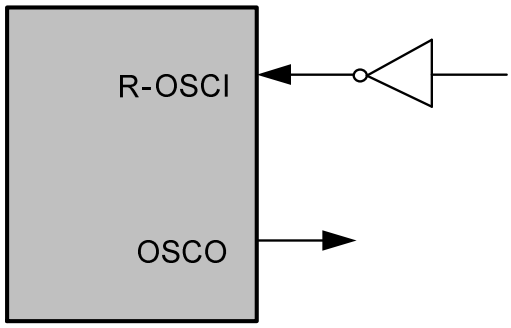


Figure 6-7 External Clock Input Circuit

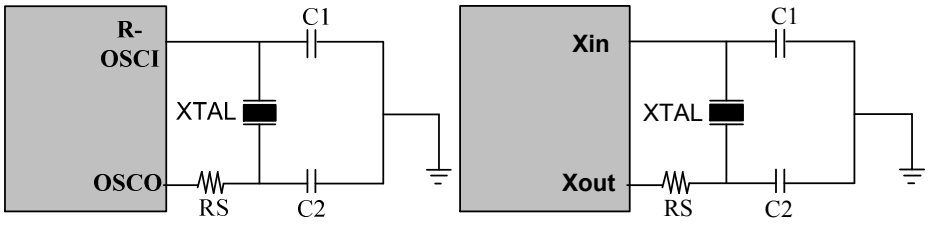


Figure 6-8 Circuit for Crystal/Resonator

Table 5 Capacitor Selection Guide for Crystal Oscillator or Ceramic Resonators

Oscillator Source	Oscillator Type	Frequency	C1 (pF)	C2 (pF)
Main oscillator	Ceramic Resonators	455kHz	100~150	100~150
		2.0 MHz	20~40	20~40
		4.0 MHz	10~30	10~30
	Crystal Oscillator	455kHz	20~40	20~150
		1.0 MHz	15~30	15~30
		2.0 MHz	15	15
		4.0 MHz	15	15
Sub-oscillator	Crystal Oscillator	32.768kHz	25	25

6.6.4 RC Oscillator Mode with Internal Capacitor

If both precision and cost are taken into consideration, this LSI also offers a special oscillation mode, which has an on-chip internal capacitor and an external resistor connected to VDD. The internal capacitor functions as temperature compensator. In order to obtain more accurate frequency, a precise resistor is recommended.

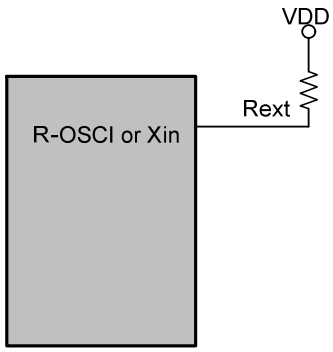


Figure 6-9 Circuit for Internal C Oscillator Mode

Table 6 RC Oscillator Frequencies

Pin	Rext	Average Fosc 5V, 25℃	Average Fosc 3V, 25℃
R-OSCI	51k	2.2221 MHz	2.1972 MHz
	100k	1.1345 MHz	1.1203 MHz
	300k	381.36kHz	374.77kHz
Xin	2.2M	32.768kHz	32.768kHz

Note: *Measured from QFP packages with frequency drift of about ±30%.*
Values are provided for design reference only.

6.7 Power-on Considerations

Any microcontroller (as with this LSI) is not warranted to start operating properly before the power supply stabilizes in a steady state. This LSI has an on-chip Power-on Reset (POR) with detection level range as shown on the table below. The circuitry eliminates the extra external reset circuit but will work well only if the VDD rises quickly enough (50ms or less). However, under critical applications, extra devices are still required to assist in solving power-on problems.

Power-on voltage detector provided

IC	Voltage Range
EM78P516N	1.7V to 1.9V

6.7.1 External Power-on Reset Circuit

This circuit implements an external RC to produce a reset pulse (see Figure 6-10). The pulse width (time constant) should be kept long enough to allow VDD to reach minimum operation voltage. This circuit is used when the power supply rise time is slow. Because the current leakage from the /RESET pin is ± 5 μA, it is recommended that R should not be greater than 40K. In this way, the voltage at Pin /RESET is held below 0.2V. The diode (D) acts as a short circuit at power-down. The capacitor, C, is discharged rapidly and fully. Rin, the current-limited resistor, prevents high current discharge or ESD (electrostatic discharge) from flowing into Pin /RESET.

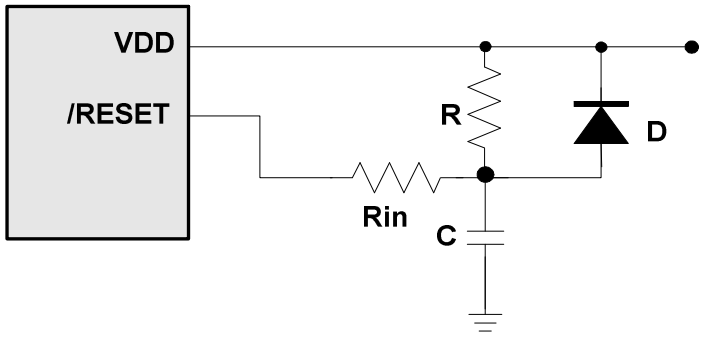


Figure 6-10 External Power-on Reset Circuit

6.7.2 Residue-Voltage Protection

When battery is replaced, device power (VDD) is disconnected but residue-voltage remains. The residue-voltage may trips below minimum VDD, but above zero. This condition may cause poor power on reset. Figure 6-11 and Figure 6-12 show how to build a residue-voltage protection circuit.

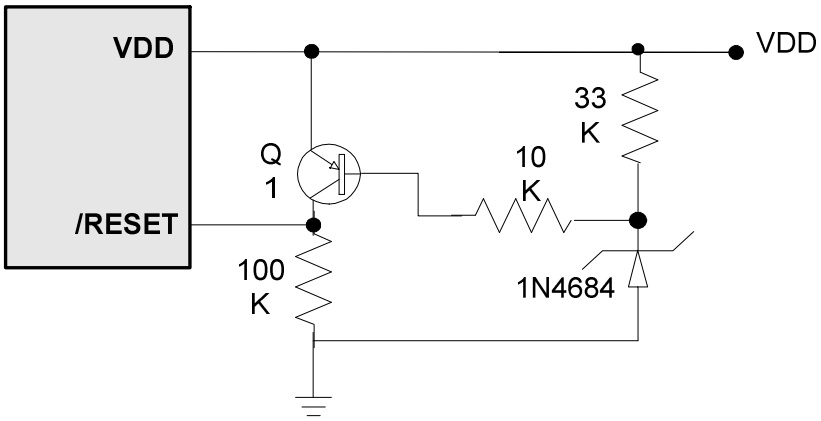


Figure 6-11 Residue Voltage Protection Circuit 1

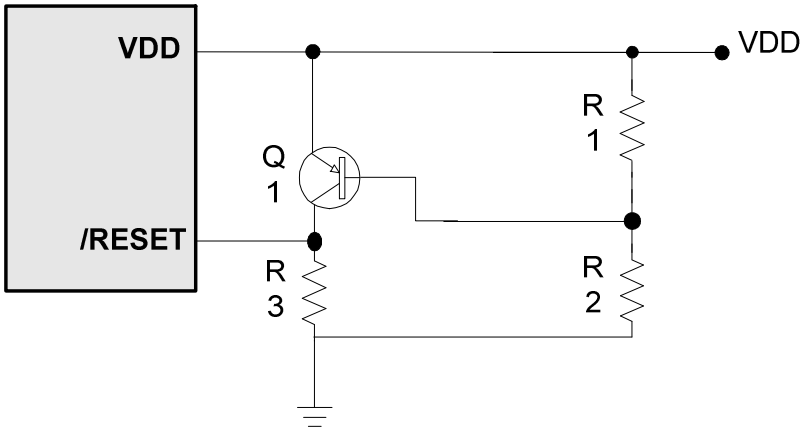


Figure 6-12 Residue Voltage Protection Circuit 2

6.8 Interrupt

This LSI has eight interrupt sources as listed below:

- TCC overflow interrupt
- External interrupt P54/INT0 pin
- External interrupt P55/INT1 pin
- Counter 1 underflow interrupt
- Counter 2 underflow interrupt
- High-pulse width timer underflow interrupt
- Low-pulse width timer underflow interrupt
- Port 6, Port 8 input status change wake-up
- Analog to Digital conversion completed

This IC has internal interrupts which are falling edge triggered or as follows**:**

- TCC timer overflow interrupt
- Four 8-bit down counter/timer underflow interrupt

If these interrupt sources change signal from high to low, the RF register will generate a "1" flag to the corresponding register if the IOCF0 register is enabled.

RF is the interrupt status register. It records the interrupt request in flag bit. IOCF0 is the interrupt mask register. Global interrupt is enabled by ENI instruction and disabled by DISI instruction. When one of the interrupts (when enabled) is generated, it will cause the next instruction to be fetch from Address 0003H~0018H according to interrupt source.

With this LSI, each individual interrupt source has its own interrupt vector as depicted in Table 3. Before the interrupt subroutine is executed, the contents of the ACC and the R3 register are initially saved by the hardware. After the interrupt service routine is completed, the ACC and R3 are restored. The existing interrupt service routine does not allow other interrupt service routine to be executed. Hence, if other interrupts occur while an existing interrupt service routine is being executed, the hardware will save the later interrupts. Only after the existing interrupt service routine is completed that the next interrupt service routine is executed.

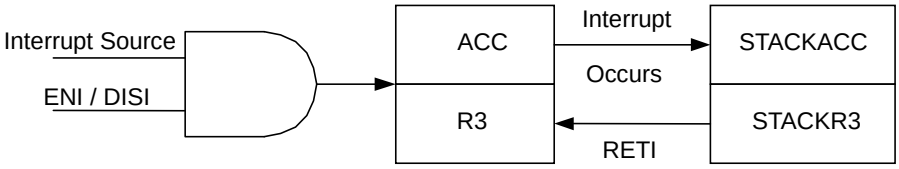


Fig. 6-13 Interrupt Back-up Diagram

Table 3 Interrupt Vector

Interrupt Vector	Interrupt Status
0003H	TCC overflow interrupt.
0006H	External interrupt P5.4/INT0 pin
0009H	External interrupt P5.5/INT1 pin
000CH	Counter 1 underflow interrupt
000FH	Counter 2 underflow interrupt
0012H	High-pulse width timer underflow interrupt
0015H	Low-pulse width timer underflow interrupt
0018H	Port 6, Port 8 input status change wake up
001BH	AD conversion complete interrupt

6.9 LCD Driver

This LSI can drive an LCD of up to 32 segments and 4 commons that can drive a total of 4×32 dots. The LCD block is made up of an LCD driver, display RAM, segment output pins, common output pins, and LCD operating power supply pins. This circuit works on normal mode, green mode and idle mode. The LCD duty; bias; the number of segment; the number of common and frame frequency are determined by the LCD controller register.

The basic structure contains a timing control that uses a subsystem clock to generate the proper timing for different duty and display accesses. The R9 register is a command register for the LCD driver which includes LCD enable/disable, bias (1/2 and 1/3), duty (1/2, 1/3, 1/4), and LCD frame frequency control. The register RA is an LCD contrast and LCD RAM address control register. The register RB is an LCD RAM data buffer. LCD booster circuit can change the operation frequency to improve VLCD2 and VLCD3 drive capability. The control register is described as follows.

6.9.1 R9/LCDCR (LCD Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BS	DS1	DS0	LCDEN	–	LCDTYPE	LCDF1	LCDF0
R/W	R/W	R/W	R/W	-	R/W	R/W	R/W

Bit 7 (BS): LCD bias select bit

"0": (1/2 bias)

"1": (1/3 bias)

Bits 6 ~ 5 (DS1 ~ DS0): LCD duty select

DS1	DS0	LCD Duty
0	0	1/2 duty
0	1	1/3 duty
1	×	1/4 duty

Bit 4 (LCDEN): LCD enable bit

"0": disable the LCD circuit

"1": enable the LCD circuit

When the LCD function is disabled, all common/segment output is set to ground (GND) level

Bit 3: Not used

Bit 2 (LCDTYPE): LCD drive waveform type select bit

LCDTYPE = "0": "A" type waveform

LCDTYPE = "1": "B" type waveform

Bits 1 ~ 0 (LCDF1 ~ LCDF0): LCD frame frequency control bits

LCDF1	LCDF0	LCD Frame Frequency (e.g. Fs=32.768kHz)		
		1/2 Duty	1/3 Duty	1/4 Duty
0	0	Fs/(256×2)=64.0	Fs/(172×3)=63.5	Fs/(128×4)=64.0
0	1	Fs/(280×2)=58.5	Fs/(188×3)=58.0	Fs/(140×4)=58.5
1	0	Fs/(304×2)=53.9	Fs/(204×3)=53.5	Fs/(152×4)=53.9
1	1	Fs/(232×2)=70.6	Fs/(156×3)=70.0	Fs/(116×4)=70.6

Note: *Fs: sub-oscillator frequency*

6.9.2 RA/LCD_ADDR (LCD Address)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	LCD_A4	LCD_A3	LCD_A2	LCD_A1	LCD_A0
-	-	-	R/W	R/W	R/W	R/W	R/W

Bits 7 ~ 5: Not used, fixed to "0"

Bits 4 ~ 0 (LCDA4 ~ LCDA0): LCD RAM address

RA (LCD Address)	RB (LCD Data Buffer)					Segment
	Bits 7 ~4	Bit 3 (LCD_D3)	Bit 2 (LCD_D2)	Bit 1 (LCD_D1)	Bit 0 (LCD_D0)	
00H	–	–	–	–	–	**SEG0**
01H	–	–	–	–	–	**SEG1**
02H	–	–	–	–	–	**SEG2**
|			|			|
1DH	–	–	–	–	–	**SEG29**
1EH	–	–	–	–	–	**SEG30**
1FH	–	–	–	–	–	**SEG31**
Common	**X**	**COM3**	**COM2**	**COM1**	**COM0**	

6.9.3 RB/LCD_DB (LCD Data Buffer)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
–	–	–	–	LCD_D3	LCD_D2	LCD_D1	LCD_D0
-	-	-	-	R/W	R/W	R/W	R/W

Bits 7 ~ 4: Not used

Bits 3 ~ 0 (LCD_D3 ~ LCD_D0): LCD RAM data transfer registers

6.9.4 RD/SBPCR (System, Booster and PLL Control Registers)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
–	CLK2	CLK1	CLK0	IDLE	BF1	BF0	CPUS
–	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 2 ~ 1 (BF1 ~ 0): LCD booster frequency select bits

BF1	BF0	Booster Frequency
0	0	Fs
0	1	Fs/4
1	0	Fs/8
1	1	Fs/16

The initial setting flow chart for LCD function

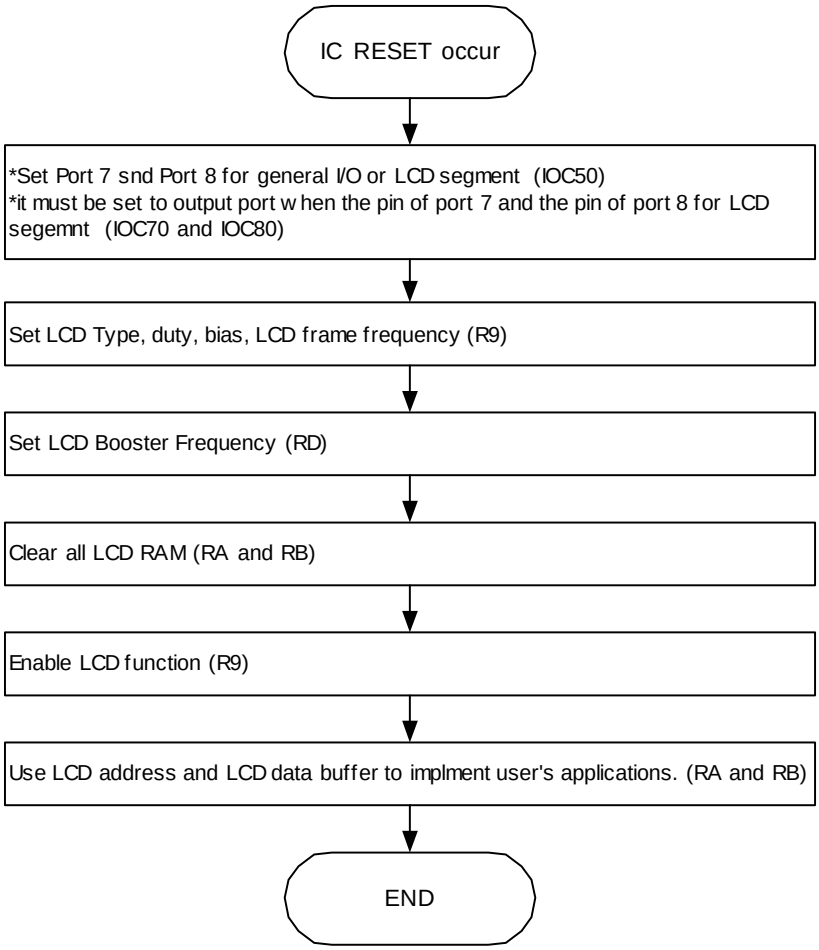
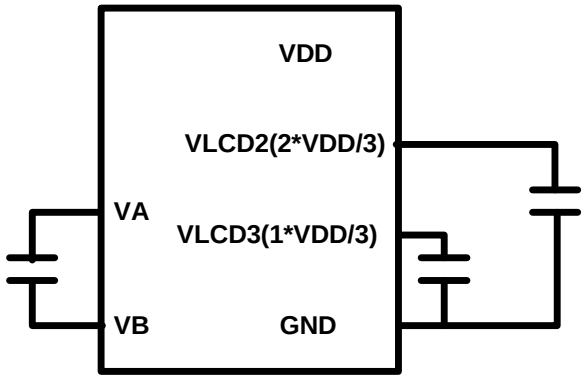
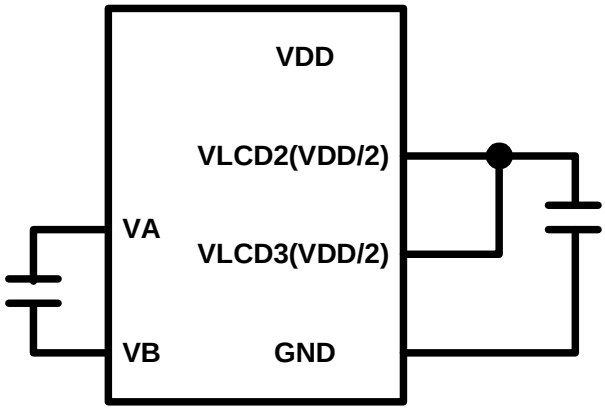


Figure 6-14 Initial Setting Flow chart for LCD Function

Boosting circuits connection for LCD voltage



External circuit for 1/3 Bias



External circuit for 1/2 Bias

Figure 6-15 Charge Bump Circuit Connection (Cext=0.1μf)

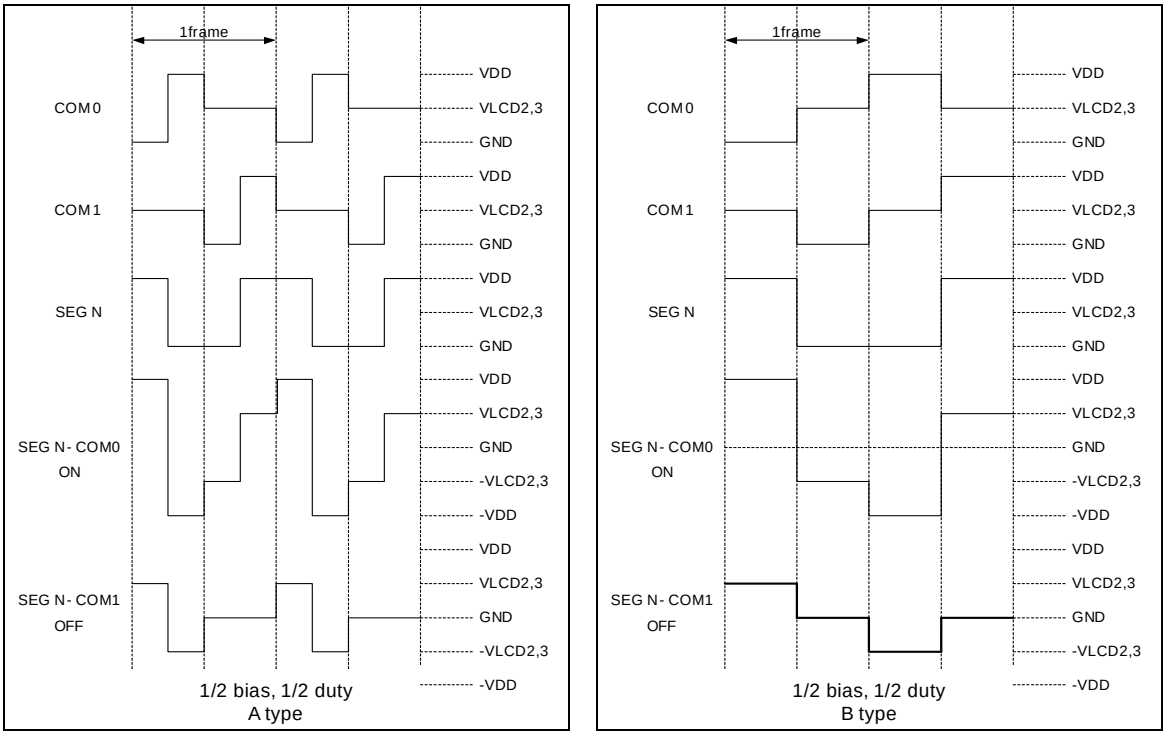


Figure 6-16 LCD Waveform for 1/2 Bias, 1/2 Duty

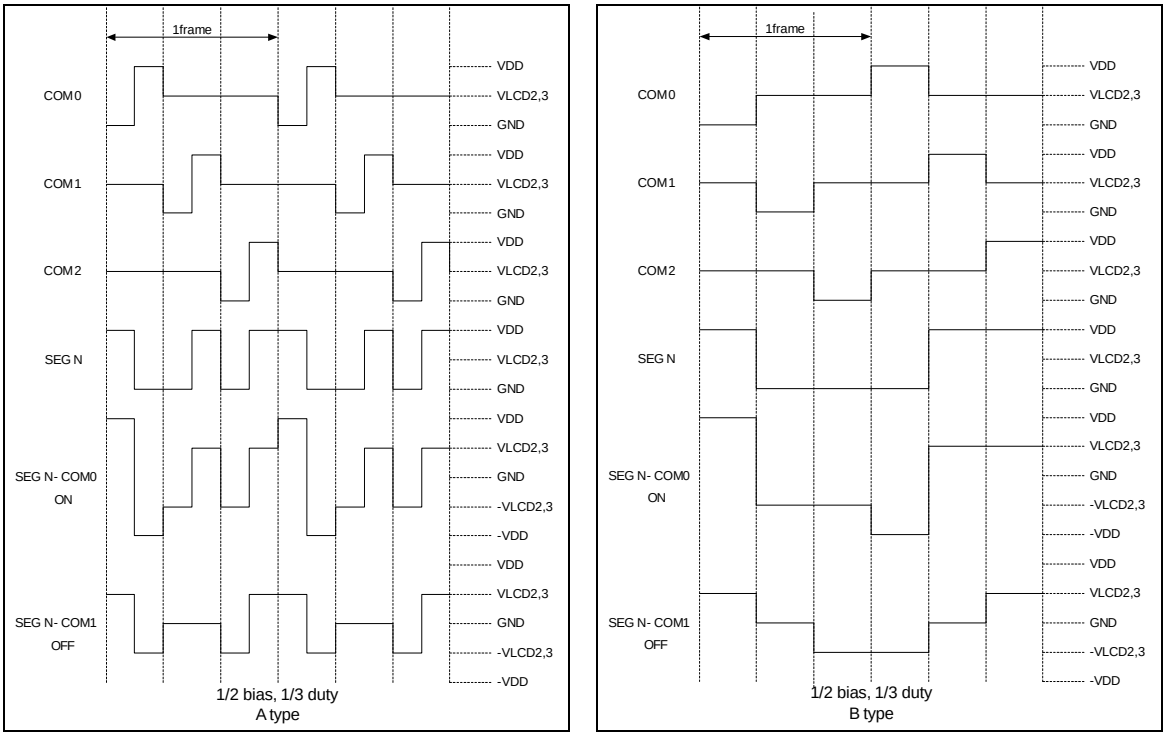


Figure 6-17 LCD Waveform for 1/2 Bias, 1/3 Duty

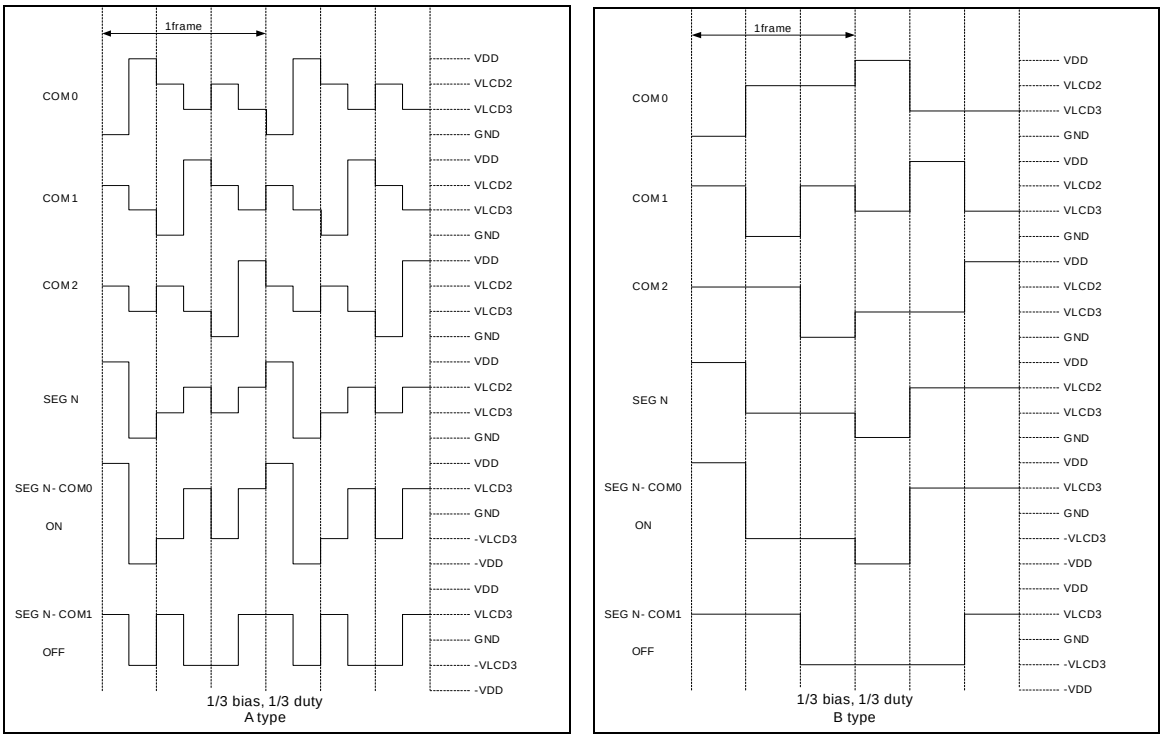


Figure 6-18 LCD Waveform for 1/3 Bias, 1/3 Duty

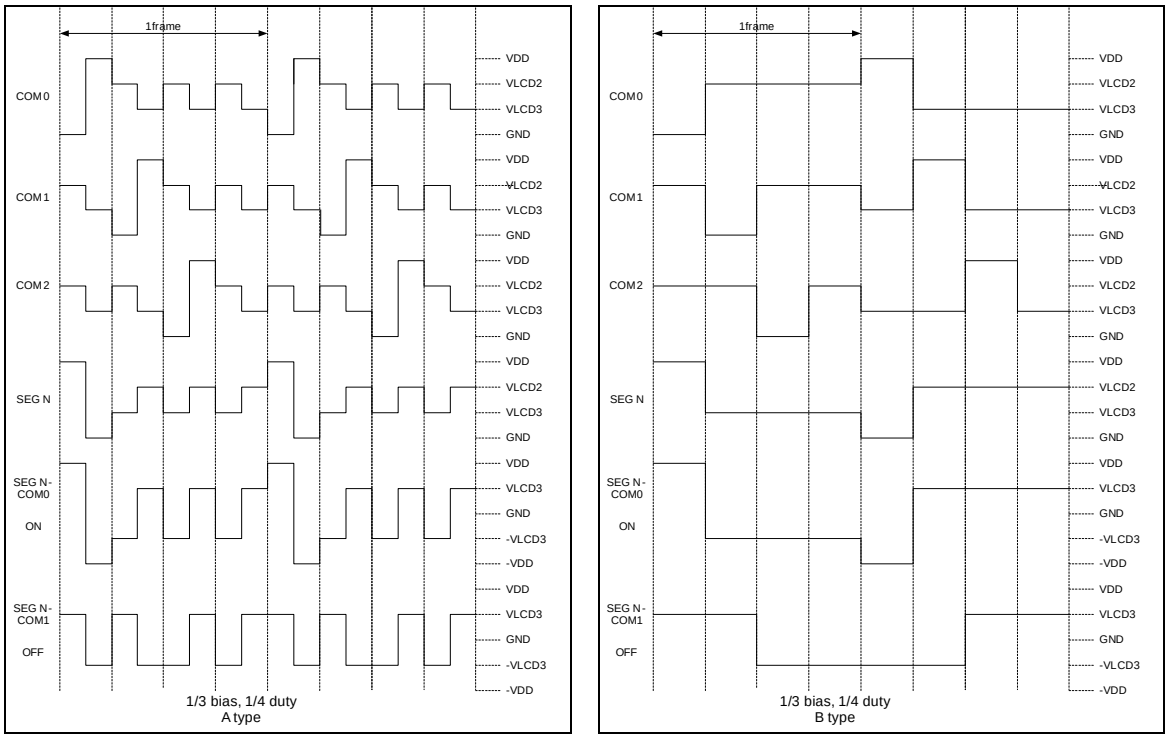


Figure 6-19 LCD Waveform for 1/3 Bias, 1/4 Duty

6.10 Infrared Remote Control Application/PWM Waveform Generation

This LSI can output infrared carrier in user-friendly or in PWM standard waveform. The IR and PWM waveform generated functions include an 8-bit down count timer/counter, high-pulse width timer, low-pulse width timer, and IR control register. The IR system block diagram is shown in Fig. 6-20. The IROUT pin waveform is determined by IR control register (RE), IOC90 (Counters 1 and 2 control register), IOCA0 (high-pulse width timer, low-pulse width timer control register), IOCC0 (Counter 2 preset), IOCD0 (high-pulse width timer preset register), and IOCE0 (low-pulse width timer preset register). Details on Fcarrier, high-pulse time, and low pulse time are explained as follows**:**

If Counter 2 clock source is F_T (this clock source can be set by IOC91), then

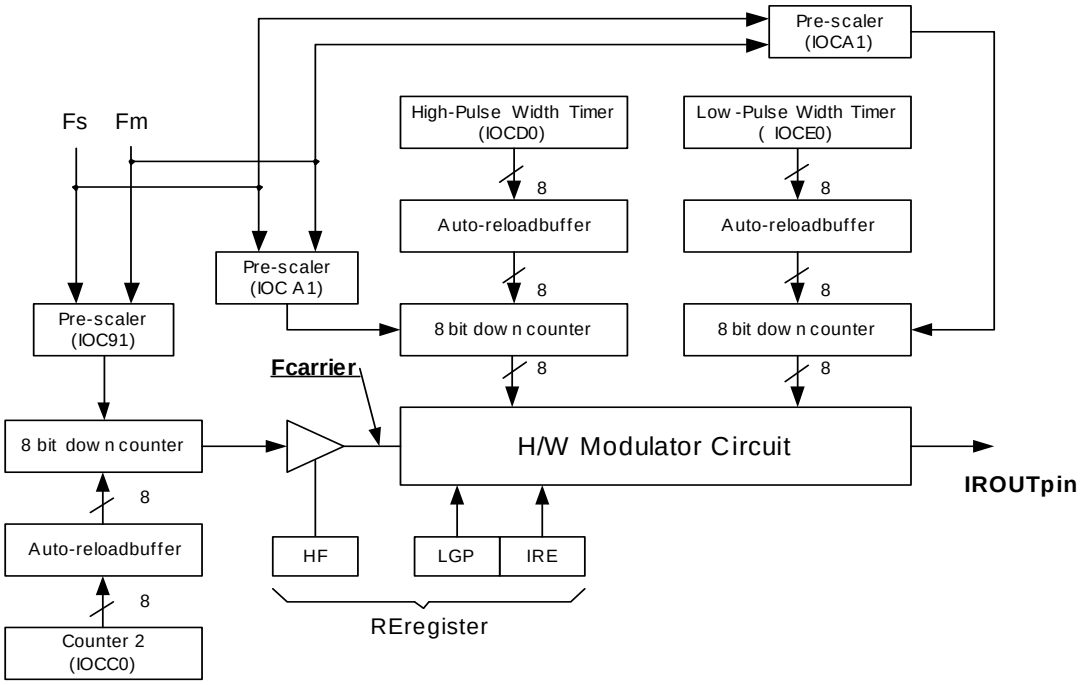
$$F_{carrier} = \frac{F_T}{2 \times (1 + decimal \quad of \quad Counter \quad 2 \quad preset \quad value \quad (IOCC \quad 0)) \times prescaler}$$

If the high-pulse width timer clock source is FT (this clock source can be set by IOCA1), then

$$T_{high \quad pulse \quad time} = \frac{prescaler \quad \times (1 + decimal \quad of \quad high \quad pulse \quad width \quad timer \quad value \quad (IOCD \quad 0))}{F_T}$$

If the low-pulse width timer clock source is FT (this clock source can be set by IOCA1);

$$T_{low \quad pulse \quad time} = \frac{prescaler \quad \times (1 + decimal \quad of \quad low \quad pulse \quad width \quad timer \quad value \quad (IOCE \quad 0))}{F_T}$$



Fm: *main oscillator frequency* ***Fs:*** *sub-oscillator frequency*

Figure 6-20 IR/PWM System Block Diagram

The IROUT output waveform is further explained in the following figures:

Figure 6-21 LGP=0, HF=1, the IROUT waveform can modulate Fcarrier waveform when in low-pulse width time.

Figure 6-22 LGP=0, HF=0, the IROUT waveform cannot modulate Fcarrier waveform when in low-pulse width time. So IROUT waveform is determined by high-pulse time and low-pulse time. This mode can produce standard PWM waveform.

Figure 6-23 LGP=0, HF=1, the IROUT waveform can modulate Fcarrier waveform when in low-pulse width time. When IRE goes from high to low, the output waveform of IROUT will keep on transmitting until high-pulse width timer interrupt occurs.

Figure 6-24 LGP=0, HF=0, the IROUT waveform can not modulate Fcarrier waveform when in low-pulse width time. So IROUT waveform is determined by high-pulse time and low-pulse time. This mode can produce standard PWM waveform. When IRE goes from high to low, the output waveform of IROUT will keep on transmitting till high-pulse width timer interrupt occurs.

Figure6-25 LGP=1, when this bit is set to high level, the high-pulse width timer is ignored. So IROUT waveform output from low-pulse width timer is established.

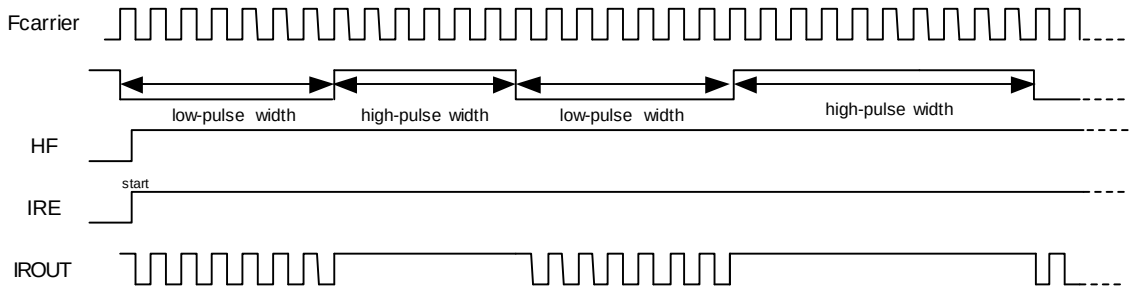


Figure 6-21 LGP=0, IROUT Pin Output Waveform

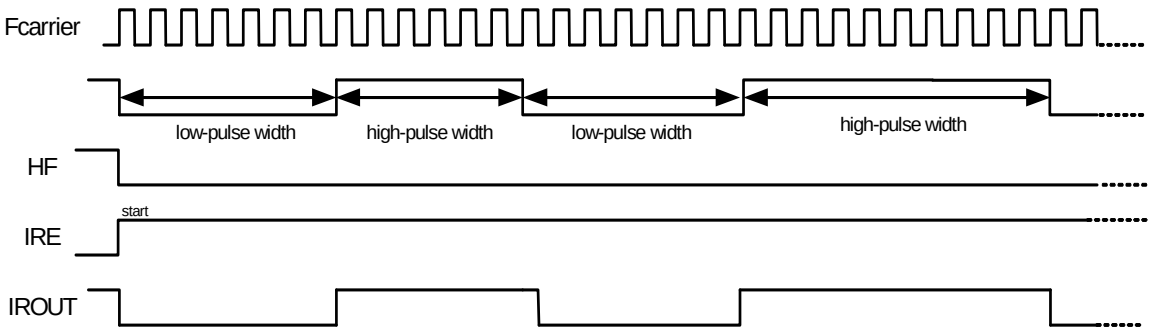


Figure 6-22 LGP=0, IROUT Pin Output Waveform

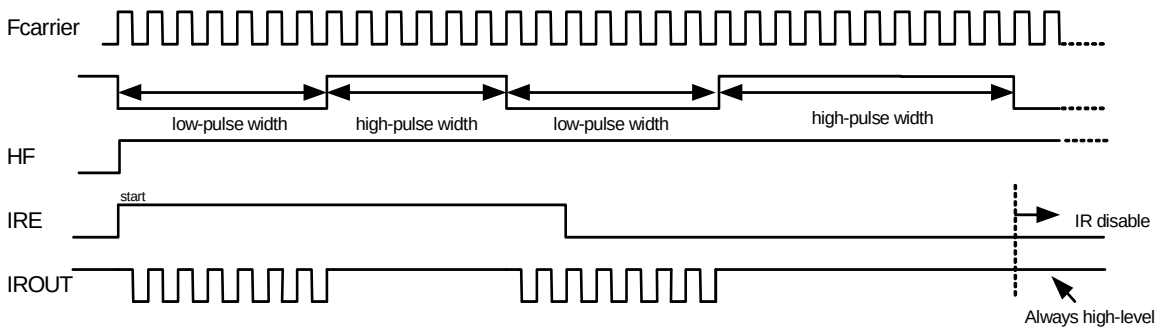


Figure 6-23 LGP=0, IROUT Pin Output Waveform

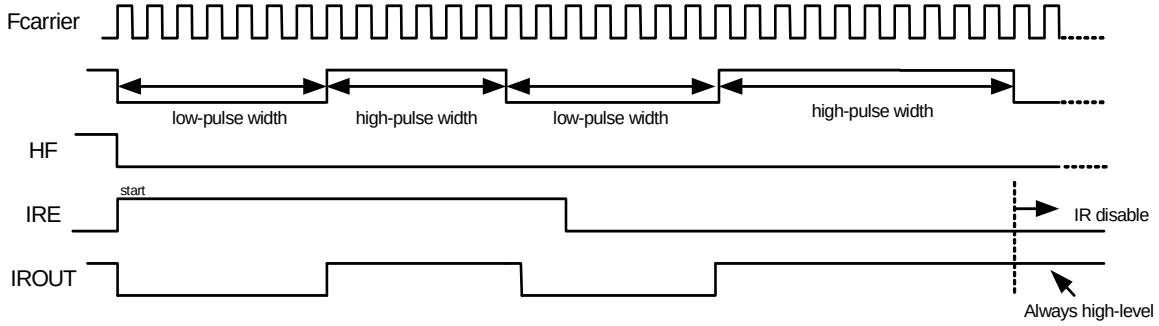


Figure 6-24 LGP=0, IROUT Pin Output Waveform

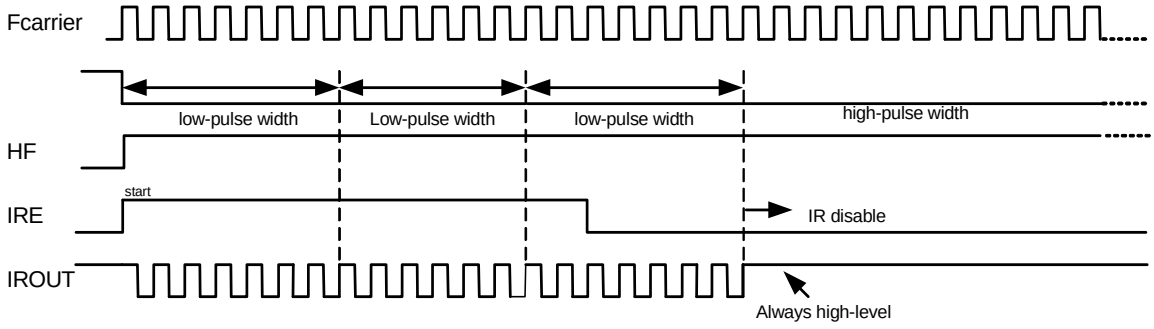
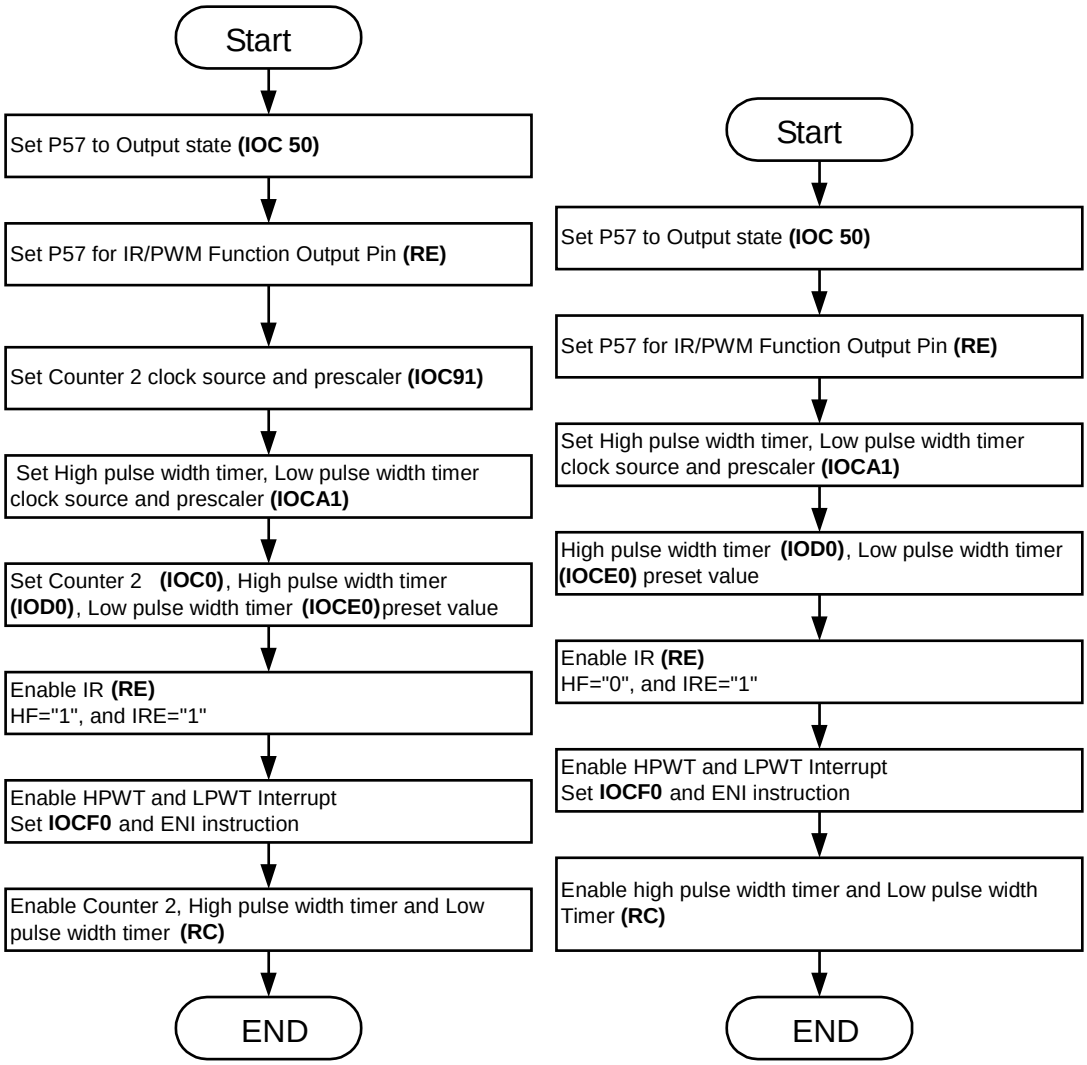


Figure 6-25 LGP=1, IROUT Pin Output Waveform

IR/PWM Function Enable Flowchart



(a) IR application (b) PWM application

Figure 6-26 IR/PWM Function Enable Flow chart

6.11 Analog-to-Digital Converter (ADC)

The analog-to-digital circuitry consists of an 16-bit analog multiplexer; two control registers (ADCR1/BANK1 RA and ADISR/BANK1 RB), two data registers (ADDH/BANK1 RD and ADDL/BANK1 RC) and an ADC with 12-bit resolution as shown in the functional block diagram below. The analog reference voltage (Vref) and the analog ground are connected via separate input pins.

The ADC module utilizes successive approximation to convert the unknown analog signal into a digital value. The result is fed to the ADDH and ADDL. Input channels are selected by the analog input multiplexer via the ADISR register bits. Connecting to the external VREF is more accurate than connecting to the internal VDD.

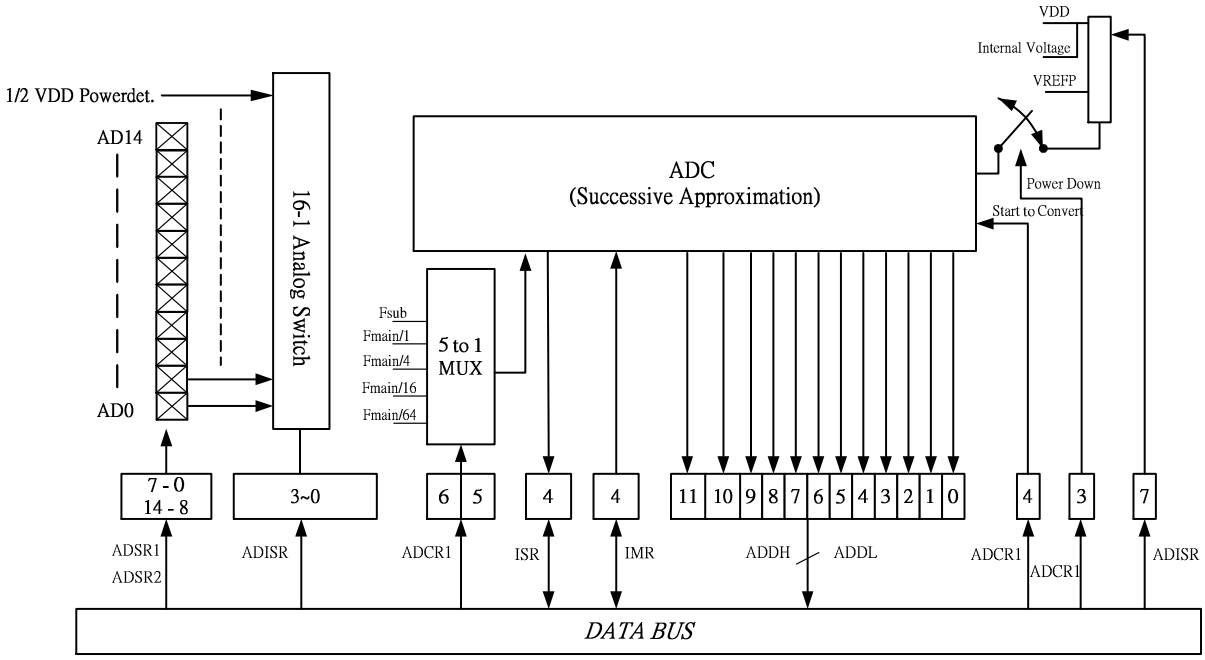


Figure 6-11 Analog-to-Digital Conversion Functional Block Diagram

6.11.1 ADC Control Register

6.11.1.1 Bank 1 R8, ADSR1 (ADC Input Select Register 1)

(Address: 08h)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADE7	ADE6	ADE5	ADE4	ADE3	ADE2	ADE1	ADE0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7 (ADE7): AD converter enable bit of P64 pin

0 = Disable AD7, P64 functions as I/O pin

1 = Enable AD7 to function as analog input pin

Bit 6 (ADE6): AD converter enable bit of P63 pin

0 = Disable AD6, P63 functions as I/O pin

1 = Enable AD6 to function as analog input pin

Bit 5 (ADE5): AD converter enable bit of P62 pin

0 = Disable AD5, P62 functions as I/O pin

1 = Enable AD5 to function as analog input pin

Bit 4 (ADE4): AD converter enable bit of P61 pin

0 = Disable AD4, P61 functions as I/O pin

1 = Enable AD4 to function as analog input pin

Bit 3 (ADE3): AD converter enable bit of P60 pin

0 = Disable AD3, P60 functions as I/O pin

1 = Enable AD3 to function as analog input pin

Bit 2 (ADE2): AD converter enable bit of P57 pin

0 = Disable AD2, P57/IROUT functions pin

1 = Enable AD2 to function as analog input pin

Bit 1 (ADE1): AD converter enable bit of P55 pin

0 = Disable AD1, P55/INT1 functions pin

1 = Enable AD1 to function as analog input pin

Bit 0 (ADE0): AD converter enable bit of P54 pin

0 = Disable AD0, P54/INT0 functions pin

1 = Enable AD0 to function as analog input pin

6.11.1.2 Bank 1 R9, ADSR2 (ADC Input Select Register 2)

(Address: 09h)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	ADE14	ADE13	ADE12	ADE11	ADE10	ADE9	ADE8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7: Not used, set to “0” all the time.

Bit 6 (ADE14): AD converter enable bit of P84 pin

0 = Disable AD14, SEG28/P84 functions pin

1 = Enable AD14 to function as analog input pin

Bit 5 (ADE13): AD converter enable bit of P85 pin

0 = Disable AD13, SEG29/P85 functions pin

1 = Enable AD13 to function as analog input pin

Bit 4 (ADE12): AD converter enable bit of P86 pin

0 = Disable AD12, SEG30/P86 functions pin

1 = Enable AD12 to function as analog input pin

Bit 3 (ADE11): AD converter enable bit of P87 pin

0 = Disable AD11, SEG31/P87 functions pin

1 = Enable AD11 to function as analog input pin

Bit 2 (ADE10): AD converter enable bit of P67 pin

0 = Disable AD10, P67 functions as I/O pin

1 = Enable AD10 to function as analog input pin

Bit 1 (ADE9): AD converter enable bit of P66 pin

0 = Disable AD9, P66 functions as I/O pin

1 = Enable AD9 to function as analog input pin

Bit 0 (ADE8): AD converter enable bit of P65 pin

0 = Disable AD8, P65 functions as I/O pin

1 = Enable AD8 to function as analog input pin

6.11.1.3 Bank 1 RA, ADCR (ADC Control Register)

(Address: 0Ah)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	CKR1	CKR0	ADRUN	ADP	-	SHS1	SHS0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7: Not used, set to "0" all the time.

Bits 6~5 (CKR1~0): Clock Rate Selection of ADC

System Mode	CKR[2:0]	Clock Rate
Normal Mode	00	$F_{Main}/16$
	01	$F_{Main}/4$
	10	$F_{Main}/64$
	11	$F_{Main}/1$
Green Mode	xxx	F_{Sub}

Bit 4 (ADRUN): ADC Starts to Run

0 : Reset on completion of the conversion by hardware, this bit cannot be reset by software.

1 : An A/D conversion starts. This bit can be set by software

Bit 3 (ADP): ADC Power

0 : ADC is in power down mode.

1 : ADC is operating normally.

Bit 2: Not used, set to "0" all the time.

Bit 1~0 (SHS1~0): Sample and Hold Timing Selection

SHS[1:0]	Sample & Hold Timing
00	2 x T_{AD}
01	4 x T_{AD}
10	8 x T_{AD}
11	12 x T_{AD}

6.11.1.4 Bank 1 RB, ADISR (ADC Input Channel and Internal Reference Selection Register)

(Address: 0Bh)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
VREFS	VREF2	VREF1	VREF0	ADIS3	ADIS2	ADIS1	ADIS0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7 (VREFS): The input source of the Vref of the ADC

0: The Vref of the ADC is connected to internal reference voltage (default value), and the P56/TCC/VREF pin carries out the function of P56/TCC.

: The Vref of the ADC is connected to P56/TCC/VREF

Bit 6~4 (VREF2~0): ADC internal reference voltage source

VREF[2:0]	ADC Internal Reference Voltage
000	VDD
001	4.0V ± 1%
010	3.0V ± 1%
011	2.5V ± 1%
1xx	2.0V ± 1%

Bits 3~0 (ADIS3~0): ADC input channel select bits

ADIS[3:0]	Selected Channel	ADIS[3:0]	Selected Channel
0000	ADC0	1000	ADC8
0001	ADC1	1001	ADC9
0010	ADC2	1010	ADC10
0011	ADC3	1011	ADC11
0100	ADC4	1100	ADC12
0101	ADC5	1101	ADC13
0110	ADC6	1110	ADC14
0111	ADC7	1111	1/2 VDD PowerDet.

6.11.1.5 Bank 1 RC, ADDL (Low Byte of Analog to Digital Converter Data)

(Address: 0Ch)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADD7	ADD6	ADD5	ADD4	ADD3	ADD2	ADD1	ADD0
R	R	R	R	R	R	R	R

Bits 7~0 (ADD7~0): Low Byte of AD Data Buffer

6.11.1.6 Bank 1 RD, ADDH (High Byte of Analog to Digital Converter Data)

(Address: 0Dh)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADD11	ADD10	ADD9	ADD8	ADD7	ADD6	ADD5	ADD4
R	R	R	R	R	R	R	R

Bits 7~0 (ADD11~4): High Byte of AD Data Buffer.

6.11.2 ADC Sampling Time

The accuracy, linearity, and speed of the successive approximation of the AD converter are dependent on the properties of the ADC and the comparator. The source impedance and the internal sampling impedance directly affect the time required to charge the sample holding capacitor. The application program controls the length of the sample time to meet the specified accuracy. Generally speaking, the program should wait for 2 μs for each KΩ of the analog source impedance and at least 2 μs for the low-impedance source. The maximum recommended impedance for analog source is 10KΩ at Vdd=5V. After the analog input channel is selected, this acquisition time must be done before the conversion is started.

6.11.3 AD Conversion Time

CKR1 and CKR0 select the conversion time (Tct), in terms of instruction cycles. This allows the MCU to run at the maximum frequency without sacrificing the AD conversion accuracy. For the EM78P516N, the conversion time per bit is about 1μs. The table below shows the relationship between Tct and the maximum operating frequencies.

System Mode	CKR[1:0]	Clock Rate	Max. Operation Frequency	Max. conversion Rate/Bit	Max. conversion Rate
Normal Mode	00	F_{Main}/16	10 MHz	625kHz (1.6µs)	16*1.6µs=25.6µs (39.06kHz)
	01	F_{Main}/4	4 MHz	1 MHz (1µs)	16*1µs=16µs (62.5kHz)
	10	F_{Main}/64	10 MHz	156.25kHz (6.4 µs)	16*6.4µs=102.4µs (9.765kHz)
	11	F_{Main}/1	1MHz	1MHz (1µs)	16*1µs=16µs (62.5kHz)
Green Mode	xxx	F_{Sub}	32.768kHz	32.768kHz (30.51µs)	16*30.51µs=488.28µs (2.048kHz)

NOTE

- *Pin not used as an analog input pin can be used as regular input or output pin.*
- *During conversion, do not perform output instruction to maintain precision for all of the pins.*

6.11.4 ADC Operation during Sleep Mode

In order to obtain a more accurate ADC value and reduce power consumption, the AD conversion remains operational during sleep mode. As the SLEP instruction is executed, all the MCU operations will stop except for the Oscillator, TCC, Timer 1, Timer 2, Timer 3, and AD conversion.

AD Conversion is considered completed as determined by**:**

1. The ADRUN bit of BANK1 RA register is cleared to “0”.
2. Waking up from AD conversion (where it remains in operation during sleep mode).

The results are fed into the ADDH and ADDL registers when conversion is completed. If the ADIE is enabled, the device will wake up. Otherwise, the AD conversion will be shut off, no matter what the status of the ADPD bit is.

6.11.5 Programming Process/Considerations

6.11.5.1 Programming Process

Follow these steps to obtain data from the ADC**:**

1. Write to the eight bits (ADE14: ADE0) on the BANK1 R8 & R9 (ADSR1&ADSR2) register to define the characteristics of R5,R6 and R8 (digital I/O, analog channels, or voltage reference pin)
2. Write to the Bank1 RA/ADCR1 register to configure the AD module**:**
   a) Select ADC input channel (ADIS3**:**ADIS0)
   b) Define AD conversion clock rate (CKR1**:**CKR0)
   c) Select the VREFS input source of the ADC
   d) Set the ADPD bit to 1 to begin sampling
3. Set the ADIE bit, if the wake-up function is employed
4. Write “ENI” instruction, if the interrupt function is employed
5. Set the ADRUN bit to 1
6. Write “SLEP+NOP” instruction
8. Wait for wake-up or for the ADRUN bit to be cleared to “0”.
9. Read the ADDH and ADDL conversion data registers. If the ADC input channel changes at this time, the ADDH and ADDL values can be cleared to ‘0’.
10. Clear the interrupt flag bit (ADIF).
11. For next conversion, go to Step 1 or Step 2 as required. At least two Tct is required before the next acquisition starts.

NOTE
In order to obtain accurate values, it is necessary to avoid any data transition on the I/O pins during AD conversion.

6.12 Code Options

The EM78P516N has one Code Option word that is not a part of the normal program memory. The option bits cannot be accessed during normal program execution.

Code Option Register and Customer ID Register arrangement distribution:

Word 1 of the code options is for customer ID code application.

Word 1
Bit 12~Bit 0

Word 0 of Code Options is for IC function setting. The following are the settings for OTP IC programming**:**

Mne-monic	Bits 12 ~ 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bits 2 ~ 0
	–	CYES	HLFS	ENWDTB	FSMD	FMMD1	FMMD0	HLP	PR2 ~ 0
1	–	High	High	Disable	High	High	High	High	Disable
0	–	Low	Low	Enable	Low	Low	Low	Low	Enable
Default	1	1	1	1	1	1	1	1	1

Bits 12 ~ 10: Not used.

These bits are set to “1” all the time.

Bit 9 (CYES): Cycle select for JMP and CALL instructions

CYES = "0": only one instruction cycle (JMP or CALL) can be executed

CYES = "1": two instruction cycles (JMP and CALL) can be executed

Bit 8 (HLFS): main or sub-oscillator select

HLFS = "0": CPU is set to select sub-oscillator when reset occurs.

HLFS = "1": CPU is set to select main-oscillator when reset occurs.

Bit 7 (ENWDTB): Watchdog timer enable/disable bit.

ENWDTB = "0": Enable watchdog timer

ENWDTB = "1": Disable watchdog timer

Bit 6 (FSMD): Sub-oscillator type selection

Bits 5, 4 (FMMD1, 0): Main Oscillator Type Selection

FSMD	FMMD1	FMMD0	Main Oscillator Type	Sub Oscillator Type
0	0	0	RC type	RC type
0	0	1	Crystal type	RC type
0	1	×	PLL type	RC type
1	0	0	RC type	Crystal type
1	0	1	Crystal type	Crystal type
1	1	×	PLL type	Crystal type

Bit 3 (HLP): Power consumption selection. If the system usually runs in green mode, it must be set to low power consumption to help support the energy saving issue. It is recommended that low power consumption mode is selected.

HLP = "0": Low power consumption mode

HLP = "1": High power consumption mode

Bits 2~0 (PR2~PR0): Protect Bits

PR2~PR0 are protection bits. Each protect status is as follows:

PR2	PR1	PR0	Protect
0	0	0	Enable
1	1	1	Disable

6.13 Instruction Set

Each instruction in the instruction set is a 13-bit word divided into an OP code and one or more operands. Normally, all instructions are executed within one single instruction cycle (one instruction consists of 2 oscillator periods), unless the program counter is changed by instruction "MOV R2,A", "ADD R2,A", or by instructions of arithmetic or logic operation on R2 (e.g. "SUB R2,A", "BS(C) R2,6", "CLR R2", ····). In this case, the execution takes two instruction cycles.

If for some reasons, the specification of the instruction cycle is not suitable for certain applications, try modifying the instruction as follows**:**

Execute within two instruction cycles the "JMP", "CALL", "RET", "RETL", and "RETI" instructions, or the conditional skip instructions ("JBS", "JBC", "JZ", "JZA", "DJZ", "DJZA") which were tested to be true. Also execute within two instruction cycles the instructions that are written to the program counter.

Additionally, the instruction set offers the following features**:**

(1) Every bit of any register can be set, cleared, or tested directly.

(2) The I/O register can be regarded as general register. That is, the same instruction can operate on I/O register.

Convention:

R *= Register designator that specifies which one of the registers (including operation and general purpose registers) is to be utilized by the instruction.*

b *= Bit field designator that selects the value for the bit located in the register R and which affects the operation.*

k *= 8 or 10-bit constant or literal value*

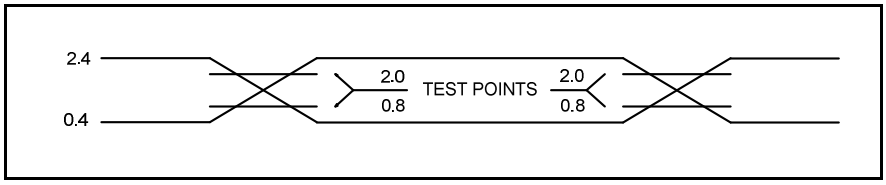
Mnemonic			Operation	Status Affected
NOP			No Operation	None
DAA			Decimal Adjust A	C
SLEP			0 → WDT, Stop oscillator	T, P
WDTC			0 → WDT	T, P
IOW	R		A → IOCR	None[1]
ENI			Enable Interrupt	None
DISI			Disable Interrupt	None
RET			[Top of Stack] → PC	None
RETI			[Top of Stack] → PC, Enable Interrupt	None
IOR	R		IOCR → A	None[1]
MOV	R,	A	A → R	None
CLRA			0 → A	Z
CLR	R		0 → R	Z
SUB	A,	R	R-A → A	Z,C,DC
SUB	R,	A	R-A → R	Z,C,DC
DECA	R		R-1 → A	Z
DEC	R		R-1 → R	Z
OR	A,	R	A ∨ R → A	Z
OR	R,	A	A ∨ R → R	Z
AND	A,	R	A & R → A	Z
AND	R,	A	A & R → R	Z
XOR	A,	R	A ⊕ R → A	Z
XOR	R,	A	A ⊕ R → R	Z
ADD	A,	R	A + R → A	Z, C, DC
ADD	R,	A	A + R → R	Z, C, DC
MOV	A,	R	R → A	Z
MOV	R,	R	R → R	Z
COMA	R		/R → A	Z
COM	R		/R → R	Z
INCA	R		R+1 → A	Z
INC	R		R+1 → R	Z
DJZA	R		R-1 → A, skip if zero	None
DJZ	R		R-1 → R, skip if zero	None

Mnemonic			Operation	Status Affected
RRCA	R		R(n) → A(n-1), R(0) → C, C → A(7)	C
RRC	R		R(n) → R(n-1), R(0) → C, C → R(7)	C
RLCA	R		R(n) → A(n+1), R(7) → C, C → A(0)	C
RLC	R		R(n) → R(n+1), R(7) → (C), C → (R(0)	C
SWAPA	R		R(0-3) → (A(4-7), R(4-7) → (A(0-3)	None
SWAP	R		R(0-3) → (R(4-7)	None
JZA	R		R+1 → A, skip if zero	None
JZ	R		R+1 → R, skip if zero	None
BC	R,	b	0→ (R(b)	None
BS	R,	b	1→ (R(b)	None
JBC	R,	b	if R(b)=0, skip	None
JBS	R,	b	if R(b)=1, skip	None
CALL	k		PC+1 → [SP], (Page, k) → (PC)	None
JMP	k		(Page, k) → (PC)	None
MOV	A,	k	k → A	None
OR	A,	k	A v k → A	Z
AND	A,	k	A & k → A	Z
XOR	A,	k	A ⊕ k → A	Z
RETL	k		k → A, [Top of Stack] → PC	None
SUB	A,	k	k-A → A	Z, C, DC
ADD	A,	k	k+A → A	Z, C, DC
PAGE	k		K→R3(5:7)	None
BANK	k		K→R4(7:6)	None

Note: *[1]This instruction is applicable to IOC50~IOF0, IOC61~IOCE1.*

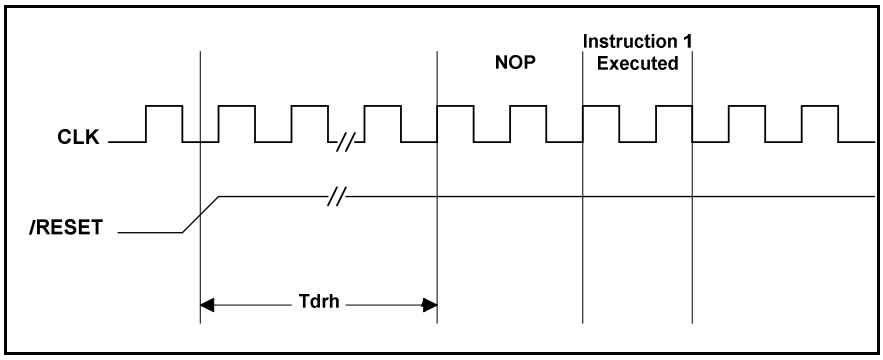
6.14 Timing Diagram

AC Test Input/Output Waveform

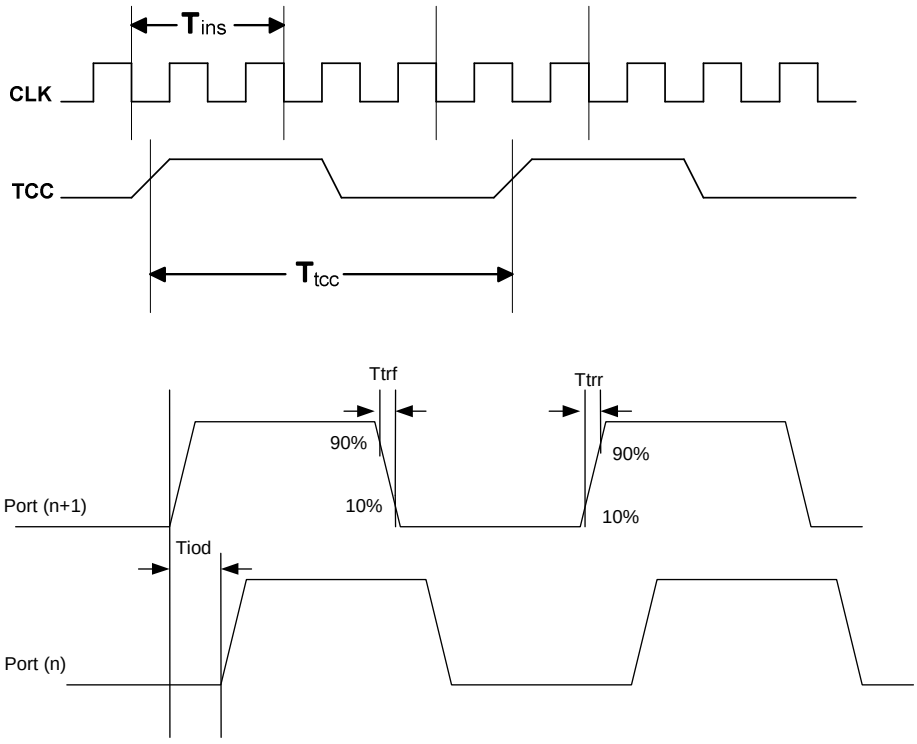


Note: *AC Testing: Input are driven at 2.4V for logic "**1**," and 0.4V for logic "**0**"*
*Timing measurements are made at 2.0V for logic "**1**," and 0.8V for logic "**0**"*

Reset Timing (CLK="0")



TCC Input Timing (CLKS="0")



*n = 0 , 2 , 4 , 6

Figure 6-27 Timing Diagrams of EM78P516N

7 Absolute Maximum Ratings

Items	Symbol	Condition	Rating		Unit
			Min.	Max.	
Supply voltage	VDD	–	GND-0.3	+7.0	V
Input voltage	V_I	Port 5 ~ Port 8	GND-0.3	VDD+0.3	V
Output voltage	V_O	Port 5 ~ Port 8	GND-0.3	VDD+0.3	V
Operation temperature	T_{OPR}	–	-40	85	℃
Storage temperature	T_{STG}	–	-65	150	℃
Power consumption	P_D	–	–	500	mW
Operating Frequency	–	–	32.768K	10M	Hz

8 Electrical Characteristics

8.1 DC Electrical Characteristics

Ta= -40°C ~85°C, VDD=5.0V, GND=0V

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
FXT	Crystal: VDD to 5V	Two cycles with two clocks	32.768	8M	10M	kHz
Fs	Sub-oscillator	Two cycles with two clocks	–	32.768	–	kHz
ERIC	External R, Internal C for Sub-oscillator	R: 300KΩ, internal capacitance	270	384	500	kHz
	External R, Internal C for Sub-oscillator	R: 2.2MΩ, internal capacitance	22.9	32.768	42.6	kHz
IIL	Input Leakage Current for Input pins	VIN = VDD, GND	-1	0	1	μA
VIH1	Input High Threshold Voltage (Schmitt Trigger)	Ports 5, 6, 7, 8	2.0	–	–	V
VIL1	Input High Threshold Voltage (Schmitt Trigger)	Ports 5, 6, 7, 8	–	–	0.8	V
VIHT1	Input High Threshold Voltage (Schmitt Trigger)	/RESET	2.0	–	–	V
VILT1	Input Low Threshold Voltage (Schmitt Trigger)	/RESET	–	–	0.8	V
VIHT2	Input High Threshold Voltage (Schmitt Trigger)	TCC, INT0, INT1	2.0	–	–	V
VILT2	Input Low Threshold Voltage (Schmitt Trigger)	TCC, INT0, INT1	–	–	0.8	V
IOH1	Drive Current (Ports 5 ~ 8)	VOH = 2.4V (IROCS="0")	–	-10	–	mA
IOL1	Sink Current (Ports 5 and 6)	VOL = 0.4V (IROCS="0")	–	10	–	mA
IOH2	IR Drive Current (P57/IROUT pin)	VOH = 2.4V (IROCS="1")	–	20	–	mA
IOL2	IR Sink Current (P57/IROUT pin)	VOL = 0.4V (IROCS="1")	–	20	–	mA

Ta= -40°C ~85°C, VDD=5.0V, GND=0V

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
IOH3	High Drive Current (Ports 5 ~ 8)	VOH = 2.4V (IROCS="0")	–	-20	–	mA
IOL3	High Sink Current (Ports 5 and 6)	VOL = 0.4V (IROCS="0")	–	20	–	mA
IPH	Pull-high current	Pull-high active, input pin at GND	-55	-75	-95	µA
IPL	Pull-low current	Pull-low active, input pin at VDD	55	75	95	µA
ISB	Sleep mode current	All input and I/O pins at VDD, Output pin floating, WDT disabled	–	0.5	1.5	µA
ICC1	Idle mode current	/RESET= 'High', CPU OFF, Sub-oscillator clock (32.768kHz) ON, output pin floating, LCD enabled, no load	–	14	18	µA
ICC2	Green mode current	/RESET= 'High', CPU ON, Sub-oscillator clock (32.768kHz), Output pin floating, WDT enabled, LCD enabled	–	22	30	µA
ICC3	Normal mode	/RESET= 'High', Fosc = 4 MHz (Crystal type, CLKS="0"), Output pin floating	–	2.2	3	mA
ICC4	Normal mode	/RESET= 'High', Fosc = 10 MHz (Crystal type, CLKS="0"), Output pin floating	–	3.1	4	mA

9 AD Converter Characteristics

Vdd=2.5V to 5.5V, Vss=0V, Ta=-40 to 85℃

Symbol		Parameter	Condition	Min.	Typ.	Max.	Unit
V_{AREF}		Analog reference voltage	V_{AREF} - V_{ASS} ≥ 2.5V	2.5	–	Vdd	V
V_{ASS}				Vss	–	Vss	V
VAI		Analog input voltage	–	V_{ASS}	–	V_{AREF}	V
IAI1	Ivdd	Analog supply current	VDD=V_{AREF}=5.0V, V_{ASS} = 0.0V (V reference from Vdd)	–	–	1400	µA
	Ivref			–	–	10	µA
IAI2	Ivdd	Analog supply current	VDD=V_{AREF}=5.0V, V_{ASS} = 0.0V (V reference from VREF)	–	–	900	µA
	IVref			–	–	500	µA
RN1		Resolution	ADREF=0, Internal VDD VDD=5.0V, VSS = 0.0V	–	9	10	Bits

RN2	Resolution	ADREF=1, External VREF VDD=VREF=5.0V, VSS = 0.0V	–	11	12	Bits
LN1	Linearity error	VDD = 2.5 to 5.5V Ta=25℃	–	–	±4	LSB
DNL	Differential nonlinear error	VDD = 2.5 to 5.5V Ta=25℃	–	–	±1	LSB
FSE1	Full scale error	VDD=V_{AREF}=5.0V, V_{ASS} = 0.0V	–	–	±8	LSB
OE	Offset error	VDD=V_{AREF}=5.0V, V_{ASS} = 0.0V	–	–	±4	LSB
ZAI	Recommended impedance of analog voltage source	–	–	–	10	KΩ
TAD	ADC clock duration	VDD=V_{AREF}=5.0V, V_{ASS} = 0.0V	1	–	–	μs
TCN	AD conversion time	VDD=V_{AREF}=5.0V, V_{ASS} = 0.0V	16	–	–	TAD
PSR	Power Supply Rejection	VDD=5.0V±0.5V	–	–	2	LSB
$V_{1/2VDD}$	Accuracy for 1/2 VDD	–	–	±3	–	%

Note:

1. These parameters are hypothetical (not tested) and provided for design reference use only.

2. When ADC is off, there is no current consumption other than minor leakage current.

3. AD conversion result will not decrease when an increase of input voltage and no missing code will result.

4. These parameters are subject to change without further notice.

8.2 AC Electrical Characteristics

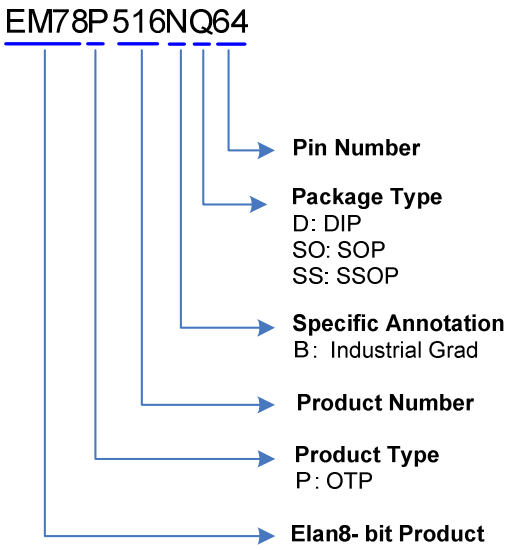
Ta=- 40°C ~ 85°C, VDD=5V±5%, GND=0V

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Dclk	Input CLK duty cycle	–	45	50	55	%
Tins	Instruction cycle time (CLKS="0")	Crystal type	100	–	DC	ns
		RC type	500	–	DC	ns
Ttcc	TCC input period	–	(Tins+20)/N*	–	–	ns
Tdrh	Device reset hold time	Ta = 25°C	11.3	16.2	21.6	ms
Trst	/RESET pulse width	Ta = 25°C	2000	–	–	ns
Twdt	Watchdog timer period	Ta = 25°C	11.3	16.2	21.6	ms
Tset	Input pin setup time	–	–	0	–	ns
Thold	Input pin hold time	–	–	20	–	ns
Tdelay	Output pin delay time	Cload=20pF	–	50	–	ns

**N= selected prescaler ratio*

APPENDIX

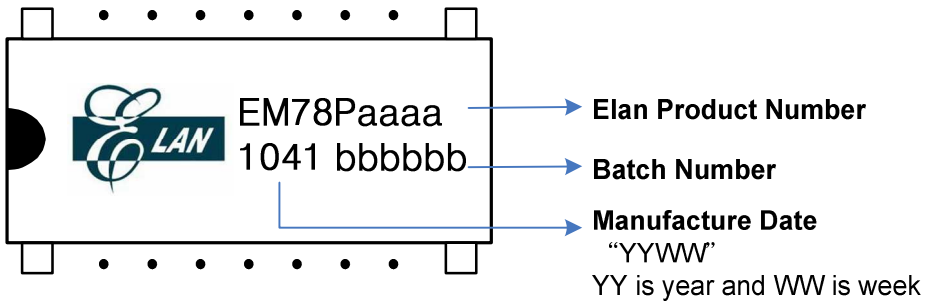
A Ordering and Manufacturing Information



For example

EM78P516NQ64

is EM78P516Nwith OTP program memory,industrial grade product, in64-pin QFP package



B Package Type

Name	Package Type	Pin Count	Package Size
EM78P516NH	Dice	59	–
EM78P516NQ64	QFP	64	14 mm × 20 mm
EM78P516NL64	LQFP	64	7 mm × 7 mm
EM78P516NL44	LQFP	44	10 mm × 10 mm
EM78P516NQ44	QFP	44	10 mm × 10 mm
EM78P516NQ64B	QFP	64	14 mm × 14 mm
EM78P516NL48	LQFP	48	7 mm × 7 mm

Note: *These are Green products that do not contain hazardous substances.*

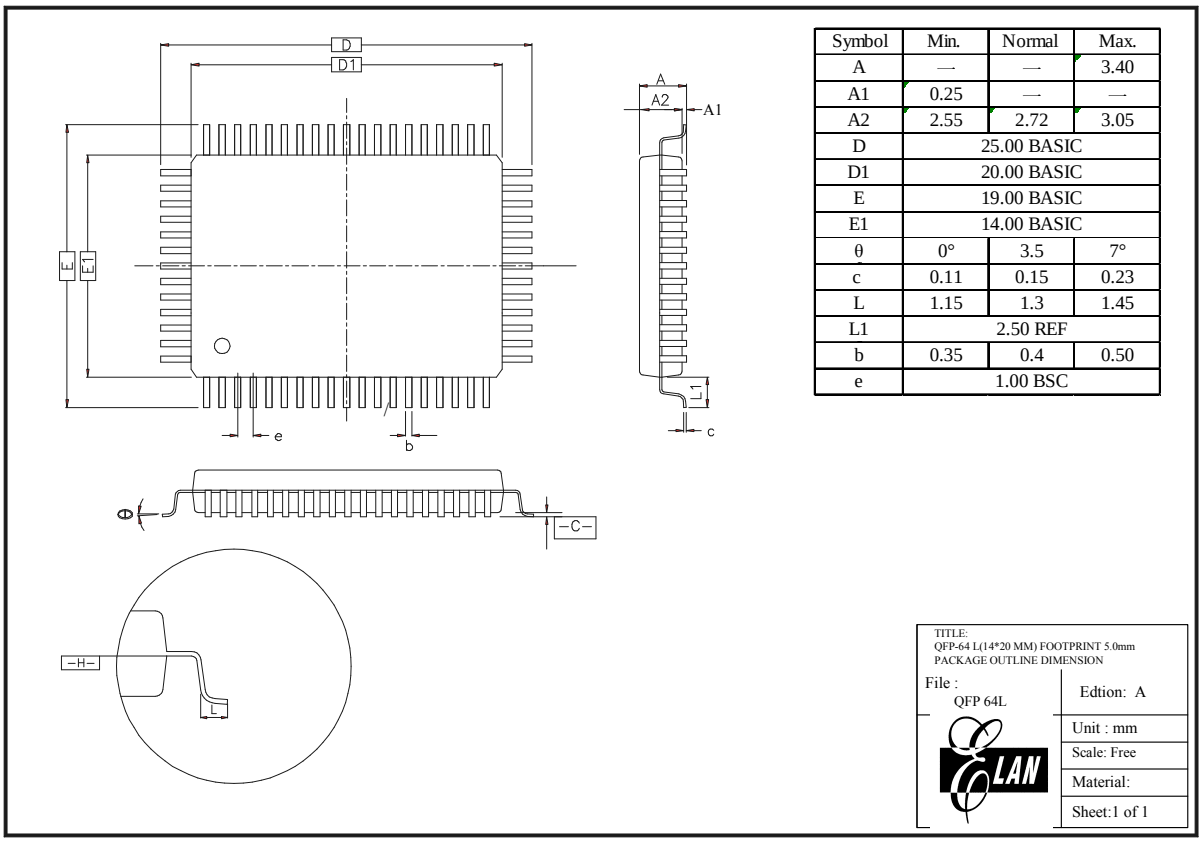
These are compatible with the third edition of Sony SS-00259 standard.

The Pb content should be less than 100ppm, and should meet Sony specifications or requirements.

Part No.	EM78P516NxS/xJ
Electroplate type	Pure Tin
Ingredient (%)	Sn:100%
Melting point (°C)	232°C
Electrical resistivity (μΩ-cm)	11.4
Hardness (hv)	8~10
Elongation (%)	>50%

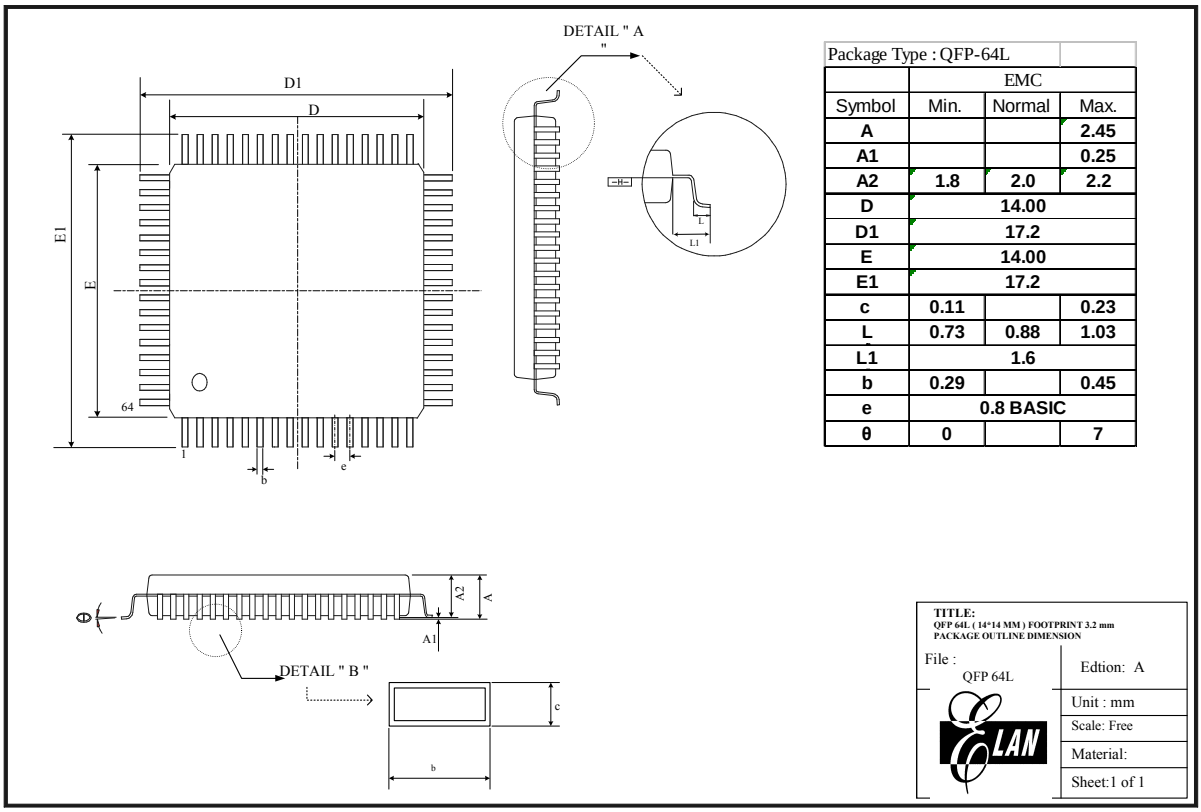
C Package Information

QFP – 64



Symbol	Min.	Normal	Max.
A	—	—	3.40
A1	0.25	—	—
A2	2.55	2.72	3.05
D	25.00 BASIC		
D1	20.00 BASIC		
E	19.00 BASIC		
E1	14.00 BASIC		
θ	0°	3.5	7°
c	0.11	0.15	0.23
L	1.15	1.3	1.45
L1	2.50 REF		
b	0.35	0.4	0.50
e	1.00 BSC		

QFP – 64



Package Type : QFP-64L

	EMC		
Symbol	Min.	Normal	Max.
A			2.45
A1			0.25
A2	1.8	2.0	2.2
D		14.00	
D1		17.2	
E		14.00	
E1		17.2	
c	0.11		0.23
L	0.73	0.88	1.03
L1		1.6	
b	0.29		0.45
e		0.8 BASIC	
θ	0		7

TITLE:
QFP 64L (14*14 MM) FOOTPRINT 3.2 mm
PACKAGE OUTLINE DIMENSION

File : QFP 64L

Edtion: A

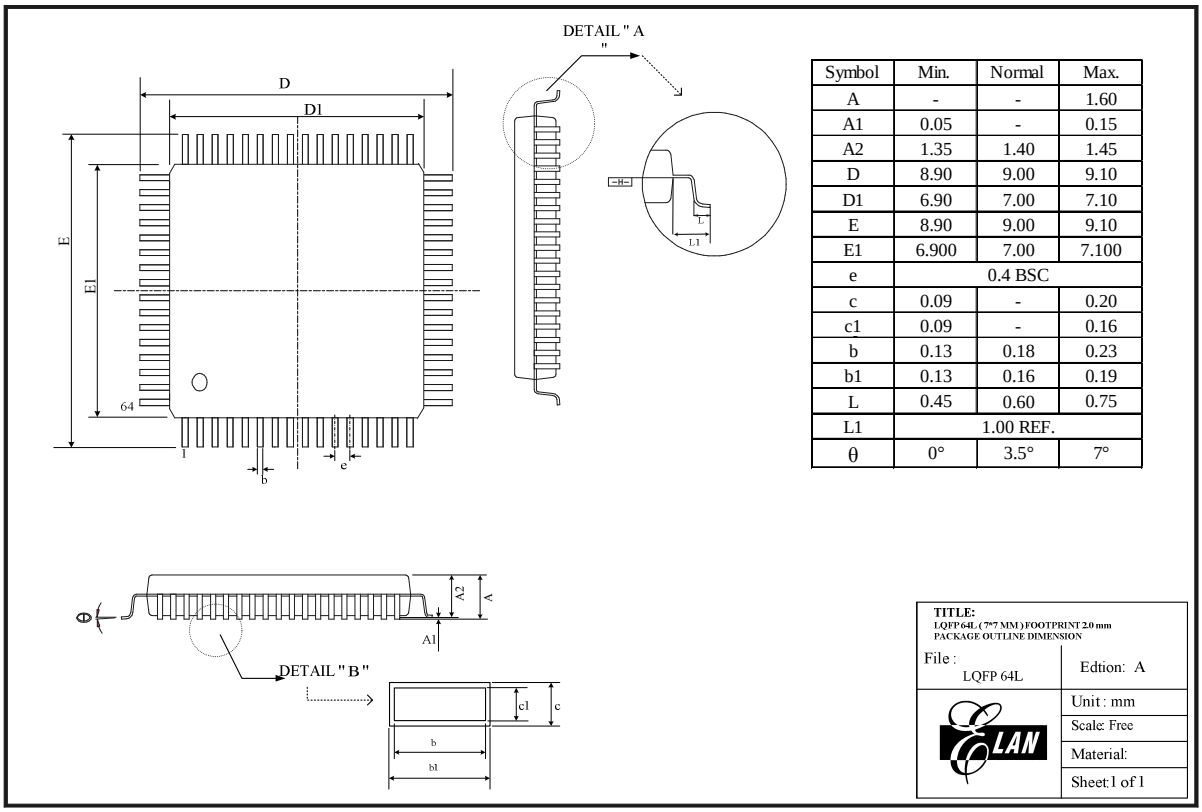
Unit : mm

Scale: Free

Material:

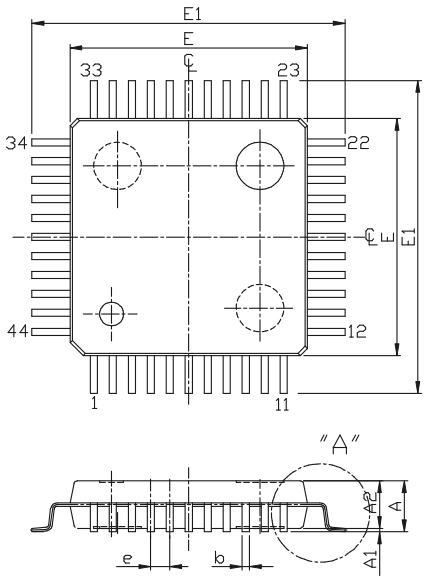
Sheet:1 of 1

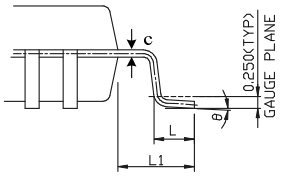
LQFP – 64



Symbol	Min.	Normal	Max.
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
D	8.90	9.00	9.10
D1	6.90	7.00	7.10
E	8.90	9.00	9.10
E1	6.900	7.00	7.100
e	0.4 BSC		
c	0.09	-	0.20
c1	0.09	-	0.16
b	0.13	0.18	0.23
b1	0.13	0.16	0.19
L	0.45	0.60	0.75
L1	1.00 REF.		
θ	0°	3.5°	7°

LQFP – 44

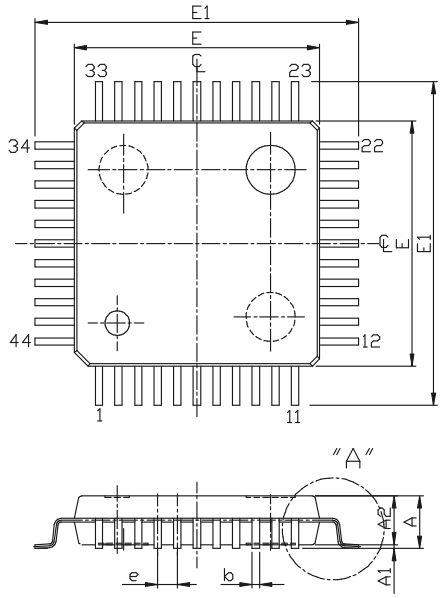


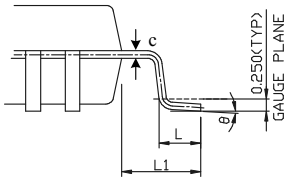


Symbol	Min.	Normal	Max.
A			1.600
A1	0.050		0.150
A2	1.350	1.400	1.450
b	0.300	0.370	0.450
c	0.090		0.200
E1	12.00 BASIC		
E	10.00 BASIC		
L	0.450	0.600	0.750
L1	1.0 (BASIC)		
e	0.8 (BASIC)		
θ°	0	3.5	7

TITLE: LQFP-44L (10*10 MM) FOOTPRINT 2.0mm PACKAGE OUTLINE DIMENSION	
File : LQFP44	Edtion: A
	Unit : mm
	Scale: Free
	Material:
	Sheet:1 of 1

QFP – 44

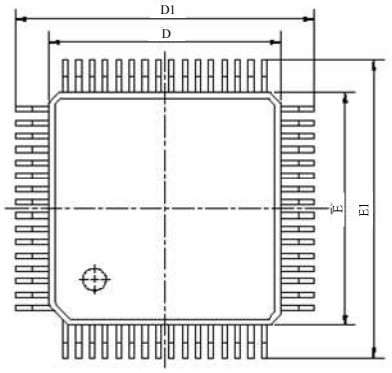


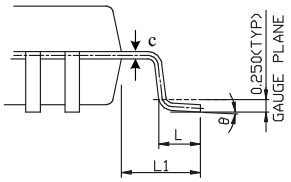


Symbol	Min.	Normal	Max.
A			2.70
A1	0.15		0.50
A2	1.80	2.00	2.20
b		0.30(TYP)	
c		0.15(TYP)	
E1	13.00	13.20	13.40
E	9.90	10.00	10.10
L	0.73	0.88	1.03
L1	1.50	1.60	1.70
e		0.80(TYP)	
θ°	0		7

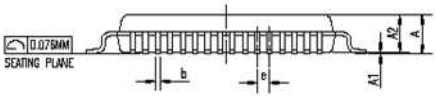
TITLE: QFP-44L(10*10 MM) FOOTPRINT 3.2mm PACKAGE OUTLINE DIMENSION	
File : QFP44	Edtion: A
	Unit : mm
	Scale: Free
	Material:
	Sheet:1 of 1

LQFP – 48





Symbal	Min	Normal	Max
A			1.60
A1	0.05		0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
b1	0.17	0.20	0.23
c	0.09		0.20
c1	0.09		0.160
D	9.00BCS		
D1	7.00BSC		
E	9.00BSC		
E1	7.00BSC		
e	0.50BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
θ	0°	3.5°	7°



TITLE:
LQFP-48L(7*7 MM) FOOTPRINT 2.0mm
PACKAGE OUTLINE DIMENSION

File : LQFP48	Edtion: A
	Unit : mm
	Scale: Free
	Material:
	Sheet:1 of 1

D EM78P516N Program Pin List

Program Pin Name	IC Pin Name	L/QFP-64 Pin Number	LQFP-48 Pin Number	L/QFP-44 Pin Number
VPP	/RESET	25	15	14
ACLK	P54/INT0	32	22	21
DINCLK	P55/INT1	33	23	22
DATAIN	P56/TCC	34	24	23
/PGMB	P60	38	26	25
/OEB	P61	39	27	26
VDD	VDD	29	19	18
GND	GND	26	16	15

E Quality Assurance and Reliability

Test Category	Test Conditions	Remarks
Solderability	Solder temperature=245±5℃, for 5 seconds up to the stopper using a rosin-type flux	–
Pre-condition	Step 1: TCT, 65℃ (15 min)~150℃ (15mins), 10 cycles	For SMD IC (such as SOP, QFP, SOJ, etc)
	Step 2: Bake at 125℃, TD (endurance)=24 hrs	
	Step 3: Soak at 30℃/60% ，TD (endurance)=192 hrs	
	Step 4: IR flow 3 cycles (Pkg thickness ≥ 2.5 mm or Pkg volume ≥ 350 mm^3 ----225 ± 5℃) (Pkg thickness ≤ 2.5 mm or Pkg volume ≤ 350 mm^3 ----240 ± 5℃)	
Temperature cycle test	-65℃ (15mins)~150℃ (15 min), 200 cycles	–
Pressure cooker test	TA =121℃, RH=100%, pressure=2 atm, TD (endurance)= 96 hrs	–
High temperature / High humidity test	TA=85℃, RH=85% ，TD (endurance) = 168, 500 hrs	–
High-temperature storage life	TA=150℃, TD (endurance) = 500, 1000 hrs	–
High-temperature operating life	TA=125℃, VCC = Max. operating voltage, TD (endurance) = 168, 500, 1000 hrs	–
Latch-up	TA=25℃, VCC = Max. operating voltage, 150mA/ 20V	–
ESD (HBM)	TA=25℃, ≥｜± 3KV｜	IP_ND,OP_ND,IO_ND IP_NS,OP_NS,IO_NS IP_PD,OP_PD,IO_PD, IP_PS,OP_PS,IO_PS, VDD-VSS(+),VDD_VSS (-) mode
ESD (MM)	TA=25℃, ≥ ｜± 300V｜	

E.1 Address Trap Detect

An address trap detect is one of the MCU embedded fail-safe functions that detects MCU malfunction caused by noise or the like. Whenever the MCU attempts to fetch an instruction from a certain section of ROM, an internal recovery circuit is auto started. If a noise-caused address error is detected, the MCU will repeat execution of the program until the noise is eliminated. The MCU will then continue to execute the next program.