EM78P528N

8-Bit Microprocessor with OTP ROM

Product Specification

DOC. VERSION 1.4

ELAN MICROELECTRONICS CORP.

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ELAN MICROELECTRONICS CORPORATION

Headquarters:
No. 12, Innovation 1st Road
Hsinchu Science Park
Hsinchu, TAIWAN 30076
Tel: +886 3 563-9977
Fax: +886 3 563-9966
webmaster@emc.com.tw
http://www.emc.com.tw

Hong Kong:
Elan (HK) Microelectronics Corporation, Ltd.
Flat A, 19F., World Tech Centre
95 How Ming Street, Kwun Tong
Kowloon, HONG KONG
Tel: +852 2723-3376
Fax: +852 2723-7780

USA:
Elan Information Technology Group (U.S.A.)
PO Box 601
Cupertino, CA 95015
U.S.A.
Tel: +1 408 366-8225
Fax: +1 408 366-8225

Shenzhen:
Elan Microelectronics Shenzhen, Ltd.
8A Floor, Microprofit Building
Gaoxin South Road 6
Shenzhen Hi-tech Industrial Park
South Area, Shenzhen
CHINA 518057
Tel: +86 755 2601-0565
Fax: +86 755 2601-0500
elan-sz@elanic.com.cn

Shanghai:
ELAN Microelectronics Shanghai, Ltd.
6F, Ke Yuan Building
No. 5 Bibo Road
Zhangjiang Hi-Tech Park
Shanghai, CHINA 201203
Tel: +86 21 5080-3866
Fax: +86 21 5080-0273
elan-sh@elanic.com.cn

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APPENDIX

Specification Revision History

Doc. Version	Revision Description	Date
1.0	Initial released version	2011/03/18
1.1	1. Modified the CPU change operating mode description. 2. Modified the ADC description. 3. Modified Figure 6-3. *CPU Operation Mode*. 4. Modified the LVD power consumption.	2012/02/08
1.2	Added LVR specifications	2013/03/29
1.3	1. Modified the Code Option default for Word 1_Bit 4 and Word 2_Bit 3 2. Added the remarks on P50	2016/01/15
1.4	1. Added User Application Note 2. Modified the package type in the Features section 3. Modified Appendix A “Ordering and Manufacturing Information”	2016/03/31

User Application Note

(Before using this chip, take a look at the following description note, it includes important messages.)

1. We strongly recommend that you have to place an external pull-down or pull-high resistor on P50 no matter what the pin function is. The purpose of this is to prevent P50 from floating.

2. The value in the dead-time register must be less than the value in the duty cycle register in order to prevent unexpected behavior on both of the PWM outputs.

3. The PWM output will not be set, if the duty cycle is “0”.

4. The internal TCC will stop running when in sleep mode. However, during AD conversion, when TCC is set to “SLEP” instruction, if the ADWE bit of the RE register is enabled, TCC will keep on running.

5. During ADC conversion, do not perform output instruction to maintain precision for all of the pins. In order to obtain accurate values, it is necessary to avoid any data transition on I/O pins during AD conversion

6. The noise rejection function is turned off in the LXT2 and sleep mode

1 General Description

The EM78P528N is an 8-bit microprocessor designed and developed with low-power, high-speed CMOS technology. It is used for 15 bits kernel simulation and it simulates the 8K×15-bit programmable ROM. Using the UIT400N, user can develop their program for ELAN's several OTP types of IC.

2 Features

- CPU configuration
  - Supports 8K×15 bits program ROM
  - (48+512) bytes general purpose register
  - 32 bytes LCD RAM
  - 8-level stacks for subroutine nesting
  - Less than 1mA at 5V/4MHz
  - Typically 15 μA at 3V/16kHz
  - Typically 22 μA, at 3V/32kHz
  - Typically 2 μA during sleep mode
  - Four CPU operation modes: Normal, Sleep, Green, Idle
- I/O port configuration
  - Six bidirectional I/O ports: P5~P9, PA
  - Four programmable pin change wake-up ports : P5~P8
  - Six programmable pull-down I/O ports: P5~P9, PA
  - Six programmable pull-high I/O ports: P5~P9, PA
  - Six programmable open-drain I/O ports: P5~P9, PA
  - Six programmable high-sink/drive I/O ports: P5~P9, PA
  - 10 external interrupt pins
- Operating voltage range:
  - 2.1V~5.5V at 0°C~70°C (commercial)
  - 2.3V~5.5V at -40°C~85°C (industrial)
- Operating frequency range (base on 2 clocks):

  Main oscillator:
  - Crystal mode:
    DC~16 MHz at 5V; DC~8 MHz at 3V; DC~4 MHz at 2.1V
  - IRC mode:
    DC~16 MHz at 5V; DC~8 MHz at 3V; DC~4 MHz at 2.1V

Internal RC Frequency	Drift Rate			
	Temperature (-40°C ~+85°C)	Voltage (2.5V~5.5V)	Process	Total
1 MHz	±2%	±1%	±1%	±4%
4 MHz	±2%	±1%	±1%	±4%
8 MHz	±2%	±1%	±1%	±4%
16 MHz	±2%	±1%	±1%	±4%

  Sub oscillator:
  - Crystal mode: 32.768kHz
  - IRC mode: 16k/32kHz
- Peripheral configuration
  - 8-bit Real Time Clock/Counter (TCC) with selective signal sources and trigger edges
  - 15+1 channels Analog-to-Digital Converter with 12-bit resolution + 1 internal reference for Vref
  - LCD: 8×23 dots, bias (1/2, 1/3), duty (static, 1/3, 1/4, 1/8)
  - Three 8-bit timers (TC1/TC2/TC3) with six modes: Timer/Counter/Capture/Window/Buzzer/PWM/ PDO (Programmable Divider Output) modes. Timers 1 and 2 can be cascaded to one 16-bit counter/timer
  - Universal Asynchronous Receiver/Transmitter (UART)
  - Serial transmitter/receiver interface (SPI): 3-wire synchronous communication
  - I^2C function with 7/10-bit address and 8-bit data transmit/receive mode
  - Four programmable watch timer: 1.0 sec, 0.5 sec, 0.25 sec, 3.91 ms
  - Four programmable Level Voltage Detector LVD: 4.5V, 4.0V, 3.3V, 2.2V
  - Power-on reset and three programmable level voltage reset POR: 1.8V (Default), LVR: 4.0, 3.5, 2.7V
  - High EFT immunity
- 25 available interrupts (12 external, 13 internal)
  - 10 external interrupts
  - Input-port status changed interrupt (wake up from sleep mode)
  - LVD interrupt
  - TCC overflow interrupt
  - Three timer interrupt
  - ADC completion interrupt
  - I^2C transfer/receive interrupt
  - UART TX, RX , RX error interrupt
  - SPI interrupt
  - Watch timer interrupt
- Single instruction cycle commands
- Package Type:
  - 44-pin QFP 10x10mm : EM78P528NQ44
  - 44-pin LQFP 10x10mm : EM78P528NL44
  - 48-pin LQFP 7x7mm : EM78P528NL48

Note: *These are Green Products which do not contain hazardous substances.*

3 Pin Configuration (Package)

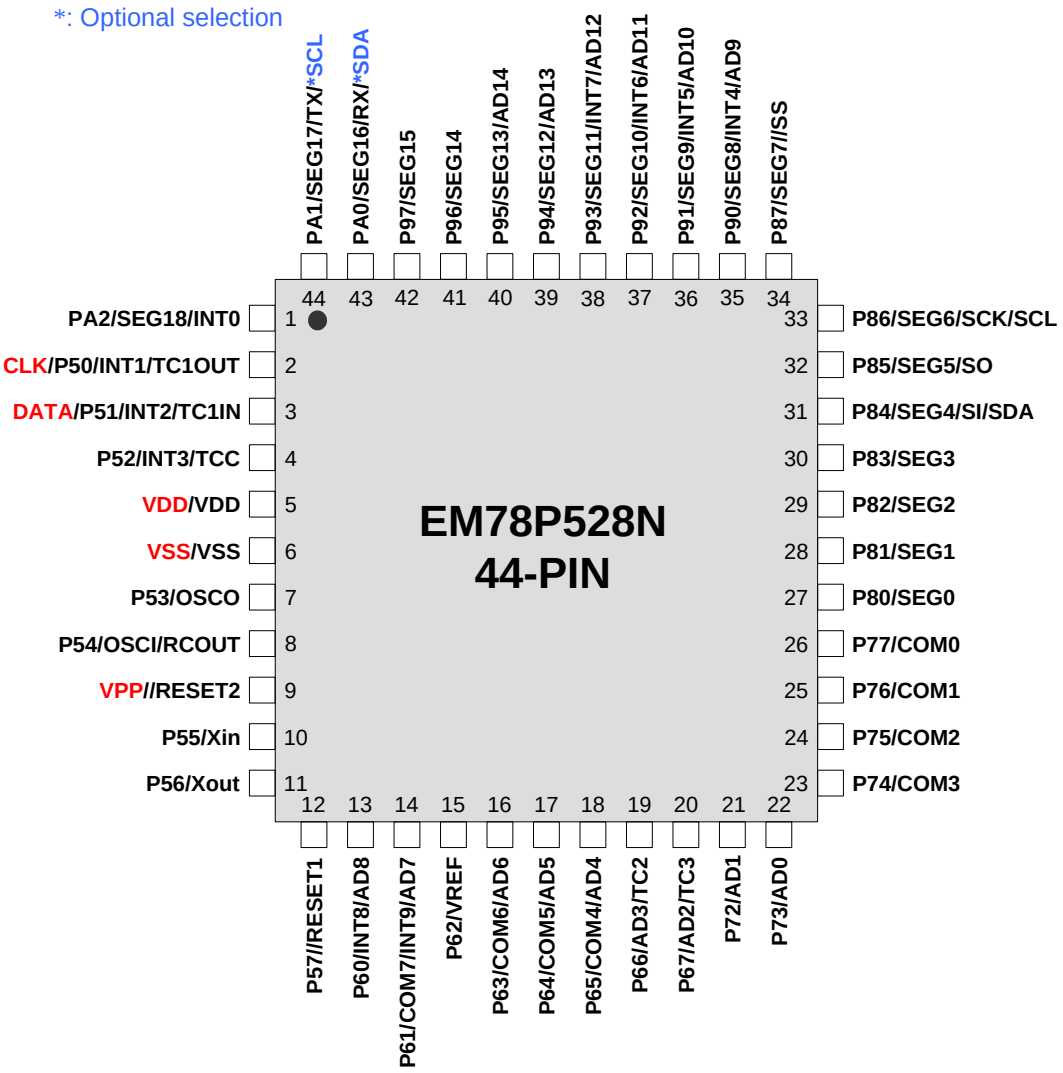


Figure 3-1 *44-pin QFP 10x10mm* EM78P528NQ44/L44

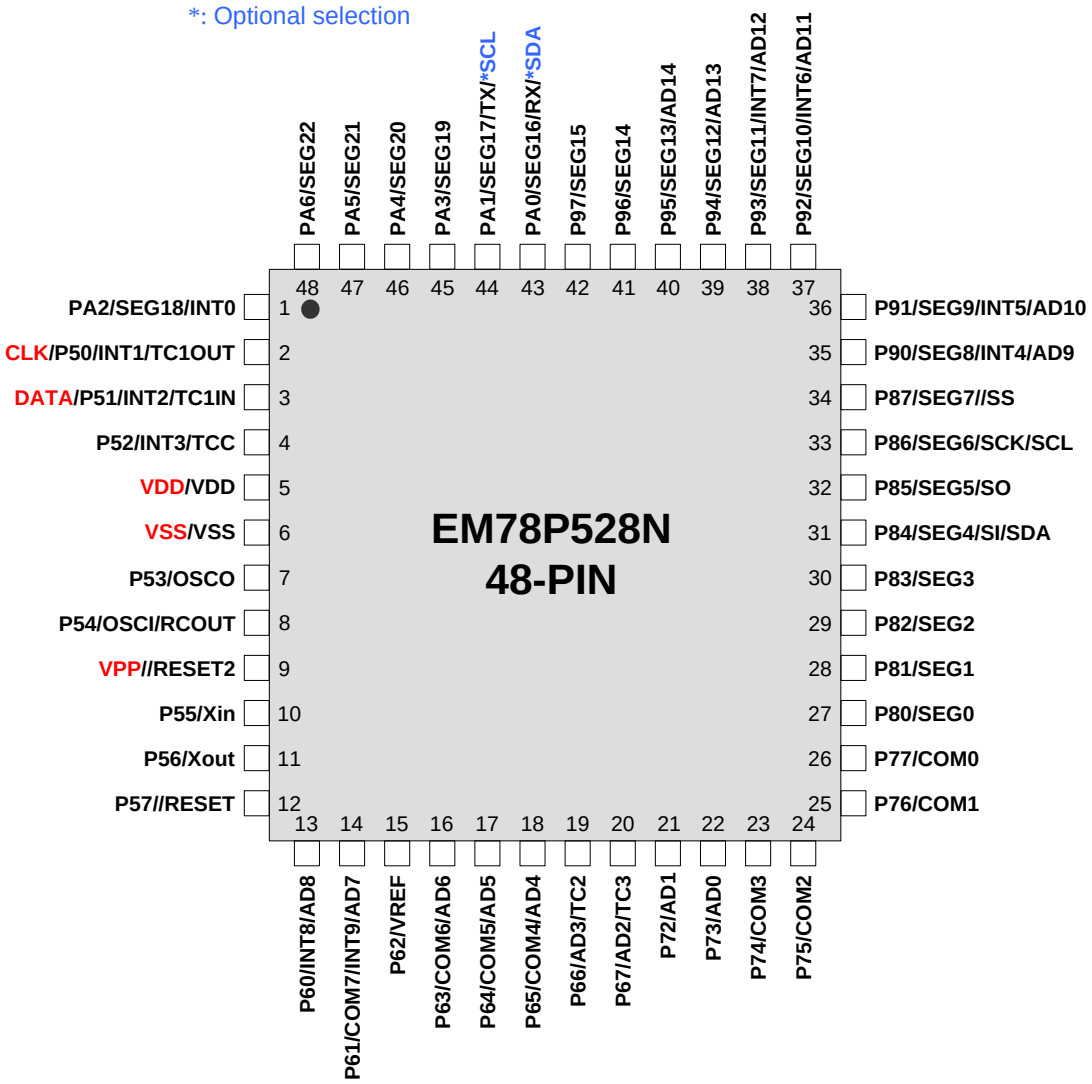


Figure 3-2 *48-pin LQFP 7x7mm* EM78P528NL48

4 Pin Description

Name	Function	Input Type	Output Type	Description
P50/INT1/ TC1OUT/ (CLK)	P50	ST	CMOS	Bidirectional I/O pin with programmable pull-low, pull-high, open-drain, high-sink/drive and pin change wake-up. **Remark: Off-chip pull-down or pull-high**
	INT1	ST	-	External interrupt pin **Remark: Off-chip pull-down or pull-high**
	T1OUT	-	CMOS	Timer 1 output (PDO/PWM/Buzzer) **Remark: Off-chip pull-down or pull-high**
	(CLK)	ST	-	Clock pin for Writer programming
P51/INT2/ TC1IN/ (DATA)	P51	ST	CMOS	Bidirectional I/O pin with programmable pull-low, pull-high, open-drain, high-sink/drive and pin change wake-up.
	INT2	ST	-	External interrupt pin
	T1IN	ST	-	Timer 1 input (Counter/Capture/Window)
	(DATA)	ST	CMOS	DATA pin for Writer programming
P52/INT3/ TCC	P52	ST	CMOS	Bidirectional I/O pin with programmable pull-low, pull-high, open-drain, high-sink/drive and pin change wake-up.
	INT3	ST	-	External Interrupt pin
	TCC	ST	-	Real Time Clock/Counter clock input
P53/OSCO	P53	ST	CMOS	Bidirectional I/O pin with programmable pull-low, pull-high, open-drain, high-sink/drive and pin change wake-up.
	OSCO	-	XTAL	Clock output of crystal/resonator oscillator
P54/OSCI/ RCOUT	P54	ST	CMOS	Bidirectional I/O pin with programmable pull-low, pull-high, open-drain, high-sink/drive and pin change wake-up.
	OSCI	XTAL	-	Clock input of crystal/resonator oscillator
	RCOUT	-	CMOS	Clock output of internal RC oscillator
P55/Xin	P55	ST	CMOS	Bidirectional I/O pin with programmable pull-low, pull-high, open-drain, high-sink/drive and pin change wake-up.
	Xin	XTAL	-	Clock input of crystal/resonator oscillator only for 32.768kHz
P56/Xout	P56	ST	CMOS	Bidirectional I/O pin with programmable pull-low, pull-high, open-drain, high-sink/drive and pin change wake-up.
	Xout	-	XTAL	Clock output of crystal/resonator oscillator only for 32.768kHz
P57/ /RESET1	P57	ST	CMOS	Bidirectional I/O pin with programmable pull-low, pull-high, open-drain, high-sink/drive and pin change wake-up.
	/RESET1	ST	-	Internal pull-high (set P57 pull-high) reset pin

(Continuation)

Name	Function	Input Type	Output Type	Description
P60/INT8/AD8	P60	ST	CMOS	Bidirectional I/O pin with programmable pull-low, pull-high, open-drain, high-sink/drive and pin change wake-up.
	INT8	ST	-	External interrupt pin
	AD8	AN	-	ADC Input 8
P61/COM7/INT9/ AD7	P61	ST	CMOS	Bidirectional I/O pin with programmable pull-low, pull-high, open-drain, high-sink/drive and pin change wake-up.
	COM7	-	AN	LCD Common 7 output
	INT9	ST	-	External interrupt pin
	AD7	AN	-	ADC Input 7
P62/VREF	P62	ST	CMOS	Bidirectional I/O pin with programmable pull-low, pull-high, open-drain, high-sink/drive and pin change wake-up.
	VREF	AN	-	Voltage reference for ADC
P63/COM6/AD6	P63	ST	CMOS	Bidirectional I/O pin with programmable pull-low, pull-high, open-drain, high-sink/drive and pin change wake-up.
	COM6	-	AN	LCD Common 6 output
	AD6	AN	-	ADC Input 6
P64/COM5/AD5	P64	ST	CMOS	Bidirectional I/O pin with programmable pull-low, pull-high, open-drain, high-sink/drive and pin change wake-up.
	COM5	-	AN	LCD Common 5 output
	AD5	AN	-	ADC Input 5
P65/COM4/AD4	P65	ST	CMOS	Bidirectional I/O pin with programmable pull-low, pull-high, open-drain, high-sink/drive and pin change wake-up.
	COM4	-	AN	LCD Common 4 output
	AD4	AN	-	ADC Input 4
P66/AD3/TC2	P66	ST	CMOS	Bidirectional I/O pin with programmable pull-low, pull-high, open-drain, high-sink/drive and pin change wake-up.
	AD3	AN	-	ADC Input 3
	TC2	ST	CMOS	Timer 2 input (Counter/Capture/Window) Timer 2 output (PDO/PWM/Buzzer)
P67/AD2/TC3	P67	ST	CMOS	Bidirectional I/O pin with programmable pull-low, pull-high, open-drain, high-sink/drive and pin change wake-up.
	AD2	AN	-	ADC Input 2
	TC3	ST	CMOS	Timer 3 input (Counter/Capture/Window) Timer 3 output (PDO/PWM/Buzzer)
P72/AD1	P72	ST	CMOS	Bidirectional I/O pin with programmable pull-low, pull-high, open-drain, high-sink/drive and pin change wake-up.
	AD1	AN	-	ADC Input 1
P73/AD0	P73	ST	CMOS	Bidirectional I/O pin with programmable pull-low, pull-high, open-drain, high-sink/drive and pin change wake-up.
	AD0	AN	-	ADC Input 0

(Continuation)

Name	Function	Input Type	Output Type	Description
P74/COM3	P74	ST	CMOS	Bidirectional I/O pin with programmable pull-low, pull-high, open-drain, high-sink/drive and pin change wake-up.
	COM3	-	AN	LCD Common 3 output
P75/COM2	P75	ST	CMOS	Bidirectional I/O pin with programmable pull-low, pull-high, open-drain, high-sink/drive and pin change wake-up.
	COM2	-	AN	LCD Common 2 output
P76/COM1	P76	ST	CMOS	Bidirectional I/O pin with programmable pull-low, pull-high, open-drain, high-sink/drive and pin change wake-up.
	COM1	-	AN	LCD Common 1 output
P77/COM0	P77	ST	CMOS	Bidirectional I/O pin with programmable pull-low, pull-high, open-drain, high-sink/drive and pin change wake-up.
	COM0	-	AN	LCD Common 0 output
P80/SEG0	P80	ST	CMOS	Bidirectional I/O pin with programmable pull-low, pull-high, open-drain, high-sink/drive and pin change wake-up.
	SEG0	-	AN	LCD Segment 0 output
P81/SEG1	P81	ST	CMOS	Bidirectional I/O pin with programmable pull-low, pull-high, open-drain, high-sink/drive and pin change wake-up.
	SEG1	-	AN	LCD Segment 1 output
P82/SEG2	P82	ST	CMOS	Bidirectional I/O pin with programmable pull-low, pull-high, open-drain, high-sink/drive and pin change wake-up.
	SEG2	-	AN	LCD Segment 2 output
P83/SEG3	P83	ST	CMOS	Bidirectional I/O pin with programmable pull-low, pull-high, open-drain, high-sink/drive and pin change wake-up.
	SEG3	-	AN	LCD Segment 3 output
P84/SEG4/SI/ SDA	P84	ST	CMOS	Bidirectional I/O pin with programmable pull-low, pull-high, open-drain, high-sink/drive and pin change wake-up.
	SEG4	-	AN	LCD Segment 4 output
	SI	ST	-	SPI serial data input
	SDA	ST	CMOS	I^2C serial data line. It is open-drain
P85/SEG5/SO	P85	ST	CMOS	Bidirectional I/O pin with programmable pull-low, pull-high, open-drain, high-sink/drive and pin change wake-up.
	SEG5	-	AN	LCD Segment 5 output
	SO	-	CMOS	SPI serial data output
P86/SEG6/SCK/ SCL	P86	ST	CMOS	Bidirectional I/O pin with programmable pull-low, pull-high, open-drain, high-sink/drive and pin change wake-up.
	SEG6	-	AN	LCD Segment 6 output
	SCK	ST	CMOS	SPI serial clock input/output
	SCL	ST	CMOS	I^2C serial clock line. It is open-drain.
P87/SEG7//SS	P87	ST	CMOS	Bidirectional I/O pin with programmable pull-low, pull-high, open-drain, high-sink/drive and pin change wake-up.
	SEG7	-	AN	LCD Segment 7 output
	/SS	ST	-	SPI Slave select pin

(Continuation)

Name	Function	Input Type	Output Type	Description
P90/SEG8/INT4/ AD9	P90	ST	CMOS	Bidirectional I/O pin with programmable pull-low, pull-high, open-drain and high-sink/drive.
	SEG8	-	AN	LCD Segment 8 output
	INT4	ST	-	External interrupt pin
	AD9	AN	-	ADC Input 9
P91/SEG9/INT5/ AD10	P91	ST	CMOS	Bidirectional I/O pin with programmable pull-low, pull-high, open-drain and high-sink/drive.
	SEG9	-	AN	LCD Segment 9 output
	INT5	ST	-	External interrupt pin
	AD10	AN	-	ADC Input 10
P92/SEG10/INT6/ AD11	P92	ST	CMOS	Bidirectional I/O pin with programmable pull-low, pull-high, open-drain and high-sink/drive.
	SEG10	-	AN	LCD Segment 10 output
	INT6	ST	-	External interrupt pin
	AD11	AN	-	ADC Input 11
P93/SEG11/INT7/ AD12	P93	ST	CMOS	Bidirectional I/O pin with programmable pull-low, pull-high, open-drain and high-sink/drive.
	SEG11	-	AN	LCD Segment 11 output
	INT7	ST	-	External interrupt pin
	AD12	AN	-	ADC Input 12
P94/SEG12/AD13	P94	ST	CMOS	Bidirectional I/O pin with programmable pull-low, pull-high, open-drain and high-sink/drive.
	SEG12	-	AN	LCD Segment 12 output
	AD13	AN	-	ADC Input 13
P95/SEG13/AD14	P95	ST	CMOS	Bidirectional I/O pin with programmable pull-low, pull-high, open-drain and high-sink/drive.
	SEG13	-	AN	LCD Segment 13 output
	AD14	AN	-	ADC Input 14
P96/SEG14	P96	ST	CMOS	Bidirectional I/O pin with programmable pull-low, pull-high, open-drain and high-sink/drive.
	SEG14	-	AN	LCD Segment 14 output
P97/SEG15	P97	ST	CMOS	Bidirectional I/O pin with programmable pull-low, pull-high, open-drain and high-sink/drive.
	SEG15	-	AN	LCD Segment 15 output
PA0/SEG16/RX/ SDA	PA0	ST	CMOS	Bidirectional I/O pin with programmable pull-low, pull-high, open-drain and high-sink/drive.
	SEG16	-	AN	LCD Segment 16 output
	RX	ST	-	UART RX input
	SDA	ST	CMOS	I^2C serial data line. It is open-drain.

(Continuation)

Name	Function	Input Type	Output Type	Description
PA1/SEG17/TX/ SCL	PA1	ST	CMOS	Bidirectional I/O pin with programmable pull-low, pull-high, open-drain and high-sink/drive.
	SEG17	-	AN	LCD Segment 17 output
	TX	-	CMOS	UART TX output
	SCL	ST	CMOS	I^2C serial clock line. It is open-drain.
PA2/SEG18/INT0	PA2	ST	CMOS	Bidirectional I/O pin with programmable pull-low, pull-high, open-drain and high-sink/drive.
	SEG18	-	AN	LCD Segment 18 output
	INT0	ST	-	External interrupt pin
PA3/SEG19	PA3	ST	CMOS	Bidirectional I/O pin with programmable pull-low, pull-high, open-drain and high-sink/drive.
	SEG19	-	AN	LCD Segment 19 output
PA4/SEG20	PA4	ST	CMOS	Bidirectional I/O pin with programmable pull-low, pull-high, open-drain and high-sink/drive.
	SEG20	-	AN	LCD Segment 20 output
PA5/SEG21	PA5	ST	CMOS	Bidirectional I/O pin with programmable pull-low, pull-high, open-drain and high-sink/drive.
	SEG21	-	AN	LCD Segment 21 output
PA6/SEG22	PA6	ST	CMOS	Bidirectional I/O pin with programmable pull-low, pull-high, open-drain and high-sink/drive.
	SEG22	-	AN	LCD Segment 22 output
VDD/(VDD)	VDD	Power	-	Power
	(VDD)	Power	-	VDD pin for Writer programming
VSS/(VSS)	VSS	Power	-	Ground
	(VSS)	Power	-	Ground pin for Writer programming
/RESET2/(VPP)	/RESET2	ST	-	Reset pin. It is open-drain
	(VPP)	Power	-	VPP pin for Writer programming

Legend: *ST : Schmitt Trigger input* *AN : Analog pin*
XTAL : Oscillation pin for crystal/resonator *CMOS : CMOS output*

NOTE

It is strongly recommended that user must place an external pull-down or pull-high resistor on P50 no matter what the pin function is.

The purpose of this is to prevent P50 from floating.

Pin control condition repeat function starting capability

Pin Function	I/O Status		Pin Control		
	I/O Direction	Pin Change WK/Int.	Pull High	Pull Low	O.D.
General Input	**Input**	**S/W**	**S/W**	**S/W**	**S/W**
General Output	**Output**	**Disable**	**S/W**	**S/W**	**S/W**
PWM	Output	Disable	S/W	S/W	S/W
TCC	Input	Disable	S/W	S/W	S/W
TC-IN	Input	Disable	S/W	S/W	S/W
TC-OUT	Output	Disable	S/W	S/W	S/W
RSTB (VPP pin)	Input	Disable	–	S/W	S/W
RSTB	Input	Disable	Init: Enable	S/W	S/W
EX_INT	Input	Disable	S/W	S/W	S/W
I^2C-SDA	Input/Output	Disable	S/W	S/W	Enable
I^2C-SCL	Input/Output	Disable	S/W	S/W	Enable
SPI-SDI	Input	Disable	S/W	S/W	S/W
SPI-SDO	Output	Disable	S/W	S/W	S/W
SPI-SCK-IN	Input	Disable	S/W	S/W	S/W
SPI-SCK-OUT	Output	Disable	S/W	S/W	S/W
UART-TX	Output	Disable	S/W	S/W	S/W
UART-RX	Input	Disable	S/W	S/W	S/W
LCD Driver	Input	Disable	Disable	Disable	S/W
AD	Input	Disable	Disable	Disable	S/W
OP/VO	Input	Disable	Disable	Disable	S/W
CMP/IN	Input	Disable	Disable	Disable	S/W
CMP/CO	Output	Disable	Disable	Disable	S/W
OSCI	Input	Disable	Disable	Disable	S/W
OSCO	Input	Disable	Disable	Disable	S/W
INMODE	Input	Disable	Disable	Disable	–
WRITER PIN	–	–	Enable	–	–
DUMPROM	Output: * Enable High drive/sink	–	–	–	–

Disable → forced to shutoff

Enable → forced to open

S/W → The initial value in the control register is set as “Disable”.

1. For non-I/O function, the Pin Change Wake-up/Interrupt function should be disabled
2. Priority: INMODE PIN > Analog function > I^2C, SPI, UART > Output Digital Function > Input Digital Function > General I/O Function

5 Functional Block Diagram

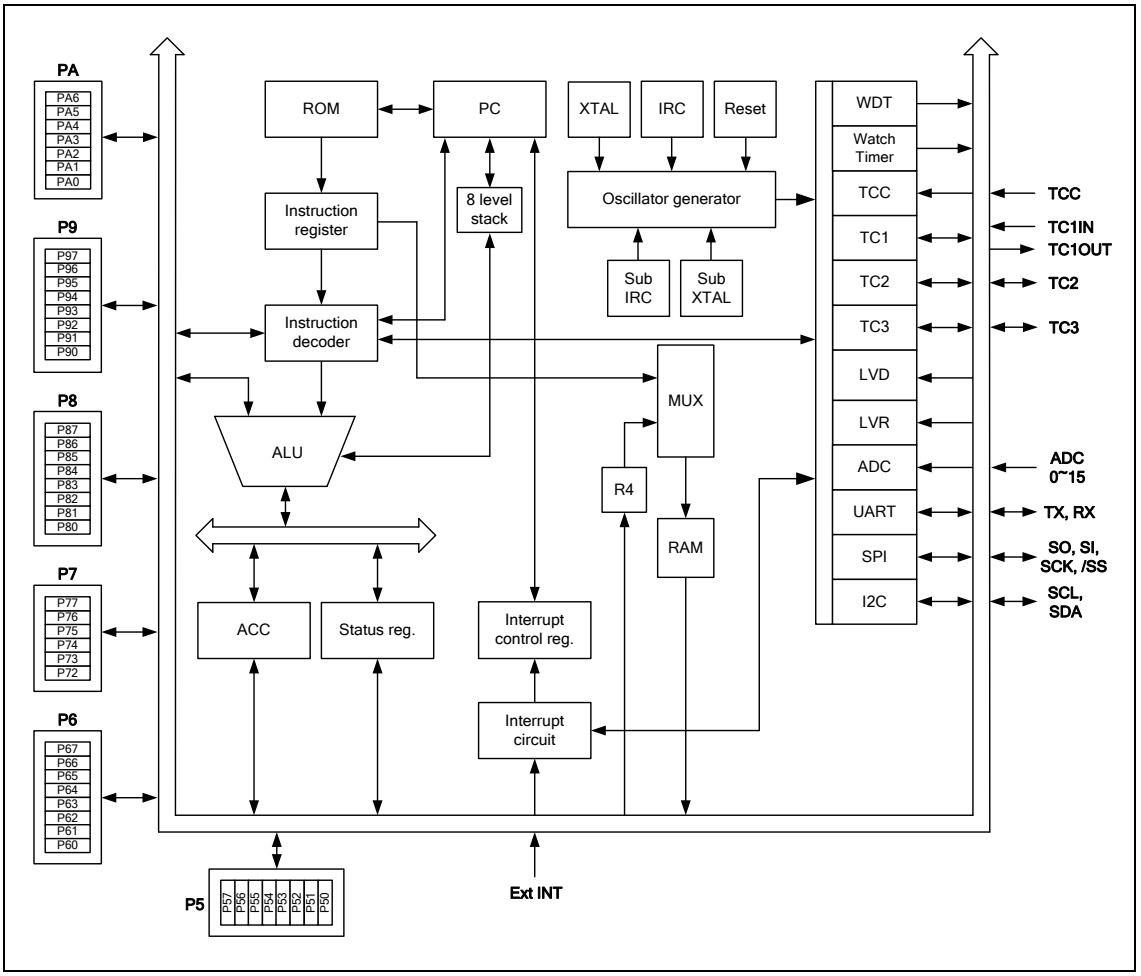


Figure 5-1 EM78P528N Functional Block Diagram

6 Functional Description

6.1 Operational Registers

6.1.1 R0 IAR (Indirect Addressing Register)

R0 is not a physically implemented register. Its major function is to perform as an indirect addressing pointer. Any instruction using R0 as a pointer actually accesses data pointed by the RAM Select Register (R4).

6.1.2 R1 BSR (Bank Selection Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
–	–	–	SBS0	–	–	GBS1	GBS0
–	–	–	R/W	–	–	R/W	R/W

Bits 7~5: Not used, set to "0" all the time.

Bit 4 (SBS0): Special register bank select bit. It is used to select Bank 0/1 of Special Registers **R5~R4F**.

0: Bank 0

1: Bank 1

Bits 3~2: Not used, fixed to 0 all the time.

Bits 1~0 (GBS1~GBS0): General register bank select bit. It is used to select Banks 0~3 of General Registers **R80~RFF**.

GBS1	GBS0	RAM Bank
0	0	0
0	1	1
1	0	2
1	1	3

6.1.3 R2 PCL (Program Counter Low)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (PC7~PC0): Low byte of program counter.

- Depending on the device type, R2 and hardware stack are 13-bit wide. The structure is depicted in Figure 6-1.

- Generates 8K×15 bits on-chip OTP ROM addresses to the relative programming instruction codes. One program page is 4096 words long.
- R2 is set as all "0"s when under reset condition.
- "JMP" instruction allows direct loading of the lower 12-bit program counter. Thus, "JMP" allows the PC to go to any location within a page.
- "CALL" instruction loads the lower 12 bits of the PC, and the present PC value will be incremented by 1 and is pushed onto the stack. Thus, the subroutine entry address can be located anywhere within a page.
- "LJMP" instruction allows direct loading of the lower 13-bit program counter. Therefore, "LJMP" allows the PC to jump to any location within 8K (2^{13}).
- "LCALL" instruction loads the lower 13 bits of the PC and PC+1 are pushed onto the stack. Thus, the subroutine entry address can be located anywhere within 8K (2^{13}).
- "RET" ("RETL k", "RETI") instruction loads the program counter with the contents of the top-level stack.
- "ADD R2, A" allows a relative address to be added to the current PC, and the ninth and above bits of the PC will increase progressively.
- "MOV R2, A" allows to load an address from the "A" register to the lower 8 bits of the PC, and the ninth and above bits of the PC will remain unchanged.
- Any instruction except “ADD R2,A” that is written to R2 (e.g. "MOV R2, A", "BC R2, 6",·etc.) will cause the ninth bit and the above bits (A8~A12) of the PC to remain unchanged.
- All instructions are single instruction cycle (Fsys/2) except “LCALL” and “LJMP” instructions. The “LCALL” and “LJMP” instructions need two instruction cycles

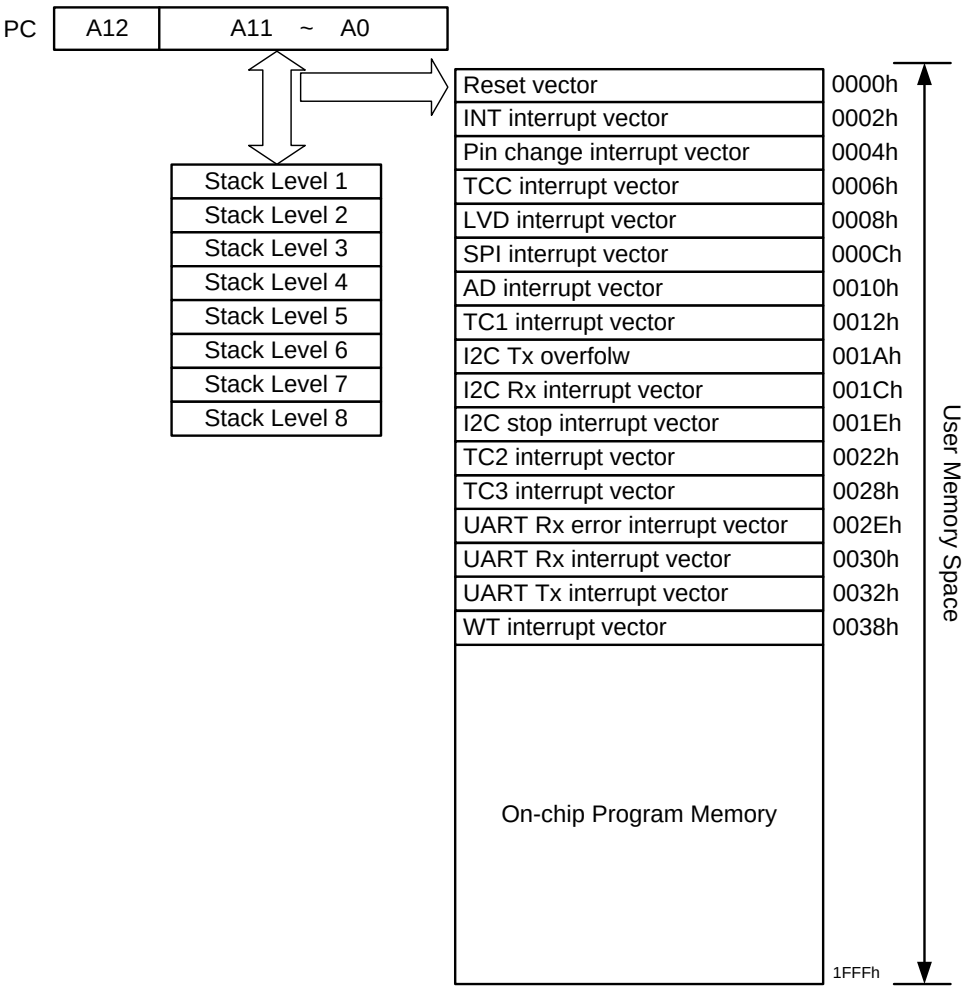


Figure 6-1 EM78P528N Program Counter Organization

■ Data Memory Configuration

Address	Bank 0	Bank 1
0X00	IAR (Indirect Addressing Register)	–
0X01	BSR (Bank Select Control Register)	
0X02	PC (Program Counter)	
0X03	SR (Status Register)	
0X04	RSR (RAM Select Register)	
0X05	Port 5	IOCR8
0X06	Port 6	IOCR9
0X07	Port 7	IOCRA
0X08	Port 8	P5PHCR
0X09	Port 9	P6PHCR
0X0A	Port A	P789APHCR
0x0B	IOC5	P5PLCR
0X0C	IOC6	P6PLCR
0X0D	IOC7	P789APLCR
0X0E	OMCR (Operating Mode Control Register)	P5HDSCR
0X0F	EIESCR1 (External Interrupt Edge Select Control Register)	P6HDSCR
0X10	WUCR1	P789AHDSCR
0X11	WUCR2	P5ODCR
0X12	WUCR3	P6ODCR
0X13	–	P789AODCR
0X14	SFR1 (Status Flag Register 1)	–
0X15	SFR2 (Status Flag Register 2)	–
0X16	SFR3 (Status Flag Register 3)	–
0X17	SFR4 (Status Flag Register 4)	–
0X18	SFR5 (Status Flag Register 5)	–
0X19	–	–
0X1A	–	–
0X1B	IMR1 (Interrupt Mask Register 1)	–
0X1C	IMR2 (Interrupt Mask Register 2)	–
0X1D	IMR3 (Interrupt Mask Register 3)	–
0X1E	IMR4 (Interrupt Mask Register 4)	–
0X1F	IMR5 (Interrupt Mask Register 5)	–
0X20	–	–
0X21	WDTCR	–

Address	Bank 0	Bank 1
0X22	TCCCR	–
0X23	TCCD	–
0X24	TC1CR1	–
0X25	TC1CR2	–
0X26	TC1DA	–
0X27	TC1DB	–
0X28	TC2CR1	–
0X29	TC2CR2	–
0X2A	TC2DA	–
0x2B	TC2DB	–
0X2C	TC3CR1	–
0X2D	TC3CR2	–
0X2E	TC3DA	–
0X2F	TC3DB	–
0X30	I^2CCR1	–
0X31	I^2CCR2	–
0X32	I^2CSA	–
0X33	I^2CDB	URCR
0X34	I^2CDAL	URS
0X35	I^2CDAH	URTD
0X36	SPICR	URRDL
0X37	SPIS	URRDH
0X38	SPIR	–
0X39	SPIW	–
0X3A	–	–
0x3B	–	–
0X3C	–	–
0X3D	–	–
0X3E	ADCR1	–
0X3F	ADCR2	–
0X40	ADISR	WCR
0X41	ADER1	–
0X42	ADER2	–
0X43	ADDL	–

Address	Bank 0	Bank 1
0X44	ADDH	–
0X45	ADCVL	TBPTL
0X46	ADCVH	TBPTH
0X47	–	STKMON
0X48	LCDCR1	PCH
0X49	LCDCR2	LVDCR
0X4A	LCDCR3	COBS1
0x4B	LCDADDR	COBS2
0X4C	LCDCCR	COBS3
0X4D	LCDSCR0	–
0X4E	LCDSCR1	–
0X4F	LCDSCR2	–
0X50	General Purpose Register	
0X51		
:		
:		
0X7F		

0X80	Bank 0	Bank 1	Bank 2	Bank 3
0X81				
:				
:				
:				
0XFE				
0XFF				

Figure 6-2 Data Memory Configuration

6.1.4 R3 SR (Status Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INT	–	–	T	P	Z	DC	C
F	–	–	R/W	R/W	R/W	R/W	R/W

Bit 7 (INT): Interrupt Enable flag

0: Interrupt masked by DISI or hardware interrupt

1: Interrupt enabled by ENI/DISI instructions

Bits 6~5: Not used, set to “0” all the time.

Bit 4 (T): Time-out bit.

Set to 1 with the "SLEP" and "WDTC" commands, or during power up and reset to “0” by WDT time-out.

Bit 3 (P): Power down bit.

Set to ”1” during power on or by a "WDTC" command and reset to ”0” by a "SLEP" command.

Bit 2 (Z): Zero flag.

Set to "1" if the result of an arithmetic or logic operation is zero.

Bit 1 (DC): Auxiliary carry flag

Bit 0 (C): Carry flag

6.1.5 R4 RSR (RAM Select Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RSR7	RSR6	RSR5	RSR4	RSR3	RSR2	RSR1	RSR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (RSR7~RSR0): these bits are used to select registers (Address: 00~FF) in indirect addressing mode. For more details refer to Figure 6-2 *Data Memory Configuration*.

6.1.6 Bank 0 R5 ~ RA Port 5 ~ Port A

R5, R6, R7, R8, R9 and RA are I/O data registers.

6.1.7 Bank 0 RB~RD IOCR5 ~ IOCR7

These registers are used to control the I/O port direction. They are both readable and writable.

0: Put the relative I/O pin as output

1: Put the relative I/O pin into high impedance (input)

6.1.8 Bank 0 RE OMCR (Operating Mode Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CPUS	IDLE	–	–	–	–	RCM1	RCM0
R/W	R/W	–	–	–	–	R/W	R/W

Bit 7 (CPUS): CPU Oscillator Source Select.

0: Fs: sub-oscillator

1: Fm: main-oscillator

When CPUS=0, the CPU oscillator selects the sub-oscillator and the main oscillator is stopped.

Bit 6 (IDLE): Idle Mode Enable Bit. This bit will determine as to which mode to go to or be activated after SLEP instruction.

0: "IDLE=0"+SLEP instruction → sleep mode

1: "IDLE=1"+SLEP instruction → idle mode

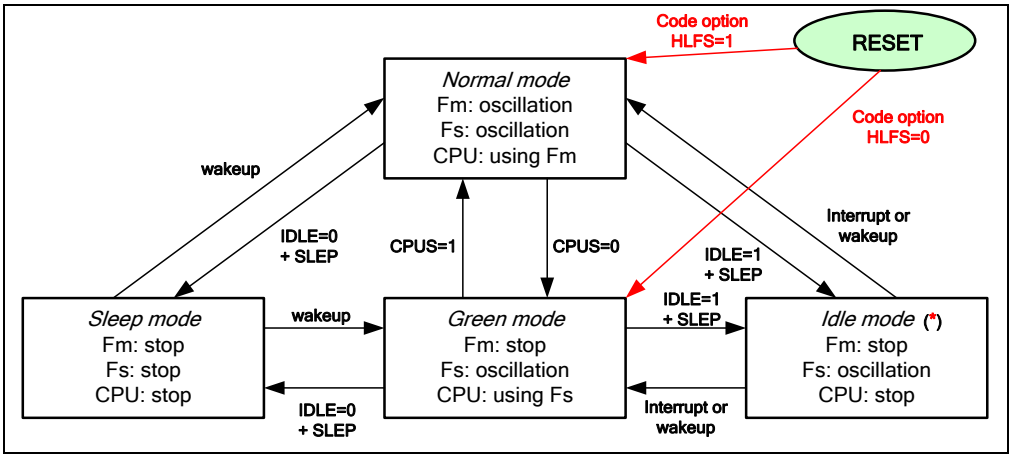


Figure 6-3 CPU Operation Mode

Note

(*) Switching Operation Mode from Idle → Normal, Idle → Green

If the clock source of the timer is Fs, the timer/counter will continue to count in Idle mode. When the matching condition of the timer/counter occurs during Idle mode, the interrupt flag of the timer/counter will be active. The MCU will jump to the interrupt vector when the corresponding interrupt is enabled.

■ Oscillation Characteristics

HLFS=1

Fmain	Fsub	Power-on LVR	Pin-Reset / WDT	
			N / G / I	S
RC	RC	16ms + WSTO + 8*1/Fmain	WSTO + 8*1/Fmain	WSTO + 8*1/Fmain
	XT	16ms + WSTO + 510*1/Fsub	WSTO + 8*1/Fmain	WSTO + 510*1/Fsub
XT	RC	16ms + WSTO + 510*1/Fmain	WSTO + 510*1/Fmain	WSTO + 510*1/Fmain
	XT	16ms + WSTO + 510*1/Fsub	WSTO + 510*1/Fmain	WSTO + 510*1/Fsub

HLFS=0

Fmain	Fsub	Power-on LVR	Pin-Reset / WDT	
			N / G / I	S
RC	RC	16ms + WSTO + 8*1/Fsub	WSTO + 8*1/Fsub	WSTO + 8*1/Fsub
	XT	16ms + WSTO + 510*1/Fsub	WSTO + 8*1/Fsub	WSTO + 510*1/Fsub
XT	RC	16ms + WSTO + 8*1/Fsub	WSTO + 8*1/Fsub	WSTO + 8*1/Fsub
	XT	16ms + WSTO + 510*1/Fsub	WSTO + 8*1/Fsub	WSTO + 510*1/Fsub

Fmain	Fsub	G → N	I → N	S → N
RC	RC	WSTO + 8*1/Fmain	WSTO + 8*1/Fmain	WSTO + 8*1/Fmain
	XT	WSTO + 8*1/Fmain	WSTO + 8*1/Fmain	WSTO + 510*1/Fsub
XT	RC	WSTO + 510*1/Fmain	WSTO + 510*1/Fmain	WSTO + 510*1/Fmain
	XT	WSTO + 510*1/Fmain	WSTO + 510*1/Fmain	WSTO + 510*1/Fsub

Fmain	Fsub	I → G	S → G
RC XT	RC	WSTO + 8*1/Fsub	WSTO + 8*1/Fsub
	XT	WSTO + 8*1/Fsub	WSTO + 510*1/Fsub

N: Normal mode *WSTO: Waiting Time from Start-to-Oscillation*
G: Green mode *I: Idle mode* *S: Sleep mode*

Bits 5~2: Not used, set to “0” all the time

Bits 1~0 (RCM1~RCM0): Internal RC mode select bits

*RCM1	*RCM0	Frequency (MHz)
0	0	1
0	1	8
1	0	16
1	1	4

***Note**:** *The initial value of RCM1~0 is the same as setting in Code Option Word 0. According to the control bit "COBS" in Code Option Word 0, the IRC frequencies can be switched by the control register or only by code option after the IC power is on.*

6.1.9 Bank 0 RF EIESCR (External Interrupt Edge Select Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EIES98	EIES76	EIES54	EIES32	EIES1	EIES0	–	–
R/W	R/W	R/W	R/W	R/W	R/W	–	–

Bit 7 (EIES98): External Interrupt Edge Select Bit (while controlling INT9 and INT8)

0: Falling edge interrupt

1: Rising edge interrupt

Bit 6 (EIES76): External Interrupt Edge Select Bit (while controlling INT7 and INT6)

0: Falling edge interrupt

1: Rising edge interrupt

Bit 5 (EIES54): External Interrupt Edge Select Bit (while controlling INT5 and INT4)

0: Falling edge interrupt

1: rising edge interrupt

Bit 4 (EIES32): External Interrupt Edge Select Bit (while controlling INT3 and INT2)

0: Falling edge interrupt

1: Rising edge interrupt

Bits 3~2 (EIES1~0): External Interrupt Edge Select Bit

0: Falling edge interrupt

1: Rising edge interrupt

Bits 1~0: Not used, set to "0" all the time

6.1.10 Bank 0 R10 WUCR1 (Wake-up Control Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
–	–	LVDWK	ADWK	INTWK1	INTWK0	–	–
–	–	R/W	R/W	R/W	R/W	–	–

Bits 7~6: Not used, set to "0" all the time

Bit 5 (LVDWK): Low Voltage Detect Wake-up Enable Bit

0: Disable Low Voltage Detect wake-up.

1: Enable Low Voltage Detect wake-up.

Bit 4 (ADWK): A/D Converter Wake-up Function Enable Bit

0: Disable AD converter wake-up

1: Enable AD converter wake-up

When the AD Complete status is used to enter an interrupt vector or to wake-up the IC from sleep/idle mode with AD conversion running, the ADWK bit must be set to "Enable".

Bits 3~2 (INTWK1~0): External Interrupt (INT pin) Wake-up Function Enable Bit

0: Disable external interrupt wake-up

1: Enable external interrupt wake-up

When the External Interrupt status changed is used to enter an interrupt vector or to wake-up the IC from sleep/idle mode, the INTWK bits must be set to "Enable".

Bits 1~0: Not used, set to "0" all the time

6.1.11 Bank 0 R11 WUCR2 (Wake-up Control Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
–	–	–	–	SPIWK	I^2CWK	–	–
–	–	–	–	R/W	R/W	–	–

Bits 7~4: Not used, set to "0" all the time.

Bit 3 (SPIWK): SPI wake-up enable bit. Functions when SPI works in Slave mode.

0: Disable SPI wake-up

1: Enable SPI wake-up

Bit 2 (I^2CWK): I^2C wake-up enable bit. It is available when I^2C works in Slave mode.

0: Disable

1: Enable

Bits 1~0: Not used, set to "0" all the time

6.1.12 Bank 0 R12 WUCR3 (Wake-up Control Register 3)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ICWKP8	ICWKP7	ICWKP6	ICWKP5	INTWK98	INTWK76	INTWK54	INTWK32
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~4 (ICWKP8~5): (Port 8~5) Pin-change Wake-up Function Enable Bit

0: Disable pin change wake-up function

1: Enable pin change wake-up function

Bits 3~0 (INTWK98/INTWK76/INTWK54/INTWK32): External Interrupt (INT pin) Wake-up Function Enable Bit (INTWK98 while controlling INT9 and INT8. INTWK76, INTWK54 and INTWK32 are similar)

0: Disable external interrupt wake-up

1: Enable external interrupt wake-up

When the External Interrupt status change is used to enter an interrupt vector or to wake-up the IC from sleep/idle mode, the INTWK bits must be set to “Enable“.

6.1.13 Bank 0 R14 SFR1 (Status Flag Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
–	–	LVDSF	ADSF	EXSF1	EXSF0	WTSF	TCSF
–	–	F	F	F	F	F	F

Each corresponding status flag is set to **“1”** when interrupt condition is triggered.

Bits 7~6: Not used, set to “0” all the time.

Bit 5 (LVDSF): Low Voltage Detector status flag.

LVDEN	LVDS2~0	LVD Voltage Interrupt Level	LVDSF
1	011	2.2V	1*
1	010	3.3V	1*
1	001	4.0V	1*
1	000	4.5V	1*
0	XXX	NA	0

* *If VDD crossovers at the LVD voltage interrupt level as VDD varies, then LVDSF = 1.*

Bit 4 (ADSF): Status flag for Analog-to-Digital conversion. Set when AD conversion is completed, reset by software.

Bits 3~2 (EXSF1~0): External interrupt status flag.

Bit 1 (WTSF): Watch timer status flag. Set when the Watch timer overflows, reset by software.

Bit 0 (TCSF): TCC overflow status flag. Set when TCC overflows, reset by software.

NOTE

If a function is enabled, the corresponding status flag would be active whether the interrupt mask is enabled or not.

6.1.14 Bank 0 R15 SFR2 (Status Flag Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
–	–	UERRSF	URSF	UTSF	TC3SF	TC2SF	TC1SF
–	–	F	F	F	F	F	F

Each corresponding status flag is set to **"1"** when interrupt condition is triggered.

Bits 7~6: Not used, set to "0" all the time

Bit 5 (UERRSF): UART receiving error Status flag. This flag is cleared by software or when UART is disabled.

Bit 4 (URSF): UART receive mode data buffer full Status flag. This flag is cleared by software.

Bit 3 (UTSF): UART transmit mode data buffer empty flag. This flag is cleared by software.

Bit 2 (TC3SF): 8-bit Timer/Counter 3 Status flag. This flag is cleared by software.

Bit 1 (TC2SF): 8-bit Timer/Counter 2 Status flag. This flag is cleared by software.

Bit 0 (TC1SF): 8-/16-bit Timer/Counter 1 Status flag. This flag is cleared by software.

6.1.15 Bank 0 R17 SFR4 (Status Flag Register 4)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P8ICSF	P7ICSF	P6ICSF	P5ICSF	SPISF	I^2CSTPSF	I^2CRSF	I^2CTSF
F	F	F	F	F	F	F	F

Bit 7 (P8ICSF): Port 8 Status flag. This flag is cleared by software.

Bit 6 (P7ICSF): Port 7 Status flag. This flag is cleared by software.

Bit 5 (P6ICSF): Port 6 Status flag. This flag is cleared by software.

Bit 4 (P5ICSF): Port 5 Status flag. This Flag is cleared by software.

Bit 3 (SPISF): SPI mode Status flag. This flag is cleared by software.

Bit 2 (I^2CSTPSF): I^2C Stop Status flag. Set when I^2C occurs at a stop signal.

Bit 1 (I^2CRSF): I^2C Receive Status flag. Set when I^2C receives 1 byte data and responds with an ACK signal. Reset by firmware or when $I^2$2C is disabled.

Bit 0 (I^2CTSF): I^2C Transmit Status flag. Set when I^2C transmits 1 byte data and receives handshake signal (ACK or NACK). Reset by firmware or when I^2C is disabled

NOTE

If a function is enabled, the corresponding Status flag would be active whether the interrupt mask is enabled or not.

6.1.16 Bank 0 R18 SFR5 (Status Flag Register 5)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EXSF9	EXSF8	EXSF7	EXSF6	EXSF5	EXSF4	EXSF3	EXSF2
F	F	F	F	F	F	F	F

Each corresponding Status flag is set to **"1"** when interrupt condition is triggered.

Bits 7~0 (EXSF9~2): External Interrupt Status flag.

NOTE

If a function is enabled, the corresponding status flag would be active regardless whether the interrupt mask is enabled or not.

6.1.17 Bank 0 R1B IMR1 (Interrupt Mask Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
–	–	LVDIE	ADIE	EXIE1	EXIE0	WTIE	TCIE
–	–	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~6: Not used, set to "0" all the time.

Bit 5 (LVDIE): LVDSF interrupt enable bit.

0: Disable LVDSF interrupt

1: Enable LVDSF interrupt

Bit 4 (ADIE): ADSF interrupt enable bit.

0: Disable ADSF interrupt

1: Enable ADSF interrupt

Bit 3 (EXIE1): EXSF1 interrupt enable bit.

0: Disable EXSF1 interrupt

1: Enable EXSF1 interrupt

Bit 2 (EXIE0): EXSF0 interrupt enable bit.

0: Disable EXSF0 interrupt

1: Enable EXSF0 interrupt

Bit 1 (WTIE): WTSF interrupt enable bit.

0: Disable WTSF interrupt

1: Enable WTSF interrupt

Bit 0 (TCIE): TCSF interrupt enable bit.

0: Disable TCSF interrupt

1: Enable TCSF interrupt

NOTE

If the interrupt mask and instruction "ENI" are enabled, the program counter would jump into the corresponding interrupt vector when the corresponding status flag is set.

6.1.18 Bank 0 R1C IMR2 (Interrupt Mask Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
–	–	UERRIE	URIE	UTIE	TC3IE	TC2IE	TC1IE
–	–	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~6: Not used, set to "0" all the time.

Bit 5 (UERRIE): UART receive error interrupt enable bit.

0: Disable UERRSF interrupt

1: Enable UERRSF interrupt

Bit 4 (URIE): UART receive mode Interrupt enable bit.

0: Disable URSF interrupt

1: Enable URSF interrupt

Bit 3 (UTIE): UART transmit mode interrupt enable bit.

0: Disable UTSF interrupt

1: Enable UTSF interrupt

Bit 2 (TC3IE): Interrupt enable bit.

0: Disable TC3SF interrupt

1: Enable TC3SF interrupt

Bit 1 (TC2IE): Interrupt enable bit.

0: Disable TC2SF interrupt

1: Enable TC2SF interrupt

Bit 0 (TC1IE): Interrupt enable bit.

0: Disable TC1SF interrupt

1: Enable TC1SF interrupt

NOTE

If the interrupt mask and instruction "ENI" are enabled, the program counter would jump to the corresponding interrupt vector when the corresponding status flag is set.

6.1.19 Bank 0 R1E IMR4 (Interrupt Mask Register 4)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P8ICIE	P7ICIE	P6ICIE	P5ICIE	SPIIE	I^2CSTPIE	I^2CRIE	I^2CTIE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~4 (P8ICIE ~P5ICIE): Ports 8~5 pin-change Interrupt Enable bit.

0: Disable P8ICSF ~ P5ICSF interrupt

1: Enable P8ICSF ~ P5ICSF interrupt

Bit 3 (SPIIE): Interrupt enable bit.

0: Disable SPISF interrupt

1: Enable SPISF interrupt

Bit 2 (I^2CSTPIE): I^2C stop interrupt enable bit.

0: Disable interrupt

1: Enable interrupt

Bit 1 (I^2CRIE): I^2C Interface Rx interrupt enable bit

0: Disable interrupt

1: Enable interrupt

Bit 0 (I^2CTIE): I^2C Interface Tx interrupt enable bit

0: Disable interrupt

1: Enable interrupt

NOTE

If the interrupt mask and instruction "ENI" are enabled, the program counter would jump to the corresponding interrupt vector when the corresponding status flag is set.

6.1.20 Bank 0 R1F IMR5 (Interrupt Mask Register 5)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EXIE9	EXIE8	EXIE7	EXIE6	EXIE5	EXIE4	EXIE3	EXIE2
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (EXIE9~2): EXSF9~2 interrupt enable bit.

0: Disable EXSF9~2 interrupt

1: Enable EXSF9~2 interrupt

INT Pin	Enable Condition	Edge	Digital Noise Reject
INTX	EXIEX	Rising or Falling	8/Fc or 32/Fc

NOTE

1. *The compound pin used as INT pin determines whether the interrupt mask is enabled or not.*
2. *If the interrupt mask and instruction "ENI" are enabled, the program counter would jump to the corresponding interrupt vector when the corresponding Status flag is set.*

6.1.21 Bank 0 R21 WDTCR (Watchdog Timer Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WDTE	–	–	–	PSWE	WPSR2	WPSR1	WPSR0
R/W	–	–	–	R/W	R/W	R/W	R/W

Bit 7 (WDTE): Watchdog Timer Enable Bit. WDTE is both readable and writable.

0: Disable WDT

1: Enable WDT

Bits 6~4: Not used, set to "0" all the time.

Bit 3 (PSWE): Prescaler enable bit for WDT

0: Prescaler disable bit. WDT rate is 1:1

1: Prescaler enable bit. WDT rate is set at Bits 2~0.

Bits 2~0 (WPSR2~ WPSR 0): WDT Prescaler Bits

WPSR2	WPSR1	WPSR0	WDT Rate
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

6.1.22 Bank 0 R22 TCCCR (TCC Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
–	TCCS	TS	TE	PSTE	TPSR2	TPSR1	TPSR0
–	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7: Not used, set to “0” all the time.

Bit 6 (TCCS): TCC Clock Source Select Bit

0: Fs (sub clock) (default)

1: Fm (main clock)

Bit 5 (TS): TCC Signal Source

0: Internal oscillator cycle clock. If P77 is used as I/O pin, TS must be 0.

1: Transition on the TCC pin, TCC period must be larger than internal instruction clock period.

Bit 4 (TE): TCC Signal Edge

0: Increment if the transition from low to high takes place on the TCC pin

1: Increment if the transition from high to low takes place on the TCC pin

Bit 3 (PSTE): Prescaler enable bit for TCC

0: Prescaler disable bit. The TCC rate is 1:1.

1: Prescaler enable bit. The TCC rate is set at Bit 2 ~ Bit 0.

Bits 2~0 (TPSR2~TPSR0): TCC Prescaler Bits

TPSR2	TPSR1	TPSR0	TCC Rate
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

6.1.23 Bank 0 R23 TCCD (TCC Data Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TCC7	TCC6	TCC5	TCC4	TCC3	TCC2	TCC1	TCC0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (TCC7~TCC0): TCC data

It is incremented by an external signal edge through the TCC pin or by the instruction cycle clock. The external signal of the TCC trigger pulse width must be greater than one instruction. The signals to increment the counter are determined by Bit 4 and Bit 5 of the TCCCR register. Writable and readable as any other registers. Whenever overflow is happened, the TCC circuit will continue to count signal edge from 0 repeatedly.

6.1.24 Bank 0 R24 TC1CR1 (Timer/Counter 1 Control Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TC1S	TC1RC	TC1SS1	TC1MOD	TC1FF	TC1OMS	TC1IS1	TC1IS0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7 (TC1S): Timer/Counter 1 start control (main switch for all modes)

0: Stop and clear the counter (default)

1: Start Timer/Counter 1

Bit 6 (TC1RC): Timer 1 Read Control Bit

0: When this bit is set to “0”, data from TC1DB cannot be read (default).

1: When this bit is set to “1”, data is read from TC1DB. The read data is the enumerated counting number.

Bit 5 (TC1SS1): Timer/Counter 1 clock source select Bit 1

0: Select internal clock as counting source (Fc) Fs/Fm (default)

1: Select external TC1 pin as counting source (Fc). It is used only for timer/counter mode.

Bit 4 (TC1MOD): Timer Operation Mode Select Bit

0: Two 8-bit timers

1: Timers 1 and 2 are cascaded as one 16-bit timer. The corresponding control register of the 16-bit timer is from Timer 1. TC1DA and TC1DB are high byte. TC2DA and TC2DB are low byte.

Bit 3 (TC1FF): Inversion for Timer/Counter 1 as PWM or PDO mode

0: Duty is Logic 1 (default)

1: Duty is Logic 0

Bit 2 (TC1OMS): Timer Output Mode Select Bit

0: Repeating mode (default)

1: One-shot mode

NOTE

One-shot mode means the timer only counts a cycle.

Bits 1~0 (TC1IS1~ TC1IS0): Timer 1 Interrupt Type Select Bits. These two bits are used when the Timer operates in PWM mode.

TC1IS1	TC1IS0	Timer 1 Interrupt Type Select
0	0	TC1DA (period) matching
0	1	TC1DB (duty) matching
1	×	TC1DA and TC1DB matching

6.1.25 Bank 0 R25 TC1CR2 (Timer/Counter 1 Control Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TC1M2	TC1M1	TC1M0	TC1SS0	TC1CK3	TC1CK2	TC1CK1	TC1CK0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~5 (TC1M2~TC1M0): Timer/Counter 1 operation mode select.

TC1M2	TC1M1	TC1M0	Operating Mode Select
0	0	0	Timer/Counter Rising Edge
0	0	1	Timer/Counter Falling Edge
0	1	0	Capture Mode Rising Edge
0	1	1	Capture Mode Falling Edge
1	0	0	Window mode
1	0	1	Programmable Divider output
1	1	0	Pulse Width Modulation output
1	1	1	Buzzer (output timer/counter clock source. The duty cycle of the clock source must be 50/50)

Bit 4 (TC1SS0): Timer/Counter 1 clock source select bit

0: Fs is used as counting source (Fc) (default)

1: Fm is used as counting source (Fc)

Bits 3~0 (TC1CK3~TC1CK0): Timer/Counter 1 clock source prescaler select

TC3CK3	TC3CK2	TC3CK1	TC3CK0	Clock Source	Resolution 8 MHz	Max. Time 8 MHz	Resolution 16kHz	Max. Time 16kHz
				Normal	F_C=8M	F_C=8M	F_C=16K	F_C=16K
0	0	0	0	F_C	125ns	32 µs	62.5 µs	16ms
0	0	0	1	$F_C/2$	250ns	64 µs	125 µs	32ms
0	0	1	0	$F_C/2^2$	500ns	128 µs	250 µs	64ms
0	0	1	1	$F_C/2^3$	1 µs	256 µs	500 µs	128ms
0	1	0	0	$F_C/2^4$	2 µs	512 µs	1ms	256ms
0	1	0	1	$F_C/2^5$	4 µs	1024 µs	2ms	512ms
0	1	1	0	$F_C/2^6$	8 µs	2048 µs	4ms	1024ms
0	1	1	1	$F_C/2^7$	16 µs	4096 µs	8ms	2048ms
1	0	0	0	$F_C/2^8$	32 µs	8192 µs	16ms	4096ms
1	0	0	1	$F_C/2^9$	64 µs	16384 µs	32ms	8192ms
1	0	1	0	$F_C/2^{10}$	128 µs	32768 µs	64ms	16384ms
1	0	1	1	$F_C/2^{11}$	256 µs	65536 µs	128ms	32768ms
1	1	0	0	$F_C/2^{12}$	512 µs	131072 µs	256ms	65536ms
1	1	0	1	$F_C/2^{13}$	1.024ms	262144 µs	512ms	131072ms
1	1	1	0	$F_C/2^{14}$	2.048ms	524.288ms	1.024s	262144ms
1	1	1	1	$F_C/2^{15}$	4.096ms	1.048s	2.048s	524288ms

6.1.26 Bank 0 R26 TC1DA (Timer/Counter 1 Data Buffer A)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TC1DA7	TC1DA6	TC1DA5	TC1DA4	TC1DA3	TC1DA2	TC1DA1	TC1DA0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (TC1DA7~0): Data Buffer A of 8-bit Timer/Counter 1

6.1.27 Bank 0 R27 TC1DB (Timer/Counter 1 Data Buffer B)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TC1DB7	TC1DB6	TC1DB5	TC1DB4	TC1DB3	TC1DB2	TC1DB1	TC1DB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (TC1DB7~0): Data Buffer B of 8-bit Timer/Counter 1

NOTE

1. *When Timer / Counter x is used in PWM mode, the duty value stored at register TCxDB must be smaller than or equal to the period value stored at register TCxDA.,i.e. duty≦period. Then the PWM waveform is generated. If the duty is larger than the period, the PWM output waveform is kept at a **high** voltage level.*
2. *The period value set by users is extra plus 1 in inner circuit.*
   For example:

When the period value is set as 0x4F, the PWM waveform will actually generate 0x50 period length.

When the period value is set as 0xFF, the PWM waveform will actually generate 0x100 period length.

6.1.28 Bank 0 R28 TC2CR1 (Timer/Counter 2 Control Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TC2S	TC2RC	TC2SS1	–	TC2FF	TC2OMS	TC2IS1	TC2IS0
R/W	R/W	R/W	–	R/W	R/W	R/W	R/W

Bit 7 (TC2S): Timer/Counter 2 start control (main switch for all modes)

0: Stop and clear the counter (default)

1: Start Timer/Counter 2

Bit 6 (TC2RC): Timer 2 Read Control Bit

0: When this bit is set to “0”, data from TC2DB cannot be read (default).

1: When this bit is set to “1”, data is read from TC2DB. The read data is the enumerated counting number.

Bit 5 (TC2SS1): Timer/Counter 2 clock source select Bit 1

0: Internal clock as counting source (Fc) - Fs/Fm (default)

1: External TC2 pin as counting source (Fc). It is used only for timer/counter mode.

Bit 4: Not used, set to "0" all the time.

Bit 3 (TC2FF): Inversion for Timer/Counter 2 as PWM or PDO mode

0: Duty is Logic 1 (default).

1: Duty is Logic 0.

Bit 2 (TC2OMS): Timer Output Mode Select Bit

0: Repeating mode (default)

1: One-shot mode

NOTE

One-shot mode means the timer only counts a cycle.

Bits 1~0 (TC2IS1~ TC2IS0): Timer 2 Interrupt Type Select Bits. These two bits are used when the Timer operates in PWM mode.

TC2IS1	TC2IS0	Timer 2 Interrupt Type Select
0	0	TC2DA (period) matching
0	1	TC2DB (duty) matching
1	×	TC2DA and TC2DB matching

6.1.29 Bank 0 R29 TC2CR2 (Timer/Counter 2 Control Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TC2M2	TC2M1	TC2M0	TC2SS0	TC2CK3	TC2CK2	TC2CK1	TC2CK0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~5 (TC2M2~TC2M0): Timer/Counter 2 operation mode select

TC2M2	TC2M1	TC2M0	Operating Mode Select
0	0	0	Timer/Counter Rising Edge
0	0	1	Timer/Counter Falling Edge
0	1	0	Capture Mode Rising Edge
0	1	1	Capture Mode Falling Edge
1	0	0	Window mode
1	0	1	Programmable Divider output
1	1	0	Pulse Width Modulation output
1	1	1	Buzzer(output timer/counter clock source. The duty cycle of the clock source must be 50/50)

Bit 4 (TC2SS0): Timer/Counter 2 Clock Source Select Bit 0

0: Fs is used as counting source (Fc) (default)

1: Fm is used as counting source (Fc)

Bits 3~0 (TC2CK3~TC2CK0): Timer/Counter 2 Clock Source Prescaler Select.

TC2CK3	TC2CK2	TC2CK1	TC2CK0	Clock Source	Resolution 8 MHz	Max. Time 8 MHz	Resolution 16kHz	Max. Time 16kHz
				Normal	F_C=8M	F_C=8M	F_C=16K	F_C=16K
0	0	0	0	F_C	125ns	32 µs	62.5 µs	16ms
0	0	0	1	$F_C/2$	250ns	64 µs	125 µs	32ms
0	0	1	0	$F_C/2^2$	500ns	128 µs	250 µs	64ms
0	0	1	1	$F_C/2^3$	1 µs	256 µs	500 µs	128ms
0	1	0	0	$F_C/2^4$	2 µs	512 µs	1ms	256ms
0	1	0	1	$F_C/2^5$	4 µs	1024 µs	2ms	512ms
0	1	1	0	$F_C/2^6$	8 µs	2048 µs	4ms	1024ms
0	1	1	1	$F_C/2^7$	16 µs	4096 µs	8ms	2048ms
1	0	0	0	$F_C/2^8$	32 µs	8192 µs	16ms	4096ms
1	0	0	1	$F_C/2^9$	64 µs	16384 µs	32ms	8192ms
1	0	1	0	$F_C/2^{10}$	128 µs	32768 µs	64ms	16384ms
1	0	1	1	$F_C/2^{11}$	256 µs	65536 µs	128ms	32768ms
1	1	0	0	$F_C/2^{12}$	512 µs	131072 µs	256ms	65536ms
1	1	0	1	$F_C/2^{13}$	1.024ms	262144 µs	512ms	131072ms
1	1	1	0	$F_C/2^{14}$	2.048ms	524.288ms	1.024s	262144ms
1	1	1	1	$F_C/2^{15}$	4.096ms	1.048s	2.048s	524288ms

6.1.30 Bank 0 R2A TC2DA (Timer/Counter 2 Data Buffer A)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TC2DA7	TC2DA6	TC2DA5	TC2DA4	TC2DA3	TC2DA2	TC2DA1	TC2DA0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (TC2DA7~ TC2DA0): Data Buffer A of 8-bit Timer/Counter 2

6.1.31 Bank 0 R2B TC2DB (Timer/Counter 2 Data Buffer B)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TC2DB7	TC2DB6	TC2DB5	TC2DB4	TC2DB3	TC2DB2	TC2DB1	TC2DB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (TC2DB7~ TC2DB0): Data Buffer B of 8-bit Timer/Counter 2

6.1.32 Bank 0 R2C TC3CR1 (Timer/Counter 3 Control Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TC3S	TC3RC	TC3SS1	−	TC3FF	TC3OMS	TC3IS1	TC3IS0
R/W	R/W	R/W	−	R/W	R/W	R/W	R/W

Bit 7 (TC3S): Timer/Counter 3 start control (main switch for all modes)

0: Stop and clear the counter (default)

1: Start Timer/Counter 3

Bit 6 (TC3RC): Timer 3 Read Control Bit

0: When this bit is set to "0", data from TC3DB cannot be read (default).

1: When this bit is set to "1", data is read from TC3DB. The read data is the enumerated counting number.

Bit 5 (TC3SS1): Timer/Counter 3 Clock Source Select Bit 1

0: Internal clock as counting source (Fc) - Fs/Fm (default)

1: External TC3 pin as counting source (Fc). It is used only for timer/counter mode.

Bit 4: Not used, set to "0" all the time.

Bit 3 (TC3FF): Inversion for Timer/Counter 3 as PWM or PDO mode.

0: Duty is Logic 1 (default).

1: Duty is Logic 0.

Bit 2 (TC3OMS): Timer Output Mode Select Bit

0: Repeating mode (default)

1: One-shot mode

NOTE

One-shot mode means the timer only counts a cycle.

Bits 1~0 (TC3IS1~ TC3IS0): Timer 3 Interrupt Type Select Bits. These two bits are used when the Timer operates in PWM mode.

TC3IS1	TC3IS0	Timer 3 Interrupt Type Select
0	0	TC3DA (period) matching
0	1	TC3DB (duty) matching
1	×	TC3DA and TC3DB matching

6.1.33 Bank 0 R2D TC3CR2 (Timer/Counter 3 Control Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TC3M2	TC3M1	TC3M0	TC3SS0	TC3CK3	TC3CK2	TC3CK1	TC3CK0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~5 (TC3M2~TC3M0): Timer/Counter 3 operation mode select.

TC3M2	TC3M1	TC3M0	Operating Mode Select
0	0	0	Timer/Counter Rising Edge
0	0	1	Timer/Counter Falling Edge
0	1	0	Capture Mode Rising Edge
0	1	1	Capture Mode Falling Edge
1	0	0	Window mode
1	0	1	Programmable Divider output
1	1	0	Pulse Width Modulation output
1	1	1	Buzzer (output timer/counter clock source. The duty cycle of the clock source must be 50/50)

Bit 4 (TC3SS0): Timer/Counter 3 Clock Source Select Bit 0

0: Fs is used as counting source (Fc) (default)

1: Fm is used as counting source (Fc)

Bits 3~0 (TC3CK3~TC3CK0): Timer/Counter 3 clock source prescaler select.

TC3CK3	TC3CK2	TC3CK1	TC3CK0	Clock Source	Resolution 8 MHz	Max. Time 8 MHz	Resolution 16kHz	Max. Time 16kHz
				Normal	F_C=8M	F_C=8M	F_C=16K	F_C=16K
0	0	0	0	F_C	125ns	32 µs	62.5 µs	16ms
0	0	0	1	$F_C/2$	250ns	64 µs	125 µs	32ms
0	0	1	0	$F_C/2^2$	500ns	128 µs	250 µs	64ms
0	0	1	1	$F_C/2^3$	1 µs	256 µs	500 µs	128ms
0	1	0	0	$F_C/2^4$	2 µs	512 µs	1ms	256ms
0	1	0	1	$F_C/2^5$	4 µs	1024 µs	2ms	512ms
0	1	1	0	$F_C/2^6$	8 µs	2048 µs	4ms	1024ms
0	1	1	1	$F_C/2^7$	16 µs	4096 µs	8ms	2048ms
1	0	0	0	$F_C/2^8$	32 µs	8192 µs	16ms	4096ms
1	0	0	1	$F_C/2^9$	64 µs	16384 µs	32ms	8192ms
1	0	1	0	$F_C/2^{10}$	128 µs	32768 µs	64ms	16384ms
1	0	1	1	$F_C/2^{11}$	256 µs	65536 µs	128ms	32768ms
1	1	0	0	$F_C/2^{12}$	512 µs	131072 µs	256ms	65536ms
1	1	0	1	$F_C/2^{13}$	1.024ms	262144 µs	512ms	131072ms
1	1	1	0	$F_C/2^{14}$	2.048ms	524.288ms	1.024s	262144ms
1	1	1	1	$F_C/2^{15}$	4.096ms	1.048s	2.048s	524288ms

6.1.34 Bank 0 R2E TC3DA (Timer/Counter 3 Data Buffer A)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TC3DA7	TC3DA6	TC3DA5	TC3DA4	TC3DA3	TC3DA2	TC3DA1	TC3DA0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (TC3DA7~ TC3DA0): Data Buffer A of 8-bit Timer/Counter 3

6.1.35 Bank 0 R2F TC3DB (Timer/Counter 3 Data Buffer B)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TC3DB7	TC3DB6	TC3DB5	TC3DB4	TC3DB3	TC3DB2	TC3DB1	TC3DB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (TC3DB7~ TC3DB0): Data Buffer B of 8-bit Timer/Counter 3

6.1.36 Bank 0 R30 I^2CCR1 (I^2C Status and Control Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Strobe/Pend	IMS	ISS	STOP	SAR_EMPTY	ACK	FULL	EMPTY
R/W	R/W	R/W	R/W	R	R	R	R

Bit 7 (Strobe/Pend): In Master mode, it is used as strobe signal to control the I^2C circuit from sending SCL clock. Automatically resets after receiving or transmitting a handshake signal (ACK or NACK).

In Slave mode, it is used as pending signal. User should clear it after writing data into the Tx buffer or retrieving data from the Rx buffer to inform the Slave I^2C circuit to release an SCL signal.

Bit 6 (IMS): I^2C Master/Slave mode select bit.

0: Slave

1: Master

Bit 5 (ISS): I^2C Fast/Standard mode select bit. (If Fm is 4 MHz and I^2CTS1~0<0,0>)

0: Standard mode (100kbit/s)

1: Fast mode (400kbit/s)

Bit 4 (STOP): In Master mode, if STOP=1 and R/nW=1 then the MCU must return a nACK signal to the Slave device before sending a STOP signal. If STOP=1 and R/nW=0 then the MCU sends a STOP signal after receiving an ACK signal. Reset when the MCU sends a STOP signal to the Slave device.

In Slave mode, if STOP=1 and R/nW=0 then the MCU must return a nACK signal to the Master device.

Bit 3 (SAR_EMPTY): Set when the MCU transmits a "1" byte data from the I²C Slave Address Register and receives an ACK (or nACK) signal. Reset when the MCU writes a "1" byte data to the I²C Slave Address Register.

Bit 2 (ACK): The ACK condition bit is set to "1" by hardware when the device responds with an "acknowledge" (ACK) signal. Reset when the device responds with a "not-acknowledge" (nACK) signal.

Bit 1 (FULL): Set by hardware when the I²C Receive Buffer Register is full. Reset by hardware when the MCU reads data from the I²C Receive Buffer Register.

Bit 0 (EMPTY): Set by hardware when I²C Transmit Buffer Register is empty and receives ACK (or nACK) signal. Reset by hardware when the MCU writes new data to I²C Transmit Buffer Register.

6.1.37 Bank 0 R31 I²CCR2 (I²C Status and Control Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
I²CBF	GCEN	–	BBF	I²CTS1	I²CTS0	–	I²CEN
R	R/W	–	R	R/W	R/W	–	R/W

Bit 7 (I²CBF): I²C Busy Flag Bit

0: Clear to "0" in Slave mode, if the received STOP signal or the I²C Slave address does not match.

1: Set when I²C communicates with Master in Slave mode.

Bit 6 (GCEN): I²C General Call Function Enable Bit

0: Disable General Call Function

1: Enable General Call Function

Bit 5: Not used, set to "0" all the time.

Bit 4 (BBF): Busy Flag Bit. I²C detection is busy in the Master mode. Read only.

Bits 3~2 (I²CTS1~I²CTS0): I²C Transmit Clock Select Bits. When using different operating frequency (Fm), these bits must be set correctly in order for the SCL clock to be consistent in Standard/Fast mode.

I²CCR1 Bit 5 = 1, Fast mode

I²CTS1	I²CTS0	SCL CLK	Operating Fm (MHz)
0	0	Fm/10	4
0	1	Fm/20	8
1	0	Fm/30	12
1	1	Fm/40	16

I²CCR1 Bit 5 = 0, Standard mode

I²CTS1	I²CTS0	SCL CLK	Operating Fm (MHz)
0	0	Fm/40	4
0	1	Fm/80	8
1	0	Fm/120	12
1	1	Fm/160	16

Bit 1: Not used, set to "0" all the time.

Bit 0 (I²CEN): I²C Enable Bit

0: Disable I²C mode

1: Enable I²C mode

6.1.38 Bank 0 R32 I²CSA (I²C Slave Address Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SA6	SA5	SA4	SA3	SA2	SA1	SA0	IRW
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~1 (SA6~SA0): When the MCU is used as Master device for I²C application, these bits are the Slave device address register.

Bit 0 (IRW): When the MCU is used as Master device for I²C application, this bit is a Read/Write transaction control bit.

0: Write

1: Read

6.1.39 Bank 0 R33 I²CDB (I²C Data Buffer Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (DB7~DB0): I²C Receive/Transmit Data Buffer.

6.1.40 Bank 0 R34 I²CDAL (I²C Device Address Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (DA7~DA0): When the MCU is used as Slave device for I²C application, this register stores the address of the MCU. It is used to identify the data on the I²C bus to extract the message delivered to the MCU.

6.1.41 Bank 0 R35 I²CDAH (I²C Device Address Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
–	–	–	–	–	–	DA9	DA8
–	–	–	–	–	–	R/W	R/W

Bits 7~2: Not used, set to "0" all the time.

Bits 1~0 (DA9~DA8): Device Address bits.

6.1.42 Bank 0 R36 SPICR (SPI Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CES	SPIE	SRO	SSE	SDOC	SBRS2	SBRS1	SBRS0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7 (CES): Clock Edge Select Bit

0: Data shifts out on a rising edge, and shifts in on a falling edge. Data is on hold during a low-level.

1: Data shifts out on a falling edge, and shift in on a rising edge. Data is on hold during a high-level.

Bit 6 (SPIE): SPI Enable Bit

0: Disable SPI mode

1: Enable SPI mode

Bit 5 (SRO): SPI Read Overflow Bit

0: No overflow

1: A new data is received while the previous data is still being held in the SPIR register. In this situation, the data in the SPIS register will be destroyed. To avoid setting this bit, user is required to read the SPIR register although only transmission is implemented. This can only occur in Slave mode.

Bit 4 (SSE): SPI Shift Enable Bit

0: Reset as soon as shifting is completed, and the next byte is ready to be shifted.

1: Start to shift, and remain on "1" while the current byte is still being transmitted.

Bit 3 (SDOC): SDO Output Status Control Bit

0: After the serial data output, the SDO remains high.

1: After the serial data output, the SDO remains low.

Bits 2~0 (SBRS2~SBRS0): SPI Baud Rate Select Bits

SBRS2	SBRS1	SBRS0	Mode	SPI Baud Rate
0	0	0	Master	Fosc/2
0	0	1	Master	Fosc/4
0	1	0	Master	Fosc/8
0	1	1	Master	Fosc/16
1	0	0	Master	Fosc/32
1	0	1	Master	Fosc/64
1	1	0	Slave	/SS enable
1	1	1	Slave	/SS disable

6.1.43 Bank 0 R37 SPIS (SPI Status Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DORD	TD1	TD0	–	OD3	OD4	–	RBF
R/W	R/W	R/W	–	R/W	R/W	–	R

Bit 7 (DORD): Data Shift of Type Control Bit

0: Shift left (MSB first)

1: Shift right (LSB first)

Bits 6~5 (TD1~TD0): SDO Status Output Delay Times Options. When CPU oscillator source use Fs from 1 CLK delay time.

TD1	TD0	Delay Time
0	0	8 CLK
0	1	16 CLK
1	0	24 CLK
1	1	32 CLK

Bit 4: Not used, set to “0” all the time.

Bit 3 (OD3): Open drain control bit

0: Open drain disable for SDO

1: Open drain enable for SDO

Bit 2 (OD4): Open drain control bit

0: Open drain disable for SCK

1: Open drain enable for SCK

Bit 1: Not used, set to “0” all the time.

Bit 0 (RBF): Read Buffer Full Flag

0: Receiving not completed, and SPIR has not fully exchanged.

1: Receiving completed, and SPIR is fully exchanged.

6.1.44 Bank 0 R38 SPIR (SPI Read Buffer Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SRB7	SRB6	SRB5	SRB4	SRB3	SRB2	SRB1	SRB0
R	R	R	R	R	R	R	R

Bits 7~0 (SRB7~SRB0): SPI Read Data Buffer

6.1.45 Bank 0 R39 SPIW (SPI Write Buffer Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SWB7	SWB6	SWB5	SWB4	SWB3	SWB2	SWB1	SWB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (SWB7~SWB0): SPI Write Data Buffer

6.1.46 Bank 0 R3E ADCR1 (Analog-to-Digital Converter Control Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CKR2	CKR1	CKR0	ADRUN	ADP	ADOM	SHS1	SHS0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~5 (CKR2~0): Clock Rate Selection of ADC

System Mode	CKR2~0	Operating Clock of ADC ($F_{AD} = 1 / T_{AD}$)	Max. F_{Main} (V_{DD} = 2.5V ~ 3V)	Max. F_{Main} (V_{DD} = 3V ~ 5.5V)
Normal Mode	000	$F_{Main}/16$	8 MHz	16 MHz
	001	$F_{Main}/8$	4 MHz	16 MHz
	010	$F_{Main}/4$	2 MHz	8 MHz
	011	$F_{Main}/2$	1 MHz	4 MHz
	100	$F_{Main}/64$	16 MHz	16 MHz
	101	$F_{Main}/32$	16 MHz	16 MHz
	110	$F_{Main}/1$	500kHz	2 MHz
	111	F_{Sub}	32.768kHz	32.768kHz
Green Mode	xxx	F_{Sub}	32.768kHz	32.768kHz

Bit 4 (ADRUN): ADC Starts to Run

In Single mode:

0: Reset on completion of the conversion by hardware, this bit cannot be reset by software.

1: A/D conversion starts. This bit can be set by software

In Continuous mode:

0: ADC is stopped

1: ADC is running unless this bit is reset by software

Bit 3 (ADP): ADC Power

0: ADC is in power down mode.

1: ADC is operating normally.

Bit 2 (ADOM): ADC Operation Mode Select

0: ADC operates in single mode.

1: ADC operates in continuous mode.

Bits 1~0 (SHS1~0): Sample and Hold Timing Select (Recommend at least 4 μs, T_{AD}**:** Period of ADC Operating Clock**)**

SHS1~0	Sample and Hold Timing
00	2 x T_{AD}
01	4 x T_{AD}
10	8 x T_{AD}
11	12 x T_{AD}

6.1.47 Bank 0 R3F ADCR2 (Analog-to-Digital Converter Control Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
–	–	ADIM	ADCMS	VPIS1	VPIS0	VREFP	–
–	–	R/W	R/W	R/W	R/W	R/W	–

Bits 7~6: Not used, set to “0” all the time.

Bit 5 (ADIM): ADC Interrupt Mode

0: Normal mode. Interrupt occurred after AD conversion is completed.

1: Compare mode. Interrupt occurred when comparison result conforms to the setting of ADCMS bits. Using continuous mode is recommended.

Bit 4 (ADCMS): ADC Compare Mode Select.

Compare mode:

0: Interrupt occurs when AD conversion data is equal to or greater than data in ADCD register (which means when ADD＞=ADCD, interrupt occurs).

1: Interrupt occurs when AD conversion data is equal to or less than the data in ADCD register (which means when ADD＜=ADCD, interrupt occurs).

Normal mode: No effect

Bits 3 ~ 2 (VPIS1~0): Internal Positive Reference Voltage Select

VPIS1~0	Reference Voltage
00	AVDD
01	4 V
10	3 V
11	2 V

Bit 1 (VREFP): Positive Reference Voltage Select

0: Internal positive reference voltage. The actual voltage is set by VPIS1~0 bits

1: From VREF pin.

Bit 0: Not used, set to "0" all the time.

NOTE

1. *When using the internal voltage reference and the Code Option Word 2<6> (IRCIRS) sets to "1", users need to wait for at least 50 µs when the first time to enable and stabilize the voltage reference. Un-stabilized reference makes conversion result inaccurate. After that, users only need to wait for at least 6 µs whenever switching voltage references.*
2. *When using the internal voltage reference and the Code Option Word 2<6> (IRCIRS) sets to "0", users only need to wait for at least 6 µs for the internal voltage reference circuit stabilized whenever switching voltage references.*

6.1.48 Bank 0 R40 ADISR (Analog-to-Digital Converter Input Channel Select Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
–	–	–	ADIS4	ADIS3	ADIS2	ADIS1	ADIS0
–	–	–	R/W	R/W	R/W	R/W	R/W

Bits 7~5: Not used, set to "0" all the time.

Bits 4~0 (ADIS4~0): ADC input channel select bits

ADIS4~0	Selected Channel	ADIS4~0	Selected Channel
00000	AD0	*10000	1/4 VDD Power Detect
00001	AD1	10001	N/A
00010	AD2	10010	N/A
00011	AD3	10011	N/A
00100	AD4	10100	N/A
00101	AD5	10101	N/A
00110	AD6	10110	N/A
00111	AD7	10111	N/A
01000	AD8	11000	N/A
01001	AD9	11001	N/A
01010	AD10	11010	N/A
01011	AD11	11011	N/A
01100	AD12	11100	N/A
01101	AD13	11101	N/A
01110	AD14	11110	N/A
01111	N/A	11111	N/A

* *Used for internal signal source. Users only need to set ADIS4~0=10000. These AD input channels are instantly active.*

6.1.49 Bank 0 R41 ADER1 (Analog-to-Digital Converter Input Control Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADE7	ADE6	ADE5	ADE4	ADE3	ADE2	ADE1	ADE0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7 (ADE7): ADC enable bit of P61 pin.

0: Disable AD7, P61 acts as I/O pin.

1: Enable AD7 to act as analog input pin.

Bit 6 (ADE6): ADC enable bit of P63 pin.

0: Disable AD6, P63 acts as I/O pin

1: Enable AD6 to act as analog input pin

Bit 5 (ADE5): ADC enable bit of P64 pin.

0: Disable AD5, P64 acts as I/O pin

1: Enable AD5 to act as analog input pin

Bit 4 (ADE4): ADC enable bit of P65 pin.

0: Disable AD4, P65 acts as I/O pin

1: Enable AD4 to act as analog input pin

Bit 3 (ADE3): ADC enable bit of P66 pin.

0: Disable AD3, P66 act as I/O pin

1: Enable AD3 to act as analog input pin

Bit 2 (ADE2): ADC enable bit of P67 pin.

0: Disable AD2, P67 acts as I/O pin

1: Enable AD2 to act as analog input pin

Bit 1 (ADE1): ADC enable bit of P72 pin.

0: Disable AD1, P72 acts as I/O pin

1: Enable AD1 to act as analog input pin

Bit 0 (ADE0): ADC enable bit of P73 pin.

0: Disable AD0, P73 acts as I/O pin

1: Enable AD0 to act as analog input pin

6.1.50 Bank 0 R42 ADER2 (Analog-to-Digital Converter Input Control Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
–	ADE14	ADE13	ADE12	ADE11	ADE10	ADE9	ADE8
–	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7: Not used, set to “0” all the time.

Bit 6 (ADE14): ADC enable bit of P95 pin.

0: Disable AD14, P95 acts as I/O pin

1: Enable AD14 to act as analog input pin

Bit 5 (ADE13): ADC enable bit of P94 pin.

0: Disable AD13, P94 acts as I/O pin

1: Enable AD13 to act as analog input pin

Bit 4 (ADE12): ADC enable bit of P93 pin.

0: Disable AD12, P93 acts as I/O pin

1: Enable AD12 to act as analog input pin

Bit 3 (ADE11): ADC enable bit of P92 pin.

0: Disable AD11, P92 acts as I/O pin

1: Enable AD11 to act as analog input pin

Bit 2 (ADE10): ADC enable bit of P91 pin.

0: Disable AD10, P91 acts as I/O pin

1: Enable AD10 to act as analog input pin

Bit 1 (ADE9): ADC enable bit of P90 pin.

0: Disable AD9, P90 acts as I/O pin

1: Enable AD9 to act as analog input pin

Bit 0 (ADE8): ADC enable bit of P60 pin.

0: Disable AD8, P60 acts as I/O pin

1: Enable AD8 to act as analog input pin

6.1.51 Bank 0 R43 ADDL (Low Byte of Analog-to-Digital Converter Data)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADD7	ADD6	ADD5	ADD4	ADD3	ADD2	ADD1	ADD0
R	R	R	R	R	R	R	R

Bits 7~0 (ADD7~ ADD0): Low Byte of AD Data Buffer

6.1.52 Bank 0 R44 ADDH (High Byte of Analog-to-Digital Converter Data)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADD15	ADD14	ADD13	ADD12	ADD11	ADD10	ADD9	ADD8
R	R	R	R	R	R	R	R

Bits 7~0 (ADD15~ ADD8): High Byte of AD Data Buffer.

The format of AD data is dependent on Code Option ADFM. The following table shows how the data justify the different ADFM settings.

ADFM1~0			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
12 bits	0	ADDH	-	-	-	-	ADD11	ADD10	ADD9	ADD8
		ADDL	ADD7	ADD6	ADD5	ADD4	ADD3	ADD2	ADD1	ADD0
	1	ADDH	ADD11	ADD10	ADD9	ADD8	ADD7	ADD6	ADD5	ADD4
		ADDL	-	-	-	-	ADD3	ADD2	ADD1	ADD0

6.1.53 Bank 0 R45 ADCVL (Low Byte of Analog-to-Digital Converter Compare Value)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADCV7	ADCV6	ADCV5	ADCV4	ADCV3	ADCV2	ADCV1	ADCV0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (ADCV7~ ADCV0): Low Byte Data for AD Compare Value.

User should use the data format as with ADDH and ADDL register. Otherwise faulty values will result after AD comparison.

6.1.54 Bank 0 R46 ADCVH (High Byte of Analog-to-Digital Converter Compare Value)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADCV15	ADCV14	ADCV13	ADCV12	ADCV11	ADCV10	ADCV9	ADCV8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (ADCV15~ ADCV8): High Byte Data for AD Compare Value

User should use the data format as with ADDH and ADDL registers. Otherwise, faulty values will result after AD comparison.

6.1.55 Bank 0 R48 LCDCR1 (LCD Driver Control Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LCDEN	LCDTYPE	–	BS	DS1	DS0	LCDF1	LCDF0
R/W	R/W	–	R/W	R/W	R/W	R/W	R/W

Bit 7 (LCDEN): LCD enable bit

0: Disable LCD driver Power-on during COM/SEG initial pull-low

1: Enable LCD driver

Bit 6 (LCDTYPE): LCD type select bit

0: A type waveform

1: B type waveform

Bit 5: Not used, set to “0” all the time.

Bit 4 (BS): bias select bit

BS	LCD bias
0	1/2 bias
1	1/3 bias

Bits 3~2 (DS1~DS0): LCD duty select bits

DS1	DS0	LCD duty
0	0	1/2 duty
0	1	1/3 duty
1	0	1/4 duty
1	1	1/8 duty

Bits 1~0 (LCDF1~LCDF0): LCD frame rate select bits

LCDF1	LCDF0	LCD Frame Frequency (Fs=32.768kHz from Cystal Osciilator)			
		1/2 duty	1/3 duty	1/4 duty	1/8 duty
0	0	Fs/(2*8*8*4)=64.0	Fs/(3*8*11*2)=62.0	Fs/(4*8*8*2)=64.0	Fs/(8*8*8)=64.0
0	1	Fs/(2*8*9*4)=56.8	Fs/(3*8*12*2)=56.8	Fs/(4*8*9*2)=56.8	Fs/(8*8*9)=56.8
1	0	Fs/(2*8*10*4)=51.2	Fs/(3*8*13*2)=52.5	Fs/(4*8*10*2)=51.2	Fs/(8*8*10)=51.2
1	1	Fs/(2*8*7*4)=73.1	Fs/(3*8*10*2)=68.2	Fs/(4*8*7*2)=73.1	Fs/(8*8*7)=73.1

LCDF1	LCDF0	LCD Frame Frequency (*Fs□32kHz from IRC)			
		1/2 duty	1/3 duty	1/4 duty	1/8 duty
0	0	Fs/(2*8*8*4)=62.5	Fs/(3*8*11*2)=60.6	Fs/(4*8*8*2) =62.5	Fs/(8*8*8)=62.5
0	1	Fs/(2*8*9*4)=55.6	Fs/(3*8*12*2)=55.6	Fs/(4*8*9*2) =55.6	Fs/(8*8*9)=55.6
1	0	Fs/(2*8*10*4)=50.0	Fs/(3*8*13*2)=51.3	Fs/(4*8*10*2) =50.0	Fs/(8*8*10)=50.0
1	1	Fs/(2*8*7*4)=71.4	Fs/(3*8*10*2)=66.7	Fs/(4*8*7*2) =71.4	Fs/(8*8*7)=71.4

Note: *The 32kHz frequency from the internal RC is dedicated for LCD application, not for the MCU kernel.

6.1.56 Bank 0 R49 LCDCR2 (LCD Driver Control Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
–	RBS1	RBS0	DYMEN	–	–	–	–
–	R/W	R/W	R/W	–	–	–	–

Bit 7: Not used, set to “0” all the time.

Bits 6~5 (RBS1~ RBS0): Resistor for Resistive Bias Selection

Bias	RBS1~0	Ohms (Ω)
1/2	00	270k
	01	150k
	10	90k
	11	30k
1/3	00	180k
	01	100k
	10	60k
	11	20k

Bit 4 (DYMEN): Dynamic Mode Enable

0: Disable

1: Enable

When Dynamic mode is enabled, 1/8 Clock LCD resistance of 20kΩ will switch to fast charging and 7/8 Clock LCD selection of LCD bias stalls resistance (RBS1 ~ 0 ≠ 11). If selected RBS1 ~ 0 = 11 (20kΩ) do not perform switching action.

Bits 3~0: Not used, set to “0” all the time.

6.1.57 Bank 0 R4A LCDCR3 (LCD Driver Control Register 3)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
–	–	–	–	–	LCDCC2	LCDCC1	LCDCC0
–	–	–	–	–	R/W	R/W	R/W

Bits 7~3: Not used, set to “0” all the time.

Bits 2~0 (LCDCC2~ LCDCC0): LCD Contrast Control (Only for R-Type LCD)

LCDCC2~0	V_{LCD}
000	1 x VDD
001	0.96 x VDD
010	0.93 x VDD
011	0.87 x VDD
100	0.82 x VDD
101	0.74 x VDD
110	0.66 x VDD
111	0.60 x VDD

6.1.58 Bank 0 R4B LCDADDR (Address of LCD RAM)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
–	–	–	LCDA4	LCDA3	LCDA2	LCDA1	LCDA0
–	–	–	R/W	R/W	R/W	R/W	R/W

Bits 7~5: Not used, set to “0” all the time.

Bits 4~0 (LCDA4~ LCDA0): Address of LCD RAM. This register is used for 00H~16H corresponding to SEG0~SEG22.

6.1.59 Bank 0 R4C LCDDB (Data of LCD RAM)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LCDD7	LCDD6	LCDD5	LCDD4	LCDD3	LCDD2	LCDD1	LCDD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (LCDD7~ LCDD0): LCD RAM data register

The following table shows the organization of the LCD RAM and the relation between the Data RAM and the LCD signal

Address of LCD RAM	Data of LCD RAM								SEG
	Bit 7 (LCDD7)	Bit 6 (LCDD6)	Bit 5 (LCDD5)	Bit 4 (LCDD4)	Bit 3 (LCDD3)	Bit 2 (LCDD2)	Bit 1 (LCDD1)	Bit 0 (LCDD0)	
0x00h	-	-	-	-	-	-	-	-	SEG0
0x01h	-	-	-	-	-	-	-	-	SEG1
0x02h	-	-	-	-	-	-	-	-	SEG2
|	|	|	|	|	|	|	|	|	|
0x14h	-	-	-	-	-	-	-	-	SEG20
0x15h	-	-	-	-	-	-	-	-	SEG21
0x16h	-	-	-	-	-	-	-	-	SEG22
COM	COM7	COM6	COM5	COM4	COM3	COM2	COM1	COM0	—

6.1.60 Bank 0 R4D LCDSCR0 (LCD COM/SEG Pin Control Register 0)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
–	LCDSM2	LCDSM1	LCDSM0	–	LCDCM2	LCDCM1	LCDCM0
–	R/W	R/W	R/W	–	R/W	R/W	R/W

Bit 7: Not used, set to 0 all the time

Bits 6~4 (LCDSM2~ LCDSM0): LCD pin switch for SEG16~SEG22

LCDSM 2~0	Number of SEG signals	Description
x00	16 segments mode max. (default)	SEG0~SEG15 pins are switched individually. SEG16~SEG22 pins are switched to general purpose I/O ports.
001	18 segments mode max.	SEG0~SEG15 pins are switched individually. SEG16~SEG17 pins are switched to LCD segment signals. SEG18~SEG22 pins are switched to general purpose I/O ports.
010	20 segments mode max.	SEG0~SEG15 pins are switched individually. SEG16~SEG19 pins are switched to LCD segment signals. SEG20~SEG22 pins are switched to general purpose I/O ports.
x11	23 segments mode max.	SEG0~SEG15 pins are switched individually. SEG16~SEG22 pins are switched to LCD segment signals.
101	17 segments mode max.	SEG0~SEG15 pins are switched individually. SEG16~SEG21 pins are switched to general purpose I/O ports. SEG22 pin is switched to LCD segment signals.
110	18 segments mode max.	SEG0~SEG15 pins are switched individually. SEG16~SEG19 pins are switched to general purpose I/O ports. SEG20~SEG22 pins are switched to LCD segment signals.

Bit 3: Not used, set to “0” all the time.

Bits 2~0 (LCDCM2~ LCDCM0): LCD port switch for COM0~COM7.

LCDCM 2~0	Number of COM signals	Description
0xx	No common mode (default)	COM0~COM7 pins are switched to general purpose I/O ports.
100	2 common modes	COM0~COM1 pins are switched to LCD common signals. COM2~COM7 pins are switched to general purpose I/O ports.
101	3 common modes	COM0~COM2 pins are switched to LCD common signals. COM3~COM7 pins are switched to general purpose I/O ports.
110	4 common modes	COM0~COM3 pins are switched to LCD common signals. COM4~COM7 pins are switched to general purpose I/O ports.
111	8 common modes	COM0~COM7 pins are switched to LCD common signals.

6.1.61 Bank 0 R4E LCDSCR1 (LCD SEG Pin Control Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1	SEG0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (SEG7~ SEG0): LCD Pin Switch for SEG7~SEG0

0: Function as normal I/O or other functions (default)

1: Function as LCD segment pins

6.1.62 Bank 0 R4F LCDSCR2 (LCD Segment Control Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SEG15	SEG14	SEG13	SEG12	SEG11	SEG10	SEG9	SEG8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (SEG15~ SEG8): LCD Pin Switch for SEG15~SEG8

0: Function as normal I/O or other functions (default)

1: Function as LCD segment pins

6.1.63 Bank 1 R5~R7 IOCR8~IOCA

These registers are used to control I/O port direction. They are both readable and writable.

0: Put the relative I/O pin as output

1: Put the relative I/O pin into high impedance

6.1.64 Bank 1 R8 P5PHCR (Port 5 Pull-high Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PH57	PH56	PH55	PH54	PH53	PH52	PH51	PH50
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (PH57~PH50): Control bit used to enable pull-high of the P57~P50 pins

0: Enable internal pull-high

1: Disable internal pull-high

6.1.65 Bank 1 R9 P6PHCR (Port 6 Pull-high Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PH67	PH66	PH65	PH64	PH63	PH62	PH61	PH60
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (PH67~PH60): Control bit used to enable pull-high of the P67~P60 pins

0: Enable internal pull-high

1: Disable internal pull-high

6.1.66 Bank 1 RA P789APHCR (Port 7~A Pull-high Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PAHPH	PALPH	P9HPH	P9LPH	P8HPH	P8LPH	P7HPH	P7LPH
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7 (PAHPH): Control bit used to enable pull-high of Port A high nibble (PA7~PA4) pin

Bit 6 (PALPH): Control bit used to enable pull-high of Port A low nibble (PA3~PA0) pin

Bit 5 (P9HPH): Control bit used to enable pull-high of Port 9 high nibble (P97~P94) pin

Bit 4 (P9LPH): Control bit used to enable pull-high of Port 9 low nibble (P93~P90) pin

Bit 3 (P8HPH): Control bit used to enable pull-high of Port 8 high nibble (P87~P84) pin

Bit 2 (P8LPH): Control bit used to enable pull-high of Port 8 low nibble (P83~P80) pin

Bit 1 (P7HPH): Control bit used to enable pull-high of Port 7 high nibble (P77~P74) pin

Bit 0 (P7LPH): Control bit used to enable pull-high of Port 7 low nibble (P73~P72) pin

6.1.67 Bank 1 RB P5PLCR (Port 5 Pull-low Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PL57	PL56	PL55	PL54	PL53	PL52	PL51	PL50
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (PL57~PL50): Control bit used to enable pull-low of P57~P50 pins

0: Enable internal pull-low

1: Disable internal pull-low

6.1.68 Bank 1 RC P6PLCR (Port 6 Pull-low Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PL67	PL66	PL65	PL64	PL63	PL62	PL61	PL60
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (PL67~PL60): Control bit used to enable pull-low of P67~P60 pins

0: Enable internal pull-low

1: Disable internal pull-low

6.1.69 Bank 1 RD P789APLCR (Port 7~A Pull-low Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PAHPL	PALPL	P9HPL	P9LPL	P8HPL	P8LPL	P7HPL	P7LPL
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7 (PAHPL): Control bit used to enable pull-low of Port A high nibble (PA7~PA4) pin

Bit 6 (PALPL): Control bit used to enable pull-low of Port A low nibble (PA3~PA0) pin

Bit 5 (P9HPL): Control bit used to enable pull-low of Port 9 high nibble (P97~P94) pin

Bit 4 (P9LPL): Control bit used to enable pull-low of Port 9 low nibble (P93~P90) pin

Bit 3 (P8HPL): Control bit used to enable pull-low of Port 8 high nibble (P87~P84) pin

Bit 2 (P8LPL): Control bit used to enable pull-low of Port 8 low nibble (P83~P80) pin

Bit 1 (P7HPL): Control bit used to enable pull-low of Port 7 high nibble (P77~P74) pin

Bit 0 (P7LPL): Control bit used to enable pull-low of Port 7 low nibble (P73~P72) pin

6.1.70 Bank 1 RE P5HDSCR (Port 5 High Drive/Sink Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
H57	H56	H55	H54	H53	H52	H51	H50
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (H57~H50): P57~P50 high drive/sink current control bits

0: Enable high drive/sink

1: Disable high drive/sink

6.1.71 Bank 1 RF P6HDSCR (Port 6 High Drive/Sink Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
H67	H66	H65	H64	H63	H62	H61	H60
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (H67~H60): P67~P60 high drive/sink current control bits

0: Enable high drive/sink

1: Disable high drive/sink

6.1.72 Bank 1 R10 P789AHDSCR (Port 7~A High Drive/Sink Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PAHHDS	PALHDS	P9HHDS	P9LHDS	P8HHDS	P8LHDS	P7HHDS	P7LHDS
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7 (PAHHDS): Control bit used to enable high drive/sink of Port A high nibble (PA7~PA4) pin

Bit 6 (PALHDS): Control bit used to enable high drive/sink of Port A low nibble (PA3~PA0) pin

Bit 5 (P9HHDS): Control bit used to enable high drive/sink of Port 9 high nibble (P97~P94) pin

Bit 4 (P9LHDS): Control bit used to enable high drive/sink of Port 9 low nibble (P93~P90) pin

Bit 3 (P8HHDS): Control bit used to enable high drive/sink of Port 8 high nibble (P87~P84) pin

Bit 2 (P8LHDS): Control bit used to enable high drive/sink of Port 8 low nibble (P83~P80) pin

Bit 1 (P7HHDS): Control bit used to enable high drive/sink of Port 7 high nibble (P77~P74) pin

Bit 0 (P7LHDS): Control bit used to enable high drive/sink of Port 7 low nibble (P73~P72) pin

6.1.73 Bank 1 R11 P5ODCR (Port 5 Open-drain Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OD57	OD56	OD55	OD54	OD53	OD52	OD51	OD50
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (OD57~OD50): P57~P50 Open-drain control bits

0: Disable open-drain function

1: Enable open-drain function

6.1.74 Bank 1 R12 P6ODCR (Port 6 Open-drain Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OD67	OD66	OD65	OD64	OD63	OD62	OD61	OD60
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (OD67~OD60): P67~P60 Open-drain control bits

0: Disable open-drain function

1: Enable open-drain function

6.1.75 Bank 1 R13 P789AODCR (Ports 7~A Open-drain Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PAHOD	PALOD	P9HOD	P9LOD	P8HOD	P8LOD	P7HOD	P7LOD
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7 (PAHOD): Control bit used to enable open-drain of Port A high nibble (PA7~PA4) pin

Bit 6 (PALOD): Control bit used to enable open-drain of Port A low nibble (PA3~PA0) pin

Bit 5 (P9HOD): Control bit used to enable open-drain of Port 9 high nibble (P97~P94) pin

Bit 4 (P9LOD): Control bit used to enable open-drain of Port 9 low nibble (P93~P90) pin

Bit 3 (P8HOD): Control bit used to enable open-drain of Port 8 high nibble (P87~P84) pin

Bit 2 (P8LOD): Control bit used to enable open-drain of Port 8 low nibble (P83~P80) pin

Bit 1 (P7HOD): Control bit used to enable open-drain of Port 7 high nibble (P77~P74) pin

Bit 0 (P7LOD): Control bit used to enable open-drain of Port 7 low nibble (P73~P72) pin

6.1.76 Bank 1 R33 URCR (UART Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
UINVEN	UMODE1	UMODE0	BRATE2	BRATE1	BRATE0	UTBE	TXE
R/W	R/W	R/W	R/W	R/W	R/W	R	R/W

Bit 7 (UINVEN): Enable UART TXD and RXD Port Inverse Output Bit

0: Disable TXD and RXD port inverse output.

1: Enable TXD and RXD port inverse output.

Bits 6~5 (UMODE1~UMODE0): UART mode select bits

UMODE1	UMODE0	UART Mode
0	0	7-bit
0	1	8-bit
1	0	9-bit
1	1	Reserved

Bits 4~2 (BRATE2~BRATE0): Transmit Baud rate select

BRATE2	BRATE1	BRATE0	Baud Rate	8 MHz
0	0	0	Fc/13	38400
0	0	1	Fc/26	19200
0	1	0	Fc/52	9600
0	1	1	Fc/104	4800
1	0	0	Fc/208	2400
1	0	1	Fc/416	1200
1	1	0	TC3	–
1	1	1	Reserved	

Bit 1 (UTBE): UART transfer buffer empty flag. Set to “1” when transfer buffer is empty. Reset to “**0**” automatically when writing to the URTD register. The UTBE bit will be cleared by hardware when enabling transmission. The UTBE bit is read-only. Therefore, writing to the URTD register is necessary in starting transmission shifting.

Bit 0 (TXE): Enable transmission

0: Disable

1: Enable

6.1.77 Bank 1 R34 URS (UART Status Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
URTD8	EVEN	PRE	PRERR	OVERR	FMERR	URBF	RXE
W	R/W	R/W	R/W	R/W	R/W	R	R/W

Bit 7 (URTD8): UART Transmit Data Bit 8. Write only.

Bit 6 (EVEN): Select parity check

0: Odd parity

1: Even parity

Bit 5 (PRE): Enable parity addition

0: Disable

1: Enable

Bit 4 (PRERR): Parity error flag. Set to 1 when parity error occurred, clear to 0 by software.

Bit 3 (OVERR): Over running error flag. Set to 1 when overrun error occurred, clear to 0 by software.

Bit 2 (FMERR): Framing error flag. Set to 1 when framing error occurred, clear to 0 by software.

Bit 1 (URBF): UART read buffer full flag. Set to 1 when one character is received. Reset to 0 automatically when read from the URS register. URBF will be cleared by hardware when enabling receiving. The URBF bit is read-only. Therefore, reading the URS register is necessary to avoid overrun error.

Bit 0 (RXE): Enable receiving

0: Disable

1: Enable

6.1.78 Bank 1 R35 URTD (UART Transmit Data Buffer Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
URTD7	URTD6	URTD5	URTD4	URTD3	URTD2	URTD1	URTD0
W	W	W	W	W	W	W	W

Bits 7~0 (URTD7~URTD0): UART transmit data buffer. Write only.

6.1.79 Bank 1 R36 URRDL (UART Receive Data Low Buffer Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
URRD7	URRD6	URRD5	URRD4	URRD3	URRD2	URRD1	URRD0
R	R	R	R	R	R	R	R

Bits 7~0 (URRD7~URRD0): UART Receive Data Buffer. **Read only**.

6.1.80 Bank 1 R37 URRDH (UART Receive Data High Buffer Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
URRD8	–	–	–	–	–	–	–
R	–	–	–	–	–	–	–

Bit 7 (URRD8): UART Receive Data Bit 8. **Read only.**

Bits 6~0: Not used, set to “0” all the time.

6.1.81 Bank 1 R40 WCR (Watch Timer Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WTE	WTSSB1	WTSSB0	–	–	–	–	–
R/W	R/W	R/W	–	–	–	–	–

Bit 7 (WTE): Watch Timer Enable Bit

0: Disable

1: Enable

Bits 6~5 (WTSSB1~ WTSSB0): Watch Timer Interval Select Bits

WTSSB1	WTSSB0	Timer Interval Select	Timer Interval Select (LXT2=32.768kHz)
0	0	32768/Fs	1.0s
0	1	16384/Fs	0.5s
1	0	8192/Fs	0.25s
1	1	128/Fs	3.91ms

Bits 4~0: Not used, set to “0” all the time.

6.1.82 Bank 1 R45 TBPTL (Table Pointer Low Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TB7	TB6	TB5	TB4	TB3	TB2	TB1	TB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (TB7~TB0): Table Pointer Address Bits 7~0.

6.1.83 Bank 1 R46 TBPTH (Table Pointer High Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
HLB	GP1	GP0	TB12	TB11	TB10	TB9	TB8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7 (HLB): Take MLB or LSB at machine code

Bits 6~5 (GP1~GP0): General Purpose read/write bits

Bits 4~0 (TB12~TB8): Table Pointer Address Bits 12~8.

6.1.84 Bank 1 R47 STKMON (Stack Monitor)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
STOV	–	–	–	STL3	STL2	STL1	STL0
R	–	–	–	R	R	R	R

Bit 7 (STOV): Stack pointer overflow indication bit. Read only.

Bits 6~4: Not used, set to “0” all the time.

Bits 3~0 (STL3~ STL0): Stack pointer number. Read only.

6.1.85 Bank 1 R48 PCH (Program Counter High)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
–	–	–	PC12	PC11	PC10	PC9	PC8
–	–	–	R/W	R/W	R/W	R/W	R/W

Bits 7~5: Not used, set to “0” all the time.

Bits 4~0 (PC12~PC8): Program Counter high byte.

6.1.86 Bank 1 R49 LVDCR (Low Voltage Detector Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LVDEN	LVDS2	LVDS1	LVDS0	LVDB	–	–	–
R/W	R/W	R/W	R/W	R	–	–	–

Bit 7 (LVDEN): Low Voltage Detector Enable Bit

0: Disable low voltage detector

1: Enable low voltage detector

Bits 6~4 (LVDS2~LVDS0): Low Voltage Detector Level Bits

LVDEN	LVDS2~0	LVD Voltage Interrupt Level	LVDB
1	011	VDD < 2.2V	0
		VDD > 2.2V	1
1	010	VDD < 3.3V	0
		VDD > 3.3V	1
1	001	VDD < 4.0V	0
		VDD > 4.0V	1
1	000	VDD < 4.5V	0
		VDD > 4.5V	1
0	XX	NA	1

Bit 3 (LVDB): Low Voltage Detector State Bit. This is a read only bit. When the VDD pin voltage is lower than LVD voltage interrupt level (selected by LVDS2 ~ LVDS0), this bit will be cleared.

0: Low voltage is detected.

1: Low voltage is not detected or LVD function is disabled.

Bits 2~0: Not used, set to "0" all the time.

6.1.87 Bank 1 R4A~R4C: (Reserve)

6.1.88 Bank 0 R50~R7F, Bank 0~3 R80~RFF

All of these are 8-bit general-purpose registers.

6.2 TCC/WDT and Prescaler

There are two 8-bit counters available as prescalers for the TCC and WDT respectively. The TPSR0~ TPSR2 bits of the TCCCR register (Bank 0 R22) are used to determine the ratio of the TCC prescaler. Likewise, the WPSR0~WPSR2 bits of the WDTCR register (Bank 0 R21) are used to determine the prescaler of WDT. The prescaler counter will be cleared by the instructions each time they are written into TCC. The WDT and prescaler counter will be cleared by the "WDTC" and "SLEP" instructions. Figure 6-3 depicts the Block Diagram of TCC/WDT.

The clock source of TCC can be internal clock or external signal input (edge selectable from the TCC pin). If the TCC signal source is from an internal clock, the TCC will be incremented by 1 at Fc clock (without prescaler). If the TCC signal source is from an external clock input, the TCC will be incremented by 1 at every falling edge or rising edge of the TCC pin. The TCC pin input time length (kept in High or low level) must be greater than 1/Fc. **The TCC will stop running when sleep mode occurs.**

The Watchdog timer is a free running on-chip RC oscillator. The WDT will keep on running even after the oscillator driver has been turned off (i.e. in sleep mode). During normal operation or sleep mode, a WDT time-out (if enabled) will cause the device to reset. The WDT can be enabled or disabled at any time during normal mode by software programming. Refer to WDTE bit of WDTCR (Bank 0 R21) register. With no prescaler, the WDT time-out period is approximately 16 ms[1] (one oscillator start-up timer period).

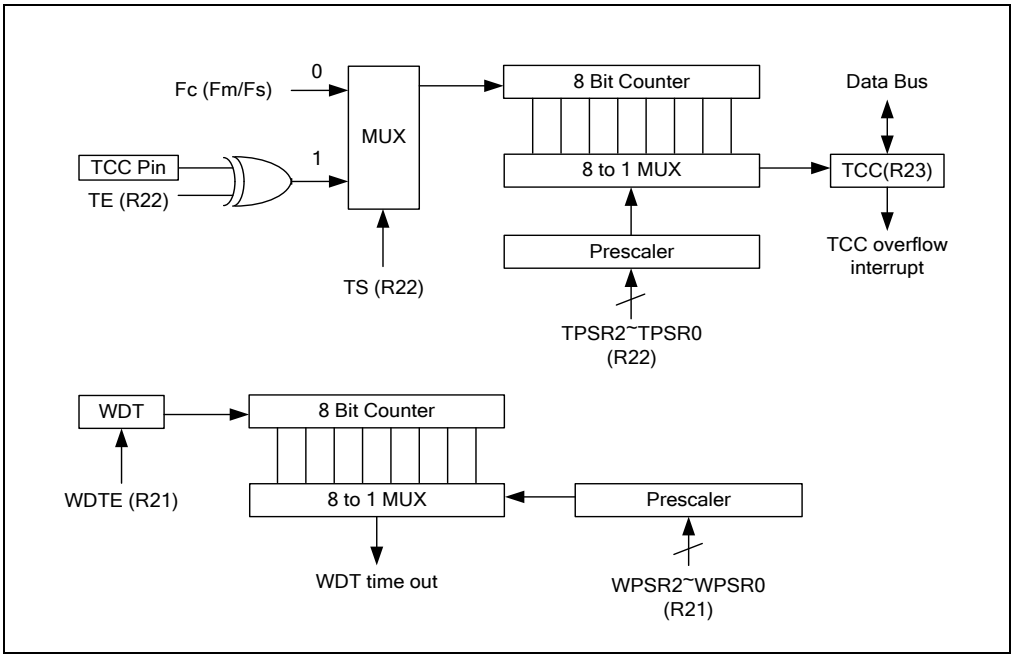


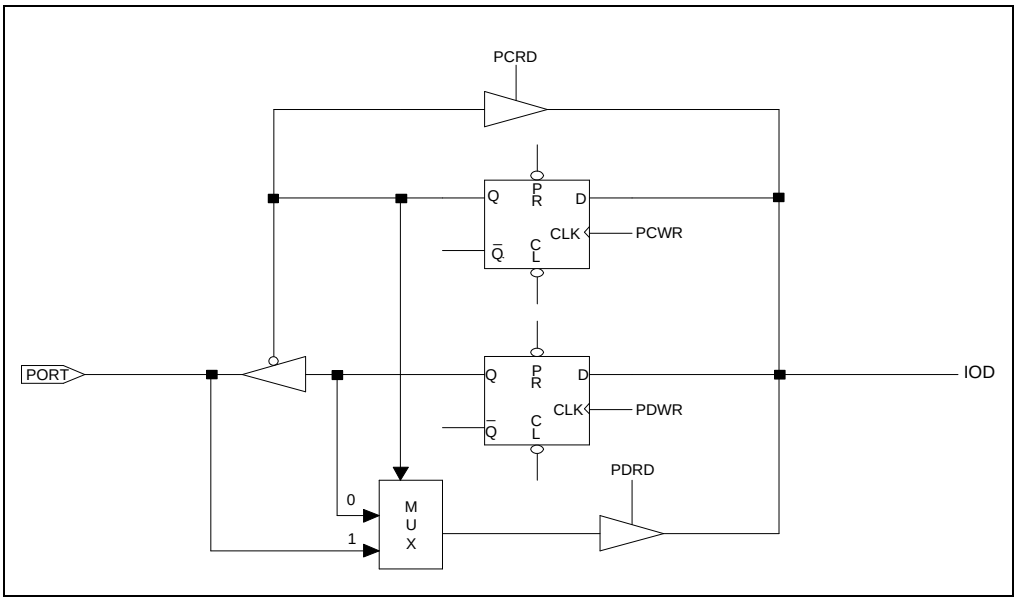
Figure 6-3 TCC and WDT Block Diagram

6.3 I/O Ports

The I/O registers, Port 5~Port A are bidirectional tri-state I/O ports. All can be pulled-high and pulled-low internally by software. In addition, they can also have open-drain output and high sink/drive setting by software. Ports 5~8 have wake up and interrupt function. Furthermore, Ports 5~8 also have input status change interrupt function. Each I/O pin can be defined as "input" or "output" pin by the I/O control register (IOC5 ~ IOCA).

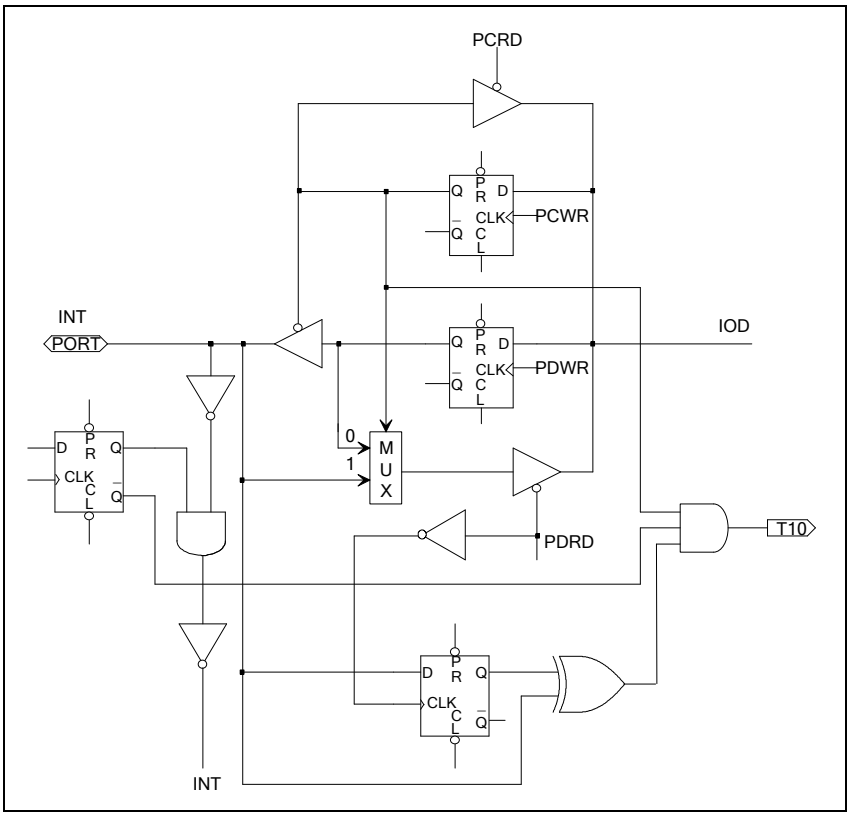
The I/O registers and I/O control registers are both readable and writable. The I/O interface circuits for Port 5 ~ Port A are shown in Figures 6-4 ~ 6-7.

[1] VDD=2.1~5.5V, Temp= -40°C~85°C, WDT Time-out period = 16ms ± 10%.



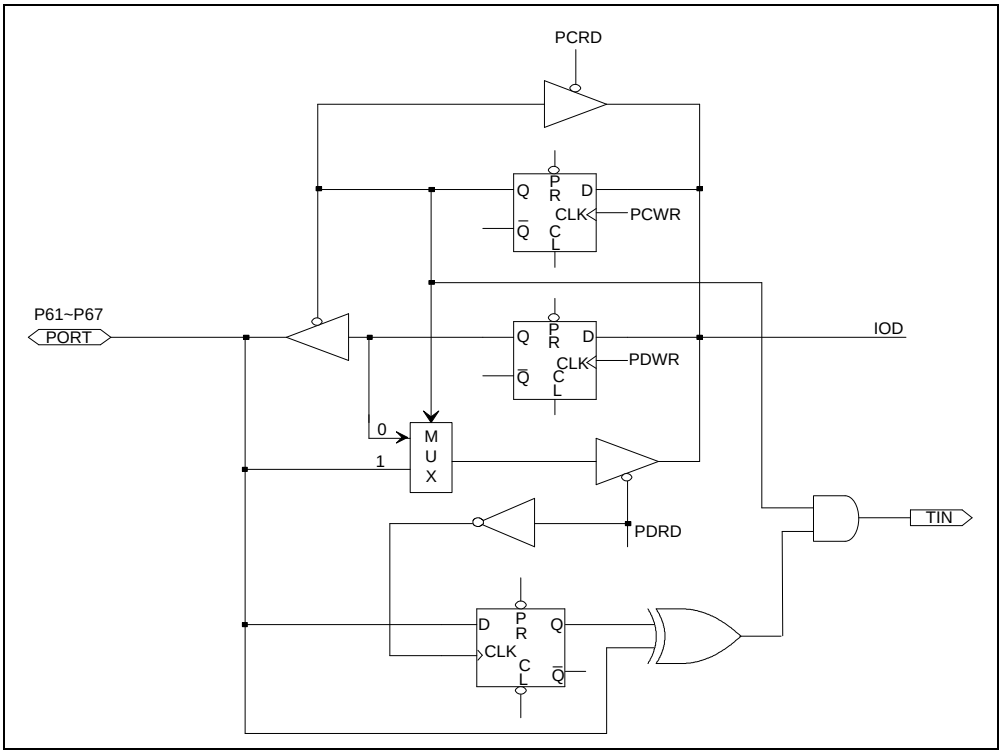
Note: Pull-down is not shown in the figure.

Figure 6-4 Circuit of I/O Port and I/O Control Register for Port 9~A



Note: Pull-high (down) and Open-drain are not shown in the figure.

Figure 6-5 Circuit of I/O Port and I/O Control Register for /INT



Note: Pull-high (down) and Open-drain are not shown in the figure.

Figure 6-6 Circuit of I/O Port and I/O Control Register for Ports 5~8

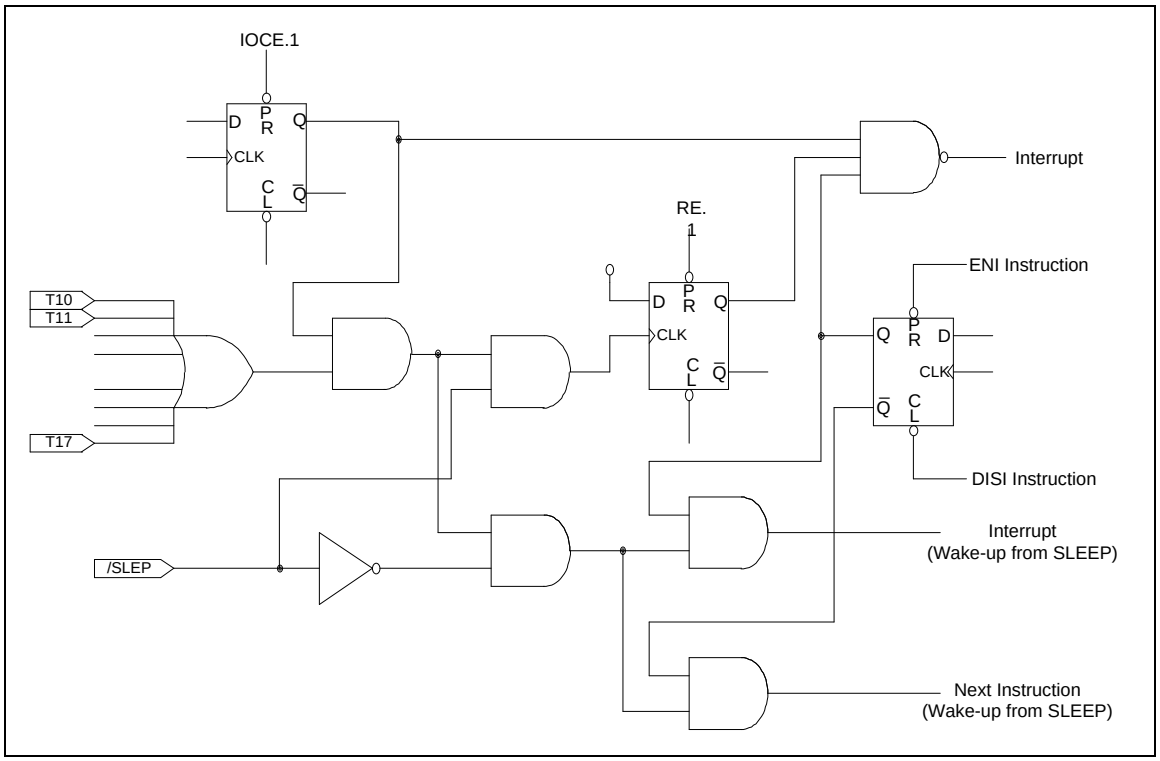


Figure 6-7 Block Diagram of I/O Port 5~8 with Input Change Interrupt/Wake-up

Table 1 Usage of Ports 5~8 Input Changed Wake-up/Interrupt Function

Usage of Ports 5~8 Input Status Changed Wake-up/Interrupt	
(I) Wake-up	(II) Wake-up and interrupt
(a) Before Sleep	(a) Before Sleep
1. Disable WDT	1. Disable WDT
2. Read I/O Port (MOV R6,R6)	2. Read I/O Port (MOV R6,R6)
3. Execute "ENI" or "DISI"	3. Execute "ENI" or "DISI"
4. Enable wake-up bit (Set WUE6H=1, WUE6L=1)	4. Enable wake-up bit (Set WUE6H=1, WUE6L=1)
5. Execute "SLEP" instruction	5. Enable interrupt (Set ICIE =1)
(b) After wake-up	6. Execute "SLEP" instruction
→ Next instruction	(b) After wake-up
	1. IF "ENI" → Interrupt vector (0006H)
	2. IF "DISI" → Next instruction

6.4 Reset and Wake-up

6.4.1 Reset

A reset is initiated by one of the following events-

(1) Power-on reset

(2) /RESET pin input "low"

(3) WDT time-out (if enabled)

(4) LVR (if enabled)

The device is kept in a reset condition for a period of approx. 16ms[2] (one oscillator start-up timer period) after the reset is detected. If the /Reset pin goes “low” or WDT time-out is active, a reset is generated, in IRC mode the reset time is WSTO and 8 clocks, High XTAL mode reset time is WSTO and 510 clocks. In low XTAL mode, the reset time is WSTO and 510 clocks (Fsub). Once a reset occurs, the following functions are performed. Refer to Figure 6-8.

- The oscillator is running, or will be started.
- The Program Counter (R2) is set to all "0".
- All I/O port pins are configured as input mode (high-impedance state).
- The Watchdog timer and prescaler are cleared.
- The control register bits are set according to the entries shown in Table 2 Summary of Register Initial Values after Reset.

[2] VDD=2.1~5.5V, Temp=-40°C~85°C, WDT time-out period = 16ms ± 10%.

Sleep (power down) mode is asserted by executing the “SLEP” instruction. While entering sleep mode, WDT (if enabled) is cleared but keeps on running. After wake-up is generated, in IRC mode the wake-up time is WSTO and 8 clocks, High XTAL mode wake-up time is WSTO and 510 clocks. In low XTAL mode, the wake-up time is WSTO and 510 clocks (Fsub). The controller can be awakened by :

(1) External reset input on /RESET pin.

(2) WDT time-out (if enabled).

(3) External (/INT) pin changes (if INTWKX is enabled).

(4) Port input status changes (if ICWKPX is enabled).

(5) SPI received data when SPI acts as a Slave device (if SPIWK is enabled).

(6) I^2C received data when I^2C acts as a Slave device (if I^2CWK is enabled).

(7) Low Voltage Detector (if LVDWK enable).

(8) A/D conversion completed (if ADWK is enabled).

The first two cases will cause the EM78P528N to reset. The T and P flags of R3 can be used to determine the source of the reset (wake-up). Case 3~8 are considered the continuation of program execution and the global interrupt ("ENI" or "DISI" being executed) determines whether or not the controller branches to the interrupt vector following a wake-up. If ENI is executed before SLEP, the instruction will begin to execute from the Address 0X02~0X38 by each interrupt vector after wake-up. If DISI is executed before SLEP, the execution will restart from the instruction right next to SLEP after wake-up.

Only one of Cases 3 to 8 can be enabled before entering into sleep mode. That is,

[a] If WDT is enabled before SLEP, the EM78P528N can be waken-up only by Case 1 or Case 2. For further details refer to Section 6.5, *Interrupt*.

[b] If the External (INT9~0) pin change is used to wake-up the EM78P528N and the INTWKX bit is enabled before SLEP, WDT must be disabled. Hence, the EM78P528N can be waken-up only by Case 3.

[c] If Port Input Status Change is used to wake-up the EM78P528N and the corresponding wake-up setting is enabled before SLEP, WDT must be disabled. Hence, the EM78P528N can be waken-up only by Case 4.

[d] When SPI acts as Slave device, after receiving data the EM78P528N will wake-up and the SPIWK bit of Bank 0 R11 register is enabled before SLEP, WDT must be disabled by software. Hence, the EM78P528N can be waken-up only by Case 5.

[e] When I^2C acts as Slave device, after receiving data, the EM78P528N will wake-up and the I^2CWK bit of Bank 0 R11 register is enabled before SLEP, WDT must be disabled by software. Hence, the EM78P528N can be waken-up only by Case 6.

[f] If Low voltage detector is used to wake-up the EM78P528N and the LVDWK bit of Bank 0 R10 register is enabled before SLEP, WDT must be disabled by software. Hence, the EM78P528N can be wake-up only by Case 7.

[g] If AD conversion completed is used to wake-up the EM78P528N and the ADWK bit of Bank 0 R10 register is enabled before SLEP, WDT must be disabled by software. Hence, the EM78P528N can be waken-up only by Case 8.

Table 2 All kinds of Wake-up modes and Interrupt modes are shown below:

Wake-up Signal	Condition Signal	Sleep Mode		Idle Mode		Green Mode		Normal Mode	
		DISI	ENI	DISI	ENI	DISI	ENI	DISI	ENI
TCC (Used as Timer)	TCIE=0	Wake-up is invalid		Wake-up is invalid		Interrupt is invalid		Interrupt is invalid	
	TCIE=1			Wake up + Next Instruction	Wake up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
TCC (Used as Counter)	TCIE=0	Wake-up is invalid		Wake-up is invalid		Interrupt is invalid		Interrupt is invalid	
	TCIE=1	Wake up + Next Instruction	Wake up + Interrupt Vector	Wake up + Next Instruction	Wake up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
TC1/2/3 Interrupt (Used as Timer)	TC1/2/3IE=0	Wake-up is invalid		Wake-up is invalid		Interrupt is invalid		Interrupt is invalid	
	TC1/2/3IE=1			Wake up + Next Instruction	Wake up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
TC1/2/3 Interrupt (Used as Counter)	TC1/2/3IE=0	Wake-up is invalid		Wake-up is invalid		Interrupt is invalid		Interrupt is invalid	
	TC1/2/3IE=1	Wake up + Next Instruction	Wake up + Interrupt Vector	Wake up + Next Instruction	Wake up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
Watch Timer	WTIE=0	Wake-up is invalid		Wake-up is invalid.		Interrupt is invalid.		Interrupt is invalid.	
	WTIE=1			–	Wake up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector

(Continuation)

Wake-up Signal	Condition Signal	Sleep Mode		Idle Mode		Green Mode		Normal Mode	
		DISI	ENI	DISI	ENI	DISI	ENI	DISI	ENI
External INT	INTWKx = 0, EXIEx = 0	Wake-up is invalid		Wake-up is invalid		Interrupt is invalid		Interrupt is invalid	
	INTWKx = 0, EXIEx = 1	Wake-up is invalid		Wake-up is invalid		Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
	INTWKx = 1, EXIEx = 0	Wake up + Next Instruction		Wake up + Next Instruction		Interrupt is invalid		Interrupt is invalid	
	INTWKx = 1, EXIEx = 1	Wake up + Next Instruction	Wake up + Interrupt Vector	Wake up + Next Instruction	Wake up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
Pin change	ICWKPx = 0, PxICIE = 0	Wake-up is invalid		Wake-up is invalid		Interrupt is invalid		Interrupt is invalid	
	ICWKPx = 0, PxICIE = 1	Wake-up is invalid		Wake-up is invalid		Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
	ICWKPx = 1, PxICIE = 0	Wake up + Next Instruction		Wake up + Next Instruction		Interrupt is invalid		Interrupt is invalid	
	ICWKPx = 1, PxICIE = 1	Wake up + Next Instruction	Wake up + Interrupt Vector	Wake up + Next Instruction	Wake up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
AD Conversion complete	ADWK = 0, ADIE = 0	Wake-up is invalid		Wake-up is invalid		Interrupt is invalid		Interrupt is invalid	
	ADWK = 0, ADIE = 1	Wake-up is invalid		Wake-up is invalid		Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
	ADWK = 1, ADIE = 0	Wake up + Next Instruction		Wake up + Next Instruction		Interrupt is invalid		Interrupt is invalid	
	ADWK = 1, ADIE = 1	Wake up + Next Instruction	Wake up + Interrupt Vector	Wake up + Next Instruction	Wake up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
SPI (Slave mode)	SPIWK = 0, SPIE = 0	Wake-up is invalid		Wake-up is invalid		Interrupt is invalid		Interrupt is invalid	
	SPIWK = 0, SPIE = 1	Wake-up is invalid		Wake-up is invalid		Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
	SPIWK = 1, SPIE = 0	Wake up + Next Instruction		Wake up + Next Instruction		Interrupt is invalid		Interrupt is invalid	
	SPIWK = 1, SPIE = 1	Wake up + Next Instruction	Wake up + Interrupt Vector	Wake up + Next Instruction	Wake up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector

(Continuation)

Wake-up Signal	Condition Signal	Sleep Mode		Idle Mode		Green Mode		Normal Mode	
		DISI	ENI	DISI	ENI	DISI	ENI	DISI	ENI
I^2C (Slave mode)	I^2CWK=0 I^2CRIE=0	Wake-up is invalid		Wake-up is invalid		Interrupt is invalid		Interrupt is invalid	
	I^2CWK=0 I^2CRIE=1	Wake-up is invalid		Wake-up is invalid		Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
	I^2CWK=1 I^2CRIE=0	Wake up + Next Instruction		Wake up + Next Instruction		Interrupt is invalid		Interrupt is invalid	
	I^2CWK=1 I^2CRIE=1	Wake up + Next Instruction	Wake up + Interrupt Vector	Wake up + Next Instruction	Wake up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
UART Transmit complete Interrupt	UTIE = 0	Wake-up is invalid		Wake-up is invalid		Interrupt is invalid.		Interrupt is invalid.	
	UTIE = 1					Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
UART Receive data Buffer full Interrupt	URIE = 0	Wake-up is invalid		Wake-up is invalid		Interrupt is invalid		Interrupt is invalid	
	URIE = 1					Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
UART Receive Error Interrupt	UERRIE = 0	Wake-up is invalid		Wake-up is invalid		Interrupt is invalid		Interrupt is invalid	
	UERRIE = 1					Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
Low Voltage Detector	LVDWK = 0, LVDIE = 0	Wake-up is invalid		Wake-up is invalid		Interrupt is invalid		Interrupt is invalid	
	LVDWK = 0, LVDIE = 1	Wake-up is invalid		Wake-up is invalid		Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
	LVDWK = 1, LVDIE = 0	Wake up + Next Instruction		Wake up + Next Instruction		Interrupt is invalid		Interrupt is invalid	
	LVDWK = 1, LVDIE = 1	Wake up + Next Instruction	Wake up + Interrupt Vector	Wake up + Next Instruction	Wake up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
Low Voltage Reset		Wake up + Reset		Wake up + Reset		Reset		Reset	
WDT Timeout		Wake up + Reset		Wake up + Reset		Reset		Reset	

6.4.2 Status of RST, T, and P of the Status Register

A reset condition is initiated by the following events:

1. Power-on condition,
2. High-low-high pulse on /RESET pin
3. Watchdog timer time-out
4. When LVR occurs

The values of T and P, listed in Table 4 are used to check how the processor wakes up. Table 4 shows the events that may affect the status of T and P.

Table 4 Values of RST, T and P after reset

Reset Type	T	P
Power on	1	1
/RESET during Operating mode	*P	*P
/RESET wake-up during Sleep mode	1	0
WDT during Operating mode	0	*P
WDT wake-up during Sleep mode	0	0
Wake-up on pin change during Sleep mode	1	0

***P:** *Previous status before reset*

Table 5 Status of T and P Being Affected by Events

Event	T	P
Power on	1	1
WDTC instruction	1	1
WDT time-out	0	*P
SLEP instruction	1	0
Wake-up on pin change during Sleep mode	1	0

***P:** *Previous value before reset*

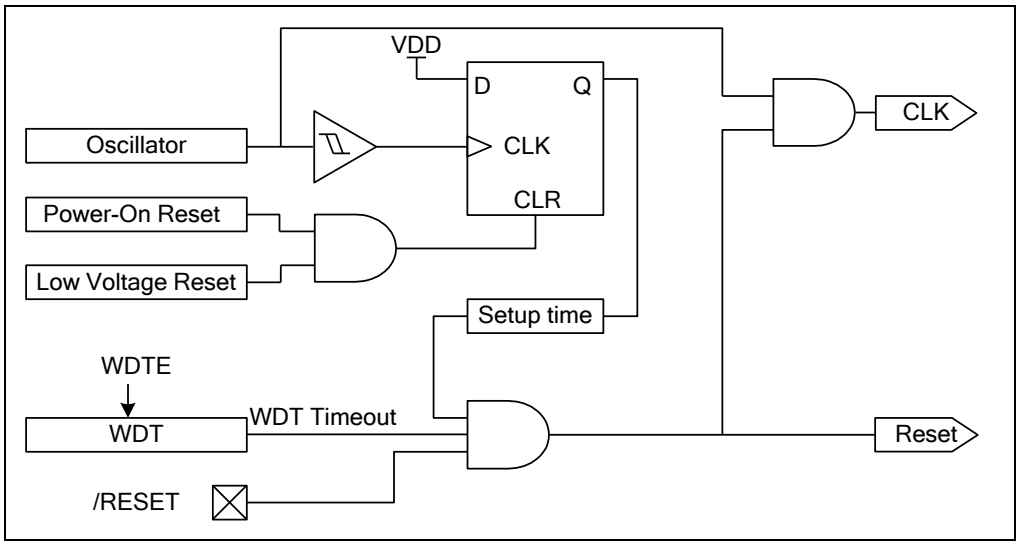


Figure 6-8 Block Diagram of Controller Reset

Table 3 Summary of Register Initial Values after Reset

Legend: U: *Unknown or don't care* ***P:*** *Previous value before reset*
C: *Same with Code option* ***t:*** *Check Table 4*

Address	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x00	Bank 0/1 R0 IAR	Bit Name	-	-	-	-	-	-	-	-
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0x01	Bank 0/1 R1 BSR	Bit Name	-	-	-	SBS0	-	-	GBS1	GBS0
		Power-on	U	U	U	0	U	U	0	0
		/RESET and WDT	U	U	U	0	U	U	0	0
		Wake-up from Sleep/Idle	U	U	U	P	U	U	P	P
0x02	Bank 0/1 R2 PCL	Bit Name	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0x03	Bank 0/1 R3 SR	Bit Name	INT	-	-	T	P	Z	DC	C
		Power-on	0	U	U	1	1	U	U	U
		/RESET and WDT	0	U	U	t	t	P	P	P
		Wake-up from Sleep/Idle	P	U	U	t	t	P	P	P
0x04	Bank 0/1 R4 RSR	Bit Name	RSR7	RSR6	RSR5	RSR4	RSR3	RSR2	RSR1	RSR0
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X05	Bank 0 R5 Port 5	Bit Name	P57	P56	P55	P54	P53	P52	P51	P50
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P

(Continuation)

Address	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x06	Bank 0 R6 Port 6	Bit Name	P67	P66	P65	P64	P63	P62	P61	P60
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0x07	Bank 0 R7 Port 7	Bit Name	P77	P76	P75	P74	P73	P72	-	-
		Power-on	0	0	0	0	0	0	U	U
		/RESET and WDT	0	0	0	0	0	0	U	U
		Wake-up from Sleep/Idle	P	P	P	P	P	P	U	U
0x08	Bank 0 R8 Port 8	Bit Name	P87	P86	P85	P84	P83	P82	P81	P80
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0x09	Bank 0 R9 Port 9	Bit Name	P97	P96	P95	P94	P93	P92	P91	P90
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0x0A	Bank 0 RA Port A	Bit Name	-	PA6	PA5	PA4	PA3	PA2	PA1	PA0
		Power-on	U	0	0	0	0	0	0	0
		/RESET and WDT	U	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	U	P	P	P	P	P	P	P
0X0B	Bank 0 RB IOCR5	Bit Name	IOC57	IOC56	IOC55	IOC54	IOC53	IOC52	IOC51	IOC50
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0x0C	Bank 0 RC IOCR6	Bit Name	IOC67	IOC66	IOC65	IOC64	IOC63	IOC62	IOC61	IOC60
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P

(Continuation)

Address	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0X0D	Bank 0 RD IOCR7	Bit Name	IOC77	IOC76	IOC75	IOC74	IOC73	IOC72	-	-
		Power-on	1	1	1	1	1	1	U	U
		/RESET and WDT	1	1	1	1	1	1	U	U
		Wake-up from Sleep/Idle	P	P	P	P	P	P	U	U
0x0E	Bank 0 RE OMCR	Bit Name	CPUS	IDLE	-	-	-	-	RCM1	RCM0
		Power-on	1	1	U	U	U	U	C	C
		/RESET and WDT	1	1	U	U	U	U	C	C
		Wake-up from Sleep/Idle	P	P	U	U	U	U	P	P
0x0F	Bank 0 RF EIESCR	Bit Name	EIES98	EIES76	EIES54	EIES32	EIES1	EIES0	-	-
		Power-on	1	1	1	1	1	1	U	U
		/RESET and WDT	1	1	1	1	1	1	U	U
		Wake-up from Sleep/Idle	P	P	P	P	P	P	U	U
0x10	Bank 0 R10 WUCR1	Bit Name	-	-	LVDWK	ADWK	INTWK1	INTWK0	-	-
		Power-on	U	U	0	0	0	0	U	U
		/RESET and WDT	U	U	0	0	0	0	U	U
		Wake-up from Sleep/Idle	U	U	P	P	P	P	U	U
0x11	Bank 0 R11 WUCR2	Bit Name	-	-	-	-	SPIWK	I^2CWK	-	-
		Power-on	U	U	U	U	0	0	U	U
		/RESET and WDT	U	U	U	U	0	0	U	U
		Wake-up from Sleep/Idle	U	U	U	U	P	P	U	U
0x12	Bank 0 R12 WUCR3	Bit Name	ICWKP8	ICWKP7	ICWKP6	ICWKP5	INTWK 98	INTWK 76	INTWK 54	INTWK 32
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X14	Bank 0 R14 SFR1	Bit Name	-	-	LVDSF	ADSF	EXSF1	EXSF0	WTSF	TCSF
		Power-on	U	U	0	0	0	0	0	0
		/RESET and WDT	U	U	0	0	0	0	0	0
		Wake-up from Sleep/Idle	U	U	P	P	P	P	P	P

(Continuation)

Address	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0X15	Bank 0 R15 SFR2	Bit Name	-	-	UERRSF	URSF	UTSF	TC3SF	TC2SF	TC1SF
		Power-on	U	U	0	0	0	0	0	0
		/RESET and WDT	U	U	0	0	0	0	0	0
		Wake-up from Sleep/Idle	U	U	P	P	P	P	P	P
0X17	Bank 0 R17 SFR4	Bit Name	P8ICSF	P7ICSF	P6ICSF	P5ICSF	SPISF	I^2CSTPSF	I^2CRSF	I^2CTSF
		Power-on	U	U	U	U	0	0	0	0
		/RESET and WDT	U	U	U	U	0	0	0	0
		Wake-up from Sleep/Idle	U	U	U	U	P	P	P	P
0X18	Bank 0 R18 SFR5	Bit Name	EXSF9	EXSF8	EXSF7	EXSF6	EXSF5	EXSF4	EXSF3	EXSF2
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X1B	Bank 0 R1B IMR1	Bit Name	-	-	LVDIE	ADIE	EXIE1	EXIE0	WTIE	TCIE
		Power-on	U	U	0	0	0	0	0	0
		/RESET and WDT	U	U	0	0	0	0	0	0
		Wake-up from Sleep/Idle	U	U	P	P	P	P	P	P
0X1C	Bank 0 R1C IMR2	Bit Name	-	-	UERRSF	URIE	UTIE	TC3IE	TC2IE	TC1IE
		Power-on	U	U	0	0	0	0	0	0
		/RESET and WDT	U	U	0	0	0	0	0	0
		Wake-up from Sleep/Idle	U	U	P	P	P	P	P	P
0X1E	Bank 0 R1E IMR4	Bit Name	P8ICIE	P7ICIE	P6ICIE	P5ICIE	SPIIE	I^2CSTPIE	I^2CRIE	I^2CTIE
		Power-on	U	U	U	U	0	0	0	0
		/RESET and WDT	U	U	U	U	0	0	0	0
		Wake-up from Sleep/Idle	U	U	U	U	P	P	P	P
0X1F	Bank 0 R1F IMR5	Bit Name	EXIE9	EXIE8	EXIE7	EXIE6	EXIE5	EXIE4	EXIE3	EXIE2
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P

(Continuation)

Address	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0X21	Bank 0 R21 WDTCR	Bit Name	WDTE	-	-	-	PSWE	WPSR2	WPSR1	WPSR0
		Power-on	0	U	U	U	0	0	0	0
		/RESET and WDT	0	U	U	U	0	0	0	0
		Wake-up from Sleep/Idle	P	U	U	U	P	P	P	P
0X22	Bank 0 R22 TCCR	Bit Name	-	TCCS	TS	TE	PSTE	TPSR2	TPSR1	TPSR0
		Power-on	U	0	0	0	0	0	0	0
		/RESET and WDT	U	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	U	P	P	P	P	P	P	P
0X23	Bank 0 R23 TCCD	Bit Name	TCC7	TCC6	TCC5	TCC4	TCC3	TCC2	TCC1	*TCC0*
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X24	Bank 0 R24 TC1CR1	Bit Name	TC1S	TC1RC	TC1SS1	TC1MOD	TC1FF	TC1OMS	TC1IS1	TC1IS0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X25	Bank 0 R25 TC1CR2	Bit Name	TC1M2	TC1M1	TC1M0	TC1SS0	TC1CK3	TC1CK2	TC1CK1	TC1CK0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X26	Bank 0 R26 TC1DA	Bit Name	TC1DA7	TC1DA6	TC1DA5	TC1DA4	TC1DA3	TC1DA2	TC1DA1	TC1DA0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X27	Bank 0 R27 TC1DB	Bit Name	TC1DB7	TC1DB6	TC1DB5	TC1DB4	TC1DB3	TC1DB2	TC1DB1	TC1DB0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P

(Continuation)

Address	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0X28	Bank 0 R28 TC2CR1	Bit Name	TC2S	TC2RC	TC2SS1	-	TC2FF	TC2OMS	TC2IS1	TC2IS0
		Power-on	0	0	0	U	0	0	0	0
		/RESET and WDT	0	0	0	U	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	U	P	P	P	P
0X29	Bank 0 R29 TC2CR2	Bit Name	TC2M2	TC2M1	TC2M0	TC2SS0	TC2CK3	TC2CK2	TC2CK1	TC2CK0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X2A	Bank 0 R2A TC2DA	Bit Name	TC2DA7	TC2DA6	TC2DA5	TC2DA4	TC2DA3	TC2DA2	TC2DA1	TC2DA0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X2B	Bank 0 R2B TC2DB	Bit Name	TC2DB7	TC2DB6	TC2DB5	TC2DB4	TC2DB3	TC2DB2	TC2DB1	TC2DB0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X2C	Bank 0 R2C TC3CR1	Bit Name	TC3S	TC3RC	TC3SS1	-	TC3FF	TC3OMS	TC3IS1	TC3IS0
		Power-on	0	0	0	U	0	0	0	0
		/RESET and WDT	0	0	0	U	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	U	P	P	P	P
0X2D	Bank 0 R2D TC3CR2	Bit Name	TC3M2	TC3M1	TC3M0	TC3SS0	TC3CK3	TC3CK2	TC3CK1	TC3CK0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X2E	Bank 0 R2E TC3DA	Bit Name	TC3DA7	TC3DA6	TC3DA5	TC3DA4	TC3DA3	TC3DA2	TC3DA1	TC3DA0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P

(Continuation)

Address	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0X2F	Bank 0 R2F TC3DB	Bit Name	TC3DB7	TC3DB6	TC3DB5	TC3DB4	TC3DB3	TC3DB2	TC3DB1	TC3DB0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X30	Bank 0 R30 I^2CCR1	Bit Name	Strobe/ Pend	IMS	ISS	STOP	SAR_ EMPTY	ACK	FULL	EMPTY
		Power-on	0	0	0	0	1	0	0	1
		/RESET and WDT	0	0	0	0	1	0	0	1
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X31	Bank 0 R31 I^2CCR2	Bit Name	I^2CBF	GCEN	-	BBF	I^2CTS1	I^2CTS0	-	I^2CEN
		Power-on	0	0	U	0	0	0	U	0
		/RESET and WDT	0	0	U	0	0	0	U	0
		Wake-up from Sleep/Idle	P	P	U	P	P	P	U	P
0X32	Bank 0 R32 I^2CSA	Bit Name	SA6	SA5	SA4	SA3	SA2	SA1	SA0	IRW
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X33	Bank 0 R33 I^2CDB	Bit Name	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X34	Bank 0 R34 I^2CDAL	Bit Name	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X35	Bank 0 R35 I^2CDAH	Bit Name	-	-	-	-	-	-	DA9	DA8
		Power-on	U	U	U	U	U	U	1	1
		/RESET and WDT	U	U	U	U	U	U	1	1
		Wake-up from Sleep/Idle	U	U	U	U	U	U	P	P

(Continuation)

Address	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0X36	Bank 0 R36 SPICR	Bit Name	CES	SPIE	SRO	SSE	SDOC	SBRS2	SBRS1	SBRS0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X37	Bank 0 R37 SPIS	Bit Name	DORD	TD1	TD0	-	OD3	OD4	-	RBF
		Power-on	0	0	0	U	0	0	U	0
		/RESET and WDT	0	0	0	U	0	0	U	0
		Wake-up from Sleep/Idle	P	P	P	U	P	P	U	P
0X38	Bank 0 R38 SPIR	Bit Name	SRB7	SRB6	SRB5	SRB4	SRB3	SRB2	SRB1	SRB0
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X39	Bank 0 R39 SPIW	Bit Name	SWB7	SWB6	SWB5	SWB4	SWB3	SWB2	SWB1	SWB0
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X3E	Bank 0 R3E ADCR1	Bit Name	CKR2	CKR1	CKR0	ADRUN	ADP	ADOM	SHS1	SHS0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X3F	Bank 0 R3F ADCR2	Bit Name	-	-	ADIM	ADCMS	VPIS1	VPIS0	VREFP	-
		Power-on	U	U	0	0	0	0	0	U
		/RESET and WDT	U	U	0	0	0	0	0	U
		Wake-up from Sleep/Idle	U	U	P	P	P	P	P	U
0X40	Bank 0 R40 ADISR	Bit Name	-	-	-	ADIS4	ADIS3	ADIS2	ADIS1	ADIS0
		Power-on	U	U	U	0	0	0	0	0
		/RESET and WDT	U	U	U	0	0	0	0	0
		Wake-up from Sleep/Idle	U	U	U	P	P	P	P	P

(Continuation)

Address	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0X41	Bank 0 R41 ADER1	Bit Name	ADE7	ADE6	ADE5	ADE4	ADE3	ADE2	ADE1	ADE0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X42	Bank 0 R42 ADER2	Bit Name	-	ADE14	ADE13	ADE12	ADE11	ADE10	ADE9	ADE8
		Power-on	U	0	0	0	0	0	0	0
		/RESET and WDT	U	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	U	P	P	P	P	P	P	P
0X43	Bank 0 R43 ADDL	Bit Name	ADD7	ADD6	ADD5	ADD4	ADD3	ADD2	ADD1	ADD0
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	U	U	U	U	U	U	U	U
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X44	Bank 0 R44 ADDH	Bit Name	ADD15	ADD14	ADD13	ADD12	ADD11	ADD10	ADD9	ADD8
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	U	U	U	U	U	U	U	U
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X45	Bank 0 R45 ADCVL	Bit Name	ADCV7	ADCV6	ADCV5	ADCV4	ADCV3	ADCV2	ADCV1	ADCV0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X46	Bank 0 R46 ADCVH	Bit Name	ADCV15	ADCV14	ADCV13	ADCV12	ADCV11	ADCV10	ADCV9	ADCV8
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X48	Bank 0 R48 LCDCR1	Bit Name	LCDEN	LCDTYPE	-	BS	DS1	DS0	LCDF1	LCDF0
		Power-on	0	0	U	0	0	0	0	0
		/RESET and WDT	0	0	U	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	U	P	P	P	P	P

(Continuation)

Address	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0X49	Bank 0 R49 LCDCR2	Bit Name	-	RBS1	RBS0	DYMEN	-	-	-	-
		Power-on	U	0	0	0	U	U	0	0
		/RESET and WDT	U	0	0	0	U	U	0	0
		Wake-up from Sleep/Idle	U	P	P	P	U	U	P	P
0X4A	Bank 0 R4A LCDCR3	Bit Name	-	-	-	-	-	LCDCC2	LCDCC1	LCDCC0
		Power-on	U	U	U	U	U	0	0	0
		/RESET and WDT	U	U	U	U	U	0	0	0
		Wake-up from Sleep/Idle	U	U	U	U	U	P	P	P
0X4B	Bank 0 R4B LCDADDR	Bit Name	-	-	-	LCDA4	LCDA3	LCDA2	LCDA1	LCDA0
		Power-on	U	U	U	0	0	0	0	0
		/RESET and WDT	U	U	U	0	0	0	0	0
		Wake-Up from Sleep/Idle	U	U	U	P	P	P	P	P
0X4C	Bank 0 R4C LCDCDB	Bit Name	LCDD7	LCDD6	LCDD5	LCDD4	LCDD3	LCDD2	LCDD1	LCDD0
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X4D	Bank 0 R4D LCDSCR0	Bit Name	-	LCDSM2	LCDSM1	LCDSM0	-	LCDCM2	LCDCM1	LCDCM0
		Power-on	U	0	0	0	U	0	0	0
		/RESET and WDT	U	0	0	0	U	0	0	0
		Wake-up from Sleep/Idle	U	P	P	P	U	P	P	P
0X4E	Bank 0 R4E LCDSCR1	Bit Name	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1	SEG0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X4F	Bank 0 R47 LCDSCR2	Bit Name	SEG15	SEG14	SEG13	SEG12	SEG11	SEG10	SEG9	SEG8
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P

(Continuation)

Address	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0X05	Bank 1 R5 IOCR8	Bit Name	IOC87	IOC86	IOC85	IOC84	IOC83	IOC82	IOC81	IOC80
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X06	Bank 1 R6 IOCR9	Bit Name	IOC97	IOC96	IOC95	IOC94	IOC93	IOC92	IOC91	IOC90
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X07	Bank 1 R7 IOCRA	Bit Name	-	IOCA6	IOCA5	IOCA4	IOCA3	IOCA2	IOCA1	IOCA0
		Power-on	U	1	1	1	1	1	1	1
		/RESET and WDT	U	1	1	1	1	1	1	1
		Wake-up from Sleep/Idle	U	P	P	P	P	P	P	P
0X08	Bank 1 R8 P5PHCR	Bit Name	PH57	PH56	PH55	PH54	PH53	PH52	PH51	PH50
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X09	Bank 1 R9 P6PHCR	Bit Name	PH67	PH66	PH65	PH64	PH63	PH62	PH61	PH60
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X0A	Bank 1 RA P789APHCR	Bit Name	PAHPH	PALPH	P9HPH	P9LPH	P8HPH	P8LPH	P7HPH	P7LPH
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X0B	Bank 1 RB P5PLCR	Bit Name	PL57	PL56	PL55	PL54	PL53	PL52	PL51	PL50
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P

(Continuation)

Address	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0X0C	Bank 1 RC P6PLCR	Bit Name	PL67	PL66	PL65	PL64	PL63	PL62	PL61	PL60
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X0D	Bank 1 RD P789APLCR	Bit Name	PAHPL	PALPL	P9HPL	P9LPL	P8HPL	P8LPL	P7HPL	P7LPL
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X0E	Bank 1 RE P5HDSCR	Bit Name	HDS57	HDS56	HDS55	HDS54	HDS53	HDS52	HDS51	HDS50
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X0F	Bank 1 RF P6HDSCR	Bit Name	HDS67	HDS66	HDS65	HDS64	HDS63	HDS62	HDS61	HDS60
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X10	Bank 1 R10 P789AHDSCR	Bit Name	PAHHDS	PALHDS	P9HHDS	P9LHDS	P8HHDS	P8LHDS	P7HHDS	P7LHDS
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X11	Bank 1 R11 P5ODCR	Bit Name	OD57	OD56	OD55	OD54	OD53	OD52	OD51	OD50
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X12	Bank 1 R2 P6ODCR	Bit Name	OD67	OD66	OD65	OD64	OD63	OD62	OD61	OD60
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P

(Continuation)

Address	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0X13	Bank 1 R13 P789AODCR	Bit Name	PAHOD	PALOD	P9HOD	P9LOD	P8HOD	P8LOD	P7HOD	P7LOD
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X33	Bank 1 R33 URCR	Bit Name	UINVEN	UMODE1	UMODE0	BRATE2	BRATE1	BRATE0	UTBE	TXE
		Power-on	0	0	0	0	0	0	1	0
		/RESET and WDT	0	0	0	0	0	0	1	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X34	Bank 1 R34 URS	Bit Name	URTD8	EVEN	PRE	PRERR	OVERR	FMERR	URBF	RXE
		Power-on	U	0	0	0	0	0	0	0
		/RESET and WDT	P	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X35	Bank 1 R35 URTD	Bit Name	URTD7	URTD6	URTD5	URTD4	URTD3	URTD2	URTD1	URTD0
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X36	Bank 1 R36 URRDL	Bit Name	URRD7	URRD6	URRD5	URRD4	URRD3	URRD2	URRD1	URRD0
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X37	Bank 1 R37 URRDH	Bit Name	URRD8	-	-	-	-	-	-	-
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	P	U	U	U	U	U	U	U
		Wake-up from Sleep/Idle	P	U	U	U	U	U	U	U
0X40	Bank 1 R40 WCR	Bit Name	WTE	WTSSB1	WTSSB0	-	-	-	-	-
		Power-on	0	0	0	U	U	U	U	U
		/RESET and WDT	0	0	0	U	U	U	U	U
		Wake-up from Sleep/Idle	P	P	P	U	U	U	U	U

(Continuation)

Address	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0X45	Bank 1 R45 TBPTL	Bit Name	TB7	TB6	TB5	TB4	TB3	TB2	TB1	TB0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X46	Bank 1 R46 TBPTH	Bit Name	HLB	GP1	GP0	TB12	TB11	TB10	TB9	TB8
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X47	Bank 1 R47 STKMON	Bit Name	STOV	-	-	-	STL3	STL2	STL1	STL0
		Power-on	0	U	U	U	0	0	0	0
		/RESET and WDT	0	U	U	U	0	0	0	0
		Wake-up from Sleep/Idle	P	U	U	U	P	P	P	P
0X48	Bank 1 R48 PCH	Bit Name	-	-	-	PC12	PC11	PC10	PC9	PC8
		Power-on	U	U	U	0	0	0	0	0
		/RESET and WDT	U	U	U	0	0	0	0	0
		Wake-up from Sleep/Idle	U	U	U	P	P	P	P	P
0X49	Bank 1 R49 LVDCR	Bit Name	LVDEN	LVDS2	LVDS1	LVDS0	LVDB	-	-	-
		Power-on	0	0	0	0	1	U	U	U
		/RESET and WDT	0	0	0	0	1	U	U	U
		Wake-up from Sleep/Idle	P	P	P	P	P	U	U	U

0X50 ~ 0X7F	Bank 0 R50~R7F	Bit Name	-	-	-	-	-	-	-	-
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X80 ~ 0XFF	Bank 0~3 R80~RFF	Bit Name	-	-	-	-	-	-	-	-
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P

6.5 Interrupt

The EM78P528N has 25 interrupts (11 external, 14 internal) as listed below:

Interrupt Source		Enable Condition	Int. Flag	Int. Vector	Priority
Internal/External	Reset	-	-	0	High 0
External	INT	ENI + EXIE=1	EXSF	2	1
External	Pin change	ENI +ICIE=1	ICSF	4	2
Internal	TCC	ENI + TCIE=1	TCSF	6	3
Internal	LVD	ENI+LVDEN & LVDIE=1	LVDSF	8	4
Internal	SPI	ENI + SPIIE=1	SPISF	C	5
Internal	AD	ENI + ADIE=1	ADSF	10	6
Internal	TC1(TCXDA)	ENI + TC1IE=1	TC1SF	12	7
Internal	I^2C Transmit	ENI+ I^2CTIE	I^2CTSF	1A	8
Internal	I^2C Receive	ENI+ I^2CRIE	I^2CRSF	1C	9
Internal	I^2CSTOP	ENI+ $I^2CSTPIE$	$I^2CSTPSF$	1E	10
Internal	TC2(TCXDA)	ENI + TC2IE=1	TC2SF	22	11
Internal	TC3(TCXDA)	ENI + TC3IE=1	TC3SF	28	12
Internal	UART Receive error	ENI+UERRIE=1	UERRSF	2E	13
Internal	UART Receive	ENI + URIE=1	URSF	30	14
Internal	UART Transmit	ENI + UTIE=1	UTSF	32	15
Internal	Watch timer	ENI+WTIE=1	WTSF	38	16

Bank 0 R14~R18 are the interrupt status registers that record the interrupt requests in relative flags/bits. Bank 0 R1B~R1F is the Interrupt Mask register. The global interrupt is enabled by the ENI instruction and is disabled by the DISI instruction. When one of the enabled interrupts occurs, the next instruction will be fetched from their individual address. The interrupt flag bit must be cleared by instructions before leaving the interrupt service routine and before interrupts are enabled to avoid recursive interrupts.

The flag (except ICSF bit delete) in the Interrupt Status Register is set regardless of the status of its mask bit or the execution of ENI. The RETI instruction ends the interrupt routine and enables the global interrupt (the execution of ENI).

External interrupt is equipped with digital noise rejection circuit (input pulse of less than **4 system clock time** is eliminated as noise), **but in Low XTAL oscillator (LXT) mode, the noise rejection circuit is disabled**. When an interrupt (Falling edge) is generated by the External interrupt (when enabled), the next instruction will be fetched from Address 0X02H.

Before the interrupt subroutine is executed, the contents of ACC, R3 (Bit 0~Bit 4) and R4 registers are saved by hardware. If another interrupt occurs, the ACC, R3 (Bit 0~Bit 4) and R4 registers will be replaced by the new interrupt. After the interrupt service routine is finished, ACC, R3 (Bit 0~Bit 4) and R4 are restored.

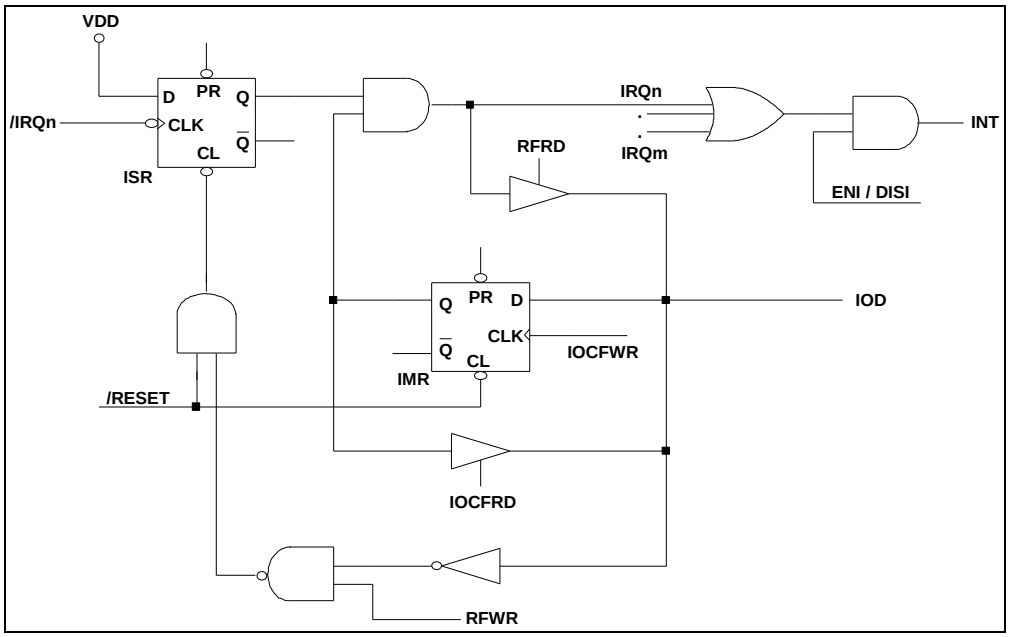


Figure 6-9a Interrupt Input Circuit

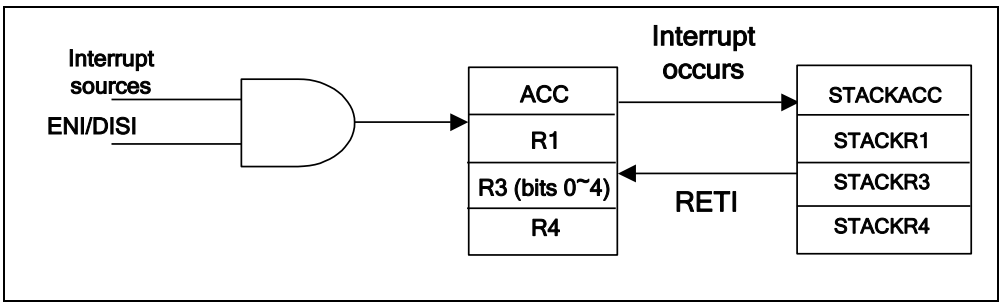


Figure 6-9b Interrupt Backup Diagram

6.6 A/D Converter

R_BANK	Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bank 0	0x3E	ADCR1	CKR2	CKR1	CKR0	ADRUN	ADP	ADOM	SHS1	SHS0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 0	0x3F	ADCR2	-	-	ADIM	ADCMS	VPIS1	VPIS0	VREFP	-
			-	-	R/W	R/W	R/W	R/W	R/W	-
Bank 0	0x40	ADISR	-	-	-	ADIS4	ADIS3	ADIS2	ADIS1	ADIS0
			-	-	-	R/W	R/W	R/W	R/W	R/W
Bank 0	0x41	ADER1	ADE7	ADE6	ADE5	ADE4	ADE3	ADE2	ADE1	ADE0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 0	0x42	ADER2	-	ADE14	ADE13	ADE12	ADE11	ADE10	ADE9	ADE8
			-	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 0	0x43	ADDL	ADD7	ADD6	ADD5	ADD4	ADD3	ADD2	ADD1	ADD0
			R	R	R	R	R	R	R	R
Bank 0	0x44	ADDH	ADD15	ADD14	ADD13	ADD12	ADD11	ADD10	ADD9	ADD8
			R	R	R	R	R	R	R	R
Bank 0	0x45	ADCVL	ADCV7	ADCV6	ADCV5	ADCV4	ADCV3	ADCV2	ADCV1	ADCV0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 0	0x46	ADCVH	ADCV15	ADCV14	ADCV13	ADCV12	ADCV11	ADCV10	ADCV9	ADCV8
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 0	0x10	WUCR2	-	-	-	ADWK	-	-	-	-
			-	-	-	R/W	-	-	-	-
Bank 0	0x15	SFR1	-	-	-	ADSF	-	-	-	-
			-	-	-	R/W	-	-	-	-
Bank 0	0x1B	IMR1	-	-	-	ADIE	-	-	-	-
			-	-	-	R/W	-	-	-	-

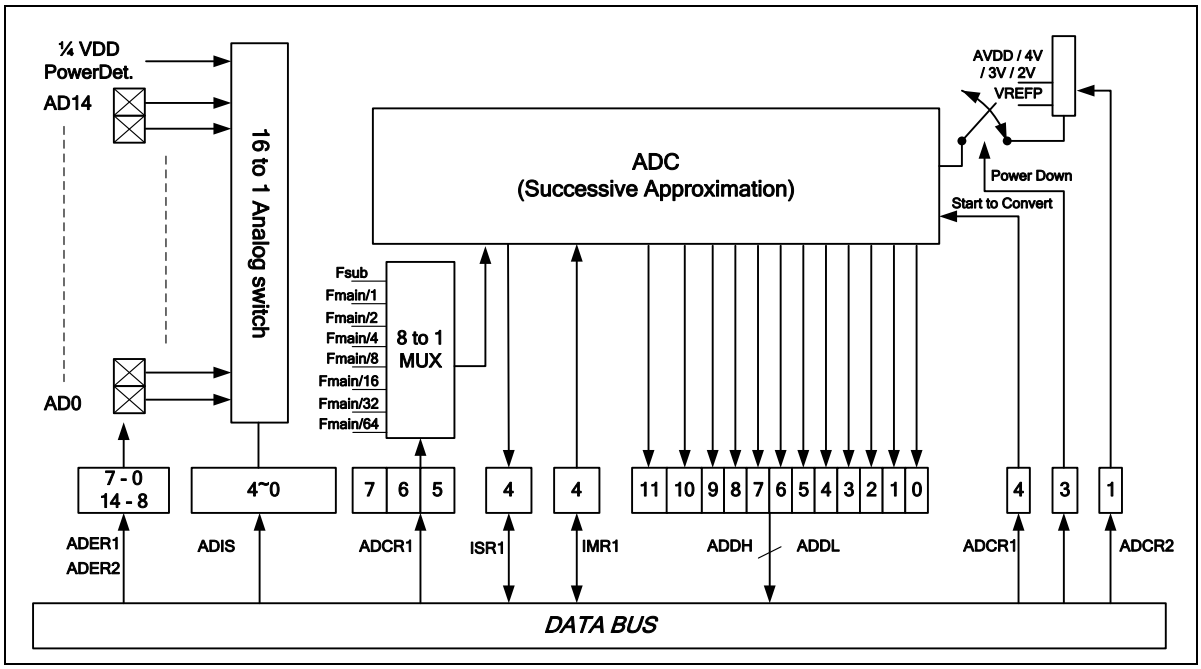


Figure 6-10 AD Converter Functional Block Diagram

This is a 12-bit successive approximation register analog-to-digital converter (SAR ADC). There are two reference voltages for SAR ADC. The positive reference voltage can select internal AVDD, internal voltage sources or external input pin by setting the VREFP and VPIS1~0 bits in ADCR2. Connecting to external positive reference voltage provides more accuracy than using internal AVDD.

6.6.1 ADC Data Register

When the AD conversion is completed, the result is loaded to the ADDH and ADDL. And the ADSF is set if ADIE is enabled.

6.6.2 A/D Sampling Time

The accuracy, linearity, and speed of the successive approximation AD converter are dependent on the properties of the ADC. The source impedance and the internal sampling impedance directly affect the time required to charge the sample and hold capacitor. The application program controls the length of the sample time to meet the specified accuracy. The maximum recommended impedance for the analog source is 10kΩ at VDD = 5V. After the analog input channel is selected; this acquisition time must be done before AD conversion can be started.

6.6.3 A/D Conversion Time

CKR2~0 select the conversion time (TAD). This allows the MCU to run at maximum frequency without sacrificing the accuracy of AD conversion. The following tables show the relationship between T_{AD} and the maximum operating frequencies. The T_{AD} is 0.5 µs for 3V~5.5V and T_{AD} is 2 µs for 2.5V~3V.

1. V_{DD} = 3V ~ 5.5V (T_{AD} is 0.5 µs)

System Mode	CKR[2:0]	Operating Clock of ADC (F_{AD} = 1 / T_{AD})	Max. F_{Main} (V_{DD} = 3V ~ 5.5V)	Conversion Time of One Word (SHS1~0 = 10*)
Normal Mode	000	F_{Main} / 16	16 MHz	21 µs
	001	F_{Main} / 8	16 MHz	10.5 µs
	010	F_{Main} / 4	8 MHz	10.5 µs
	011	F_{Main} / 2	4 MHz	10.5 µs
	100	F_{Main} / 64	16 MHz	84 µs
	101	F_{Main} / 32	16 MHz	42 µs
	110	F_{Main} / 1	2 MHz	10.5 µs
	111	F_{Sub}	32.768 kHz	640 µs
Green Mode	xxx	F_{Sub}	32.768 kHz	640 µs

* Conversion Time = Sample and Hold (SHS[1:0]=10, 8 * T_{AD}) + 12 * Bit Conversion Time (12 * T_{AD}) + Delay Time between setting ADSTART bit and starting first T_{AD}.

2. V_{DD} = 2.5V ~ 3V (T_{AD} is 2 µs)

System Mode	CKR[2:0]	Operating Clock of ADC (F_{AD} = 1 / T_{AD})	Max. F_{Main} (V_{DD} = 2.5V ~ 3V)	Conversion Time of One Word (SHS[1:0] = 10*)
Normal Mode	000	F_{Main} / 16	8 MHz	42 µs
	001	F_{Main} / 8	4 MHz	42 µs
	010	F_{Main} / 4	2 MHz	42 µs
	011	F_{Main} / 2	1 MHz	42 µs
	100	F_{Main} / 64	16 MHz	84 µs
	101	F_{Main} / 32	16 MHz	42 µs
	110	F_{Main} / 1	0.5 MHz	42 µs
	111	F_{Sub}	32.768 kHz	640 µs
Green Mode	xxx	F_{Sub}	32.768 kHz	640 µs

* Conversion Time = Sample and Hold (SHS[1:0]=10, 8 * T_{AD}) + 12 * Bit Conversion Time (12 * T_{AD}) + Delay Time between setting ADSTART bit and starting first T_{AD} (0.5 * T_{AD}).

6.6.4 ADC Operation during Sleep Mode

In order to obtain a more accurate ADC value and reduce power consumption, the AD conversion remains operational during sleep mode. As the SLEP instruction is executed, all the MCU operations will stop except for the Oscillator, TCC, TC1~3 and AD conversion.

The AD Conversion is considered completed as determined by:

1. The ADRUN bit of the Bank 0-R3E register is cleared to “0”.
2. The ADSF bit of the Bank 0-R15 register is set to “1”.
3. The ADWK bit of the Bank 0-R10 register is set to “1”. Wakes up from ADC conversion (where it remains in operation during sleep mode).
4. Wake up and execution of the next instruction if the ADIE bit of the Bank 0-R1B is enabled and the “DISI” instruction is executed.
5. Wake up and enters into Interrupt vector if the ADIE bit of Bank 0-R1B is enabled and the “ENI” instruction is executed.
6. Enters into an Interrupt vector if the ADIE bit of the Bank 0-R1B is enabled and the “ENI” instruction is executed.

The results are fed into the ADDL and ADDH registers when the conversion is completed. If the ADWK is enabled, the device will wake up. Otherwise, the AD conversion will be shut off, no matter what the status of the ADPD bit is.

6.6.5 Programming Process/Considerations

Follow these steps to obtain data from the ADC:

1. Write to the 15 bits (ADE14~0) on the Bank 0-R41~R42 (ADER1~2) register to define the characteristics of P60~P61, P63~P67, P72~P73 and P90~P95 (digital I/O, analog channels, or voltage reference pin)
2. Write to the Bank 0-R3E/ADCON register to configure the AD module:
   a) Select the ADC input channel (ADIS4~0)
   b) Define the AD conversion clock rate (CKR2~0)
   c) Select the VREFS input source of the ADC
   d) Set the ADPD bit to “**1**” to begin sampling
3. Set the ADWK bit, if the wake-up function is employed
4. Set the ADIE bit, if the interrupt function is employed
5. Write “ENI” instruction, if the interrupt function is employed

6. Set the ADRUN bit to **"1"**
7. Write "SLEP" instruction or Polling.
8. Wait for either Wake-up or for the ADRUN bit to be cleared to "**0**" , and the Status flag (ADSF) is set "**1**", or ADC interrupt occurs.
9. Read the ADDL and ADDH conversion data registers. If the ADC input channel changes at this time, the ADDL and ADDH values can be cleared to "**0**".
10. Clear the status flag (ADSF).
11. For next conversion, go to Step 1 or Step 2 as required. At least two T_{AD} are required before the next acquisition starts. On the other hand, the timing setting ADRUN = 1 must be later than the timing setting ADPD=1, and the difference between the two timing is also two T_{AD}.

NOTE
In order to obtain accurate values, it is necessary to avoid any data transition on the I/O pins during AD conversion

6.6.6 Programming Process for Detecting Internal VDD

VDD is detected within the operation, as described in the previous section the difference is that before starting the ADC conversion, the first detection of VDD is ready. Therefore in Detecting VDD:

It should be noted that before starting the AD conversion operation, the channel has to be switched to 1/4VDD channel, the voltage divider is started, then AD can be converted. Several points to note is that, precise conversion values can be added in the VDD Pin capacitance, or more than twice the conversion, taking the average or the last few strokes data in order to increase the reliability of the data.

Note that usually before VDD is detected, do not switch the channel to 1/4VDD channel, as it has always been a DC current consumption, must be switched to another channel analog multiplexer, and it will be shut out of the resistor divider, which requires user attention.

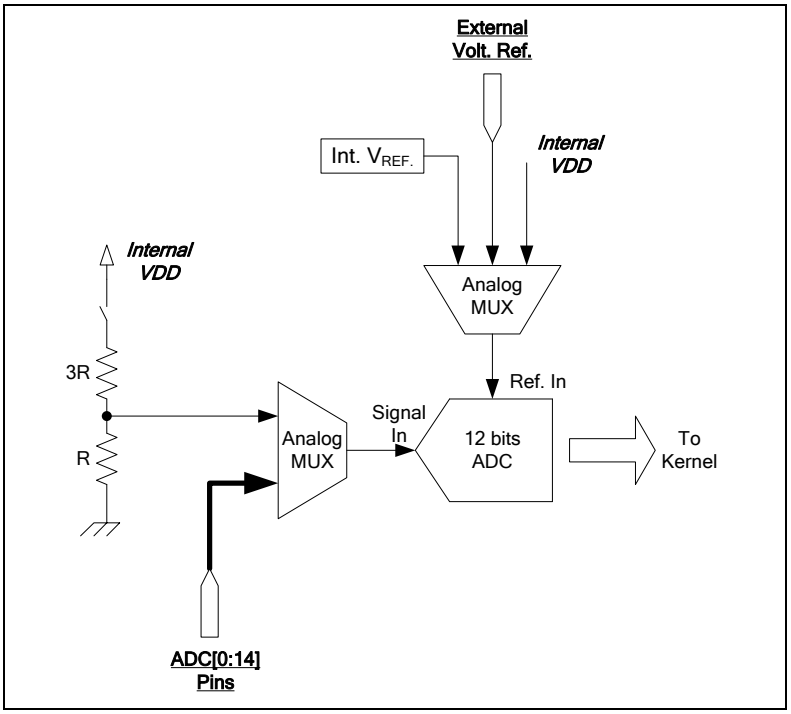


Figure 6-11 ADC and VDD Detection Block Diagram

6.6.7 Sample Demo Programs

A. Define System Control Registers

```
IAR   == 0X00    ; Indirect addressing register
SR    == 0X03    ; Status register
WUCR2 == 0x10    ; Wakeup Control Register 2
SFR1  == 0x15    ; Status Flag Register 1 of Interrupt
IMR1  == 0x1B    ; Interrupt Mask Register 1
```

B. Define I/O Control Registers

```
PORT6 == 0X06
PORT7 == 0X07
PORT9 == 0X09
IOCR6 == 0x0C    ; I/O Control Register of Port 6
IOCR7 == 0x0D    ; I/O Control Register of Port 7
IOCR9 == 0x06    ; I/O Control Register of Port 9(Bank 1)
```

C. ADC Control Register

```
ADCR1 == 0x3E    ;  7     6     5     4     3     2     1     0
                 ; CKR1  CKR1  CKR0 ADRUN  ADP   ADOM  SHS1 SHS0
ADISR == 0x40    ; ADC input select register
ADDH  == 0x44    ; The contents are the results of ADC[11:8]
ADDL  == 0x45    ; The contents are the results of ADC[7:0]
```

D. Define Bits in ADCR1

```
ADP   == 0x3     ; Power Mode of ADC
ADRUN == 0x4     ; ADC is executed as the bit is set
```

E. Program Starts

```
ORG  0           ; Initial address
JMP  INITIAL     ;

ORG  0x12        ; ADC Interrupt vector
JMP  CLRRE
;
;(User program section)
;
CLRRE:
MOV  A, SFR1
AND  A, @0BXXX0XXXX ; To clear the ADSF bit, "X" by application
MOV  SFR1, A
BS   ADCR1, ADRUN   ; To start to execute the next AD conversion
                    ; if necessary
RETI

INITIAL:
MOV  A, @0B00000001 ; To define P73 as an analog input
MOV  ADISR, A
MOV  A, @0B00001000 ; To select P73 as an analog input channel, and
                      AD power on
```

```
MOV   ADCR1, A        ; To define P73 as an input pin and set clock
                        rate at fosc/16


En_ADC:
MOV   A, @0BXXXX1XXX ; To define P73 as an input pin, and the others
                     ; are dependent on applications
MOV   IOCR7, A

MOV   A, @0BXXX1XXXX ; Enable the ADWE wake-up function of ADC, "X"
                     ; by application
MOV   WUCR2, A
MOV   A, @0BXXX1XXXX ; Enable the ADIE interrupt function of ADC,
                     ; "X" by application
MOV   IMR1, A
ENI                  ; Enable the interrupt function

BS   ADCON, ADRUN    ; Start to run the ADC

; If the interrupt function is employed, the following three lines
may be ignored

;If Sleep:
SLEP
;
;(User program section)
;

or
;If Polling:
POLLING:
JBC   ADCR1, ADRUN   ; To check the ADRUN bit continuously;
JMP   POLLING        ; ADRUN bit will be reset as the AD conversion
                     ; is completed
;
;(User program section)
```

6.7 Timer

There are three Timers in the EM78P528N. Timer 2 and Timer 3 are 8 bits up-counter. Timer 1 can be as one 8-bit up-counter or cascaded with Timer 2 as one 16-bit up-counter. If Timer 1 is used as 16-bit up-counter, the circuit resource of Timer 2 would be used. At this time, Timer 2 cannot be used.

R_BANK	Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bank 0	0x24	TC1CR1	TC1S	TC1RC	TC1SS1	TC1MOD	TC1FF	TC1OMS	TC1IS1	TC1IS0
			R/W	R/W	R/W	R/W	R	R/W	R/W	R/W
Bank 0	0x25	TC1CR2	TC1M2	TC1M1	TC1M0	TC1SS0	TC1CK3	TC1CK2	TC1CK1	TC1CK0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 0	0x26	TC1DA	TC1DA7	TC1DA6	TC1DA5	TC1DA4	TC1DA3	TC1DA2	TC1DA1	TC1DA0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 0	0x27	TC1DB	TC1DB7	TC1DB6	TC1DB5	TC1DB4	TC1DB3	TC1DB2	TC1DB1	TC1DB0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 0	0x28	TC2CR1	TC2S	TC2RC	TC2SS1	-	TC2FF	TC2OMS	TC2IS1	TC2IS0
			R/W	R/W	R/W	-	R	R/W	R/W	R/W
Bank 0	0x29	TC2CR2	TC2M2	TC2M1	TC2M0	-	TC2CK3	TC2CK2	TC2CK1	TC2CK0
			R/W	R/W	R/W	-	R/W	R/W	R/W	R/W
Bank 0	0x3A	TC2DA	TC2DA7	TC2DA6	TC2DA5	TC2DA4	TC2DA3	TC2DA2	TC2DA1	TC2DA0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 0	0x3B	TC2DB	TC2DB7	TC2DB6	TC2DB5	TC2DB4	TC2DB3	TC2DB2	TC2DB1	TC2DB0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 0	0x3C	TC3CR1	TC3S	TC3RC	TC3SS1	-	TC3FF	TC3OMS	TC3IS1	TC3IS0
			R/W	R/W	R/W	-	R	R/W	R/W	R/W
Bank 0	0x3D	TC3CR2	TC3M2	TC3M1	TC3M0	-	TC3CK3	TC3CK2	TC3CK1	TC3CK0
			R/W	R/W	R/W	-	R/W	R/W	R/W	R/W
Bank 0	0x3E	TC3DA	TC3DA7	TC3DA6	TC3DA5	TC3DA4	TC3DA3	TC3DA2	TC3DA1	TC3DA0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 0	0x3F	TC3DB	TC3DB7	TC3DB6	TC3DB5	TC3DB4	TC3DB3	TC3DB2	TC3DB1	TC3DB0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 0	0x16	SFR2	-	-	-	-	-	TC3DIF	TC2DIF	TC1DIF
			-	-	-	-	-	F	F	F
Bank 0	0x1C	IMR2	-	-	-	-	-	TC3DIE	TC2DIE	TC1DIE
			-	-	-	-	-	R/W	R/W	R/W

6.7.1 Timer/Counter Mode

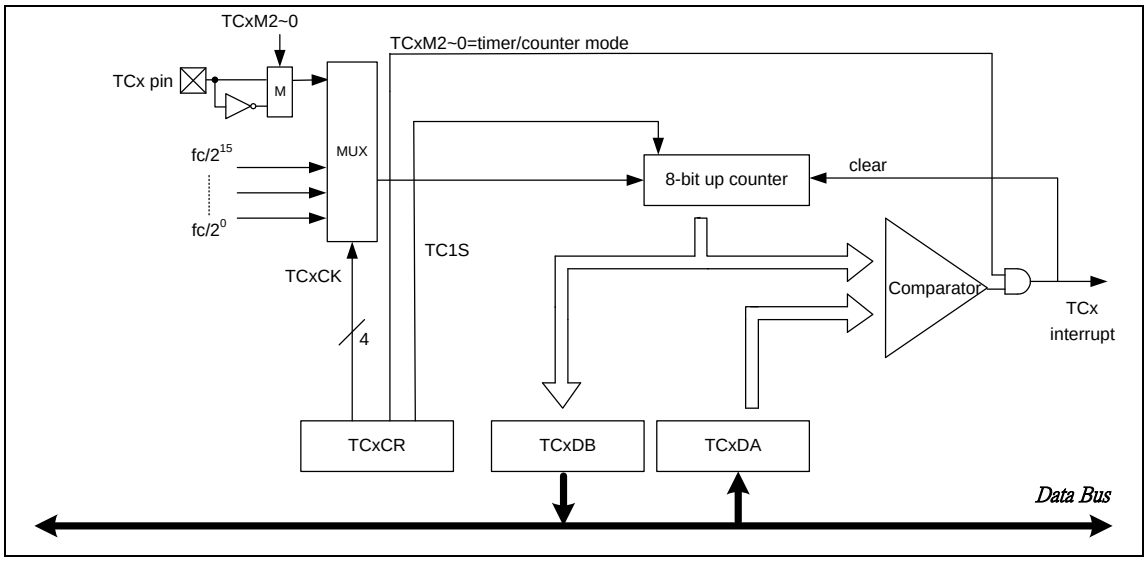


Figure 6-12a Timer/Counter Mode Block Diagram

In Timer/Counter mode, counting up is performed using internal clock or TCx pin. When the contents of the up-counter are matched with the TCxDA, then interrupt is generated and the counter is cleared. Counting up resumes after the counter is cleared. The current contents of the up-counter are loaded into TCxDB by setting TCxRC to "1".

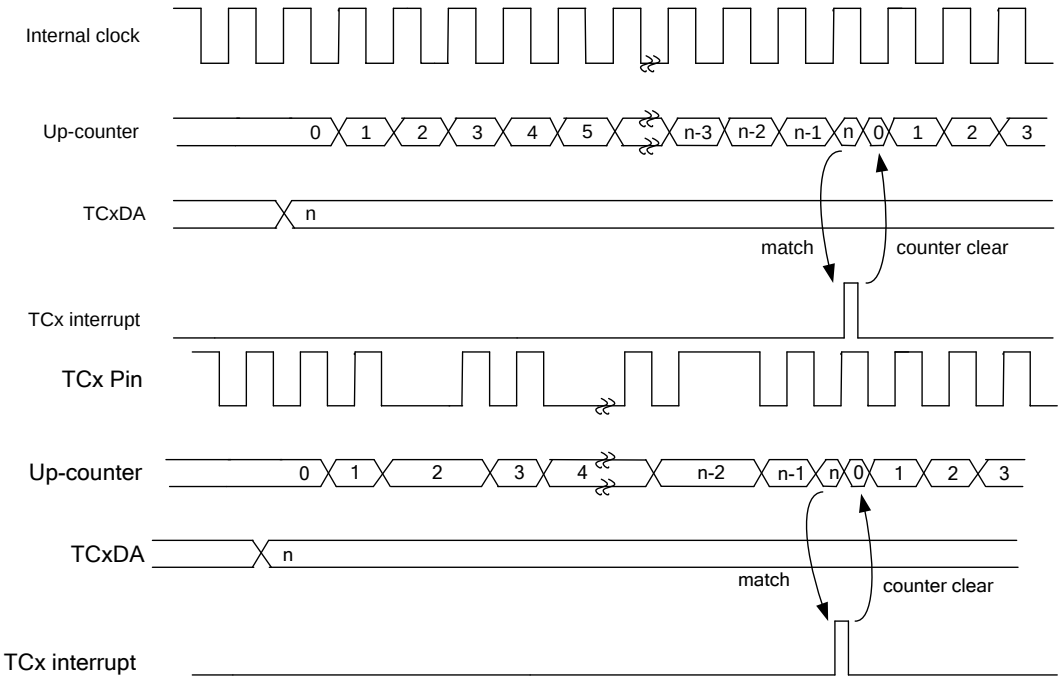


Figure 6-12b Timer/Counter Mode Waveform

6.7.2 Window Mode

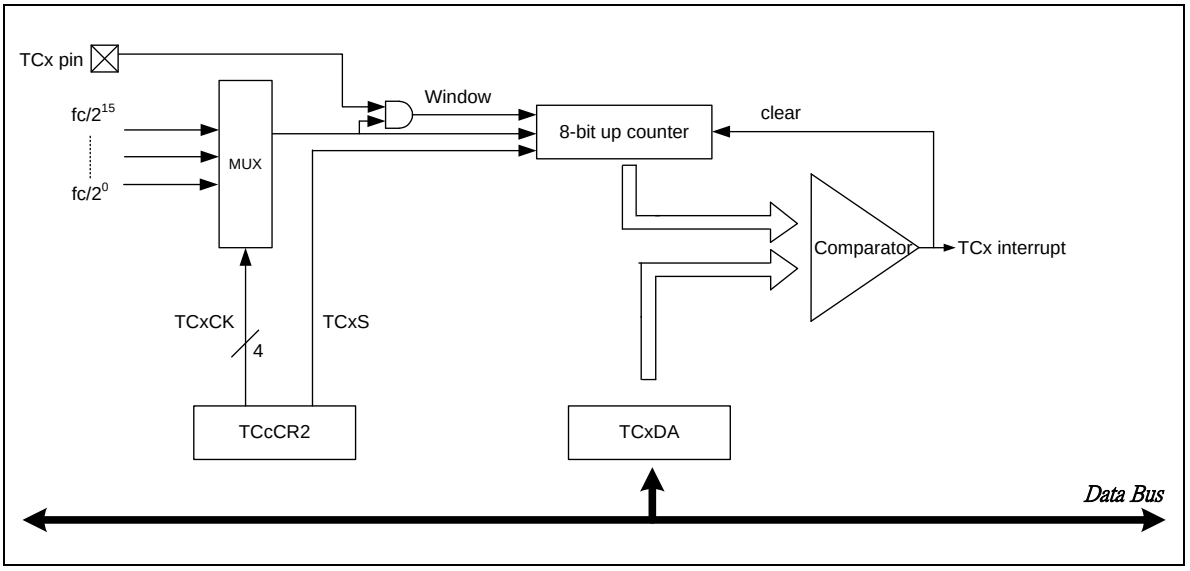


Figure 6-13a Window Mode Block Diagram

In Window mode, counting up is performed on a rising edge of the pulse that is logical AND of an internal clock and the TCx pin (window pulse). When the contents of the up-counter are matched with the TCxDA, then interrupt is generated and the counter is cleared. The frequency (window pulse) must be slower than the selected internal clock.

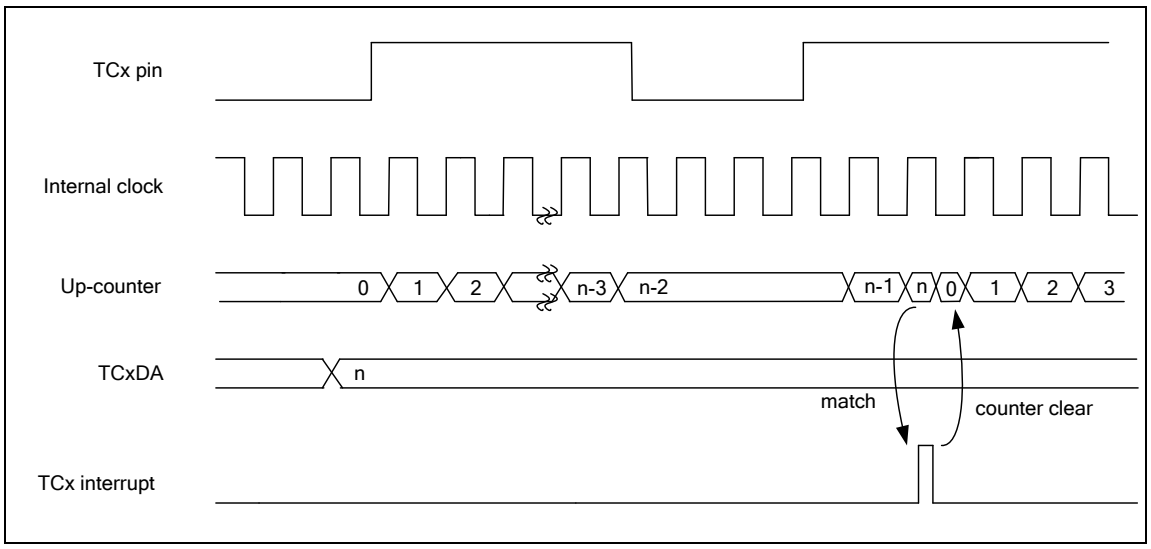


Figure 6-13b Window Mode Waveform

6.7.3 Capture Mode

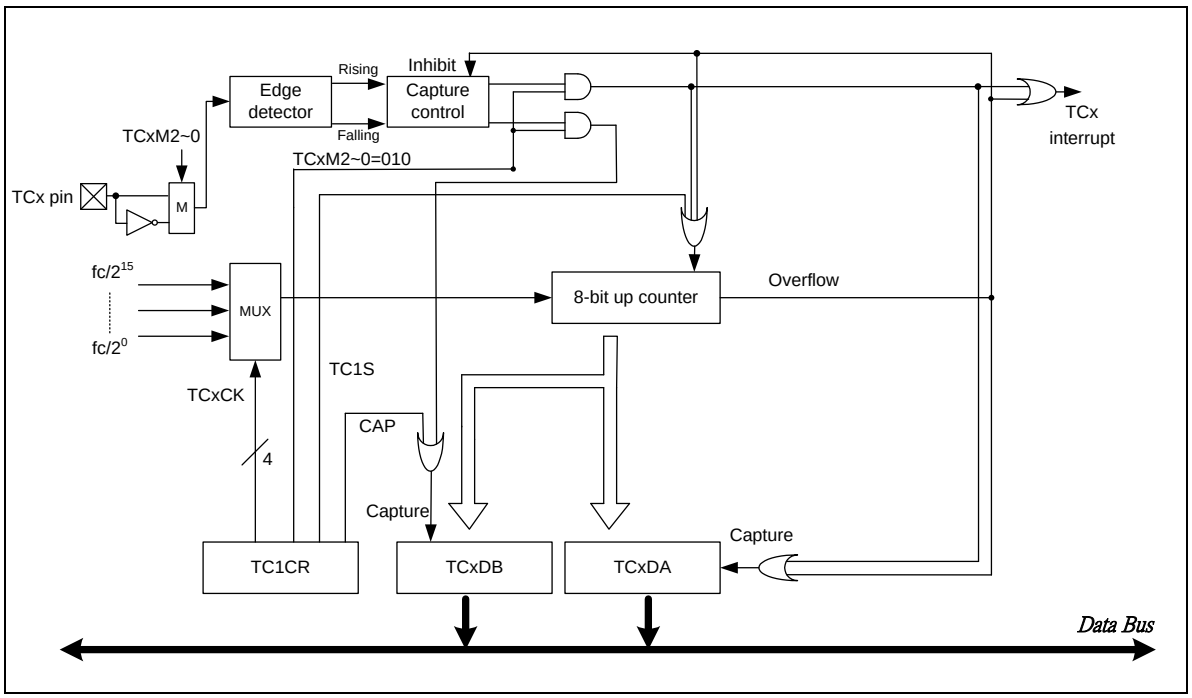


Figure 6-14a Capture Mode Block Diagram

In Capture mode, the pulse width, period and duty of the TCx input pin are measured in this mode, which can be used to decode the remote control signal. The counter is free running by the internal clock. On a rising (falling) edge of TCx pin, the contents of the counter is loaded into TCxDA, then the counter is cleared and interrupt is generated. On a falling (rising) edge of TC1 pin, the contents of the counter are loaded into TCxDB. At this time, the counter is still counting. Once the next rising edge of TCx pin is triggered, the contents of the counter are loaded into TCxDA, the counter is cleared and interrupt is generated again. If overflow before the edge is detected, the FFH is loaded into TCxDA and an overflow interrupt is generated. During interrupt processing, it can be determined whether or not there is an overflow by checking whether or not the TCxDA value is FFH. After an interrupt (capture to TCxDA or overflow detection) is generated, capture and overflow detection are halted until TCxDA is read out.

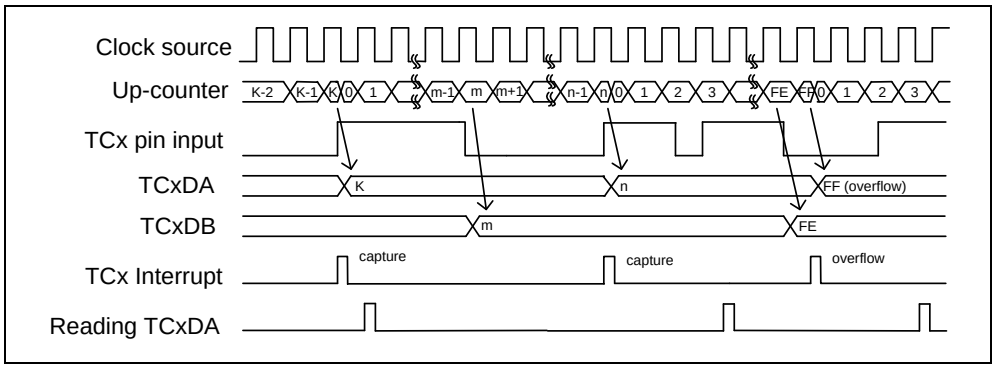


Figure 6-14b Capture Mode Waveform

6.7.4 Programmable Divider Output Mode and Pulse Width Modulation Mode

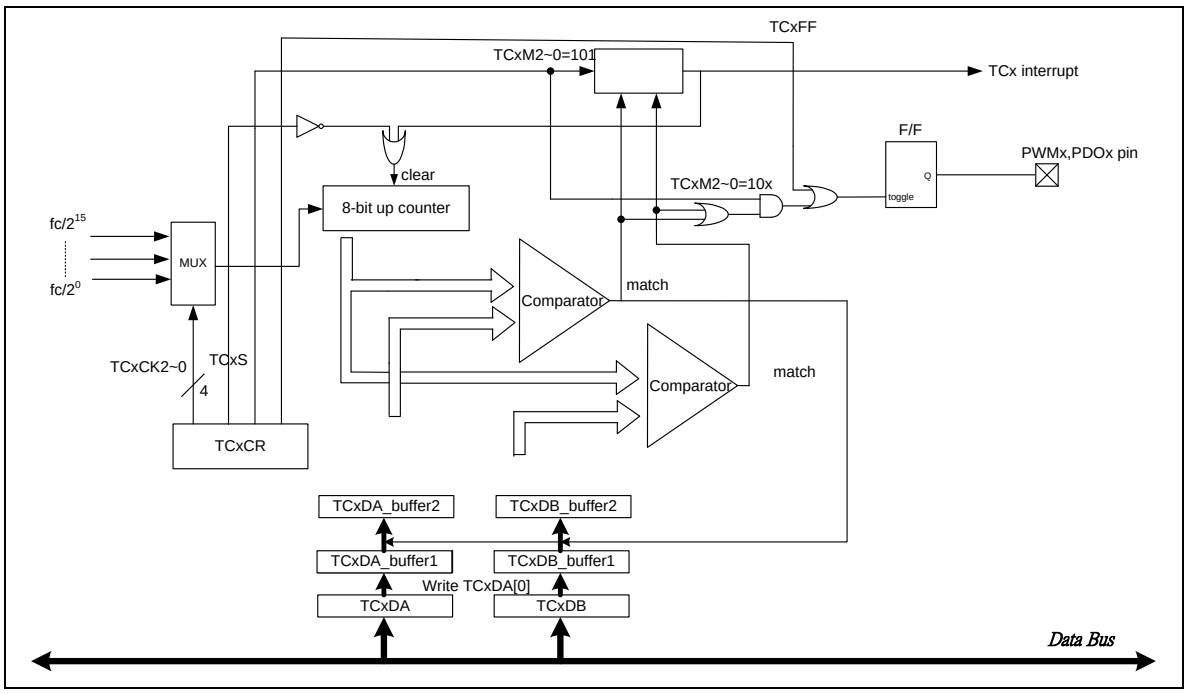


Figure 6-15a PDO/PWM Mode Block Diagram

■ **Programmable Divider Output (PDO)**

In Programmable Divider Output (PDO) mode, counting up is performed using the internal clock. The contents of TCxDA are compared with the contents of the up-counter. The F/F output is toggled and the counter is cleared each time a match is found. The F/F output is inverted and output to PDO pin. This mode can generate 50% duty pulse output. The PDO pin is initialized to "**0**" during reset. A TCx interrupt is generated each time the PDO output is toggled.

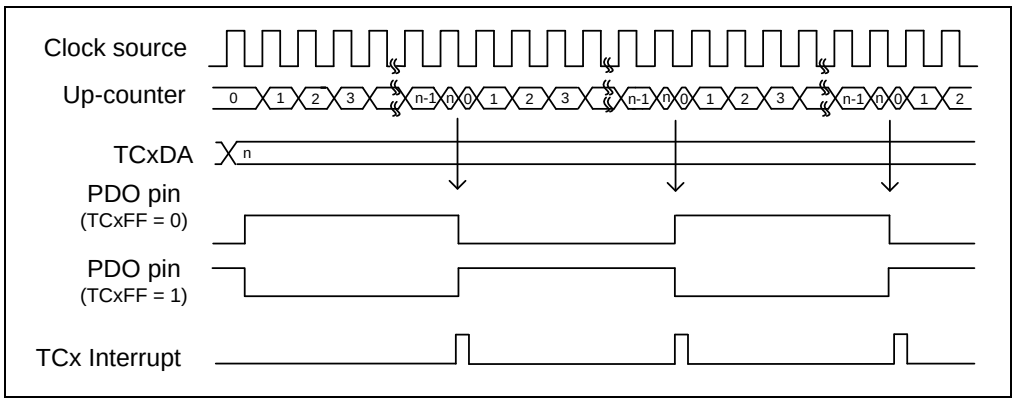


Figure 6-15b PDO Mode Waveform

- **Pulse Width Modulation (PWM)**

In Pulse Width Modulation (PWM) Output mode, counting up is performed using the internal clock with prescaler. The Duty of PWMx control by TCxDB, and the period of PWMx control by TCxDA. The pulse at the PWMx pin is held to high level as long as TCxS=1 or timerx matches TCxDA, while the pulse is held to low level as long as Timerx matches TCxDB. Once TCxFF is set to 1, the signal of PWMx is inverted. A TCx interrupt is generated and defined by TCxIS. On the other hand, the TCxDA and TCxDB can be written anytime, but the data of TCxDA and TCxDB are latched only at writing TCxDA0. Therefore, the new duty and new period of PWM appear at the PMW pin at the last period–match.

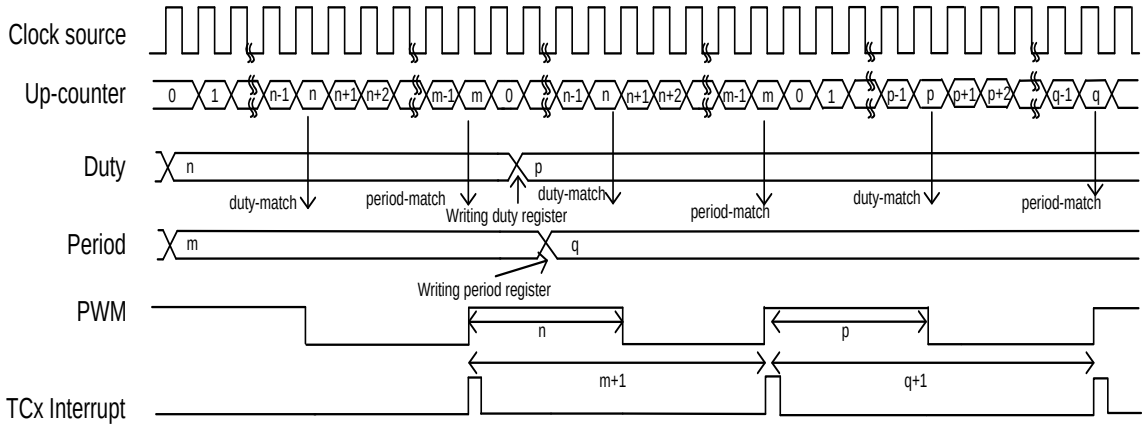


Figure 6-15c PWM Mode Waveform

6.7.5 Buzzer Mode

The TCx pin outputs the clock after dividing the frequency.

6.8 UART (Universal Asynchronous Receiver/Transmitter)

Registers for UART Circuit

R_BAN	Addr.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bank 0	0x16	SFR2	-	-	UERRSF	URSF	UTSF	-	-	-
			-	-	R/W	R/W	R/W	-	-	-
Bank 0	0x1C	IMR2	-	-	UERRIE	URIE	UTIE	-	-	-
			-	-	R/W	R/W	R/W	-	-	-
Bank 1	0X33	URCR	UINVEN	UMODE1	UMODE0	BRATE2	BRATE1	BRATE0	UTBE	TXE
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 1	0X34	URS	URTD8	EVEN	PRE	PRERR	OVERR	FMERR	URB	RXE
			W	R/W	R/W	R/W	R/W	R/W	R	R/W
Bank 1	0x35	URTD	URTD7	URTD6	URTD5	URTD4	URTD3	URTD2	URT	URT
			W	W	W	W	W	W	W	W
Bank 1	0X36	URRDL	URRD7	URRD6	URRD5	URRD4	URRD3	URRD2	URR	URR
			R	R	R	R	R	R	R	R
Bank 1	0X37	URRDH	URRD8	-	-	-	-	-	-	-
			R	-	-	-	-	-	-	-

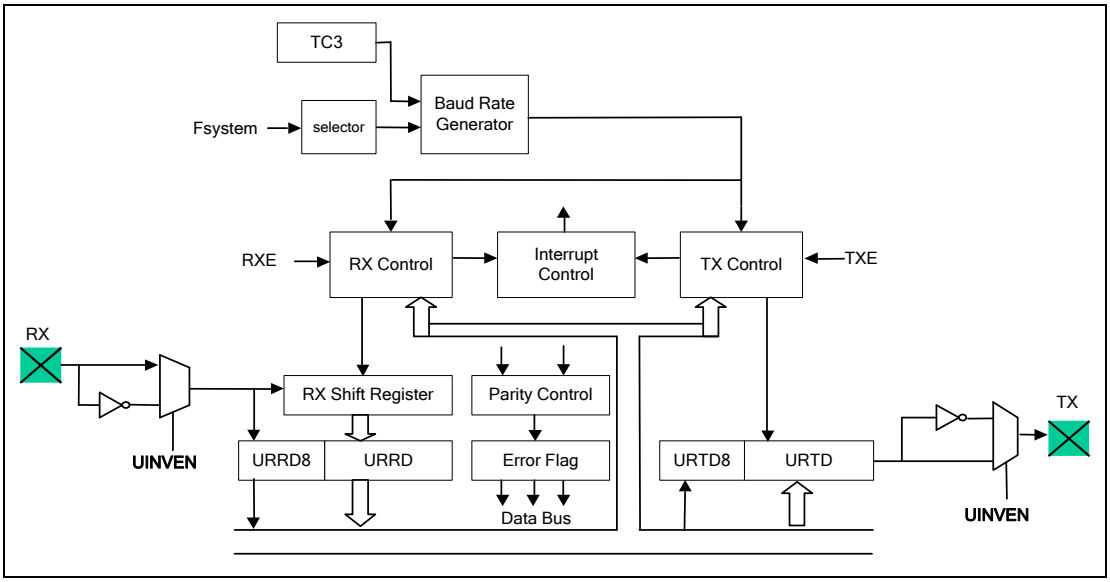


Figure 6-16 UART Functional Block Diagram

In Universal Asynchronous Receiver Transmitter (UART), each transmitted or received character is individually synchronized by framing it with a start bit and stop bit.

Full duplex data transfer is possible since the UART has independent transmit and receive sections. Double buffering for both sections allows the UART to be programmed for continuous data transfer.

The figure below shows the general format of one character sent or received. The communication channel is normally held in the marked state (high). Character transmission or reception starts with a transition to the space state (low).

The first bit transmitted or received is the start bit (low). It is followed by the data bits, in which the least significant bit (LSB) comes first. The data bits are followed by the parity bit. If present, then the stop bit or bits (high) confirm the end of the frame.

In receiving, the UART synchronizes on a falling edge of the start bit. When two or three "0" are detected during three samples, it is recognized as normal start bit and the receiving operation is started.

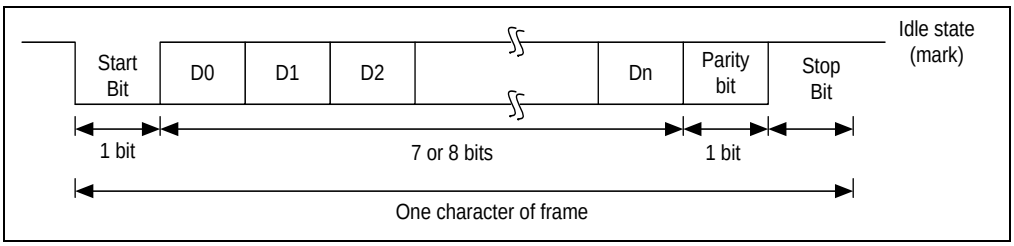


Figure 6-17 Data Format in UART

6.8.1 UART Mode

There are three UART modes. Mode 1 (7 bits data) and Mode 2 (8 bits data) allow the addition of a parity bit. The parity bit addition is not available in Mode 3. Figure 6-18a below shows the data format in each mode.

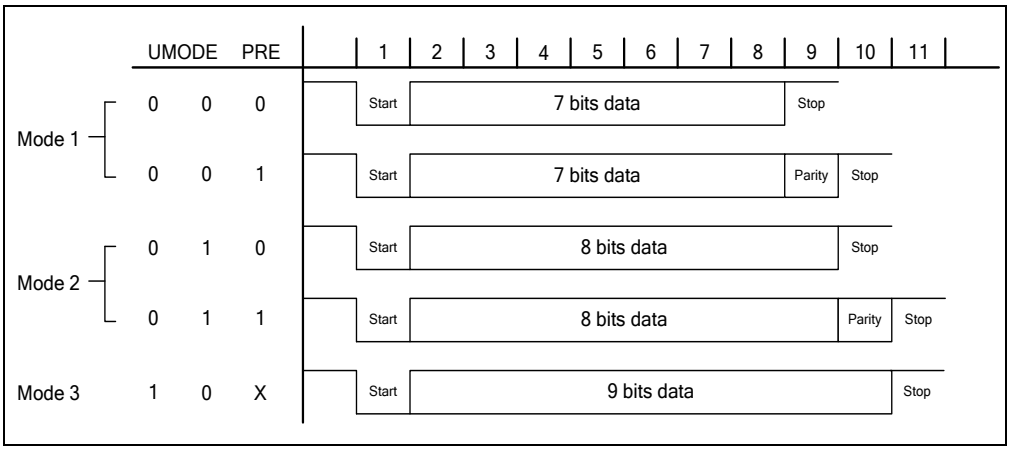


Figure 6-18a UART Model

6.8.2 Transmitting

In transmitting serial data, the UART operates as follows:

1. Set the TXE bit of the URCR1 register to enable the UART transmission function.
2. Write data into the URTD register and the UTBE bit of the URCR register will be cleared by hardware.
3. Then start transmitting.
4. Serially transmitted data are transmitted in the following order from the TX pin.
5. Start bit: one "**0**" bit is output.
6. Transmit data: 7, 8 or 9 bits data are output from the LSB to the MSB.
7. Parity bit: one parity bit (odd or even selectable) is output.
8. Stop bit: one "**1**" bit (stop bit) is output.

Mark state: output "1" continues until the start bit of the next transmitted data.

After transmitting the stop bit, the UART generates a UTSF interrupt (if enabled).

6.8.3 Receiving

In receiving, the UART operates as follows:

1. Set the RXE bit of the URS register to enable the UART receiving function. The UART monitors the RX pin and synchronizes internally when it detects a start bit.
2. Receive data is shifted into the URRD register in the order from LSB to MSB.
3. The parity bit and the stop bit are received. After one character is received, the URBF bit of the URS register will be set to "**1**". This means UART interrupt will occur.
4. The UART makes the following checks:
   (a) Parity check: The number of "1" of the received data must match the even or odd parity setting of the EVEN bit in the URS register.
   (b) Frame check: The start bit must be "0" and the stop bit must be "1".
   (c) Overrun check: The URBF bit of the URS register must be cleared (that means the URRD register should be read out) before the next received data is loaded into the URRD register.

   If any checks failed, the UERRSF interrupt will be generated (if enabled), and an error flag is indicated in PRERR, OVERR or FMERR bit. The error flag should be cleared by software, otherwise, UERRSF interrupt will occur when the next byte is received.
5. Read received data from URRD register. And URBF bit will be set by hardware.

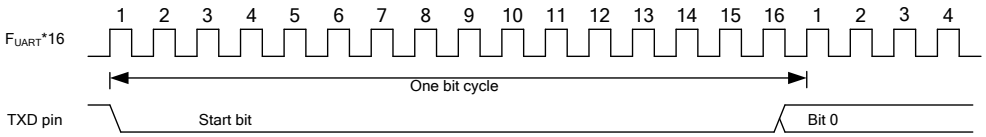
6.8.4 Baud Rate Generator

The baud rate generator is comprised of a circuit that generates a clock pulse to determine the transfer speed for transmission/reception in the UART.

The BRATE2~BRATE0 bits of the URC register can determine the desired baud rate.

6.8.5 UART Timing

1. Transmission Counter Timing:



2. Receiving Counter Timing:

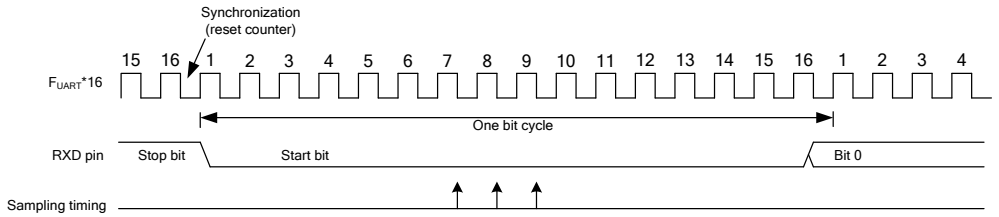


Figure 6-18b UART Timing Diagrams

6.9 SPI (Serial Peripheral Interface)

R_BANK	Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bank 0	0X36	SPICR	CES	SPIE	SRO	SSE	SDOC	SBRS2	SBRS1	SBRS0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 0	0X37	SPIS	DORD	TD1	TD0	-	OD3	OD4	-	RBF
			R/W	R/W	R/W	-	R/W	R/W	-	R
Bank 0	0X38	SPIR	SRB7	SRB6	SRB5	SRB4	SRB3	SRB2	SRB1	SRB0
			R	R	R	R	R	R	R	R
Bank 0	0X39	SPIW	SWB7	SWB6	SWB5	SWB4	SWB3	SWB2	SWB1	SWB0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 0	0X18	SFR4	-	-	-	-	SPISF	-	-	-
			-	-	-	-	R/W	-	-	-
Bank 0	0X1E	IMR4	-	-	-	-	SPIIE	-	-	-
			-	-	-	-	R/W	-	-	-

6.9.1 Overview and Feature

Overview:

Figures 6-19 and 6-20 show how the EM78P528N communicates with other devices through SPI module. If EM78P528N is a Master controller, it sends clock through the SCK pin. A couple of 8-bit data are transmitted and received at the same time. However, if the EM78P528N is defined as a Slave, its SCK pin could be programmed as an input pin. Data will continue to be shifted based on both the clock rate and the selected edge. User can also set SPIS Bit 7 (DORD) to determine the SPI transmission order, SPICR Bit 3 (SDOC) to control SDO pin after serial data output status and SPIS Bit 6 (TD1), Bit 5 (TD0) determines the SDO status output delay times.

Features:

1. Operation in either Master mode or Slave mode
2. Three-wire or four-wire full duplex synchronous communication
3. Programmable baud rates of communication
4. Programming clock polarity, (Bank 0 R36 Bit 7)
5. Interrupt flag available for the read buffer full
6. SPI transmission order
7. After serial data output SDO status select
8. SDO status output delay times
9. SPI handshake pin
10. Up to 4 MHz (maximum) bit frequency

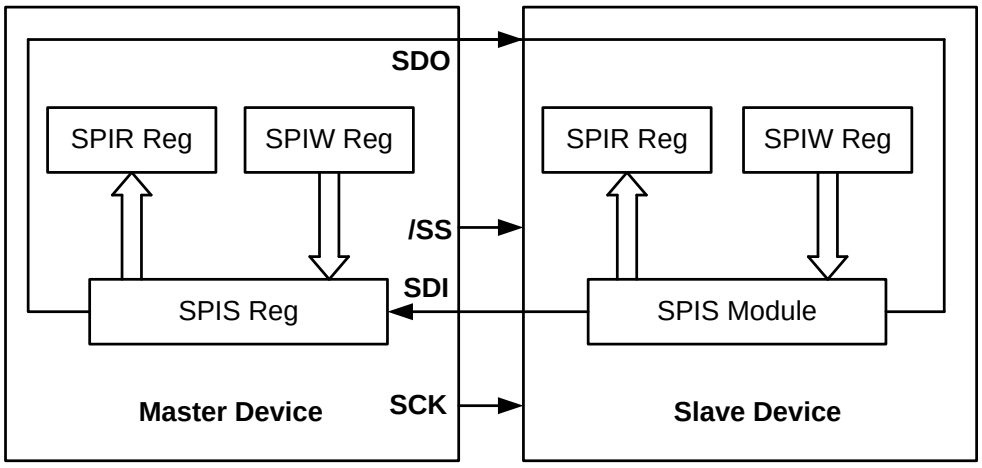


Figure 6-19 SPI Master/Slave Communication

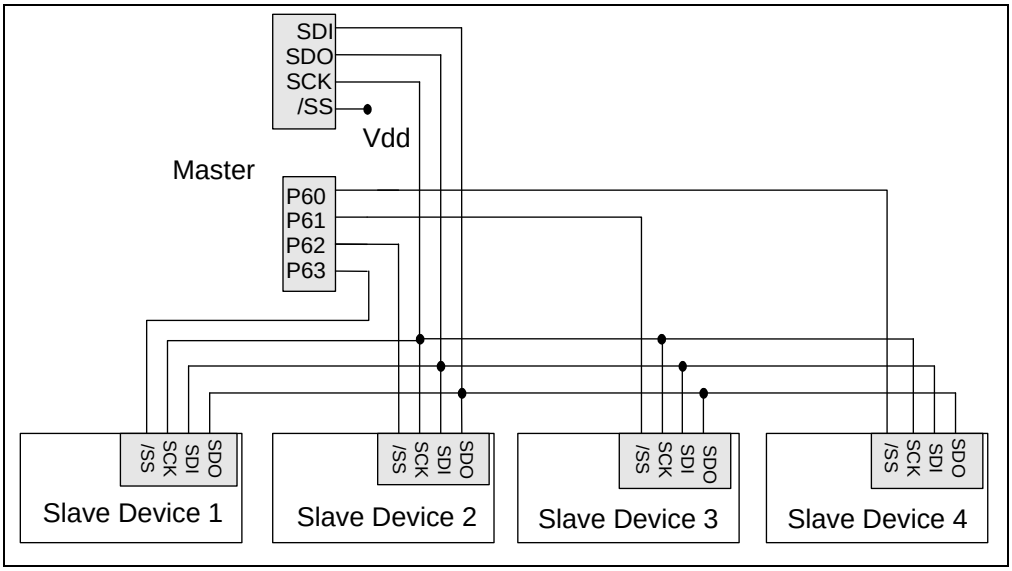


Figure 6-20 SPI Configuration of Single-Master and Multi-Slave

6.9.2 SPI Functional Description

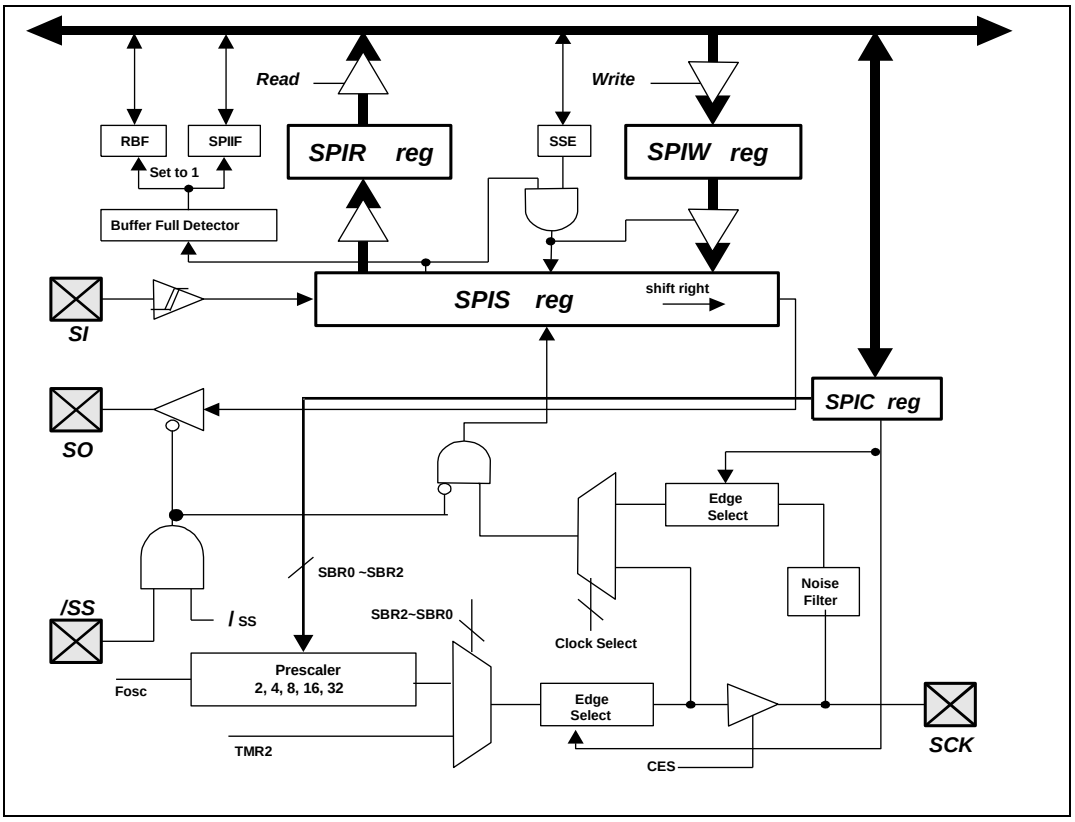


Figure 6-21 SPI Block Diagram

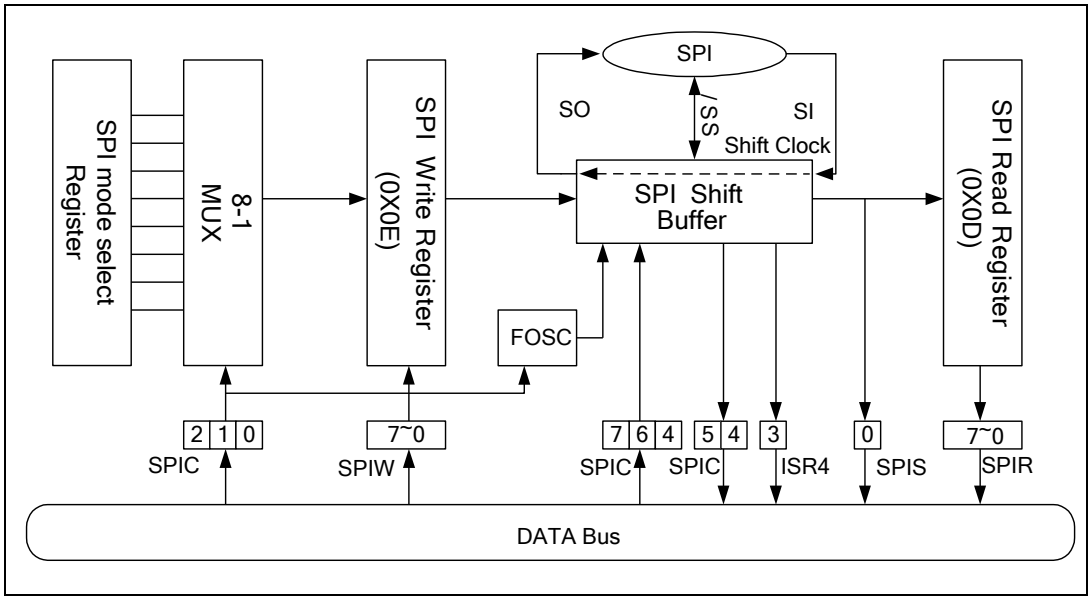


Figure 6-22 Functional Block Diagram of SPI Transmission

Below are the functions of each block and explanations on how to carry out the SPI communication with the signals depicted in Figures 6-21 and 6-22.

- P84/SDA/SI/SEG4: Serial Data In
- P85/SO/SEG5: Serial Data Out
- P86/SCL/SCK/SEG6: Serial Clock
- P87//SS/AD9/SEG8: /Slave Select (Option). This pin (/SS) may be required during a Slave mode
- RBF: Set by Buffer Full Detector
- Buffer Full Detector: Set to 1 when an 8-bit shifting is completed.
- SSE: Loads the data in SPIS register, and begin to shift
- SPIS reg.: Shifting byte in and out. The MSB is shifted first. Both the SPIR and the SPIW registers are shift at the same time. Once data are written, SPIS starts transmission / reception. The data received will be moved to the SPIR register as the shifting of the 8-bit data is completed. The RBF (Read Buffer Full) flag and the SPISF (SPI Interrupt) flag are then set.
- SPIR reg.: Read buffer. The buffer will be updated as the 8-bit shifting is completed. The data must be read before the next reception is completed. The RBF flag is cleared as the SPIR register reads.
- SPIW reg.: Write buffer. The buffer will deny any attempts to write until the 8-bit shifting is completed.

The SSE bit will be kept in “1” if the communication is still undergoing. This flag must be cleared as the shifting is completed. Users can determine if the next write attempt is available.

- SBRS2~SBRS0: Programming the clock frequency/rates and sources.
- Clock Select: Selecting either the internal or the external clock as the shifting clock.
- Edge Select: Selecting the appropriate clock edges by programming the CES bit

6.9.3 SPI Signal and Pin Description

The detailed functions of the four pins, SI, SO, SCK, and /SS are as follows:

P84/SDA/SI/SEG4:

- Serial Data In
- Receive sequentially, the Most Significant Bit (MSB) first, Least Significant Bit (LSB) last,
- Defined as high-impedance, if not selected
- Program the same clock rate and clock edge to latch on both the Master and Slave devices
- The byte received will update the transmitted byte
- The RBF will be set as the SPI operation is completed
- Timing is shown in Figures 6-23 and 6-24.

P85/SO/SEG5:

- Serial Data Out
- Transmit sequentially; the Most Significant Bit (MSB) first, Least Significant Bit (LSB) last
- Program the same clock rate and clock edge to latch on both the Master and Slave devices
- The received byte will update the transmitted byte
- The CES bit will be reset, as the SPI operation is completed
- Timing is shown in Figures 6-23 and 6-24.

P86/SCL/SCK/SEG6:

- Serial Clock
- Generated by a Master device
- Synchronize the data communication on both the SI and SO pins
- The CES is used to select the edge to communicate.
- The SBR0~SBR2 is used to determine the baud rate of communication
- The CES, SBR0, SBR1, and SBR2 bits have no effect in Slave mode
- Timing is shown in Figures 6-23 and 6-24.

P87//SS/AD9/SEG8:

- Slave Select; negative logic
- Generated by a Master device to signify the Slave(s) to receive data
- Goes low before the first cycle of SCK appears, and remains low until the last (eighth) cycle is completed
- Ignores the data on the SI and SO pins while /SS is high, because the SO is no longer driven
- Timing is shown in Figures 6-23 and 6-24.

6.9.4 SPI Mode Timing

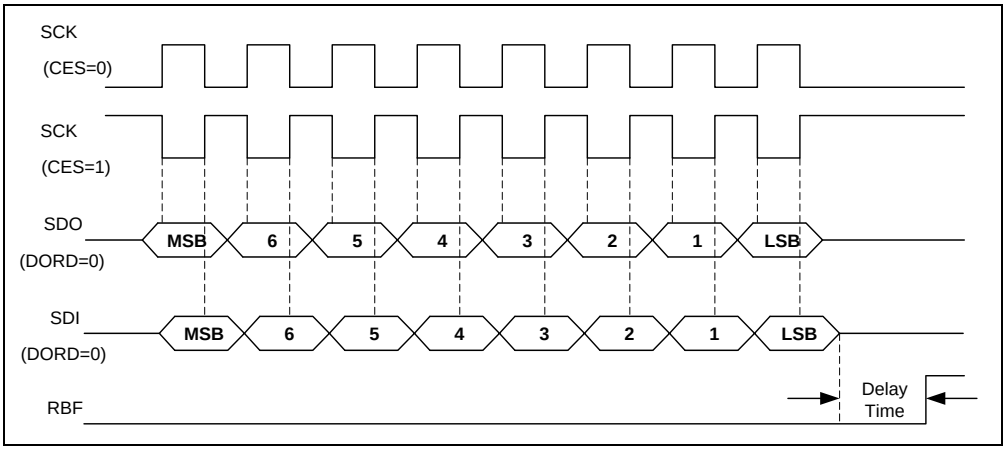


Figure 6-23 SPI Mode with /SS Disabled

The SCK edge is selected by programming bit CES. The waveform shown in Figure 6-23 is applicable regardless of whether the EM78P528N is in Master or Slave mode with /SS disabled. However, the waveform in Figure 6-24 can only be implemented in Slave mode with /SS enabled.

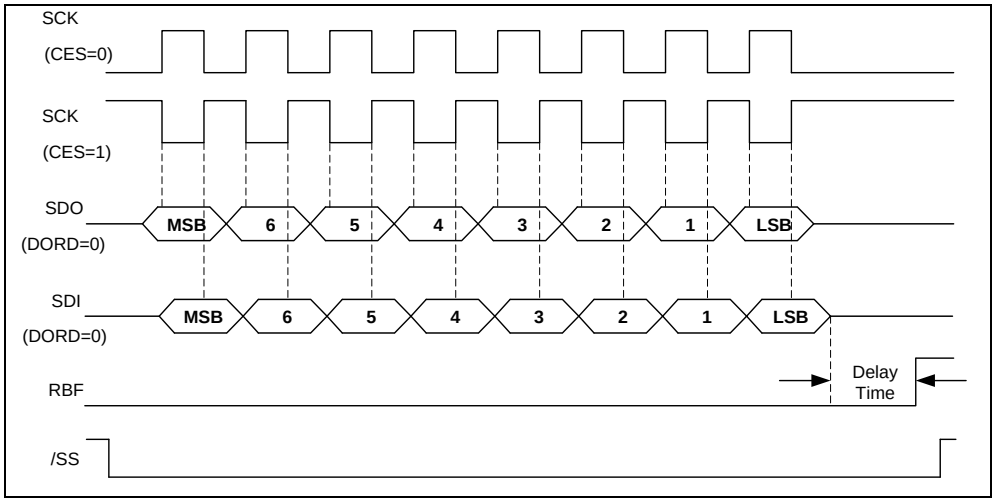


Figure 6-24 SPI Mode with /SS Enabled

6.10 I²C Function

R_BANK	Addr.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bank 0	0x30	I²CCR1	Strobe/Pend	IMS	ISS	STOP	SAR_EMPTY	ACK	FULL	EMPTY
			R/W	R/W	R/W	R/W	R	R	R	R
Bank 0	0x31	I²CCR2	I²CBF	GCEN	-	BBF	I²CTS1	I²CTS0	-	I²CEN
			R	R/W	-	R	R/W	R/W	-	R/W
Bank 0	0x32	I²CSA	SA6	SA5	SA4	SA3	SA2	SA1	SA0	IRW
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 0	0x33	I²CDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 0	0x34	I²CDAL	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 0	0x35	I²CDAH	-	-	-	-	-	-	DA9	DA8
			-	-	-	-	-	-	R/W	R/W
Bank 0	0x18	SFR4	-	-	-	-	-	I²CSTPIF	I²CRSF	I²CTSF
			-	-	-	-	-	R/W	R/W	R/W
Bank 0	0x1E	IMR4	-	-	-	-	-	I²CSTPIE	I²CRIE	I²CTIE
			-	-	-	-	-	R/W	R/W	R/W

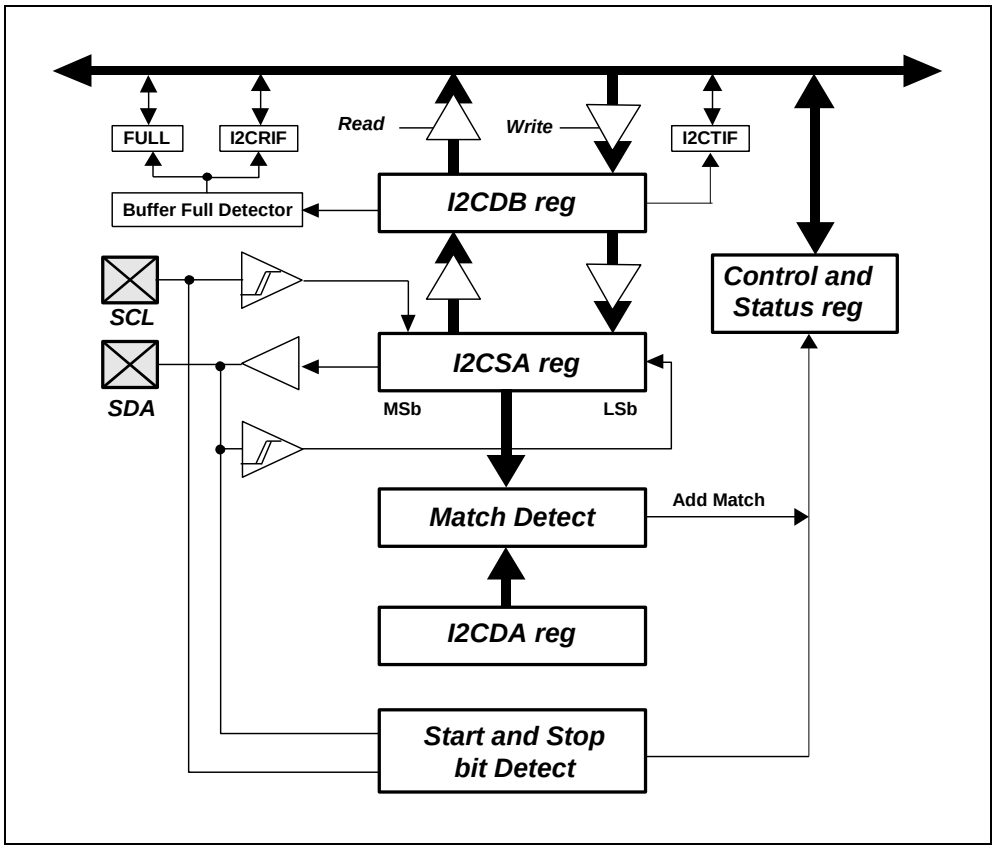


Figure 6-25 I²C Block Diagram

The EM78P528N supports a bidirectional, 2-wire bus, 7/10-bit addressing and data transmission protocol. A device that sends data onto the bus is defined as transmitter, while a device receiving data is defined as a receiver. The bus has to be controlled by a Master device which generates the Serial Clock (SCL), controls the bus access and generates the Start and Stop conditions. Both Master and Slave can operate as transmitter or receiver, but the Master device determines which mode is activated.

Both SDA and SCL are bidirectional lines, connected to a positive supply voltage via a pull-up resistor. When the bus is free, both lines are HIGH. The output stages of devices connected to the bus must have an open-drain or open-collector to perform the wired-AND function. Data on the I²C-bus can be transferred at the rates of up to 100Kbit/s in Standard mode or up to 400Kbit/sec. in Fast mode.

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW.

The I^2C Interrupt occurs as describe below:

Condition	Master/Slave	Transmit Address	Transmit Data	Stop
Master-transmitter transmits to Slave-receiver	Master	Transmit interrupt	Transmit interrupt	Stop interrupt
	Slave	Receive interrupt	Receive interrupt	Stop interrupt
Master receiver read Slave-transmitter	Master	Transmit interrupt	Receive interrupt	Stop interrupt
	Slave	Transmit interrupt	Transmit interrupt	Stop interrupt

Within the procedure of the I^2C bus, there can be unique situations which are defined as START (S) and STOP (P) conditions.

A High to Low transition on the SDA line while SCL is High is one such unique case. This situation indicates a START condition.

A Low to High transition on the SDA line while SCL is High defines a STOP condition.

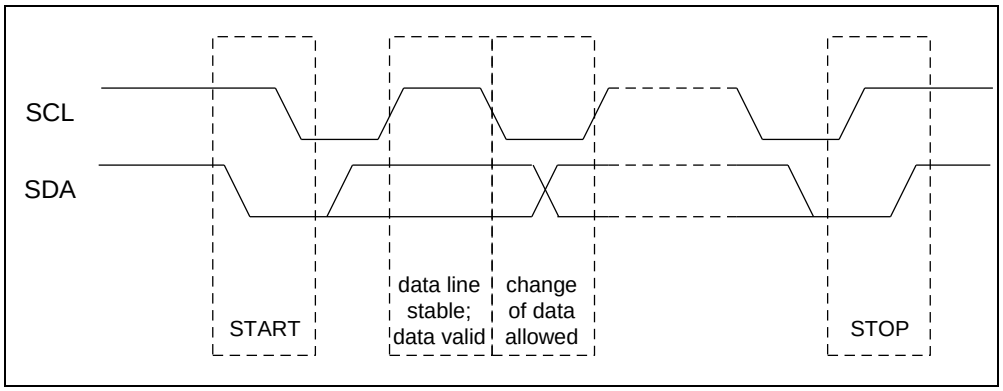


Figure 6-26 I^2C Transfer Condition

■ 7-Bit Slave Address

Master-transmitter transmits to Slave-receiver. The transfer direction is not changed.

Master reads Slave immediately after the first byte. At the moment of the first acknowledgement, the Master-transmitter becomes a Master-receiver and the Slave-receiver becomes a Slave-transmitter. This first acknowledgement is still generated by the Slave. The STOP condition is generated by the Master, which has previously sent a not-acknowledge (A). The difference between Master transmitter with Master receiver is only in R//W bit. If the R//W bit is **"0"**, the Master device is the Transmitter. Otherwise, the Master device is the Receiver. The Master-Transmitter is illustrated in Figure 6-27a "Master-Transmitter transmits to Slave–receiver with 7-Bit Slave Address", and that of the Master-Receiver is shown in Figure 6-27b "Master-Receiver Reads Slave –Transmitter with 7-Bit Slave Address".

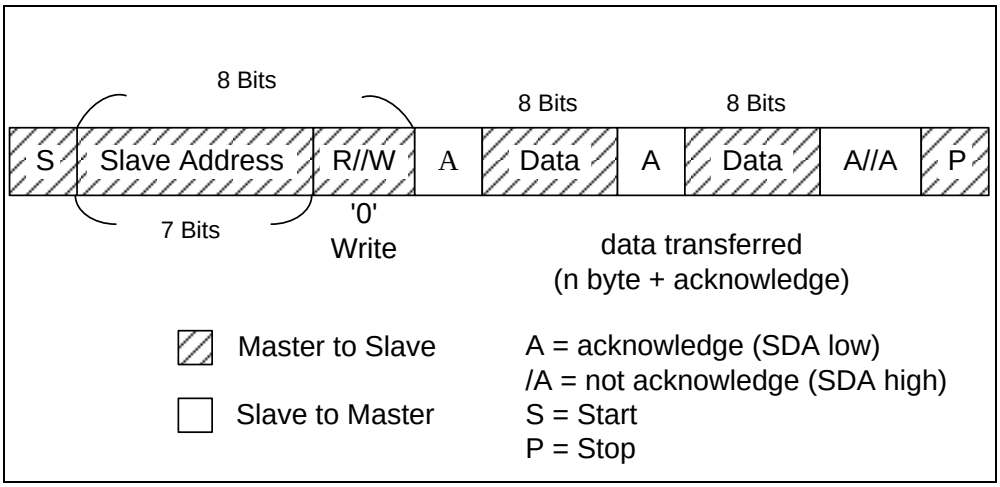


Figure 6-27a Master-Transmitter Transmits to Slave-Receiver with 7-Bit Slave Address

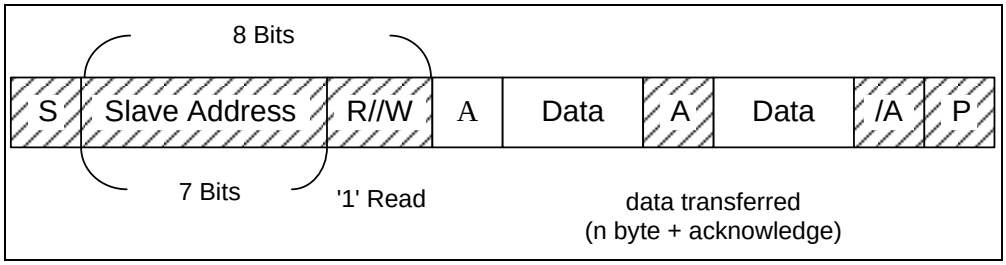


Figure 6-27b Master-Receiver Reads Slave-Transmitter with 7-Bit Slave Address

■ 10-Bit Slave Address

In 10-Bit Slave address mode, using 10 bits for addressing exploits the reserved combination 11110XX for the first seven bits of the first byte following a START (S) or repeated START (Sr) condition. The first seven bits of the first byte are the combination 11110XX of which the last two bits (XX) are the two most-significant bits of the 10-bit address. If the R/W bit is “0”, the second byte after acknowledgement would be the eight address bits of the10-bit Slave address. Otherwise, the second byte would just only be the next transmitted data from a Slave to Master device. The first bytes 11110XX are transmitted using the Slave address register (I^2CSA), and the second bytes XXXXXXXX are transmitted using the data buffer (I^2CDB).

The following explains the possible data transfer formats for 10-bit Slave address mode:

■ **Master-Transmitter Transmits to Slave-Receiver with a 10-bit Slave Address**

When the Slave receives the first byte after START bit from Master, each Slave devices will compare the seven bits of the first byte (11110XX) with their own address and the 8th bit, R//W. If the R//W bit is "0", the Slave will return the Acknowledge (A1). It is possible that more than one Slave devices will return the Acknowledge (A1). Then all Slave devices will continue to compare the second address (XXXXXXXX). If a Slave device finds a match, that particular Slave will be the only one to return an Acknowledge (A2). The matching Slave device will remain addressed by the Master until it receives a STOP condition or a repeated START condition followed by the different Slave address.

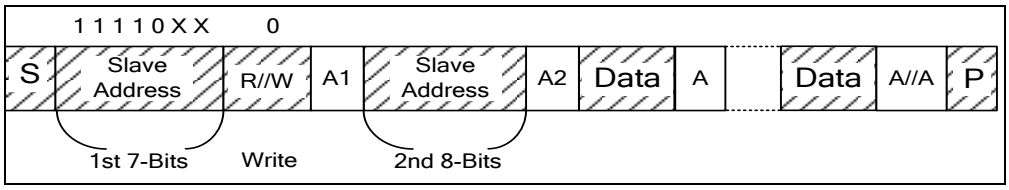


Figure 6-28a Master-Transmitter Transmits to Slave-Receiver with a 10-bit Slave Address

■ **Master-Receiver Reads Slave-Transmitter with a 10-bit Slave Address**

Up to and including acknowledge Bit A2, the procedure is the same as that described for Master-transmitter addressing a Slave receiver. After the acknowledge A2, a repeated START condition (Sr) followed by seven bits Slave address (11110XX) but the 8th bit R//W is "1", the addressed Slave device will return the acknowledge A3. If the repeated START (Sr) condition and the seven bits of first byte (11110XX) received by Slave device, all the Slave device would compare with their own address and test the 8th R//W. However, none of the Slave devices can return an acknowledgement because R//W=1.

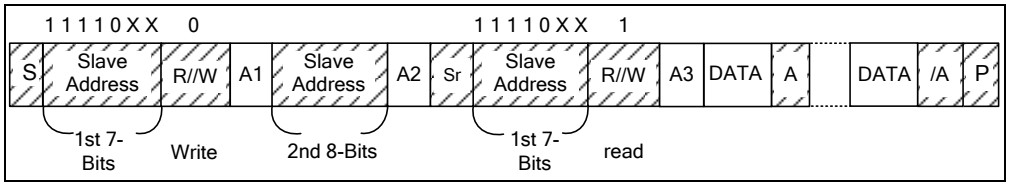


Figure 6-28b Master-Receiver Reads Slave-Transmitter with a 10-bit Slave Address

■ **Master Transmits and Receives Data to and from the Same Slave Device with 10-Bit Addresses**

The initial operation of this data transfer format is the same as explained in the above paragraph on “Master-Transmitter Transmits to Slave-Receiver with a 10-bit Slave Address.” Then the Master device starts to transmit the data to Slave device. When the Slave device receives the Acknowledge or None-Acknowledge that is followed by repeat START (Sr), the above operation under “Master-Receiver Read Slave-Transmitter with a 10-Bit Slave Address” is repeatedly performed.

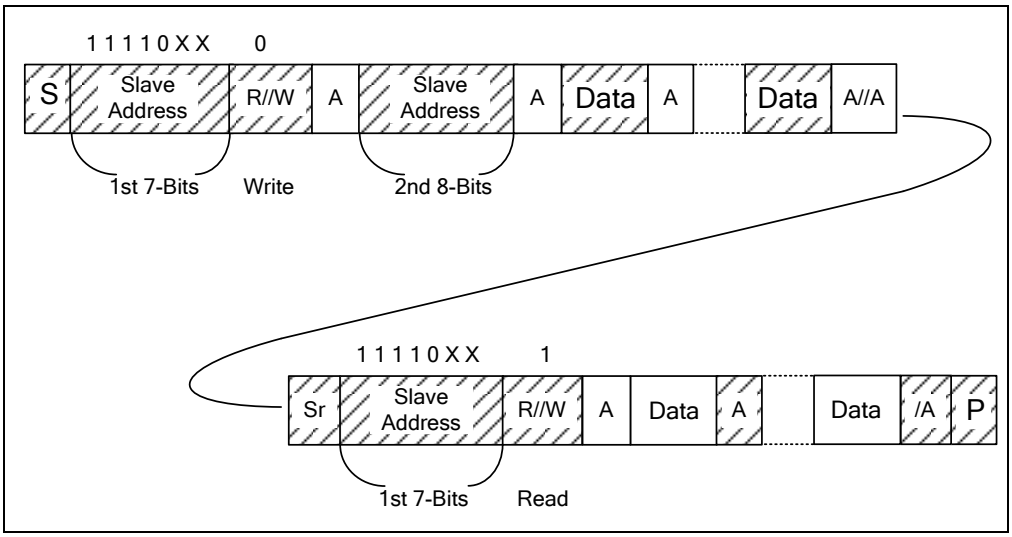


Figure 6-28c Master Addresses a Slave with 10-Bit Addresses Transmits and Receives Data with the Same Slave Device

■ **Master Device Transmits Data to Two or More Slave Devices with 10 and 7 Bits Slave Address**

For 10-bit address, the initial operation of this data transfer format is the same as explained in the above paragraph on “Master-Transmitter Transmits to Slave-Receiver with a 10-bit Slave Address,” which describes how to transmit data to Slave device. After the Master device completes the initial transmittal, and wants to continue transmitting data to another device, the Master needs to address each of the new Slave devices by repeating the initial operation mentioned above. If the Master device wants to transmit the data in 7-bit and 10-bit Slave address modes successively, this could be done after the START or repeat START conditions as illustrated in the following figures.

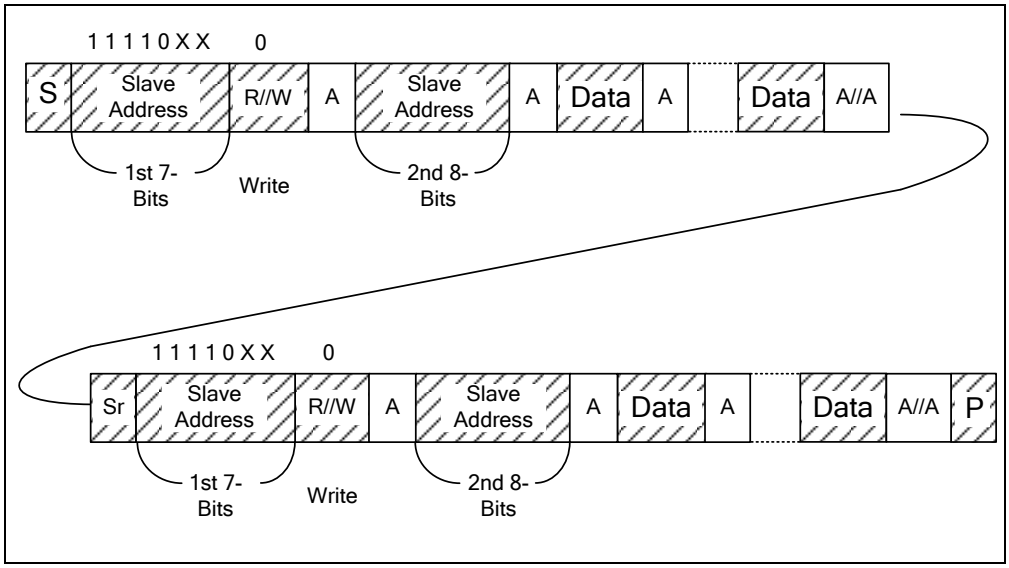


Figure 6-28d Master Transmitting to More than One Slave Devices with 10-Bit Slave Address

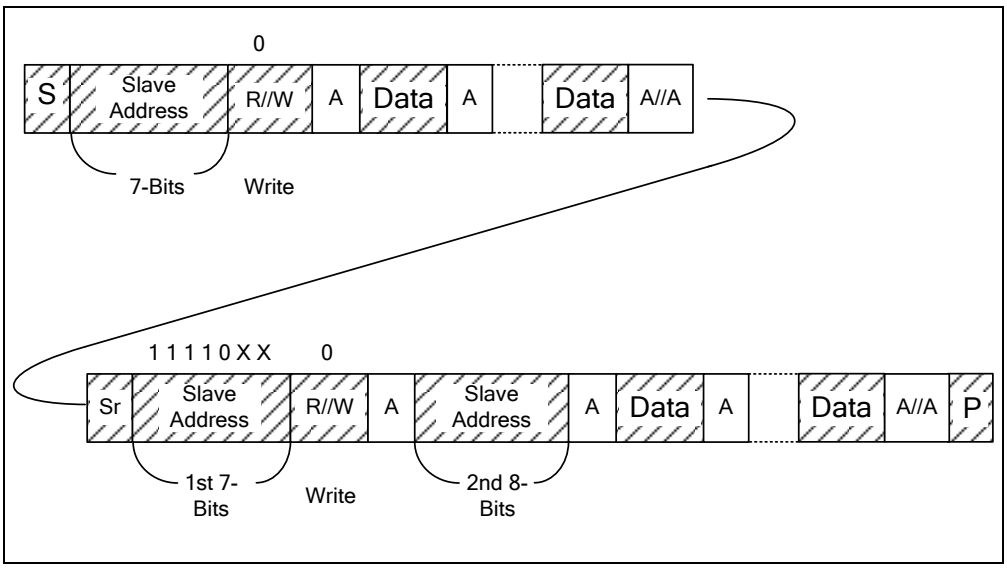


Figure 6-28e Master Successively Transmitting to 7-Bit and 10-Bit Slave Address

6.10.1 Master Mode

In transmitting (receiving) serial data, the I^2C operates as follows:

1. Set I^2CTS1~0 and ISS bits to select I^2C transmit clock source.
2. Set I^2CEN and IMS bits to enable I^2C Master function.
3. Write Slave address into the I^2CSA register and IRW bit to select read or write.
4. Set strobe bit will start transmit and then Check I^2CTSF (I^2CTSF) bit.
5. Write 1st data into the I^2CDB register, set strobe bit and Check I^2CTSF (I^2CRSF) bit.
6. Write 2nd data into the I^2CDB register, set strobe bit, Stop bit and Check I^2CTSF (I^2CRSF) bit.

6.10.2 Slave Mode

In receiving (transmitting) serial data, the I^2C operates as follows:

1. Set I^2CTS1~0, I^2CCS and ISS bits to select I^2C transmit clock source.
2. Set I^2CEN and IMS bits to enable I^2C Slave function.
3. Write device address into the I^2CDA register.
4. Check I^2CRSF (I^2CTSF) bit, read I^2CDB register (address) and then clear Pend bit.
5. Check I^2CRSF (I^2CTSF) bit, read I^2CDB register (1st data) and then clear Pend bit.
6. Check I^2CRSF (I^2CTSF) bit, read I^2CDB register (2nd data) and then clear Pend bit.
7. Check I^2CSTPSF bit, end transmission.

6.11 Liquid Crystal Display Driver (LCD Driver)

The EM78P528N supports two types of LCD (R-type) that can drive up to 23 segments and 8 commons, which drive a total of 8×23 dots. The LCD block is made up of LCD driver, display RAM, segment output pins, common output pins and LCD operating power supply pins. This circuit can work in normal mode, green mode and idle mode.

The LCD duty, bias, the number of segment, the number of common and frame frequency are determined by the LCD controller register.

The basic structure contains a timing control, which uses the main system clock or subsystem clock to generate the proper timing for different duty and display access. The Bank 1 R4B register is a command register for LCD driver that include LCD enable/disable, bias (1/2 and 1/3), duty (1/2, 1/3, 1/4) and LCD frame frequency control. The register Bank 1 R4C is LCD RAM address control register. The register Bank 1 R4D is LCD RAM data buffer. The control register is explained as follows.

Control Register

R_BANK	Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bank 0	0x48	LCDCR1	LCDEN	LCDTYPE	-	BS	DS1	DS0	LCDF1	LCDF0
			R/W	R/W	-	R/W	R/W	R/W	R/W	R/W
Bank 0	0x49	LCDCR2	-	RBS1	RBS0	DYMEN	-	-	BF1	BF0
			-	R/W	R/W	R/W	-	-	R/W	R/W
Bank 0	0x4A	LCDCR3	-	-	-	-	-	LCDCC2	LCDCC1	LCDCC0
			-	-	-	-	-	R/W	R/W	R/W
Bank 0	0x4B	LCDADDR	-	-	-	LCDA4	LCDA3	LCDA2	LCDA1	LCDA0
			-	-	-	R/W	R/W	R/W	R/W	R/W
Bank 0	0x4C	LCDDB	LCDD7	LCDD6	LCDD5	LCDD4	LCDD3	LCDD2	LCDD1	LCDD0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 0	0x4D	LCDCSCR	-	LCDSM2	LCDSM1	LCDSM0	-	LCDCM2	LCDCM1	LCDCM0
			-	R/W	R/W	R/W	-	R/W	R/W	R/W
Bank 0	0x4E	LCDSCR1	SEG7	SEG6	EG5	SEG4	SEG3	SEG2	SEG1	SEG0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 0	0x4F	LCDSCR2	SEG15	SEG14	SEG13	SEG12	SEG11	SEG10	SEG9	SEG8
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

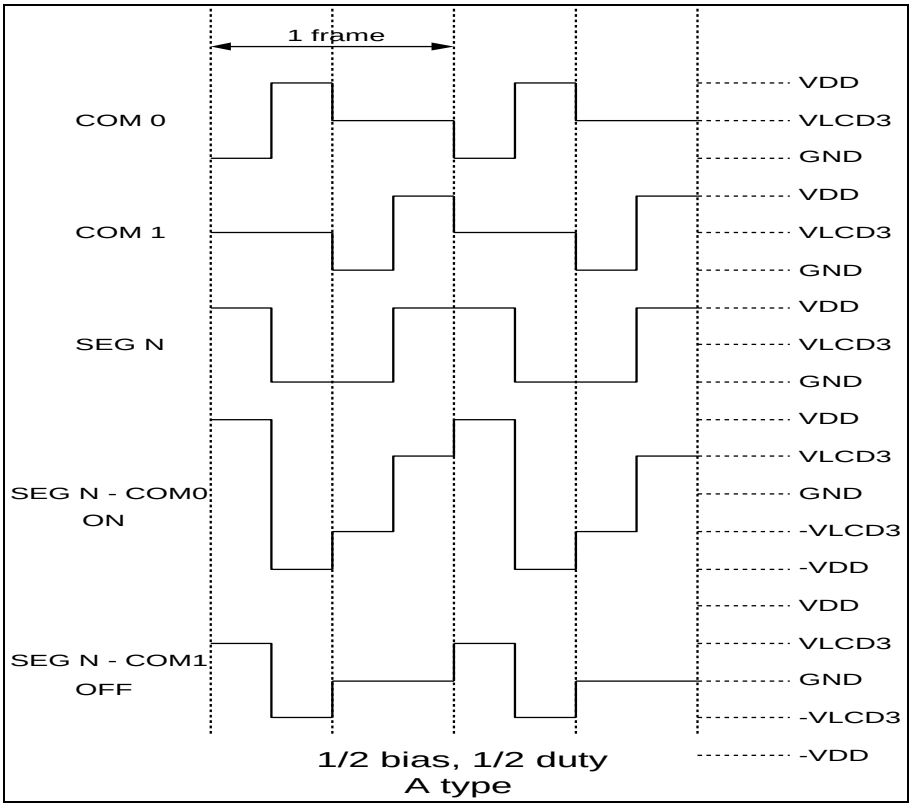


Figure 6-29a ½ Bias, ½ Duty A Type LCD Waveform

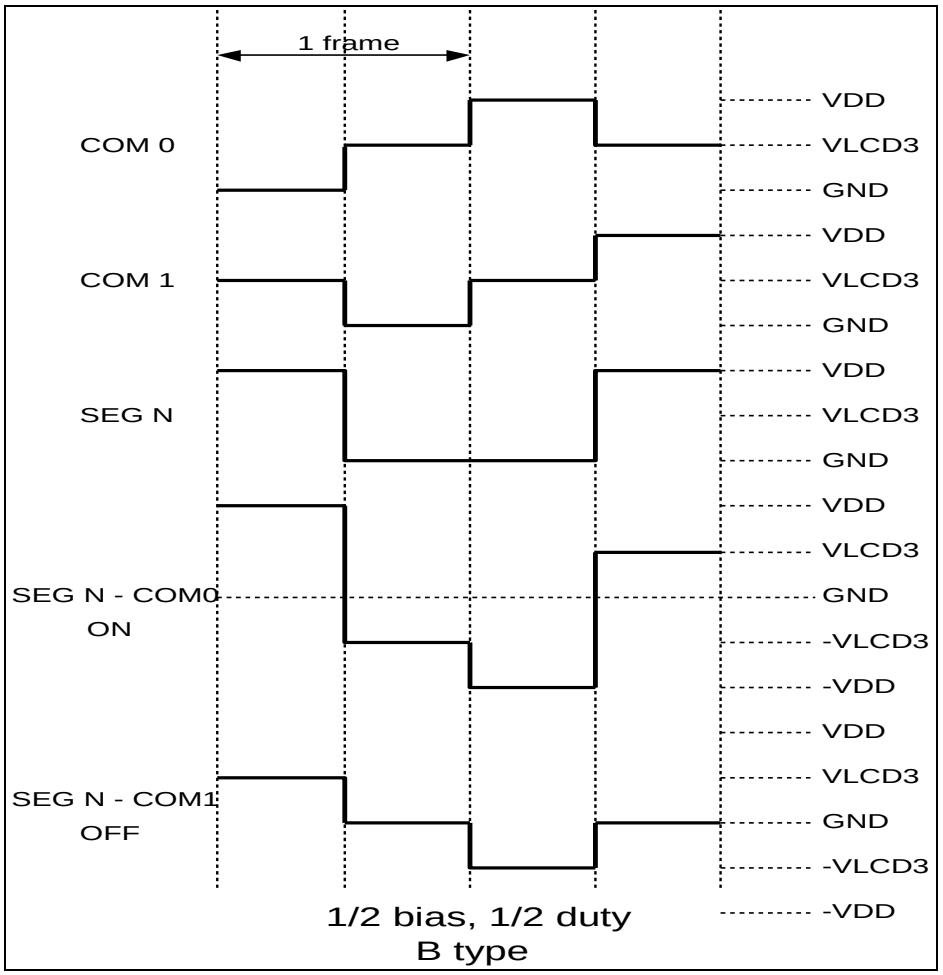


Figure 6-29b ½ Bias, ½ Duty B Type LCD Waveform

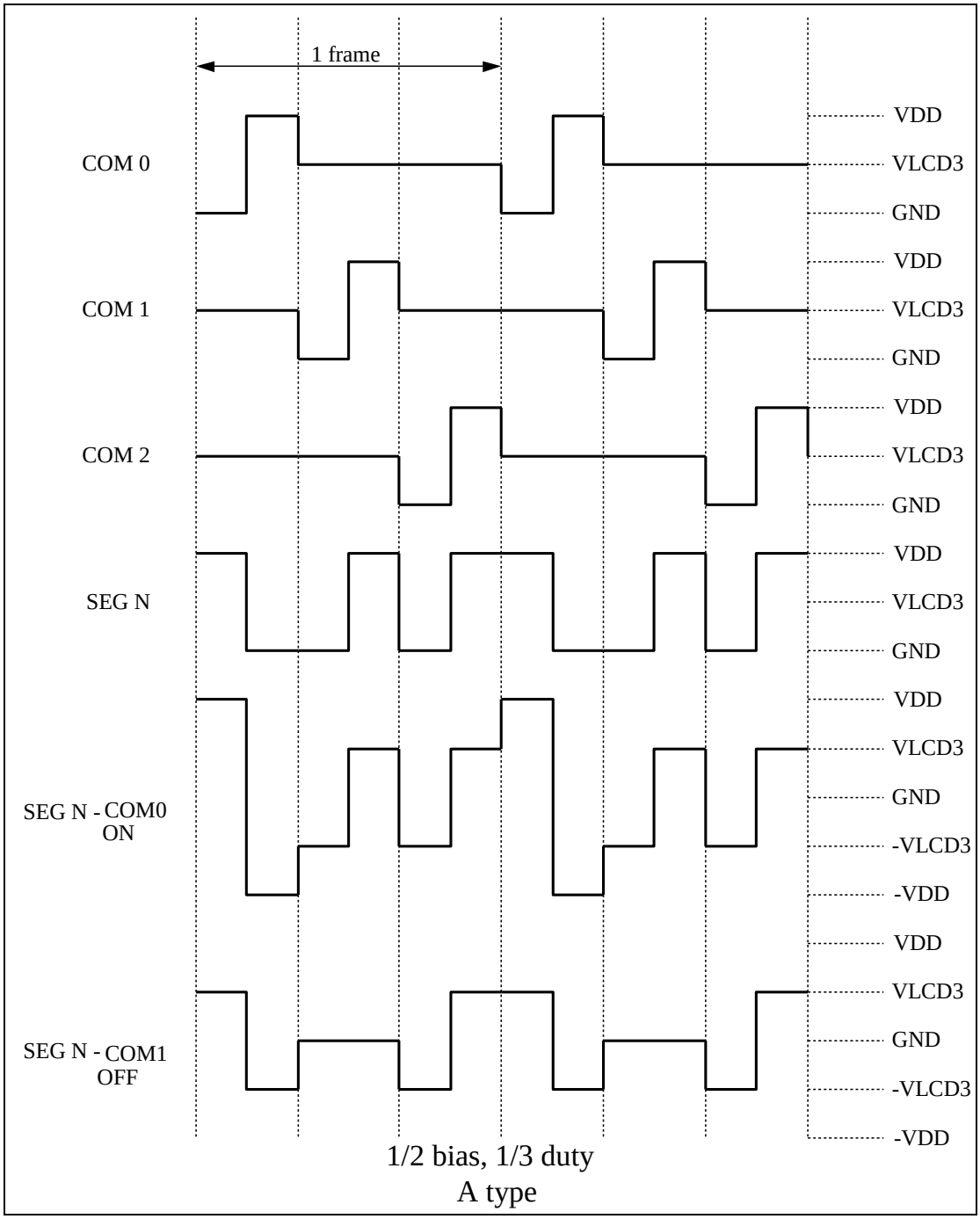


Figure 6-29c ½ Bias, 1/3 Duty A Type LCD Waveform

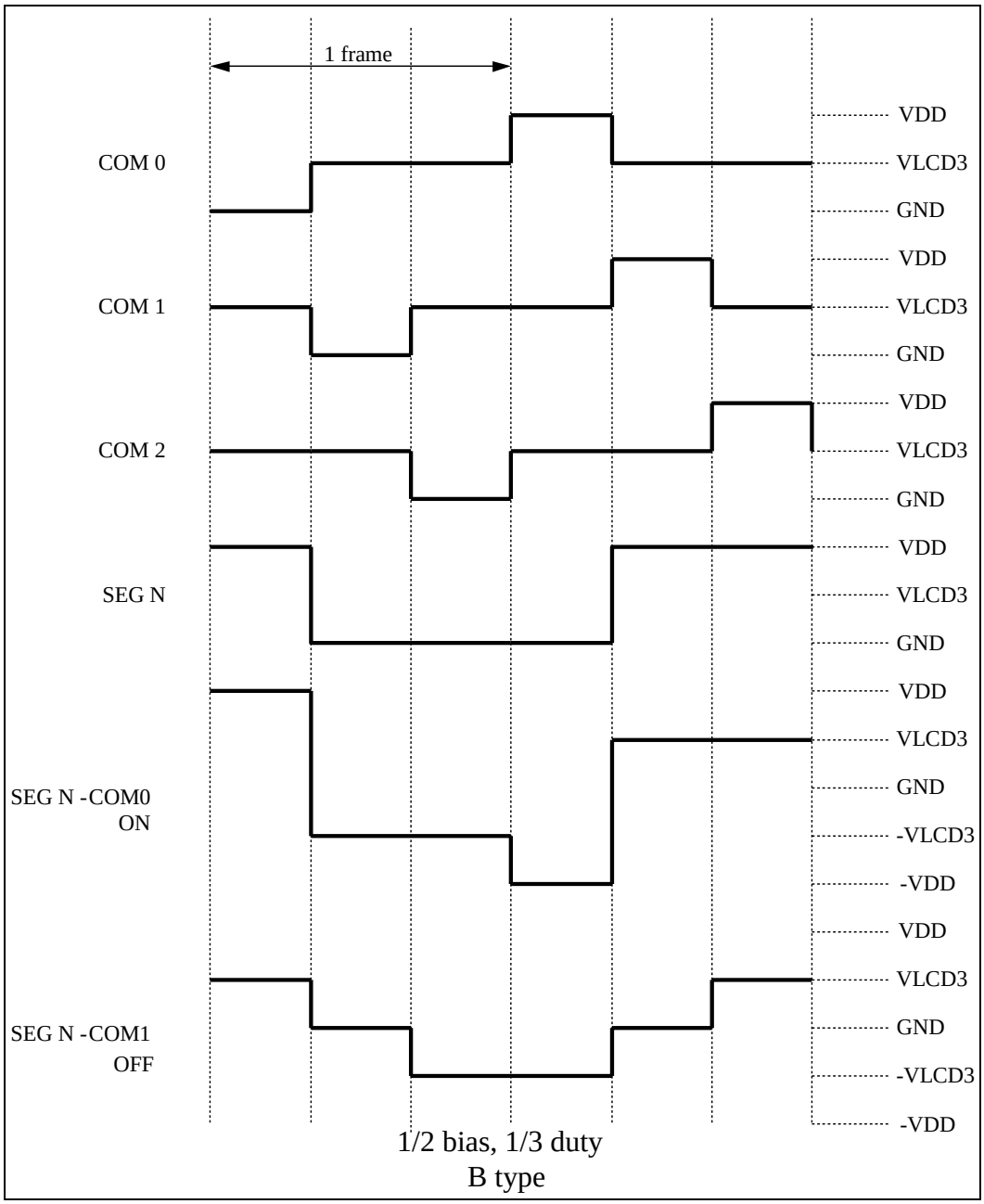


Figure 6-29d ½ Bias, 1/3 Duty B Type LCD Waveform

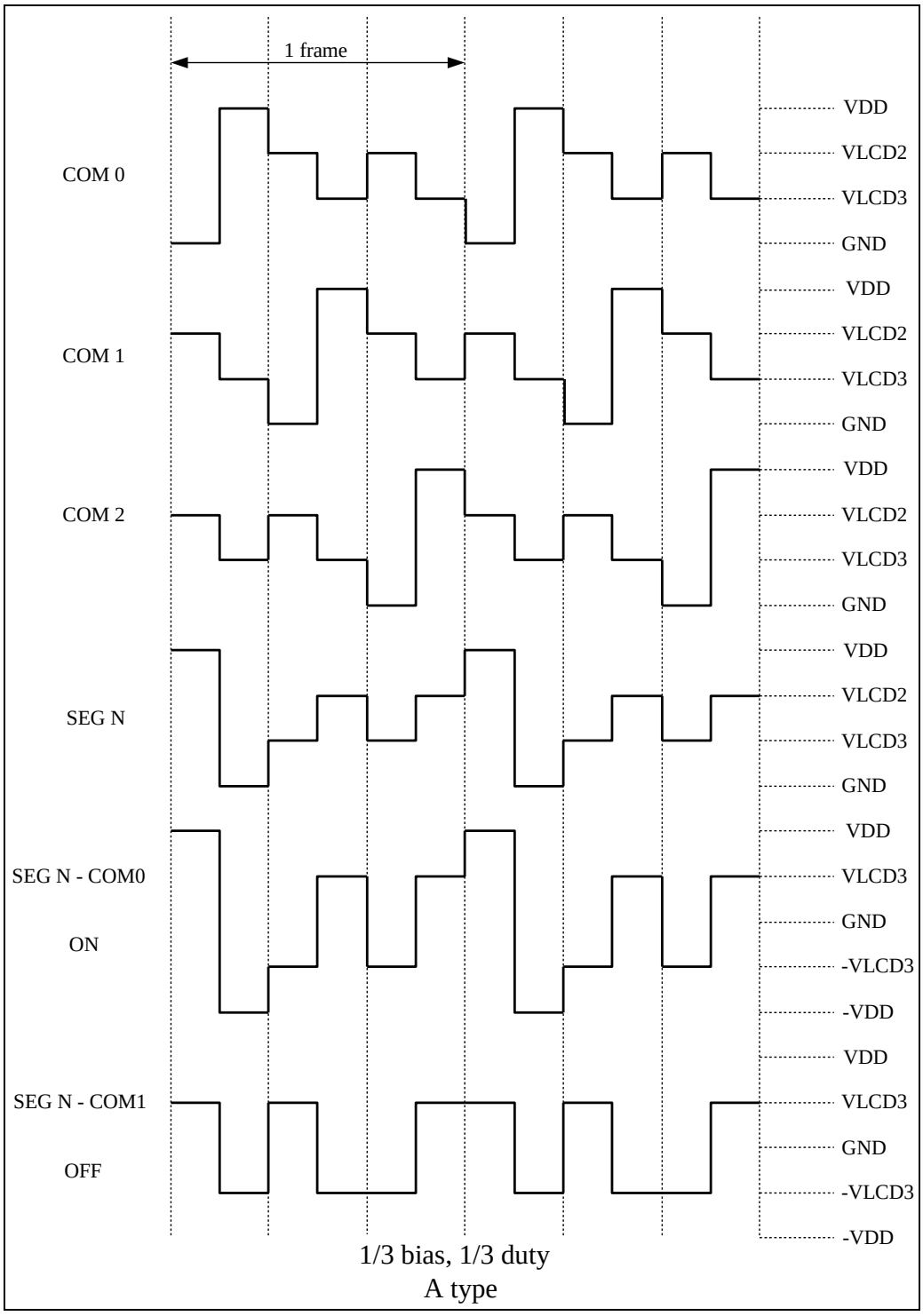


Figure 6-29e ⅓ Bias, ⅓ Duty A Type LCD Waveform

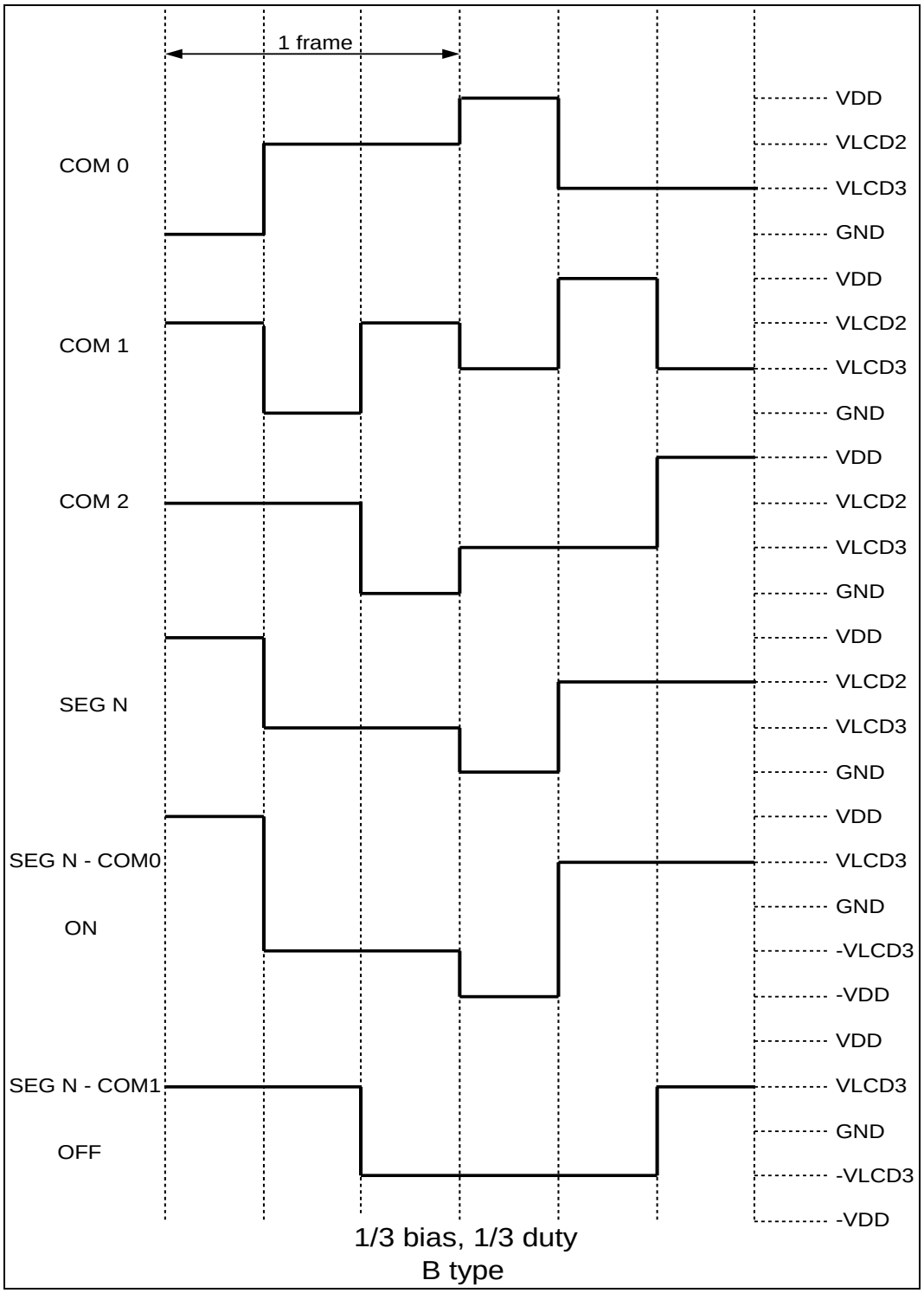


Figure 6-29f ⅓ Bias, ⅓ Duty B Type LCD Waveform

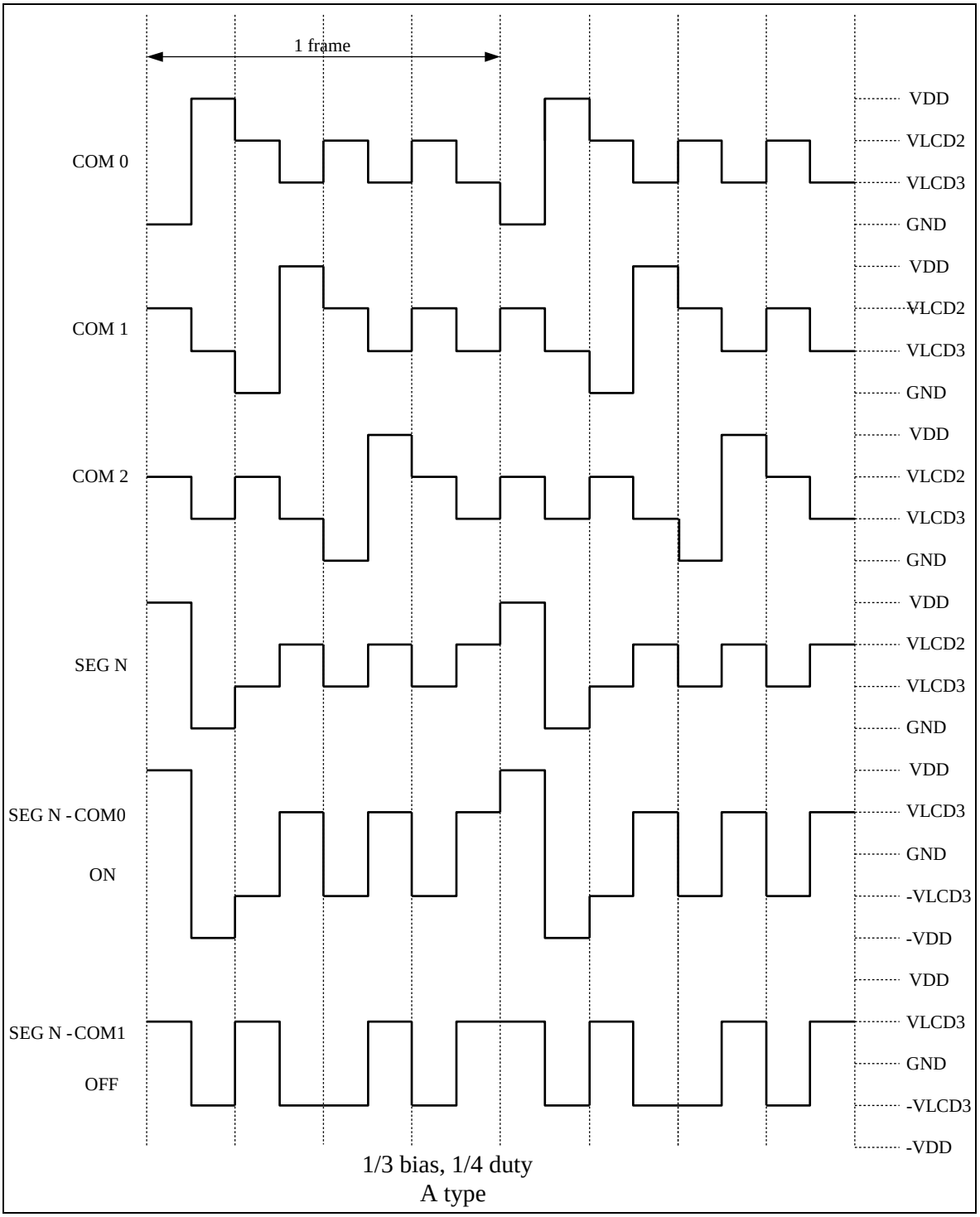


Figure 6-29g ⅓ Bias, ¼ Duty A Type LCD Waveform

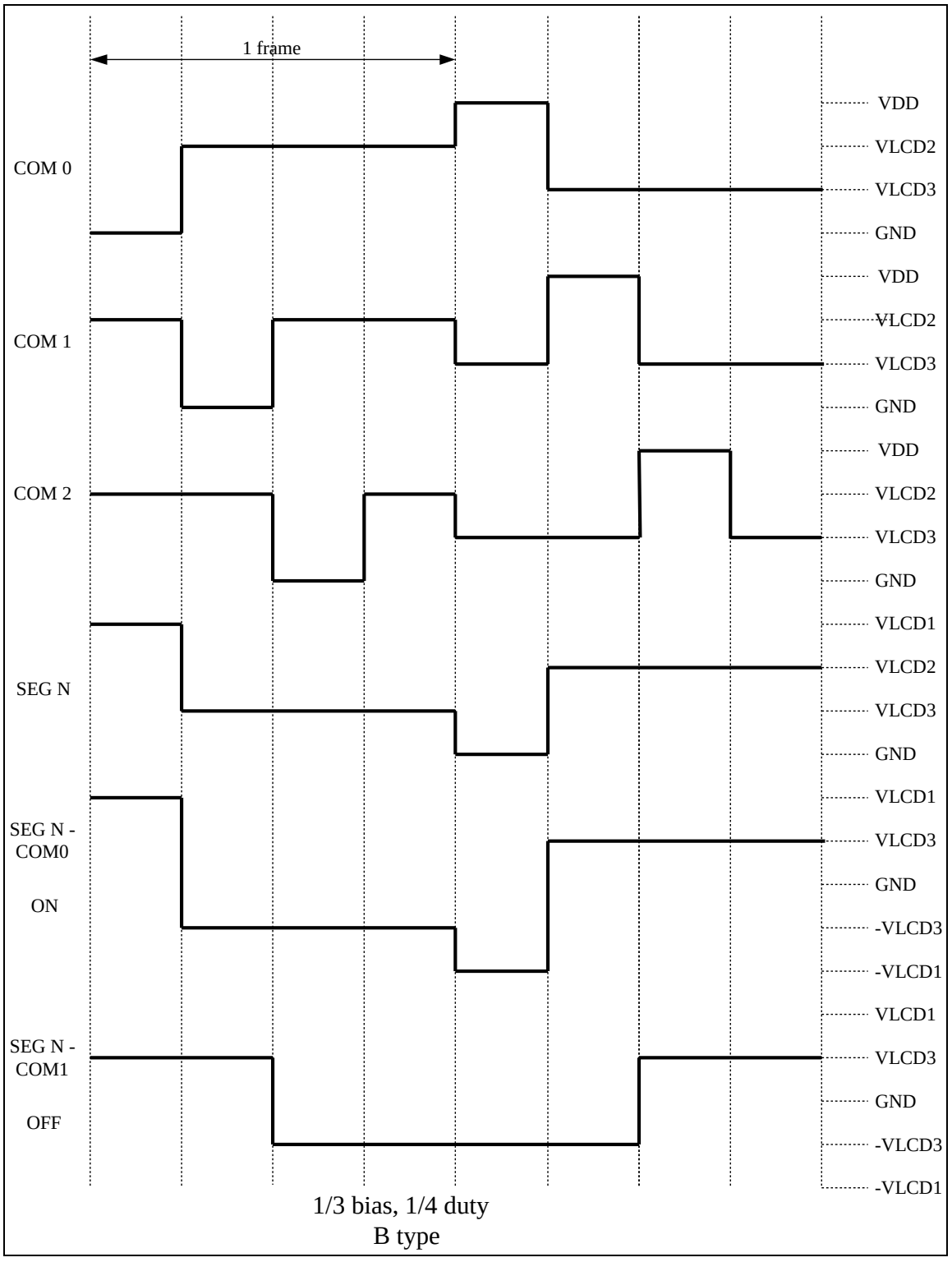


Figure 6-29h ⅓ Bias, ¼ Duty B Type LCD Waveform

6.12 LVD (Low Voltage Detector)

Under unstable power source condition, such as external power noise interference or EMS test condition, a violent power vibration could occur. At the time, the VDD could become unstable as it could be operating below working voltage. When the system supply voltage (VDD) is below operating voltage, the IC kernel will automatically keep all register status.

With LVD set at Bank 1 R45, the detailed LVD operation mode is as follows:

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LVDEN	LVDS2	LVDS1	LVDS0	LVDB	–	–	–
R/W	R/W	R/W	R/W	R	–	–	–

Bit 7 (LVDEN): Low Voltage Detector Enable Bit

0: Disable low voltage detector

1: Enable low voltage detector

Bits 6~4 (LVDS2~LVDS0): Low Voltage Detector Level Bits

LVDEN	LVDS2~0	LVD Voltage Interrupt Level	LVDSF
1	011	2.2V	1*
1	010	3.3V	1*
1	001	4.0V	1*
1	000	4.5V	1*
0	XX	NA	0

* *If Vdd crossovers at the LVD voltage interrupt level as Vdd varies, LVDSF =1.*

Bit 3 (LVDB): Low Voltage Detector State Bit. This is a read only bit. When the VDD pin voltage is lower than LVD voltage interrupt level (selected by LVDS2 ~ LVDS0), this bit will be cleared.

0: The low voltage is detected.

1: The low voltage is not detected or LVD function is disabled.

The following steps are needed to setup the LVD function:

1. Set the LVDEN to “1”, then use Bits 6~4 (LVDS2~LVDS0) of Register Bank 1 R45 to set the LVD interrupt level
2. Wait for LVD interrupt to occur
3. Clear the LVD interrupt flag

The internal LVD module uses the internal circuit to fit. When user set the LVDEN to enable the LVD module, the current consumption will increase to 30 μA.

During sleep mode, the LVD module continues to operate. If the device voltage drop slowly and crosses the detect point. The LVDSF bit will be set and the device will not wake up from Sleep mode. Until the other wake-up source to wake-up EM78P528N, the LVD interrupt flag is still set as the prior status.

When the system resets, the LVD flag will be cleared.

The Figure 6-30 shows the LVD module to detect the external voltage situation.

When VDD drops not below V_{LVD}, LVDSF keep at "0".

When VDD drops below VLVD, LVDSF set to "1". If global ENI enable, LVDSF will be set to "1", the next instruction will branch to the interrupt vector. The LVD interrupt flag is cleared to "0" by software.

When VDD drops below V_{RESET} and less than 5 μs, the system will keep all the register status and the system halts but oscillation is active. When VDD drops below VRESET and more than 5 μs, system RESET will occur, and for the following actions refer to Section 6.5.1 Reset description.

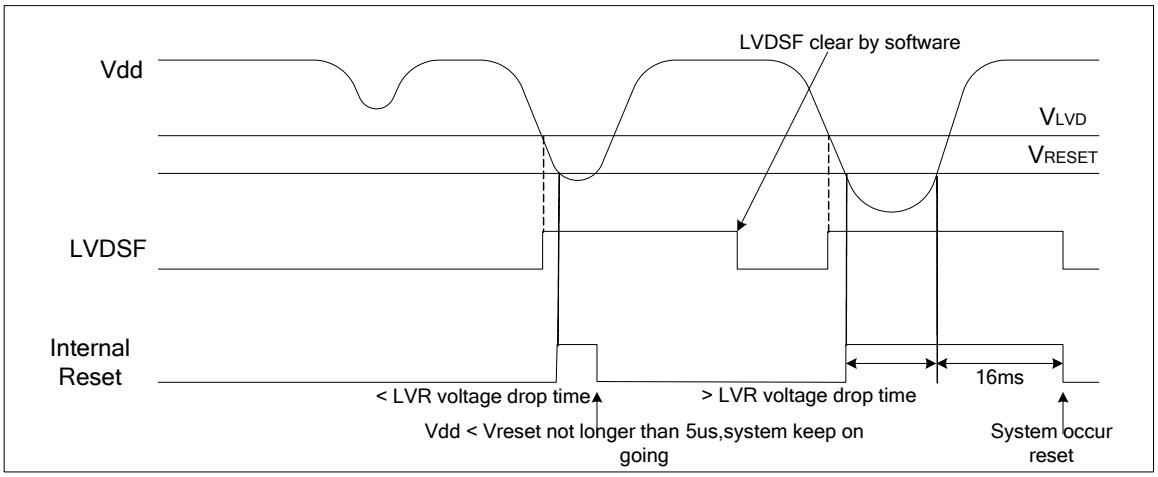


Figure 6-30 LVD Waveform Characteristics Showing Detection Point in an External Voltage Condition

6.13 Oscillator

6.13.1 Oscillator Modes

The EM78P528N can be operated in two different oscillator modes, such as Internal RC oscillator mode (IRC) and XTAL oscillator mode (XT). User need to set the main-oscillator modes by selecting the OSC2~OSC0, and set the sub-oscillator modes by selecting the FSS1~FSS0 in the Code Option register to complete the overall oscillator mode setting. Tables 6, 7, and 8 depict how these four modes are defined.

The up-limited operating frequency of crystal/resonator on the different VDD is listed in Table 6

Table 6 Main-oscillator modes defined by OSC2 ~ OSC0

Main-oscillator Mode	OSC2	OSC1	OSC0
HXT1 (High XTAL1 oscillator mode) Frequency range: 12~16 MHz	1	1	1
HXT2 (High XTAL2 oscillator mode) Frequency range: 6~12 MHz	1	1	0
XT (XTAL oscillator mode) Frequency range: 1~6 MHz	1	0	1
LXT1 (Low XTAL1 oscillator mode) Frequency range: 100K~1 MHz	1	0	0
IRC (Internal RC oscillator mode) (default) RCOUT (P54) acts as I/O pin	0	X	1
IRC (Internal RC oscillator mode) RCOUT (P54) acts as clock output pin	0	X	0

Table 7 Sub-oscillator modes defined by FSS1 ~ FSS0

Sub-oscillator Mode	FSS1	FSS0
LXT2 (Low XTAL2) oscillator mode Frequency range: 32.768kHz	0	x
Fs is 32kHz, Xin (P55) / Xout (P56) pin acts as I/O	1	0
Fs is 16kHz, Xin (P55) / Xout (P56) pin acts as I/O (default)	1	1

Note: WDT frequency is always 16kHz whatever the FSS1~0 bits are set.

Table 8 Combination of Main-oscillator and Sub-oscillator modes

Combination	Main Clock	Sub-clock
1	Crystal	Crystal
2	Crystal	IRC
3	IRC	Crystal
4	IRC	IRC

Table 9 Summary of Maximum Operating Speeds

Conditions	VDD	Fxt max. (MHz)
Two cycles with two clocks	2.2	4.0
	3.0	8.0
	5.0	16.0

6.13.2 Crystal Oscillator/Ceramic Resonators (XTAL)

In most applications, Pin OSCI and Pin OSCO can be connected with a crystal or ceramic resonator to generate oscillation and such circuitry are depicted in the following Figures. The same thing applies whether it is in HXT mode or in LXT mode. Table 10 provides the recommended values of C1 and C2. Since each resonator has its own attribute, user should refer to its specification for appropriate values of C1 and C2. The serial resistor, RS, may be necessary for AT strip cut crystal or low frequency mode.

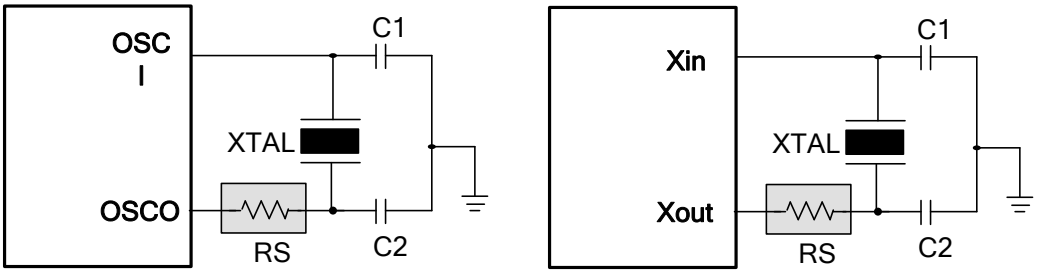


Figure 6-31 Crystal/Resonator Circuits

Table 10 Capacitor Selection Guide for Crystal Oscillator or Ceramic Resonator

Oscillator Type	Frequency Mode	Frequency	C1 (pF)	C2 (pF)
Main-oscillator (Ceramic Resonators)	LXT (100K~1 MHz)	100kHz	60pF	60pF
		200kHz	60pF	60pF
		455kHz	40pF	40pF
		1.0 MHz	30pF	30pF
	HXT2 (1M~6 MHz)	1.0 MHz	30pF	0pF
		2.0 MHz	30pF	30pF
		4.0 MHz	20pF	20pF
Main-oscillator (Crystal Oscillator)	LXT (100K~1 MHz)	100kHz	60pF	60pF
		200kHz	60pF	60pF
		455kHz	40pF	40pF
		1.0 MHz	30pF	30pF
	XT (1M~6 MHz)	1.0 MHz	30pF	30pF
		2.0 MHz	30pF	30pF
		4.0 MHz	20pF	20pF
		6.0 MH	0F	30pF
	HXT2 (6M~12 MHz)	6.0 MHz	30pF	30pF
		8.0 MHz	20pF	20pF
		12.0 MHz	30pF	30pF
	HX1 (12M~16 MHz)	12.0 MHz	30pF	30pF
		16.0 MHz	20pF	20pF
Sub-oscillator (Crystal Oscillator)	LXT2 (32.768kHz)	32.768kHz	35pF	35pF

6.13.3 Internal RC Oscillator Mode

EM78P528N offer a versatile internal RC mode with default frequency value of 4MHz. The Internal RC oscillator mode has other frequencies (16 MHz, 8 MHz and 1 MHz) that can be set by Code Option: RCM1 and RCM0. All these four main frequencies can be calibrated by programming the Code Option bits: C5~C0. The table describes a typical instance of the calibration.

Internal RC Drift Rate (Ta=25°C, VDD=5V±5%, VSS=0V)

Internal RC Frequency	Drift Rate			
	Temperature (-40℃~+85℃)	Voltage (2.5V~5.5V)	Process	Total
1 MHz	±2%	±1%	±1%	±4%
4 MHz	±2%	±1%	±1%	±4%
8 MHz	±2%	±1%	±1%	±4%
16 MHz	±2%	±1%	±1%	±4%

Note: *These are theoretical values provided for reference only. Actual values may vary depending on the actual process.*

6.14 Power-on Considerations

Any microcontroller is not guaranteed to start to operate properly before the power supply stabilizes to a steady state. The EM78P528N is equipped with a built-in Power-On Voltage Detector (POVD) with a detecting level of 2.0V. It will work well if VDD rises fast enough (50ms or less). However, in many critical applications, extra devices are still required to assist in solving power-up problems.

6.15 External Power-on Reset Circuit

The circuits shown in Figure 6-32 implement an external RC to generate a reset pulse. The pulse width (time constant) should be kept long enough for VDD to reach minimum operating voltage. Apply this circuit when the power supply has a slow rising time. Since the current leakage from the /RESET pin is about ±5 μA, it is recommended that R should not be greater than 40 KΩ in order for the /RESET pin voltage to remain at below 0.2V. The diode (D) acts as a short circuit at the moment of power down. The capacitor (C) will discharge rapidly and fully. The current-limited resistor (Rin) will prevent high current or ESD (electrostatic discharge) from flowing to Pin /RESET.

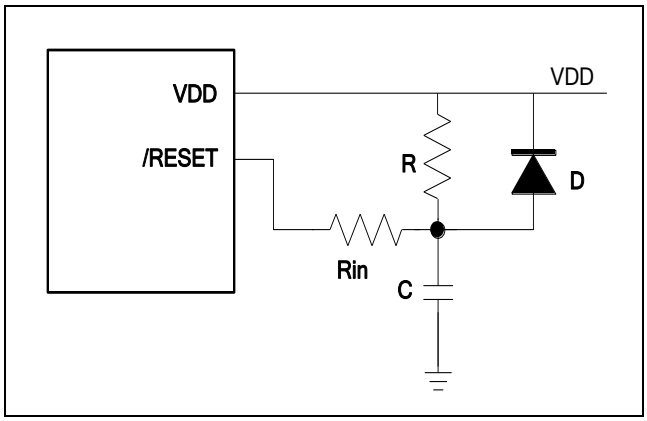


Figure 6-32 External Power-up Reset Circuit

6.16 Residue-Voltage Protection

When the battery is replaced, device power (VDD) is taken off but residue-voltage remains. The residue-voltage may trip below VDD minimum, but not to zero. This condition may cause a poor power-on reset. The following Figures 6-33a and 6-33b show how to build and accomplish a proper residue-voltage protection circuit.

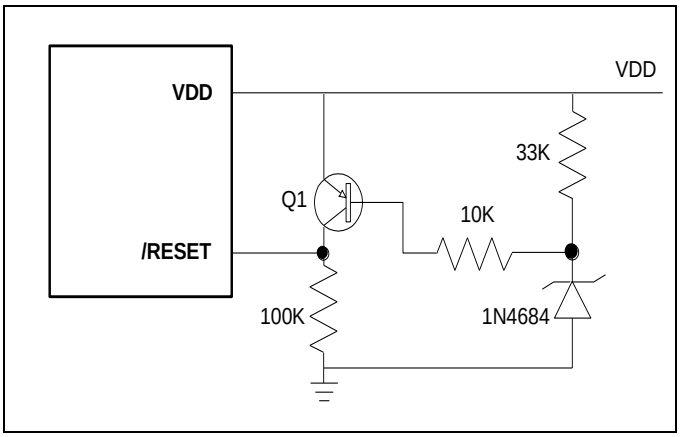


Figure 6-33a Residue Voltage Protection Circuit 1

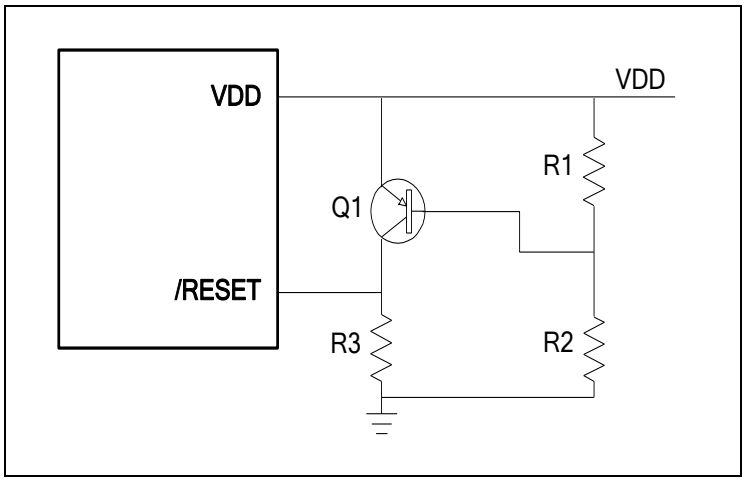


Figure 6-33b Residue Voltage Protection Circuit 2

6.17 Code Option

6.17.1 Code Option Register (Word 0)

Word 0															
Bit	Bit 14	Bit 13	Bit 12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Mnemonic	-	-	-	-	HLFS	HLP	LVR1	LVR0	RESETEN	ENWDT	NRHL	NRE	PR2	PR1	PR0
1	-	-	-	-	Normal	High	High	High	P57	Disable	32/fc	Enable	Disable		
0	-	-	-	-	Green	Low	Low	Low	/RESET1	Enable	8/fc	Disable	Enable		
Default	1	1	1	1	1	0	1	1	1	1	1	1	1		

Bits 14~11: Not used, set to "**1**" all the time.

Bit 10 (HLFS): Reset to Normal or Green Mode Select Bit

0: CPU is selected as Green mode when a reset occurs.

1: CPU is selected as Normal mode when a reset occurs (default)

Bit 9 (HLP): Power Consumption Selection

0: Low power consumption, apply to working frequency at 4 MHz or below 4 MHz

1: High power consumption, apply to working frequency above 4 MHz

Bits 8~7 (LVR1~LVR0): Low voltage reset enable bit.

LVR1	LVR0	VDD Reset Level	VDD Release Level
0	0	4.0V *	4.2V
0	1	3.5V **	3.7V
1	0	2.7V ***	2.9V
1	1	NA (Power-on Reset)	

* *If VDD < 4.0V and is kept for about 5 μs, IC will be reset.*

** *If VDD < 3.5V and is kept for about 5 μs, IC will be reset.*

*** *If VDD < 2.7V and is kept for about 5 μs, IC will be reset.*

Bit 6 (RESETEN): P57//RESET1 pin selection bit

0: Enable, /RESET1 pin. The initial value of Bank 1-R8<7> (PH57) will be set to "0" (enable internal pull-high).

1: Disable, P57 pin (default)

Bit 5 (ENWDT): WDT enable bit

0: Enable

1: Disable (default)

Bit 4 (NRHL): Noise rejection high/low pulse define bit.

0: pulses equal to 8/fc is regarded as signal

1: pulses equal to 32/fc is regarded as signal (default)

> **NOTE**
> *In Low XTAL oscillator (LXT) mode, the noise rejection high/low pulses are always 8/Fm.*

Bit 3 (NRE): Noise Rejection Enable bit

0: Disable

1: Enable (default). **But in Green, Idle, and Sleep modes the noise rejection circuit is always disabled.**

Bits 2~0 (PR2~PR0): Protect Bits. Each protect status is as follows:
(only for real chip)

PR2	PR1	PR0	Protect
0	0	0	Enable
1	1	1	Disable

6.17.2 Code Option Register (Word 1)

Word 1															
Bit	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Mnemonic	**FSS1**	**FSS0**	**C5**	**C4**	**C3**	**C2**	**C1**	**C0**	**RCM1**	**RCM0**	**-**	**OSC2**	**OSC1**	**OSC0**	**RCOUT**
1	High	High	High	High	High	High	High	High	High	High	-	High	High	High	High
0	Low	Low	Low	Low	Low	Low	Low	Low	Low	Low	-	Low	Low	Low	Low
Default	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1

Bits 14~13 (FSS1~FSS0): Sub-oscillator mode select bits.

Sub-oscillator mode	FSS1	FSS0
LXT2 mode Frequency range: 32.768kHz	0	x
Fs is 32kHz, Xin (P55) / Xout (P56) pin act as I/O	1	0
Fs is 16kHz, Xin (P55) / Xout (P56) pin act as I/O (default)	1	1

Note: *WDT frequency is always 16kHz whatever the FSS1~0 bits are set.*

Bits 12~7 (C5~C0): IRC trim bits. These are automatically set by the writer.

Bits 6~5 (RCM1~RCM0): IRC frequency select bits

RCM1	RCM0	Frequency (MHz)
0	0	1
0	1	8
1	0	16
1	1	4 (default)

Bit 4: Not used, set to "**1**" all the time.

Bits 3~1 (OSC2~OSC0): Main-oscillator mode select bits.

Main-oscillator Mode	OSC2	OSC1	OSC0
HXT1 (High XTAL1 oscillator mode) Frequency range: 16~12 MHz	1	1	1
HXT2(High XTAL2 oscillator mode) Frequency range: 12~6 MHz	1	1	0
XT (XTAL oscillator mode) Frequency range: 6~1 MHz	1	0	1
LXT1 (Low XTAL1 oscillator mode) Frequency range: 1M~100kHz	1	0	0
IRC (Internal RC oscillator mode) (default) RCOUT (P54) acts as I/O pin	0	X	1
IRC (Internal RC oscillator mode) RCOUT (P54) acts as clock output pin	0	X	0

Bit 0 (RCOUT): System Clock Output Enable Bit in IRC mode

0: OSCI pin is open drain

1: OSCI output instruction cycle time (default)

6.17.3 Code Option Register (Word 2)

Word 2															
Bit	**Bit 14**	**Bit 13**	**Bit 12**	**Bit11**	**Bit10**	**Bit9**	**Bit8**	**Bit7**	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
Mnemonic	**-**	**-**	**-**	**SC3**	**SC2**	**SC1**	**SC0**	**-**	**IRCIRS**	**-**	**I^2COPT**	**-**	**-**	**-**	**-**
1	-	-	-	High	High	High	High	-	Regulator	-	High	-	-	-	-
0	-	-	-	Low	Low	Low	Low	-	Bandgap	-	Low	-	-	-	-
Default	0	1	1	1	1	1	1	1	1	0	1	0	0	1	0

Bit 14: Not used, set to “0” all the time.

Bits 13~12: Not used, set to “1” all the time.

Bits 11~8 (SC3~SC0): Trim bits of sub frequency IRC. These are automatically set by the writer.

Bit 7: Not used, set to “1” all the time.

Bit 6 (IRCIRS): IRC Internal Reference Select

0: Bandgap

1: IRC regulator (default)

Bit 5: Not used, set to “0” all the time.

Bit 4 (I^2COPT): I^2C optional bit. It is used to switch the pin position of I^2C function.

0: Placed I^2C pins together with UART pins shown in the Pin Assignment figure.

1: Placed I^2C pins together with SPI pins shown in the Pin Assignment figure (default)

Bit 3: Not used, set to “**0**” all the time.

Bit 2: Not used, set to “**0**” all the time.

Bit 1: Not used, set to “**1**” all the time.

Bit 0: Not used, set to “**0**” all the time.

6.17.4 Code Option Register (Word 3)

Word 3															
Bit	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Mnemonic	**EFTIM**	**-**	**-**	**ADFM**	**-**	**-**	**-**	**-**	**-**	**ID5**	**ID4**	**ID3**	**ID2**	**ID1**	**ID0**
1	Light	-	-	High	-	-	-	-	-	Customer ID					
0	Heavy	-	-	Low	-	-	-	-	-						
Default	1	1	1	1	1	1	1	1	1						

Bits 14 (EFTIM): Low Pass Filter (**0:** Heavy, **1:** Light)

0: Less than 10 MHz - pass (heavy LPS)

1: Less than 25 MHz - pass (light LPS, default)

Bits13~12: Not used. Set to "**1**" all the time.

Bit 11 (ADFM): These bits control the AD data buffer format (ADDH and ADDL). Refer to the following table.

ADFM			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
12 bits	**0**	ADDH	-	-	-	-	ADD11	ADD10	ADD9	ADD8
		ADDL	ADD7	ADD6	ADD5	ADD4	ADD3	ADD2	ADD1	ADD0
	1	ADDH	ADD11	ADD10	ADD9	ADD8	ADD7	ADD6	ADD5	ADD4
		ADDL	-	-	-	-	ADD3	ADD2	ADD1	ADD0

Note: *Do not use if the hardware bits are set to "**0**".*

If ADFM=0, ADDH<7:4> = 0000.

Bits 10~6: Not used. Set to "**1**" all the time.

Bits 5~0 (ID5~ID0): Customer's ID Code **(only for real chip)**

6.18 Instruction Set

Each instruction in the instruction set is a 15-bit word divided into an OP code and one or more operands. Normally, all instructions are executed within one single instruction cycle (one instruction consists of 2 oscillator periods), unless the program counter is changed by instruction "MOV R2,A", "ADD R2,A", or by instructions of arithmetic or logic operation on R2 (e.g. "SUB R2,A", "BS(C) R2,6", "CLR R2", etc.). In this case, the execution takes two instruction cycles.

If for some reasons, the specification of the instruction cycle is not suitable for certain applications, try modifying the instruction as follows:

The conditional skip ("JBS", "JBC", "JZ", "JZA", "DJZ", "DJZA") commands which were tested to be true, are executed within two instruction cycles. The instructions that are written to the program counter also take two instruction cycles.

In addition, the instruction set has the following features:

(1) Every bit of any register can be set, cleared, or tested directly (except read only)

(2) The I/O register can be regarded as general register. That is, the same instruction can operate on I/O register.

■ **Instruction Set Convention:**

R = *Register designator that specifies which one of the registers (including operation and general purpose registers) is to be utilized by the instruction.*

b = *Bit field designator that selects the value for the bit located in the register R and which affects the operation.*

k = *8 or 12-bit constant or literal value*

Mnemonic	Operation	Status Affected
NOP	No Operation	None
DAA	Decimal Adjust A	C
SLEP	0 → WDT, Stop oscillator	T,P
WDTC	0 → WDT	T,P
ENI	Enable Interrupt	None
DISI	Disable Interrupt	None
RET	[Top of Stack] → PC	None
RETI	[Top of Stack] → PC, Enable Interrupt	None
MOV R,A	A → R	None
CLRA	0 → A	Z
CLR R	0 → R	Z
SUB A,R	R-A → A	Z, C, DC
SUB R,A	R-A → R	Z, C, DC
DECA R	R-1 → A	Z
DEC R	R-1 → R	Z
OR A,R	A ∨ R → A	Z
OR R,A	A ∨ R → R	Z

Mnemonic	Operation	Status Affected
AND A,R	A & R → A	Z
AND R,A	A & R → R	Z
XOR A,R	A ⊕ R → A	Z
XOR R,A	A ⊕ R → R	Z
ADD A,R	A + R → A	Z, C, DC
ADD R,A	A + R → R	Z, C, DC
MOV A,R	R → A	Z
MOV R,R	R → R	Z
COMA R	/R → A	Z
COM R	/R → R	Z
INCA R	R+1 → A	Z
INC R	R+1 → R	Z
DJZA R	R-1 → A, skip if zero	None
DJZ R	R-1 → R, skip if zero	None
RRCA R	R(n) → A(n-1), R(0) → C, C → A(7)	C
RRC R	R(n) → R(n-1), R(0) → C, C → R(7)	C
RLCA R	R(n) → A(n+1), R(7) → C, C → A(0)	C
RLC R	R(n) → R(n+1), R(7) → C, C → R(0)	C
SWAPA R	R(0-3) → A(4-7), R(4-7) → A(0-3)	None
SWAP R	R(0-3) ↔ R(4-7)	None
JZA R	R+1 → A, skip if zero	None
JZ R	R+1 → R, skip if zero	None
BC R,b	0 → R(b)	None
BS R,b	1 → R(b)	None
JBC R,b	if R(b)=0, skip	None
JBS R,b	if R(b)=1, skip	None
CALL k	PC+1 → [SP], (Page, k) → PC	None
JMP k	(Page, k) → PC	None
MOV A,k	k → A	None
OR A,k	A ∨ k → A	Z
AND A,k	A & k → A	Z
XOR A,k	A ⊕ k → A	Z
RETL k	k → A, [Top of Stack] → PC	None
SUB A,k	k-A → A	Z, C, DC
ADD A,k	k+A → A	Z, C, DC
SBANK k	K->R1(4)	None
GBANK k	K->R1(0)	None
LCALL k	Next instruction : k kkkk kkkk kkkk PC+1→ [SP], k→ PC	None
LJMP k	Next instruction : k kkkk kkkk kkkk K→ PC	None
TBRD R	ROM[(TABPTR)] → R	None

7 Absolute Maximum Ratings

Items	Rating		
Temperature under bias	-40°C	to	85°C
Storage temperature	-65°C	to	150°C
Input voltage	VSS-0.3V	to	VDD+0.5V
Output voltage	VSS-0.3V	to	VDD+0.5V
Operating Voltage	2.1V	to	5.5V
Operating Frequency	DC	to	16 MHz

8 DC Electrical Characteristics

VDD=5.0V, VSS=0V, Ta=25°C

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Fxt	XTAL: VDD to 3V	Two cycles with two clocks	DC	8	–	MHz
	XTAL: VDD to 5V		DC	16	–	MHz
	IRC: VDD to 5V	4 MHz, 1 MHz, 8kHz, 16 MHz	–	F	–	Hz
IRCE	Internal RC oscillator error per stage	–	–	±1	–	%
IRC1	IRC:VDD to 5V	RCM0:RCM1=1:1	–	4	–	MHz
IRC2	IRC:VDD to 5V	RCM0:RCM1=1:0	–	8	–	MHz
IRC3	IRC:VDD to 5V	RCM0:RCM1=0:1	–	16	–	MHz
IRC4	IRC:VDD to 5V	RCM0:RCM1=0:0	–	1	–	MHz
IIL	Input Leakage Current for input pins	VIN = VDD, VSS	-1	0	1	μA
VIH1	Input High Voltage (Schmitt Trigger)	Ports 5, 6, 7, 8, 9, A	0.7VDD	–	VDD+0.3V	V
VIL1	Input Low Voltage (Schmitt Trigger)	Ports 5, 6, 7, 8, 9, A	-0.3V	–	0.3VDD	V
VIHT1	Input High Threshold Voltage (Schmitt Trigger)	/RESET	0.7VDD	–	VDD+0.3V	V
VILT1	Input Low Threshold Voltage (Schmitt Trigger)	/RESET	-0.3V	–	0.3VDD	V
VIHT2	Input High Threshold Voltage (Schmitt Trigger)	TCC, INT	0.7VDD	–	VDD+0.3V	V
VILT2	Input Low Threshold Voltage (Schmitt Trigger)	TCC, INT	-0.3V	–	0.3VDD	V
VIHX1	Clock Input High Voltage	OSCI in crystal mode	2.9	3.0	3.1	V
VILX1	Clock Input Low Voltage	OSCI in crystal mode	1.7	1.8	1.9	V
IOH1	High Drive Current 1 (Ports 5~9, A)	VOH = VDD-0.1VDD	-2.7	-4.5	–	mA
IOH2	High Drive Current 2 (Ports 5~9, A)	VOH = VDD-0.1VDD	-4.8	-8	–	mA
IOL1	Low Sink Current 1 (Ports 5~9, A)	VOL = GND+0.1VDD	8.4	14	–	mA
IOL2	Low Sink Current 2 (Ports 5~9, A)	VOL = GND+0.1VDD	16.8	28	–	mA
IPH	Pull-high current	Pull-high active, input pin @ VSS	47	-72	97	μA
IPL	Pull-low current	Pull-low active, input pin @ VDD	27	52	77	μA

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit

LVR1	Low voltage reset Level 1 (2.7V)	Ta = 25°C	2.41	2.7	2.99	V
		Ta = -40°C ~ 85°C	2.14	2.7	3.25	V
LVR2	Low voltage reset Level 2 (3.5V)	Ta = 25°C	3.1	3.5	3.92	V
		Ta = -40°C ~ 85°C	2.73	3.5	4.25	V
LVR3	Low voltage reset Level 3 (4.0V)	Ta = 25°C	3.56	4.0	4.43	V
		Ta = -40°C ~ 85°C	3.16	4.0	4.81	V
ISB1	Power down current (Sleep mode)	Ta=25°C, /RESET= 'High', Fm & Fs off All input and I/O pins at VDD, Output pin floating, WDT disabled	–	1	2	μA
		Ta=85°C, /RESET= 'High', Fm & Fs off All input and I/O pins at VDD, Output pin floating, WDT disabled	–	2	2.5	μA
ISB2	Power down current (Sleep mode)	/RESET= 'High', Fm & Fs off All input and I/O pins at VDD, Output pin floating, WDT enabled	–	4.2	–	μA
ISB3	Power down current (Idle mode)	/RESET= 'High', Fm off, Fs=16kHz (IRC type), All input and I/O pins at VDD, Output pin floating, WDT enabled	–	5.6	–	μA
ISB4	Power down current (Idle mode)	/RESET= 'High', Fm off, Fs=32kHz (IRC type), Output pin floating, WDT disabled, LCD on (1/3 bias, RBS1~0=00)	–	19	–	μA
ISB5	Power down current (Idle mode)	/RESET= 'High', Fm off, Fs=32.768kHz (Crystal type), Output pin floating, WDT disabled, LCD on (1/3 bias, RBS1~0=00)	–	22	–	μA
ICC1	Operating supply current (Green mode)	/RESET= 'High', Fm off, Fs=16kHz (IRC type), output pin floating, WDT enabled	–	12.8	–	μA
ICC2	Operating supply current (Green mode)	/RESET= 'High', Fm off, Fs=32kHz (IRC type), Output pin floating, WDT enabled	–	17.6	–	μA
ICC3	Operating supply current (Green mode)	/RESET= 'High', Fm off, Fs=32.768kHz (Crystal type), output pin floating, WDT enabled	–	24.5	–	μA
ICC4	Operating supply current (Normal mode)	/RESET= 'High', Fm=4 MHz (Crystal type), Fs on, output pin floating, WDT enabled	–	1.6	–	mA
ICC5	Operating supply current (Normal mode)	/RESET= 'High', Fm=4 MHz (IRC type), Fs on, output pin floating, WDT enabled	–	1.5	–	mA
ICC6	Operating supply current (Normal mode)	/RESET= 'High', Fm=10 MHz (Crystal type), Fs on, output pin floating, WDT enabled	–	3.6	–	mA
ICC7	Operating supply current (Normal mode)	/RESET= 'High', Fm=16 MHz (IRC type), Fs on, output pin floating, WDT enabled	–	4.6	–	mA
ICC8	Operating supply current (Normal mode)	/RESET= 'High', Fm=16 MHz (Crystal type), Fs on, output pin floating, WDT enabled	–	5.7	–	mA
ILCD1	All LCD lighting	VLCD=5V, exclude CPU core operation current (no load), 1/3 bias, RBS1~0=00	–	12	–	μA
ILCD2	All LCD lighting	VLCD=5V, exclude CPU core operation current (no load), 1/3 bias, RBS1~0=01	–	20	–	μA
ILCD3	All LCD lighting	VLCD=5V, exclude CPU core operation current (no load), 1/3 bias, RBS1~0=10	–	33.5	–	μA
ILCD4	All LCD lighting	VLCD=5V, exclude CPU core operation current (no load), 1/3 bias, RBS1~0=11	–	100	–	μA

* *These parameters are characterize but not tested.*

** *Data in the Minimum, Typical, and Maximum ("Min.", "Typ.", "Max.") columns are based on characterization results at 25°C. These data are for design reference only and have not been tested.*

8.1 AD Converter Characteristics

VDD=5V, VSS=0V, Ta=25°C

Symbol		Parameter	Condition	Min.	Typ.	Max.	Unit
V_{AREF}		Analog reference voltage	V_{AREF}-V_{ASS} ≧ 2.5V	2.5	–	VDD	V
V_{ASS}				VSS	–	VSS	V
VAI		Analog input voltage	–	V_{ASS}	–	V_{AREF}	V
IAI1	Ivdd	Analog supply current	V_{AREF} = VDD = 5.5V V_{ASS} = VSS = 0V FS=100kHz, FIN=1kHz (VREF is internal VDD)	–	–	1400	μA
	Ivref			–	–	10	μA
IAI2	Ivdd	Analog supply current	V_{AREF} = VDD = 5.5V V_{ASS} = VSS = 0V FS=100kHz, FIN=1kHz (VREF is external VREF pin)	–	–	900	μA
	Ivref			–	–	500	μA
INL		Integral nonlinearity	V_{AREF} = VDD = 5V V_{ASS} = VSS = 0V FS=100kHz, FIN=1kHz	–	–	±4	LSB
DNL		Differential nonlinear	V_{AREF} = VDD = 5V V_{ASS} = VSS = 0V FS=100kHz, FIN=1kHz	–	–	±1	LSB
FSE		Full scale error	V_{AREF} = VDD = 5V V_{ASS} = VSS = 0V, Fs=100kHz	–	–	±8	LSB
OE		Offset error	V_{AREF} = VDD = 5V V_{ASS} = VSS = 0V, Fs=100kHz	–	–	±4	LSB
ZAI		Recommended impedance of analog voltage source	–	–	–	10	kΩ
TAD		A/D clock duration	VDD = 3V~5.5V V_{ASS} = VSS = 0V, FIN=1kHz	0.5	–	–	μs
			VDD = 2.5V~3V V_{ASS} = VSS = 0V, FIN=1kHz	2	–	–	μs
TSH		Sample and Hold time	VDD = 3V~5.5V V_{ASS} = VSS = 0V	4	–	–	μs
			VDD = 2.5V~3V V_{ASS} = VSS = 0V	16	–	–	μs
TCN		A/D conversion time	VDD = 2.5V~5V V_{ASS} = VSS = 0V	–	Tsh+12TAD	–	TAD

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
TADD1	AD delay time between setting “ADRUN” and starting 1st TAD	VDD=2.5~5.5V, VASS=0.0V	0.5	–	–	TAD
TADD2	AD delay time between changing “ADOM” and setting “ADRUN”	VDD=2.5~5.5V, VASS=0.0V	2	–	–	TAD
TADD3	AD delay time between changing “ADIS” and setting “ADRUN”	VDD=2.5~5.5V, VASS=0.0V	2	–	–	TAD
TADD4	AD delay time between changing “ADP” and setting “ADRUN”	VDD=2.5~5.5V, VASS=0.0V	2	–	–	TAD
PSRR	Power supply rejection ratio	VDD = 2.5 ~ 5.5V, V_{AREF} = 2.5V, V_{ASS} = VSS = 0V, Vin = 0 ~ 2.5V, FS = 25kHz	–	–	2	LSB
$A_{1/4VDD}$	Accuracy for 1/4VDD	–	–	±3	–	%

Note:

1. FS is Sample Rate or conversion rate. FIN is freq. of input test sine wave

2. The parameters are theoretical values and have not been tested. Such parameters are for design reference only.

3. There is no current consumption when ADC is off other than minor leakage current.

4. AD conversion result will not decrease when the input voltage is increased, and there is no missing code.

5. These parameters are subject to change without further notice.

8.2 VREF 2V/3V/4V Characteristics

VDD=5V, VSS=0V, Ta=25°C

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
VDD	Power Supply	–	2.1	–	5.5	V
I_{VDD}	DC Supply Current	No load	–	–	250	µA
AVref	Accuracy for Vref	Vref = 2V, 3V, 4V	–	±1	±1.75	%
Warn up time	Time ready for voltage reference	VDD = VDD_{min} - 5.5V, Cload = 19.2pf Rload = 15.36KΩ	–	30	50	µs
VDD_{min}	Minimum Power Supply	–	–	Vref + 0.2*	–	V

* ***VDD_{min} :*** *Can also work at Vref+0.1V, but has a poor PSRR.*

Note:

1. The parameters are theoretical values and have not been tested. Such parameters are for design reference only.

2. These parameters are subject to change without prior notice.

9 AC Electrical Characteristics

Ta=25°C, VDD=5V ± 5%, VSS=0V

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Dclk	Input CLK duty cycle	–	45	50	55	%
Tins	Instruction Cycle Time	Crystal type	125	–	DC	ns
		IRC type	125	–	DC	ns
Ttcx	TCX Input Period	–	Tins	–	–	ns
Tpor	Delay time after Power-on-Reset release	16kHz	–	16±3%	–	ms
Trstrl	Delay time after /RESET, WDT and LVR release	Crystal type, HLFS=1	–	WSTO+510/Fm	–	–
		IRC type, HLFS=1	–	WSTO+8/Fm	–	–
		Crystal type, HLFS=0	–	WSTO+510/Fs	–	–
		IRC type, HLFS=0	–	WSTO+8/Fs	–	–
Trsth	Hold time after /RESET and LVR reset	–	–	1	–	μs
Twdt	Watchdog timer period	16kHz	–	16±3%	–	ms
Tset	Input pin setup time	–	–	0	–	ns
Thold	Input pin hold time	–	15	20	25	ns
Tdelay	Output pin delay time	Cload=20pF Rload=1M	–	20	–	ns

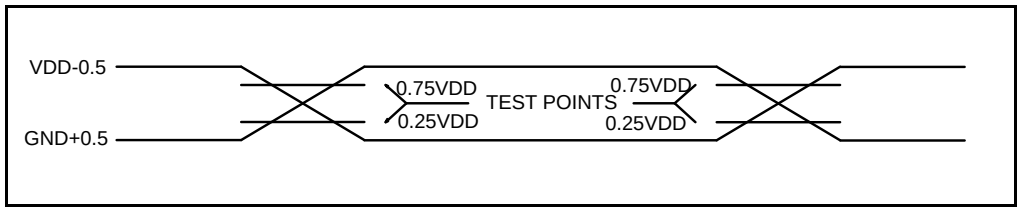
Note: * ***Tpor*** *and* ***Twdt*** *are16+/- 10% ms at Ta = -40° ~ 85℃, and VDD = 2.1~5.5V*

** *WSTO: Waiting time of Start-to-Oscillation*

1. *These parameters are hypothetical (not tested) and are provided for design reference only.*
2. *Data under Minimum, Typical and Maximum (Min., Typ. and Max.) columns are based on hypothetical results at 25℃. These data are for design reference only and have not been tested or verified.*

10 Timing Diagrams

AC Test Input / Output Waveform



Note: *AC Testing: Input are driven at VDD-0.5V for logic "**1**," and VSS+0.5V for logic "**0**"*
*Timing measurements are made at 0.75VDD for logic "**1**," and 0.25VDD for logic "**0**"*

Figure 10-1a AC Test Input / Output Waveform Timing Diagram

Reset Timing

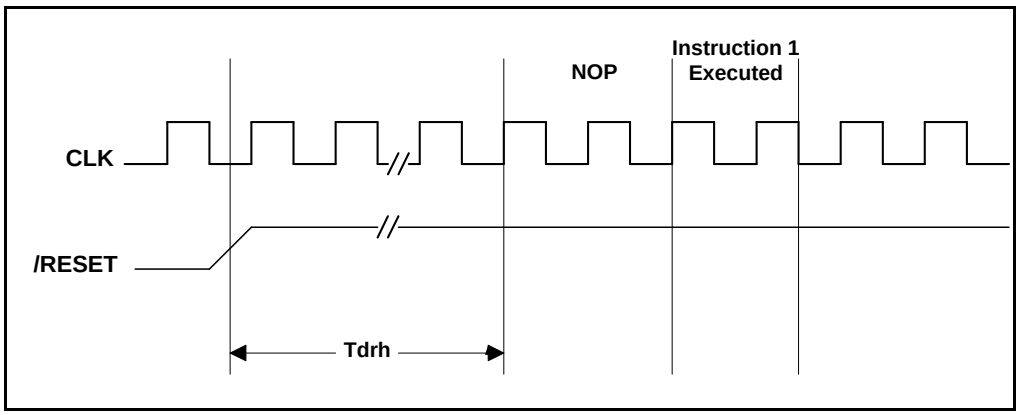


Figure 10-1b Reset Timing Diagram

TCC Input Timing

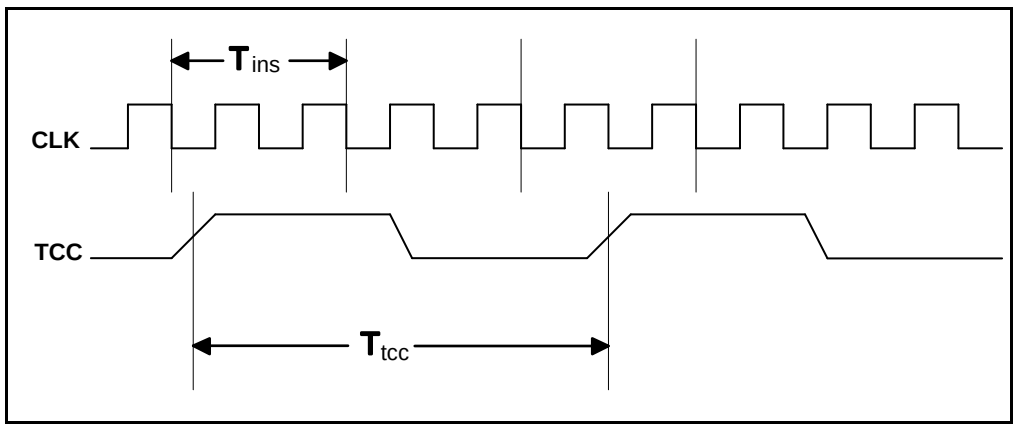
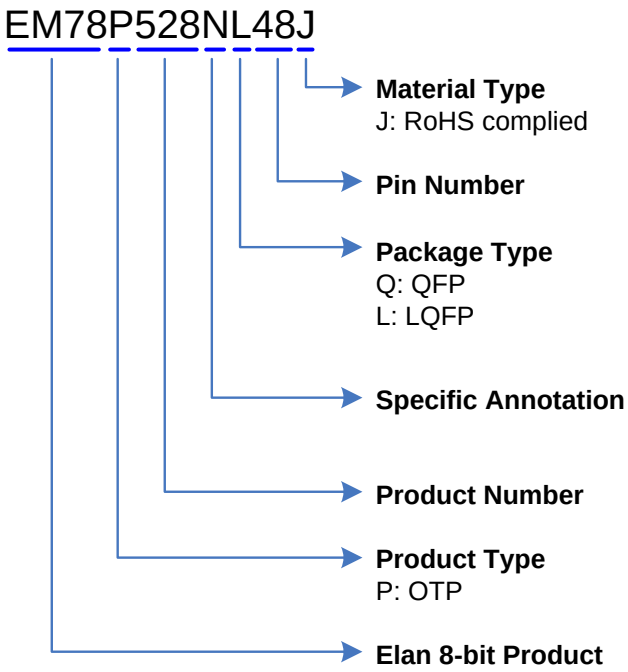


Figure 10-1c TCC Input Timing Diagram

APPENDIX

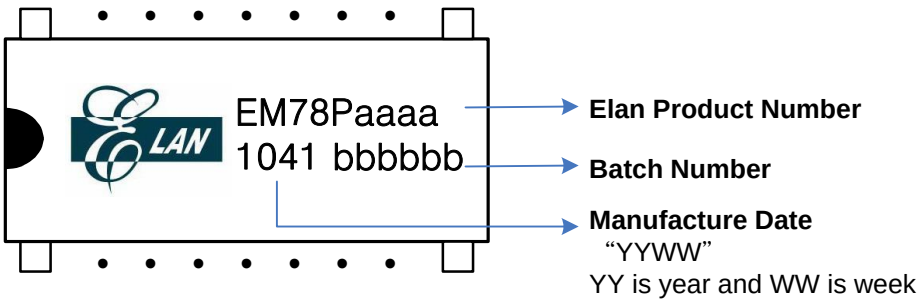
A Ordering and Manufacturing Information



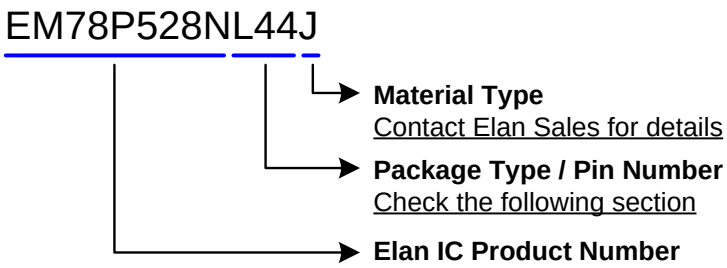
For example:

EM78P528NL48J

is EM78P528N with OTP program memory, product,
in 48-pin LQFP 7x7mm package with RoHS complied



Ordering Code



B Package Type

OTP MCU	Package Type	Pin Count	Package Size
EM78P528NQ44	QFP	44	10 mm × 10 mm
EM78P528NL44	LQFP	44	10 mm × 10 mm
EM78P528NL48	LQFP	48	7 mm × 7 mm

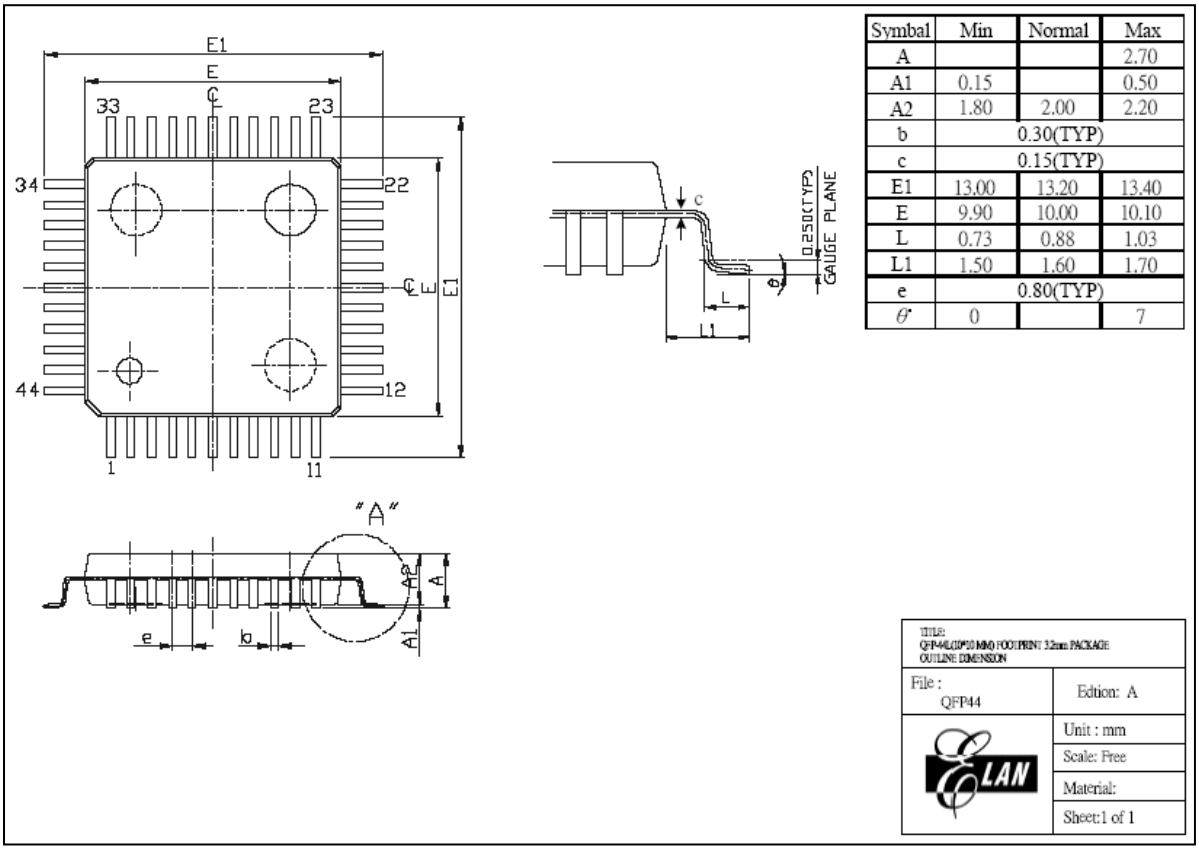
These are Green products which do not contain hazardous substances and comply with the third edition of Sony SS-00259 standard.

Pb content is less than 100ppm and complies with Sony specifications.

Part No.	EM78P528NxJ / xS
Electroplate type	Pure Tin
Ingredient (%)	Sn:100%
Melting point (°C)	232°C
Electrical resistivity (μΩ-cm)	11.4
Hardness (hv)	8~10
Elongation (%)	>50%

C Package Information

C.1 EM78P528NQ44

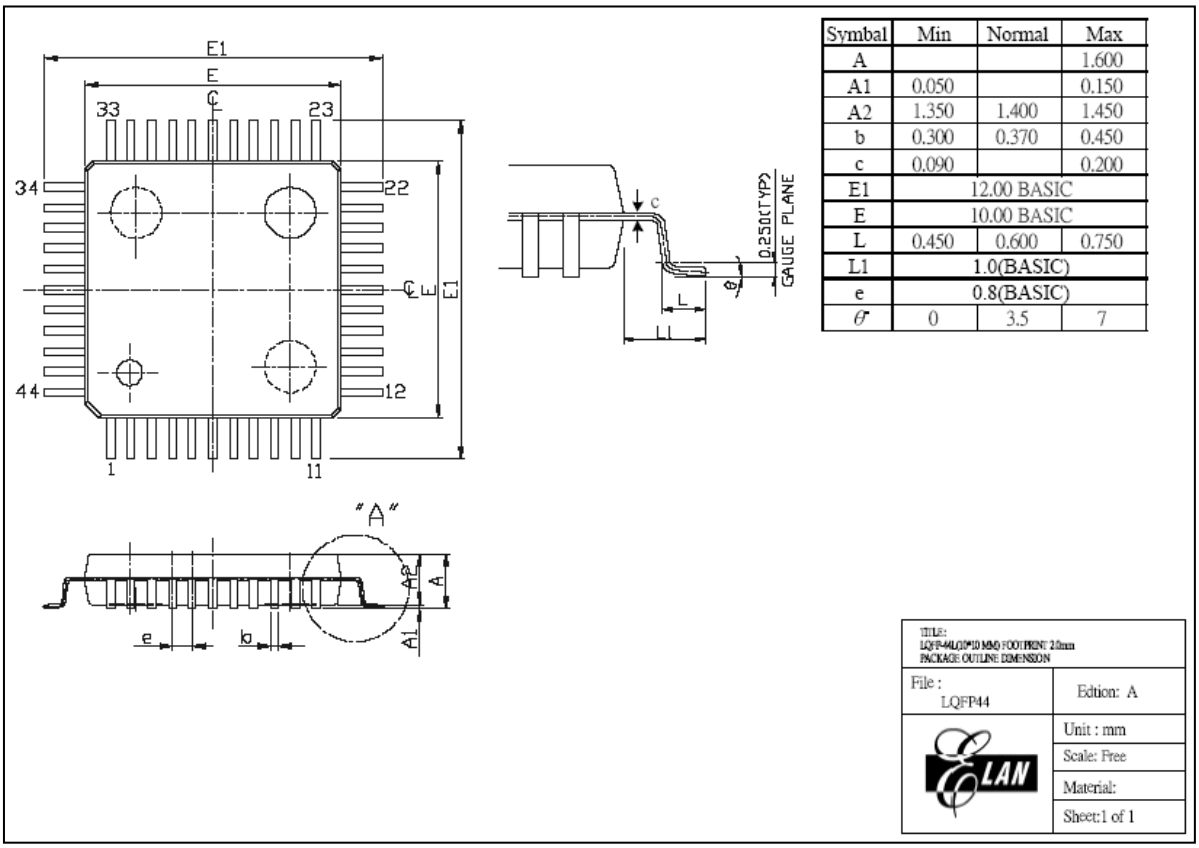


Symbal	Min	Normal	Max
A			2.70
A1	0.15		0.50
A2	1.80	2.00	2.20
b		0.30(TYP)	
c		0.15(TYP)	
E1	13.00	13.20	13.40
E	9.90	10.00	10.10
L	0.73	0.88	1.03
L1	1.50	1.60	1.70
e		0.80(TYP)	
θ	0		7

TITLE: QFP-44L(10*10 MM) FOOTPRINT 3.2mm PACKAGE OUTLINE DIMENSION	
File : QFP44	Edition: A
	Unit : mm
	Scale: Free
	Material:
	Sheet:1 of 1

Figure B-1 EM78P528N 44-pin QFP Package Type

C.2 EM78P528NL44



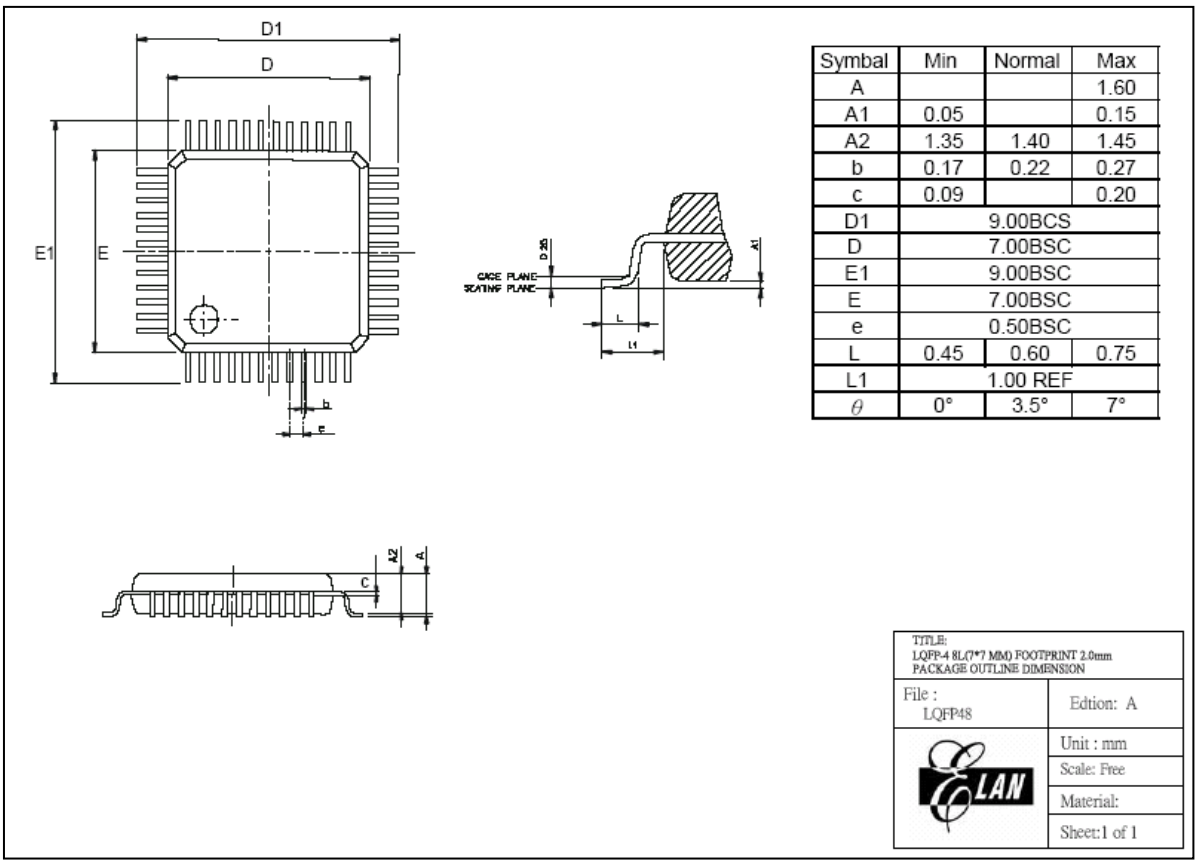
Symbal	Min	Normal	Max
A			1.600
A1	0.050		0.150
A2	1.350	1.400	1.450
b	0.300	0.370	0.450
c	0.090		0.200
E1	12.00 BASIC		
E	10.00 BASIC		
L	0.450	0.600	0.750
L1	1.0(BASIC)		
e	0.8(BASIC)		
θ	0	3.5	7

TITLE:
LQFP-44L(10*10 MM) FOOTPRINT 2.0mm
PACKAGE OUTLINE DIMENSION

File : LQFP44	Edtion: A
	Unit : mm
	Scale: Free
	Material:
	Sheet:1 of 1

Figure B-2 EM78P528N 44-pin LQFP Package Type

C.3 EM78P528NL48



Symbal	Min	Normal	Max
A			1.60
A1	0.05		0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c	0.09		0.20
D1		9.00BCS	
D		7.00BSC	
E1		9.00BSC	
E		7.00BSC	
e		0.50BSC	
L	0.45	0.60	0.75
L1		1.00 REF	
θ	0°	3.5°	7°

Figure B-3 EM78P528N 48-pin LQFP Package Type

D Quality Assurance and Reliability

Test Category	Test Conditions	Remarks
Solderability	Solder temperature=245±5°C, for 5 seconds up to the stopper using a rosin-type flux	
Pre-condition	Step 1: TCT, 65°C (15 min)~150°C (15 min), 10 cycles	For SMD IC (such as SOP, QFP, SOJ, etc)
	Step 2: Bake at 125°C, TD (endurance)=24 hrs	
	Step 3: Soak at 30°C/60% , TD (endurance)=192 hrs	
	Step 4: IR flow 3 cycles (Pkg thickness ≥ 2.5mm or Pkg volume ≥ 350 mm^3 ----225±5°C) (Pkg thickness ≤ 2.5 mm or Pkg volume ≤ 350 mm^3 ----240±5°C)	
Temperature cycle test	-65°C (15mins)~150°C (15min), 200 cycles	
Pressure cooker test	TA =121°C, RH=100%, pressure = 2 atm, TD (endurance)= 96 hrs	
High temperature / High humidity test	TA=85°C , RH=85% , TD (endurance)=168 , 500 hrs	
High-temperature storage life	TA=150°C, TD (endurance)=500, 1000 hrs	
High-temperature operating life	TA=125°C, VDD=Max. operating voltage, TD (endurance) =168, 500, 1000 hrs	
Latch-up	TA=25°C, VDD=Max. operating voltage, 800mA/40V	
ESD (HBM)	TA=25°C, ≥ | ± 4KV |	IP_ND,OP_ND,IO_ND IP_NS,OP_NS,IO_NS IP_PD,OP_PD,IO_PD, IP_PS,OP_PS,IO_PS, VDD-VSS(+),VDD_VSS(-) mode
ESD (MM)	TA=25°C, ≥ | ± 400V |	

D.1 Address Trap Detect

An address trap detect is one of the MCU embedded fail-safe functions that detects MCU malfunction caused by noise or the like. Whenever the MCU attempts to fetch an instruction from a certain section of ROM, an internal recovery circuit is auto started. If a noise caused address error is detected, the MCU will repeat execution of the program until the noise is eliminated. The MCU will then continue to execute the next program.

E EM78P528N Program Pin List

UWTR is used to program the EM78P528N IC's. The UWTR connector is selected by UWTR-ADP050-C. The software is selected by EM78P528N.

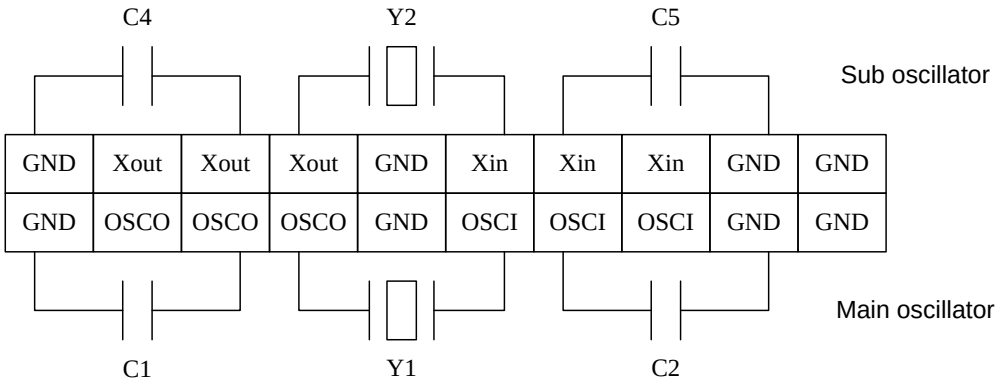
Program Pin Name	IC Pin Name	LQFP-48 Pin Number	L/QFP-44 Pin Number
CLK	P50	2	2
DATA	P51	3	3
VDD	VDD	5	5
VSS	VSS	6	6
VPP	/RESET2	9	9

F ICE 400 Oscillator Circuit (JP3)

F.1 Mode 1

Main oscillator : Crystal mode

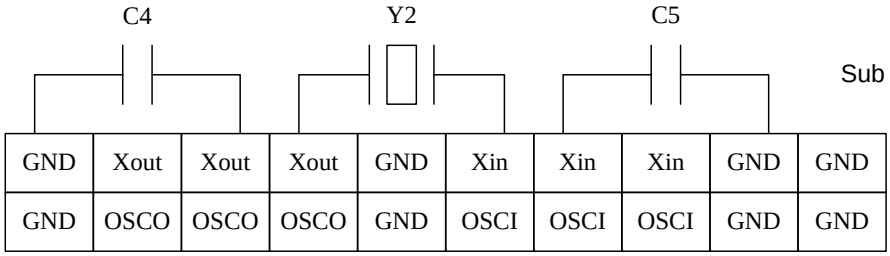
Sub oscillator : Crystal mode



F.2 Mode 2

Main oscillator : IRC mode

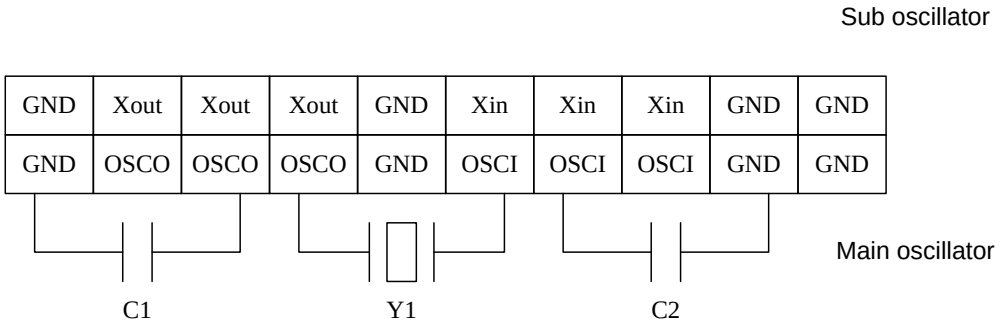
Sub oscillator : Crystal mode



F.3 Mode 3

Main oscillator : Crystal mode

Sub oscillator : IRC mode



F.4 Mode 4

Main oscillator : IRC mode

Sub oscillator : IRC mode