

Preliminary

GENERAL DESCRIPTION

The EM83040A is a dot matrix LCD driver which is fabricated by low power CMOS technology. This chip includes 80- bits shift register , 80 bits data latch and 80 bits level driver. A LCD RAM inside can be mapping to LCD signal. It converts RAM data to parallel data and output lcd waveform to LCD.

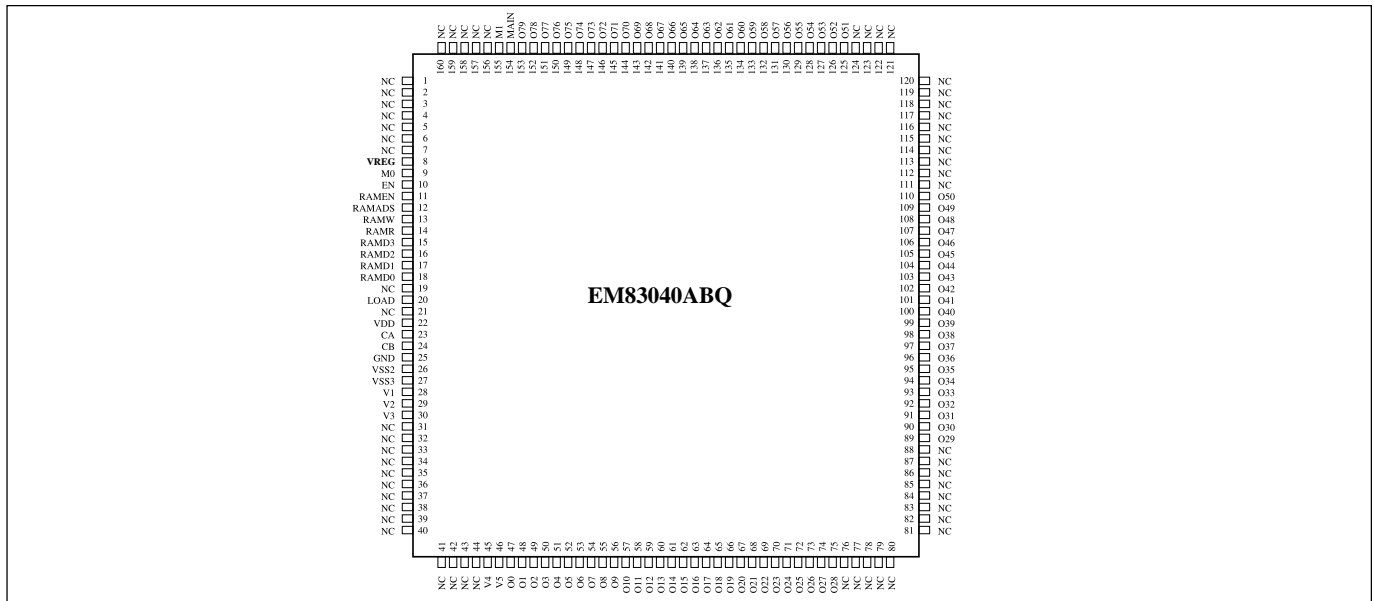
FEATURES

- (1) Supply power 2.6~6V
- (2) Internal RAM : 2.5k x 4 bits
- (3) RAM can be controlled by eight signals including four bit data bus.
- (4) LCD drive voltage :<13V
- (5) Duty: 1/32, 1/48, 1/80
- (6) Build in DC converter double and triple
- (7) Modularized function: connect to another 83040 to extent LCD matrix
- (8) One DC converter enabled and other 83040 can shared with this.
- (9) Internal regulator output for DC converter controlled by control register. (2.5V to 4.6V, 8 level)
- (10) Chip form (EM83040AH), 128 pin package (14mmx20mm EM83040AAQ), 160 pin package (EM83040ABQ)
- (11) Bias : 1/5 for 32 common, 1/7 for 48 common, 1/9 for 80 common. Fixed by internal circuit.
- (12) Internal RC clock about 250 KHz.

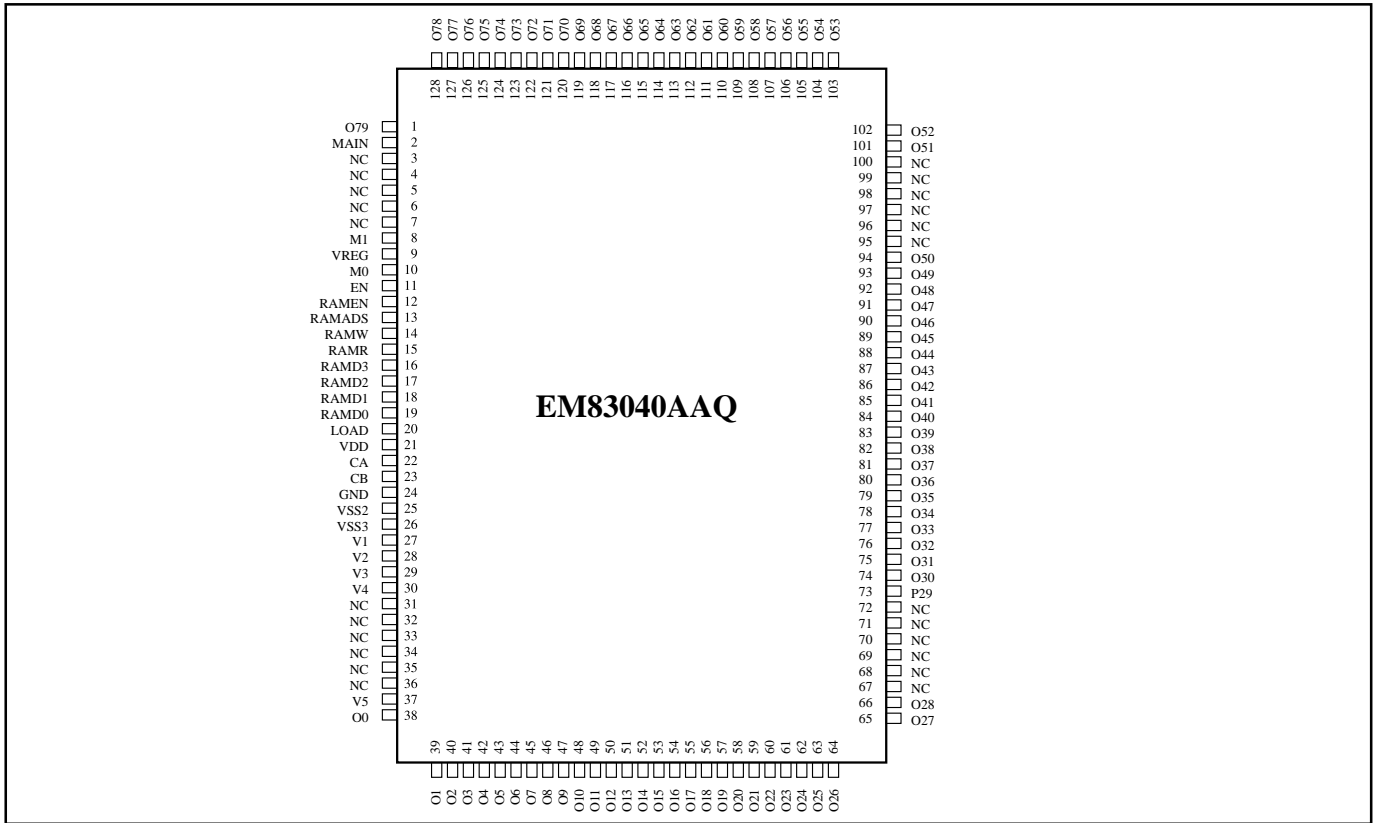
APPLICATION

- (1) Data Bank
- (2) LCD toy
- (3) Education computer

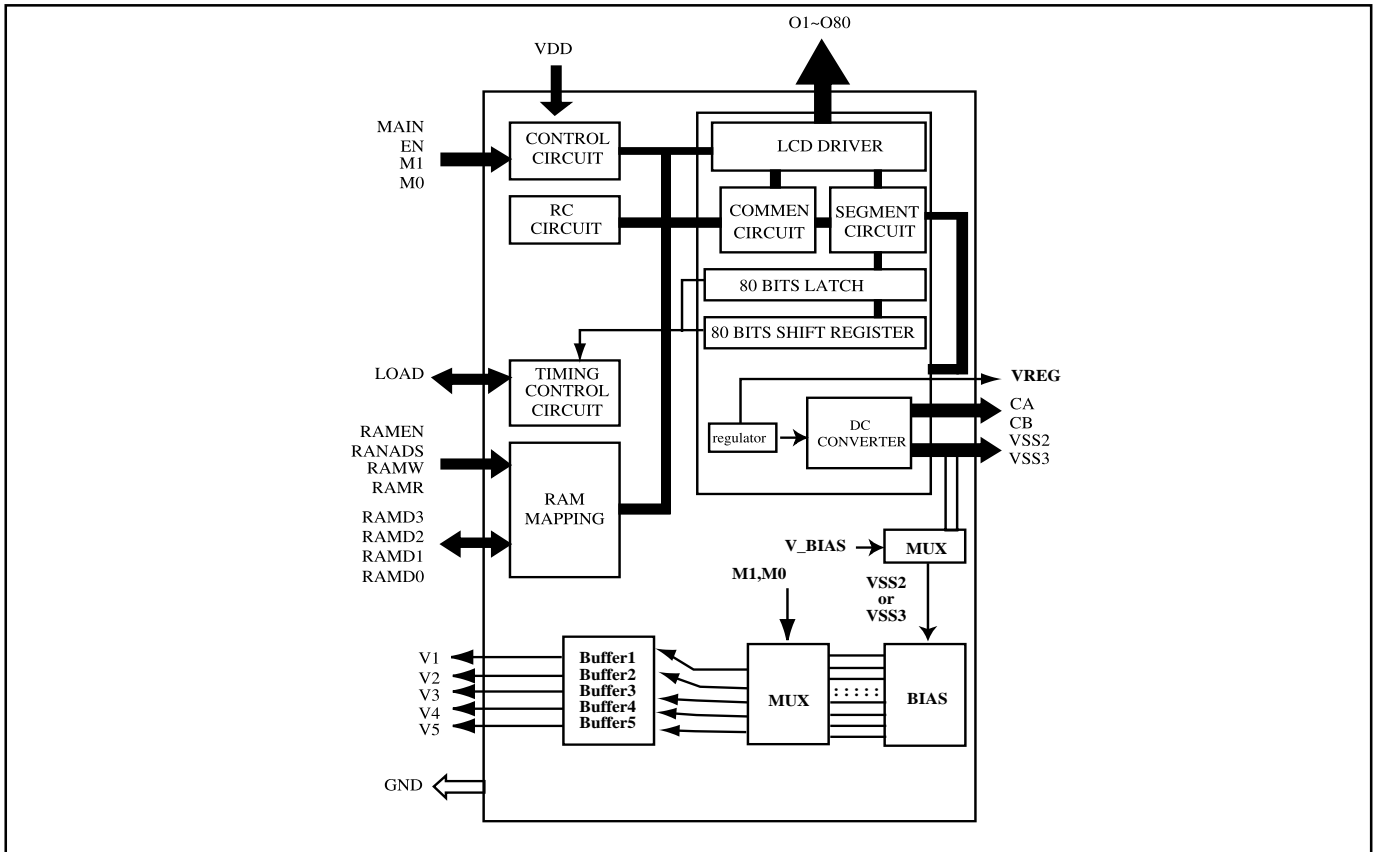
PIN ASSIGNMENTS



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BLOCK DIAGRAM



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PIN DESCRIPTIONS

| Symbol | I/O | Function |
|-------------|-------|--|
| VDD | Power | |
| GND | power | Ground |
| VSS3 | power | EN=0 and MAIN=1, 3*regulator output, EN=1 ,VSS3=VDD |
| VSS2 | Power | EN=0 and MAIN=1, 2*regulator output, EN=1, VSS2=VDD |
| MAIN | I | Master or slave control signal. MAIN=1 ,master unit MAIN=0 , slave unit |
| EN | I | This pin control whole chip power. This chip will work when this pin is connected to ground. And whole chip will disable when connect to VDD voltage. EN=0 and MAIN=1 the chip will generate VSS2, VSS3, LOAD signal and internal RC clock. EN=1, standby mode |
| M1 | I | Mode select |
| M0 | I | Mode select |
| RAMEN | | RAM read and write control signal. 1 => can not read and write. 0=> can read and write. |
| RAMADS | | RAM data select signal 1=> RAM Data , 0=>Address |
| RAMW | | RAM write signal, low write |
| RAMR | | RAM read signal, low read |
| RAMD3~RAMD0 | | RAM data or address bus |
| LOAD | I/O | LCD load signal between one COMMON signal to another . MAIN=1 , the master unit will output LOAD signal. MAIN=0 , the slave will accept the signal from master unit. |
| VREG | power | regulator output, connect a capacitor to ground. |
| CA | I | Coupling capacitor |
| CB | I | Coupling capacitor |
| V1~V5 | I | Reference voltage input ,highest V1..lowest V5 |
| O1~O80 | O | LCD waveform output |

FUNCTION DESCRIPTIONS

(1)User can use MAIN pin to chose master unit or slave unit.

| MAIN | Unit | Function |
|------|--------|---|
| 1 | MASTER | Generate these signals Load, VSS2, VSS3, Internal RC clock |
| 0 | SLAVE | Accept these signals Load, V1, V2, V3, V4, V5 |

(2)User can use M1,M2 to chose four modes. As followed

| MASTER | MAIN | M1 | M0 | Segment | Common | Bias |
|--------|------|----|----|-------------------|------------------|------|
| Mode1 | 1 | 0 | 0 | Reserved for test | | |
| Mode2 | 1 | 0 | 1 | | O(80:1)=C(80:1) | 1/9 |
| Mode3 | 1 | 1 | 0 | O(32:1)=S(32:1) | O(80:33)=C(48:1) | 1/7 |
| Mode4 | 1 | 1 | 1 | O(48:1)=S(48:1) | O(80:49)=C(32:1) | 1/5 |

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| SLAVE | MAIN | M1 | M0 | Segment | Common | |
|-------|------|----|----|-------------------|--------|-----|
| Mode1 | 0 | 0 | 0 | Reserved for test | | |
| Mode2 | 0 | 0 | 1 | O(80:1)=S(80:1) | | 1/9 |
| Mode3 | 0 | 1 | 0 | O(80:1)=S(80:1) | | 1/7 |
| Mode4 | 0 | 1 | 1 | O(80:1)=S(80:1) | | 1/5 |

* S=Segment, C=common

* (M1, M0) for master must same as slave unit.

(3)RAM control

Writer mode

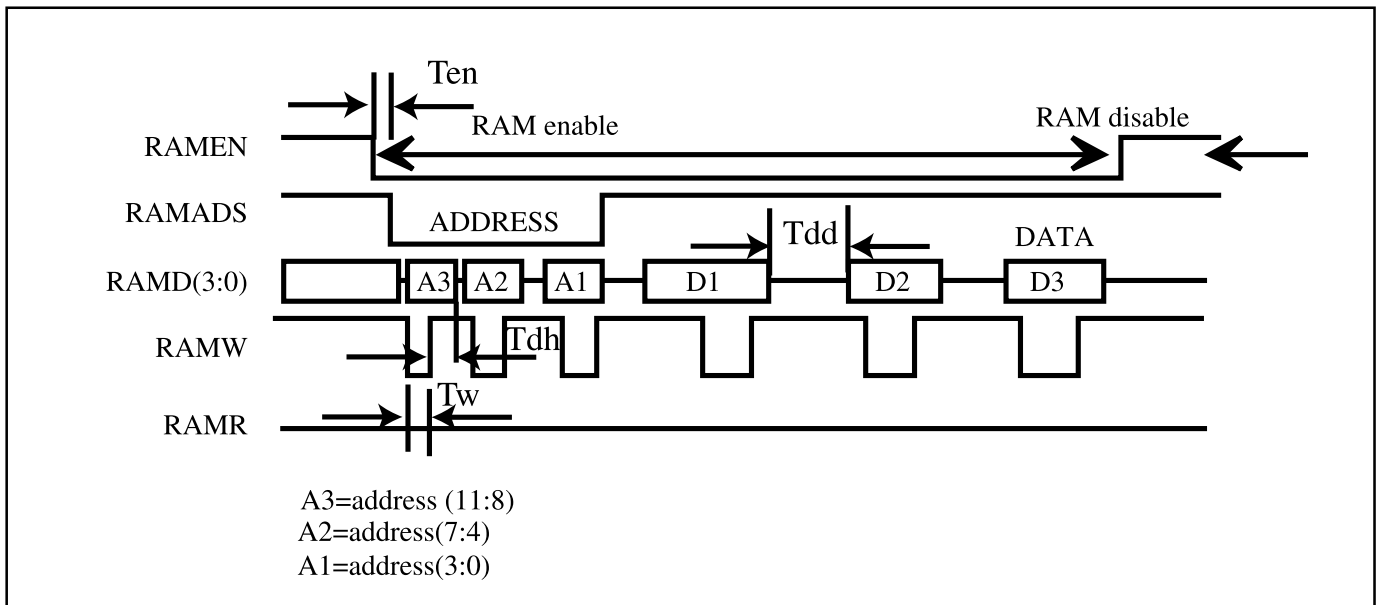


Fig.3

LCD RAM can be written or read with control signal. The RAMEN pin can select a RAM which can be read or write . The RAMADS pin can select whether RAMD(3:0) are data or address of RAM. At the address mode , RAMADS is low and user should sent address three times. From address (11:8) to address (3:0). Then it will go into data mode when RAMADS is high. In data mode , user can sent one or more nibble data which address can be increased by internal counter.

Once the RAMEN pin is high, the RAM can not read and write.

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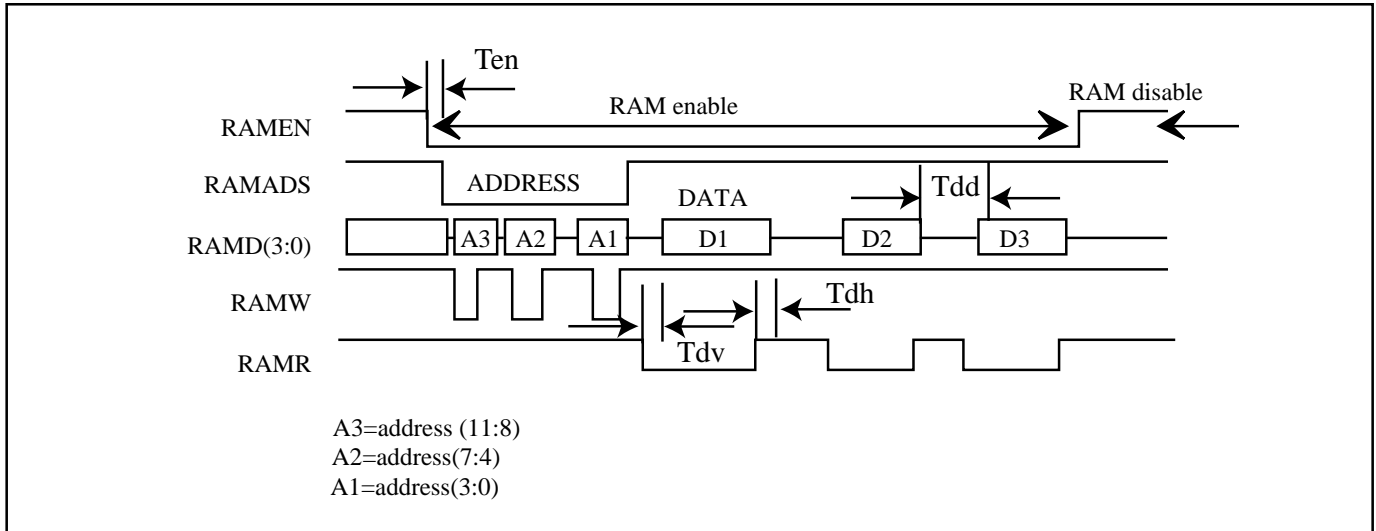


Fig.4

As same as write mode , user has to sent address three times. And read data from RAM one by one which address can be increased by internal counter. NOTE!! Be sure to make RAMR low pulse 2 μ S (T_{dv} +data) width and 2 μ S (T_{dd}) high width at least.

(5) RAM mapping

RAM address is from 0 to address 2559

User fill “1” to LCD RAM , LCD driver will generate “light” waveform. Otherwise , it will generate a “dark” waveform. The LCD RAM area is mapped to segment 1 to segment 80 from address 0 to address 19. And user can refer to fig.5 to get the idea of LCD ram mapping. The other RAM can use as general RAM for data storage. And the RAM of address 2560 is a control register.

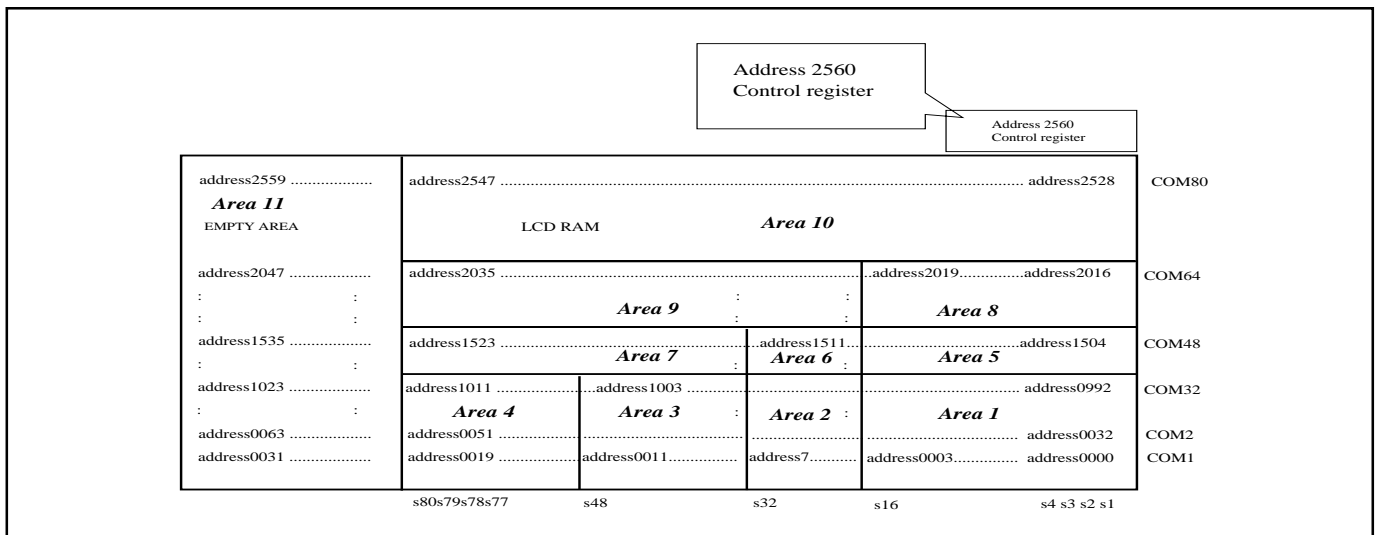
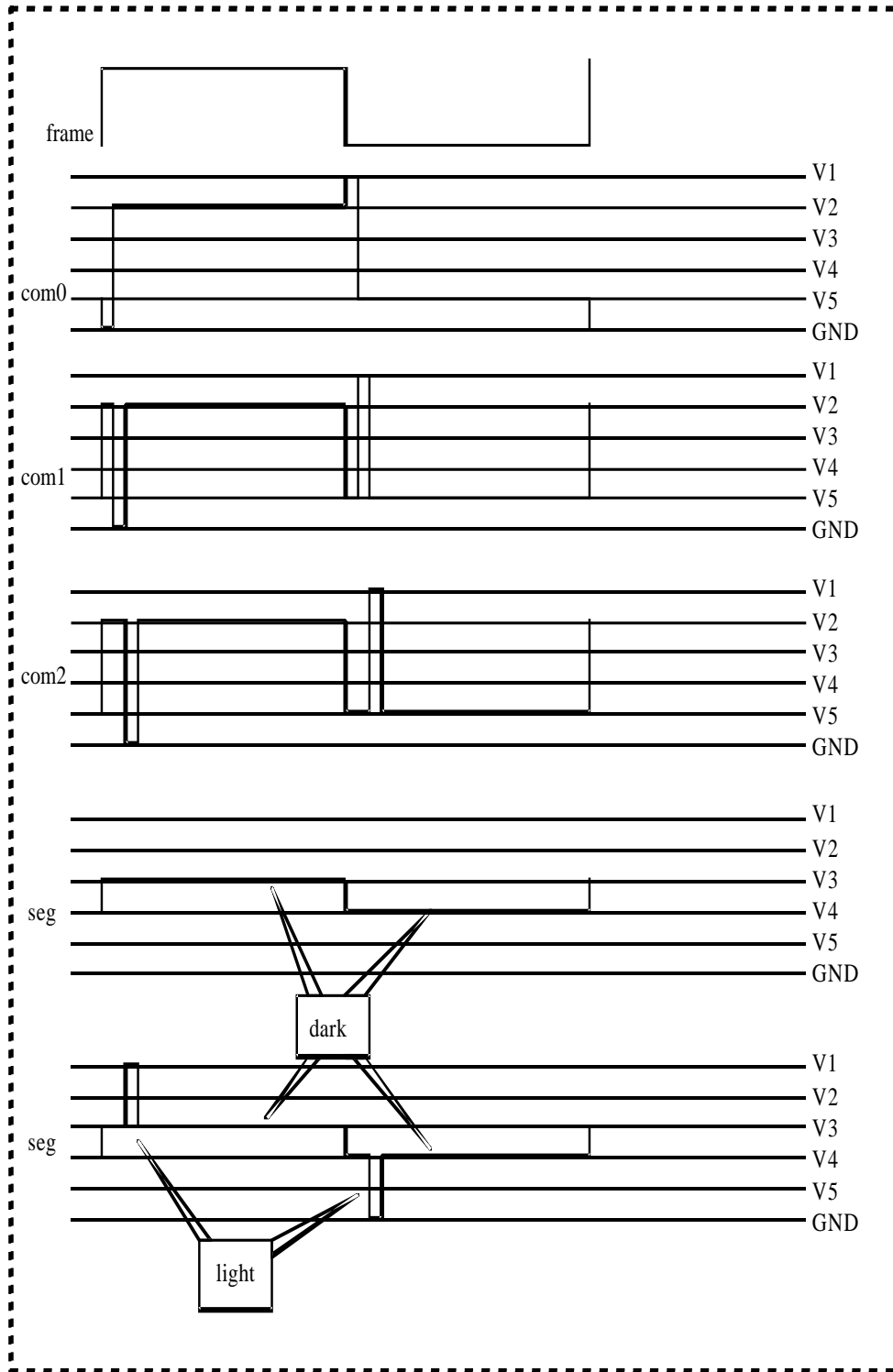


Fig.5

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(6) LCD waveform



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(7) Control register

| Address | Bit3 | Bit2 | Bit1 | Bit0 |
|---------|--------|------------|------------|------------|
| 2560 | V_BIAS | Regulator2 | Regulator1 | regulator0 |

Initial : 0000

Bit2,1,0 : internal regulator output selection.

| (regulator2, regulator1, regulator0) | Output voltage |
|--------------------------------------|----------------|
| (0,0,0) | 2.5V |
| (0,0,1) | 2.8V |
| (0,1,0) | 3.1V |
| (0,1,1) | 3.4V |
| (1,0,0) | 3.7V |
| (1,0,0) | 4.0V |
| (1,1,0) | 4.3V |
| (1,1,1) | 4.6V |

Bit3 : internal Bias voltage selection

| (V_BIAS) | BIAS voltage |
|----------|--------------|
| 0 | VSS2 |
| 1 | VSS3 |

Bias from V1 to V5

| | 1/5 bias V_BIAS=0 | 1/5 bias V_BIAS=1 | 1/7 bias V_BIAS=0 | 1/7 bias V_BIAS=1 | 1/9 bias V_BIAS=0 | 1/9 bias V_BIAS=1 |
|----|------------------------|------------------------|------------------------|------------------------|------------------------|------------------------|
| V1 | V2 | V3 | V2 | V3 | V2 | V3 |
| V2 | $V2 \cdot \frac{4}{5}$ | $V3 \cdot \frac{4}{5}$ | $V2 \cdot \frac{6}{7}$ | $V3 \cdot \frac{6}{7}$ | $V2 \cdot \frac{8}{9}$ | $V3 \cdot \frac{8}{9}$ |
| V3 | $V2 \cdot \frac{3}{5}$ | $V3 \cdot \frac{3}{5}$ | $V2 \cdot \frac{5}{7}$ | $V3 \cdot \frac{5}{7}$ | $V2 \cdot \frac{7}{9}$ | $V3 \cdot \frac{7}{9}$ |
| V4 | $V2 \cdot \frac{2}{5}$ | $V3 \cdot \frac{2}{5}$ | $V2 \cdot \frac{2}{7}$ | $V3 \cdot \frac{2}{7}$ | $V2 \cdot \frac{2}{9}$ | $V3 \cdot \frac{2}{9}$ |
| V5 | $V2 \cdot \frac{1}{5}$ | $V3 \cdot \frac{1}{5}$ | $V2 \cdot \frac{1}{7}$ | $V3 \cdot \frac{1}{7}$ | $V2 \cdot \frac{1}{9}$ | $V3 \cdot \frac{1}{9}$ |

* $V2 = VREG \cdot 2 \cdot 97\%$

* $V3 = VREG \cdot 3 \cdot 95\%$

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ABSOLUTE MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|-----------------------------|-----------------|------------------------------|------|
| DC SUPPLY VOLTAGE | V+ | <6 | V |
| INPUT VOLTAGE | V _{in} | -0.5 TO V _{DD} ±0.5 | V |
| OPERATING TEMPERATURE RANGE | T _a | 0 TO 70 | °C |

DC ELECTRICAL CHARACTERISTICS (T_A=0°C ~ 70°C, V_{DD}=3V±5%, V_{SS}=0V)

| Parameter | Sym. | Min. | Typ. | Max. | Unit | Condition |
|--------------------------------|-------------------|-------|------|-------|------|--|
| Input High voltage | V _{IH} | 2.0 | | | V | |
| Input Low current | V _{IL} | | | 0.8 | V | |
| Output High current | I _{OH} | 100 | | | μA | V _{DD} =3V |
| Input high voltage | I _{OL} | -100 | | | μA | V _{DD} =3V |
| Standby current | I _{SD} | | 1 | 4 | μA | EN=1 |
| Output high voltage | I _{OP} | | 130 | 160 | μA | EN=0, MAIN =1(MASTER) , DC converter enable, INPUT=VDD 250kHz clock, No load |
| | | | 40 | 70 | μA | EN=0 . MAIN =0 (SLAVE) , DC converter disable, INPUT=VDD 250kHz clock, No load |
| Current of a buffer (V1 to V5) | I _{buf} | 4 | 6 | 10 | μA | |
| Voltage variation of regulator | V _{reg} | V-0.1 | V | V+0.1 | V | |
| Regulator current | I _{reg} | | 10 | 15 | μA | |
| Internal Bias resistor | R _{bias} | 1800 | 2000 | 2200 | kΩ | |

AC ELECTRICAL CHARACTERISTICS

| Parameter | Sym. | Min. | Typ. | Max. | Unit |
|-------------------|--------------------|------|------|------|------|
| RC clock variable | V _{rc} | -20 | | +20 | % |
| Frame period | T _{frame} | | 1/64 | | S |
| Load period | T _{load} | | 31 | | μS |
| Enable time | T _{en} | 30 | | | μS |
| Write low pulse | T _w | 2 | | | μS |
| Data hold time | T _{dh} | 500 | | | nS |
| Data to data time | T _{dd} | 2 | | | μS |
| Data valid time | T _{dv} | 1500 | | | nS |

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AC TIMING

LCD control timing

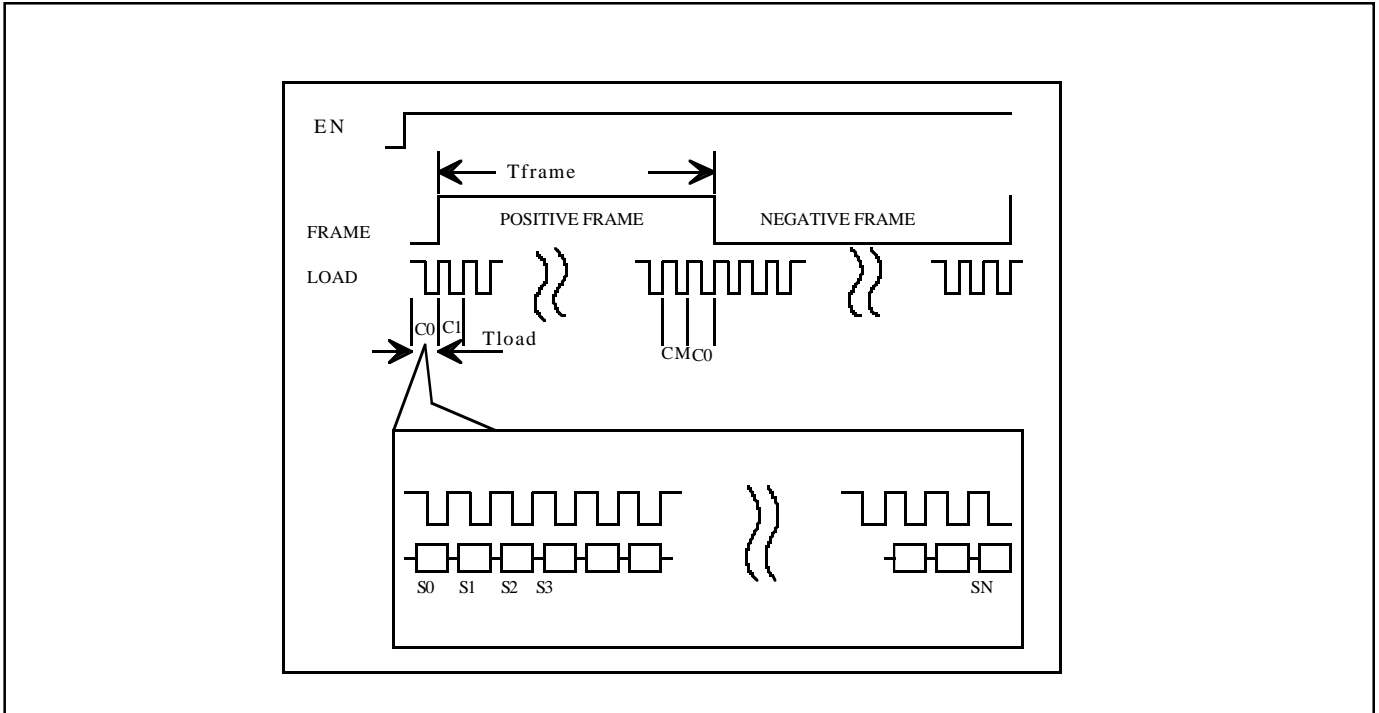


Fig .7

LCD RAM write mode

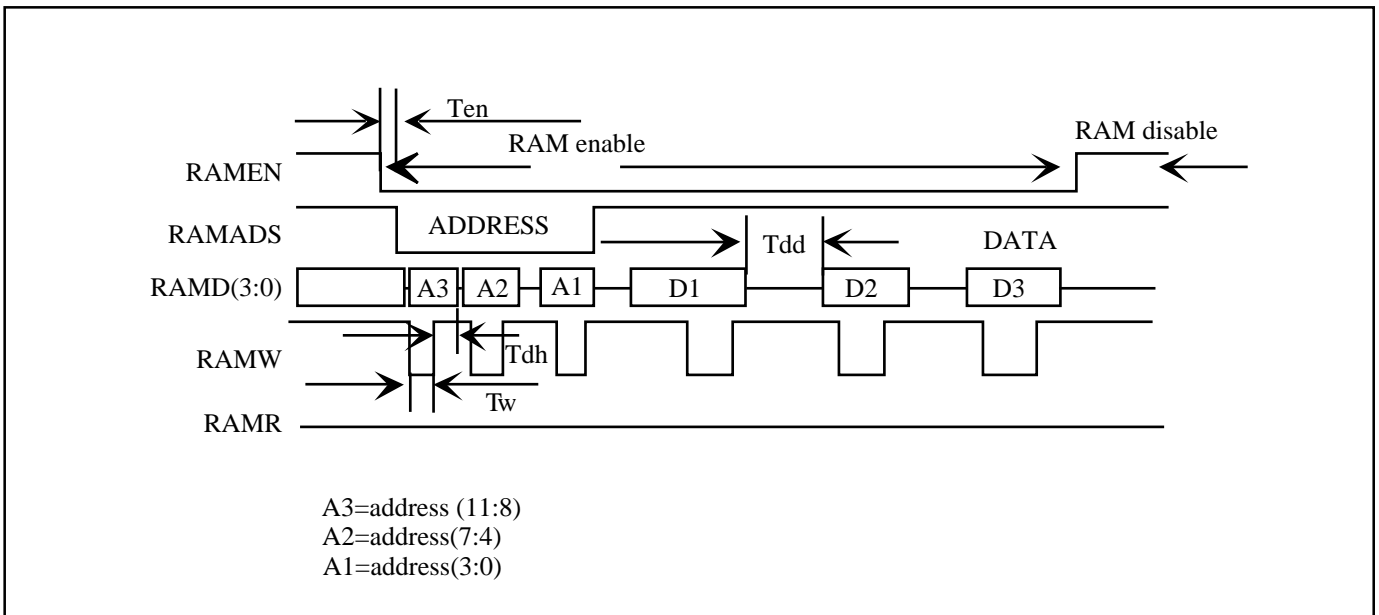


Fig .8

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LCD RAM read mode

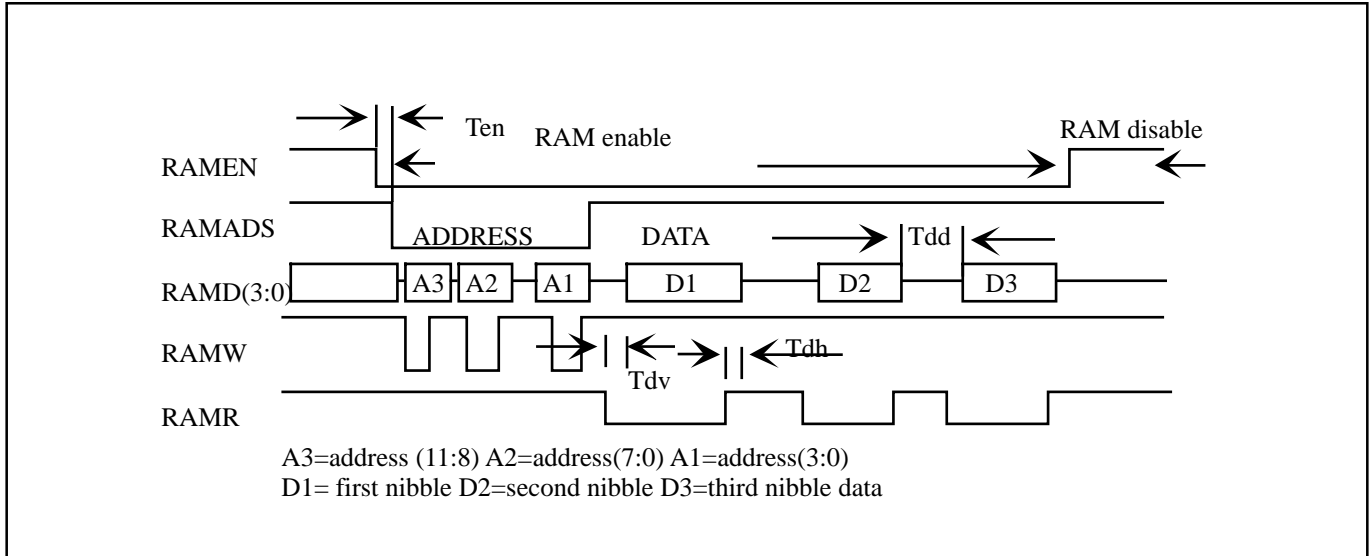


Fig .9

APPLICATION CIRCUIT

(1) C32 x S48

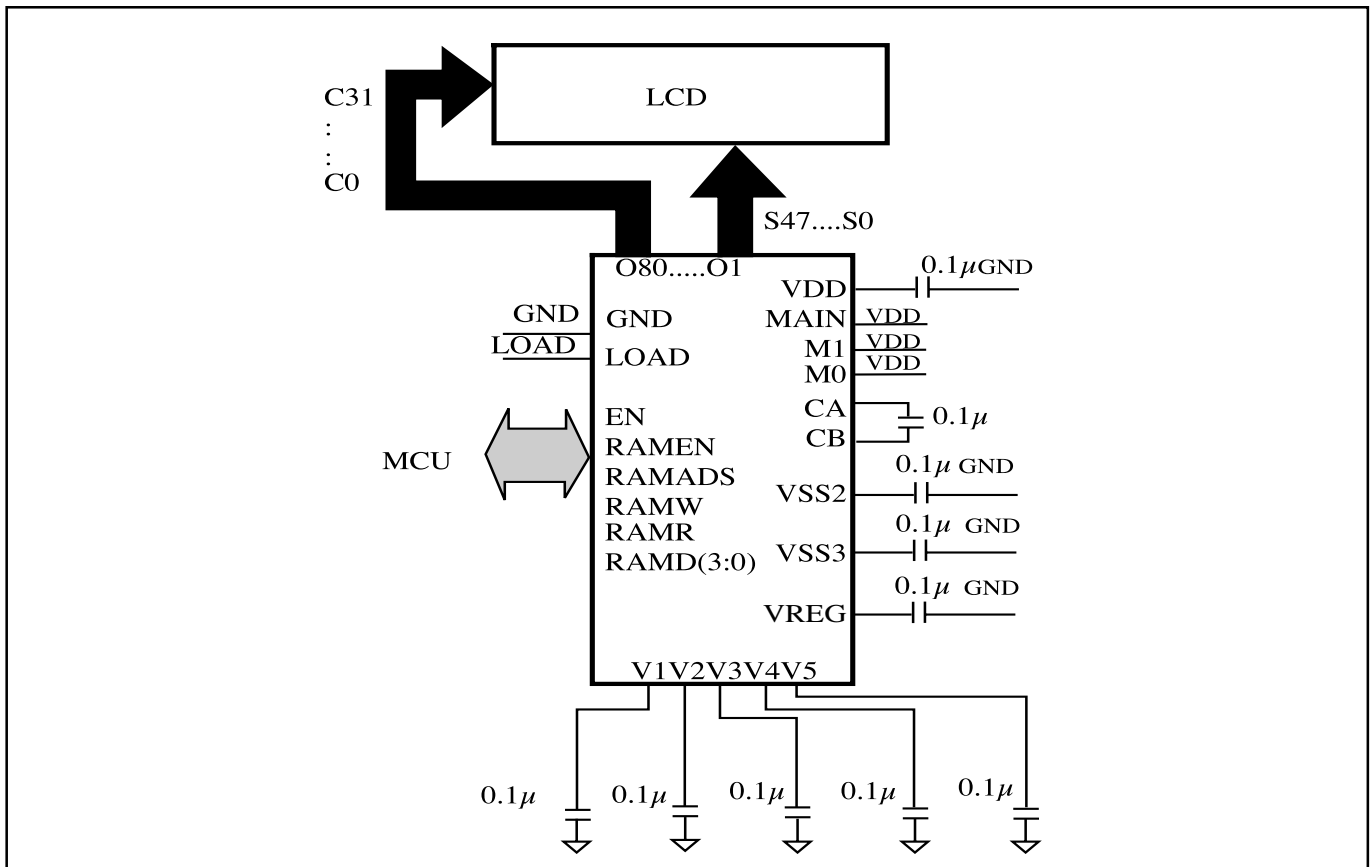


Fig .10

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(2) C32 x S128

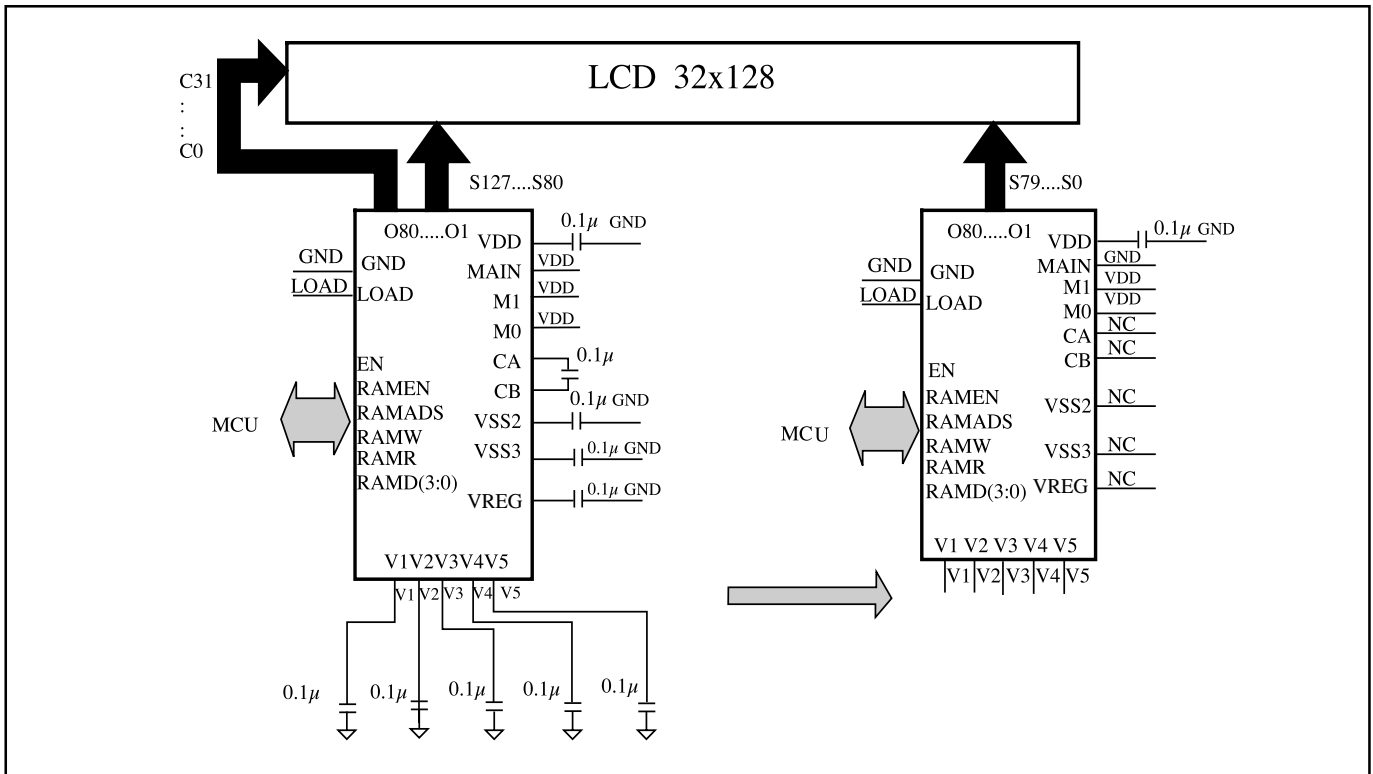


Fig .11

(3) C48 x S112

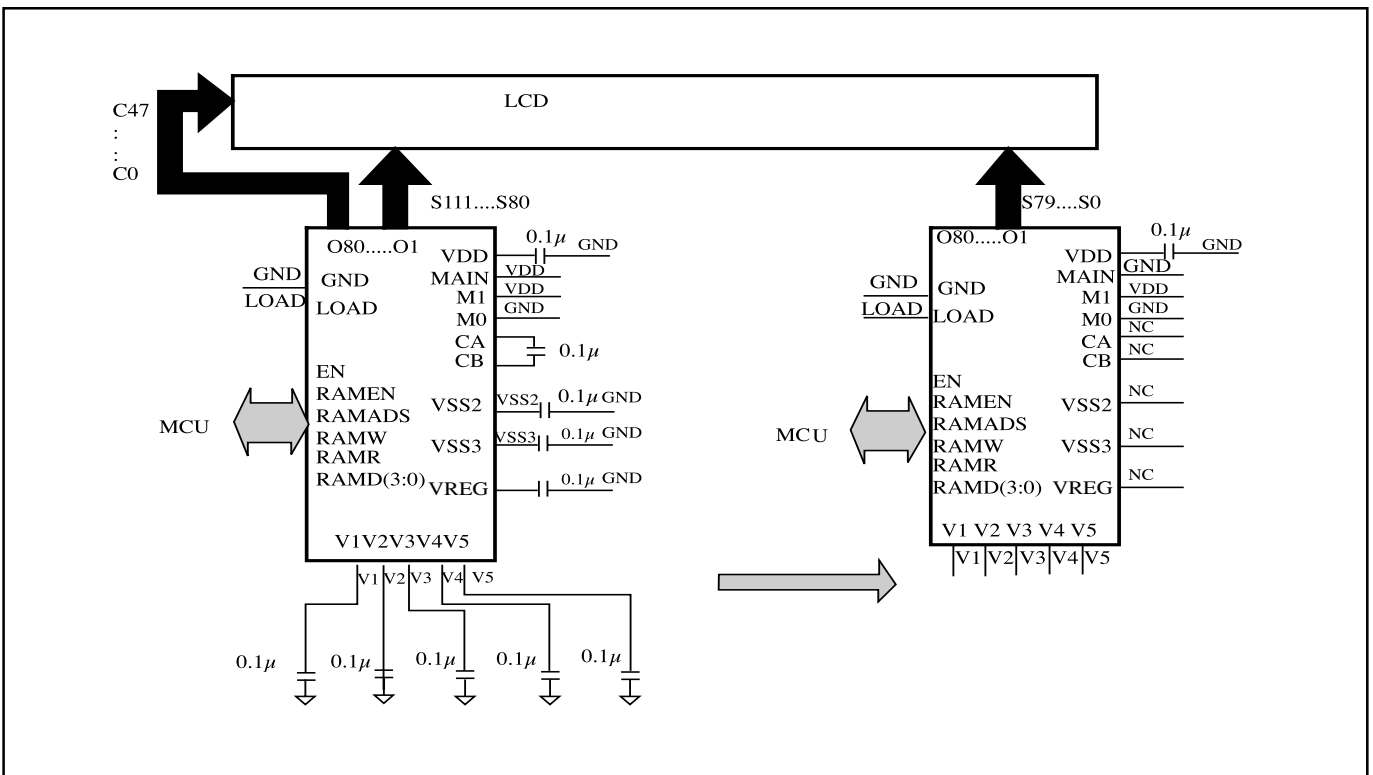


Fig .12

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(4) C80 x S160

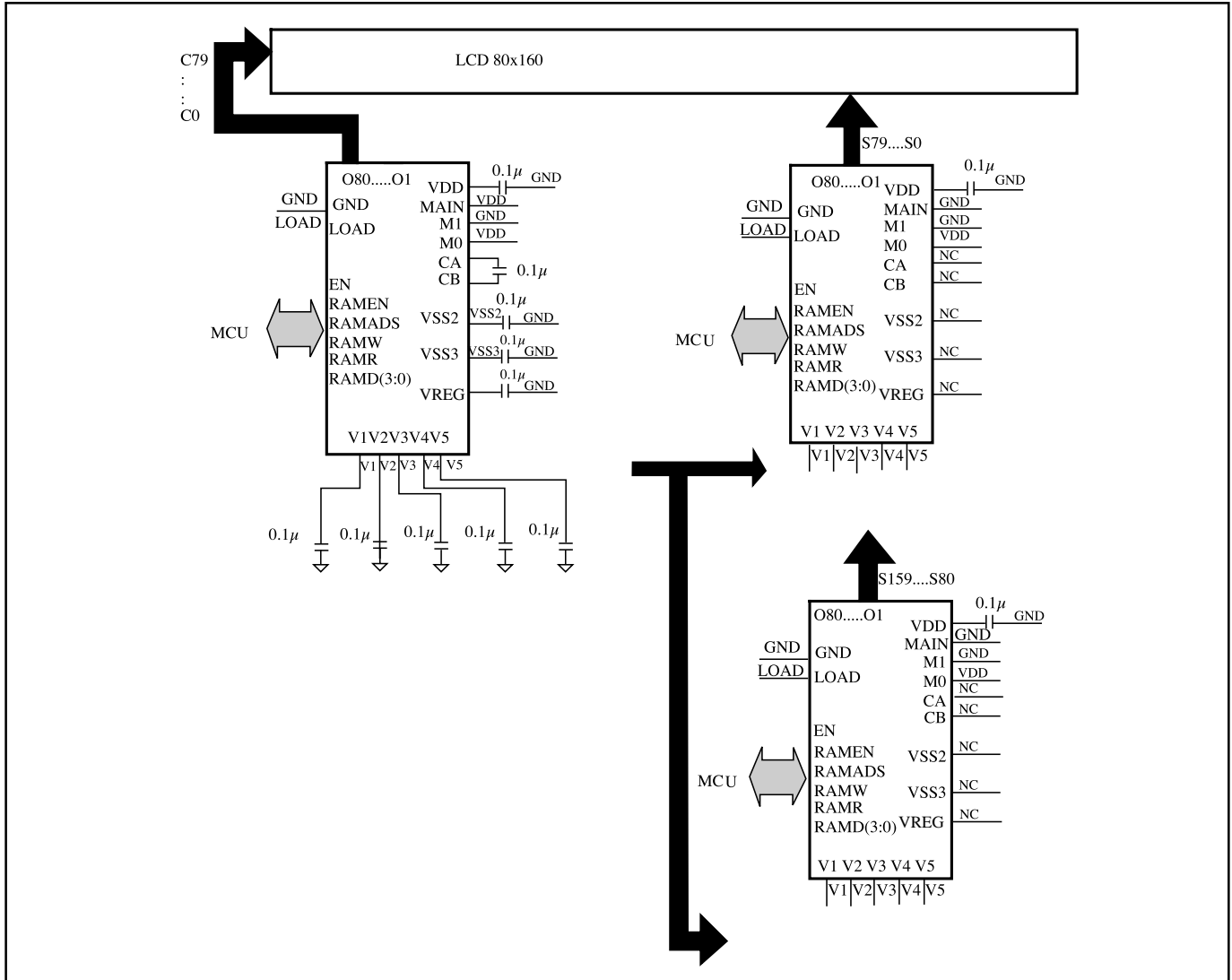
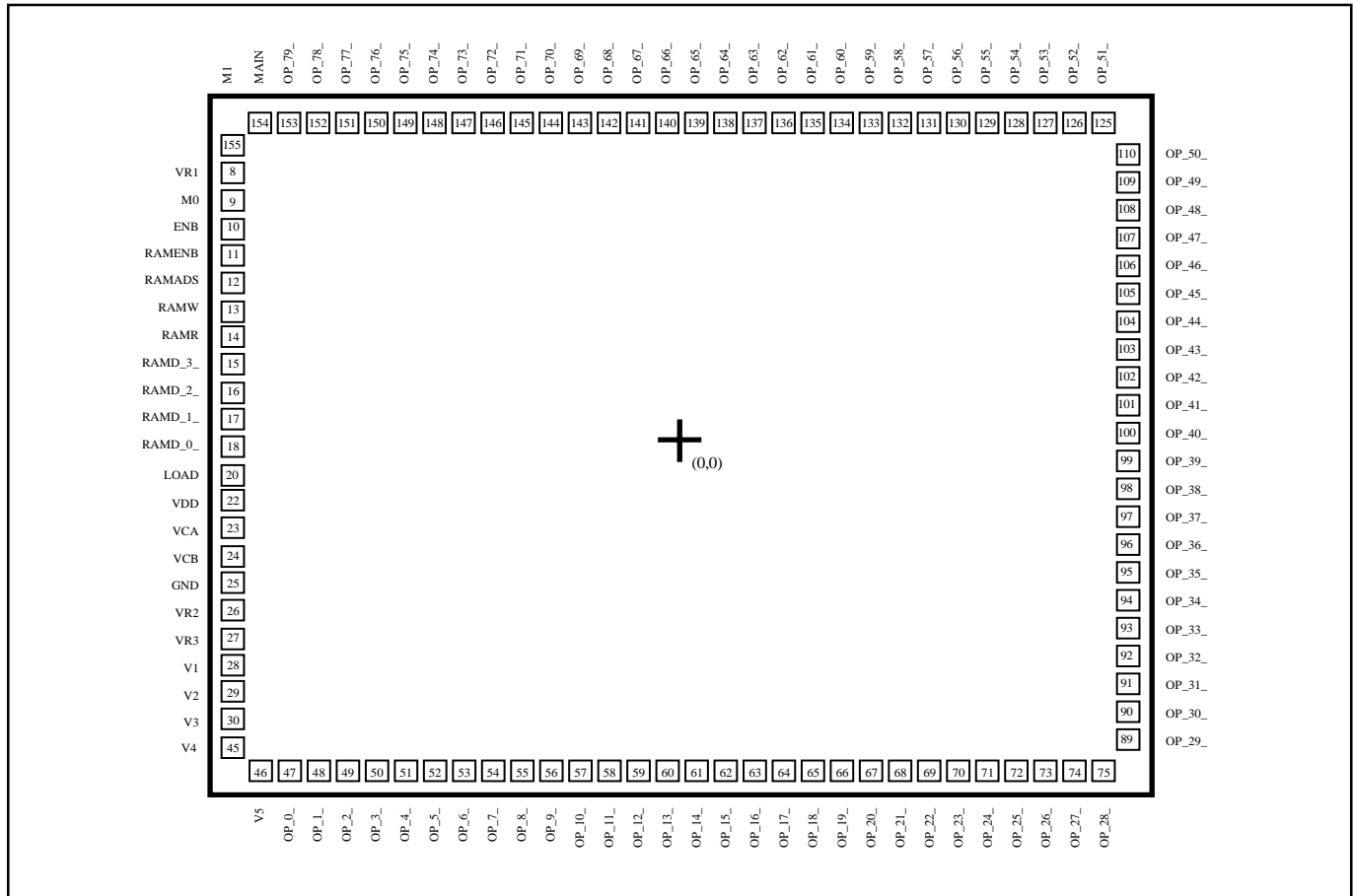


Fig .13

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PAD DIAGRAM



Chip Size : 3640 μm x 2800 μm

| Pad No. | Sym. | X | Y |
|---------|---------|---------|--------|
| 8 | VR1 | -1660.0 | 1062.5 |
| 9 | M0 | -1660.0 | 952.5 |
| 10 | ENB | -1660.0 | 842.5 |
| 11 | RAMENB | -1660.0 | 732.5 |
| 12 | RAMADS | -1660.0 | 627.5 |
| 13 | RAMW | -1660.0 | 522.5 |
| 14 | RAMR | -1660.0 | 417.5 |
| 15 | RAMD_3_ | -1660.0 | 312.5 |
| 16 | RAMD_2_ | -1660.0 | 207.5 |
| 17 | RAMD_1_ | -1660.0 | 102.5 |
| 18 | RAMD_0_ | -1660.0 | -2.5 |
| 20 | LOAD | -1660.0 | -107.5 |
| 22 | VDD | -1660.0 | -212.5 |
| 23 | VCA | -1660.0 | -317.5 |
| 24 | VCB | -1660.0 | -422.5 |
| 25 | GND | -1660.0 | -527.5 |
| 26 | VR2 | -1660.0 | -632.5 |
| 27 | VR3 | -1660.0 | -737.5 |
| 28 | V1 | -1660.0 | -842.5 |

* This specification are subject to be changed without notice.



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| Pad No. | Sym. | X | Y |
|---------|--------|---------|---------|
| 29 | V2 | -1660.0 | -952.5 |
| 30 | V3 | -1660.0 | -1062.5 |
| 45 | V4 | -1660.0 | -1172.5 |
| 46 | V5 | -1540.0 | -1240.0 |
| 47 | OP_0_ | -1430.0 | -1240.0 |
| 48 | OP_1_ | -1320.0 | -1240.0 |
| 49 | OP_2_ | -1210.0 | -1240.0 |
| 50 | OP_3_ | -1105.0 | -1240.0 |
| 51 | OP_4_ | -1000.0 | -1240.0 |
| 52 | OP_5_ | -895.0 | -1240.0 |
| 53 | OP_6_ | -790.0 | -1240.0 |
| 54 | OP_7_ | -685.0 | -1240.0 |
| 55 | OP_8_ | -580.0 | -1240.0 |
| 56 | OP_9_ | -475.0 | -1240.0 |
| 57 | OP_10_ | -370.0 | -1240.0 |
| 58 | OP_11_ | -265.0 | -1240.0 |
| 59 | OP_12_ | -160.0 | -1240.0 |
| 60 | OP_13_ | -55.0 | -1240.0 |
| 61 | OP_14_ | 50.0 | -1240.0 |
| 62 | OP_15_ | 155.0 | -1240.0 |
| 63 | OP_16_ | 260.0 | -1240.0 |
| 64 | OP_17_ | 365.0 | -1240.0 |
| 65 | OP_18_ | 470.0 | -1240.0 |
| 66 | OP_19_ | 575.0 | -1240.0 |
| 67 | OP_20_ | 680.0 | -1240.0 |
| 68 | OP_21_ | 785.0 | -1240.0 |
| 69 | OP_22_ | 890.0 | -1240.0 |
| 70 | OP_23_ | 995.0 | -1240.0 |
| 71 | OP_24_ | 1100.0 | -1240.0 |
| 72 | OP_25_ | 1205.0 | -1240.0 |
| 73 | OP_26_ | 1315.0 | -1240.0 |
| 74 | OP_27_ | 1425.0 | -1240.0 |
| 75 | OP_28_ | 1535.0 | -1240.0 |
| 89 | OP_29_ | 1660.0 | -1120.0 |
| 90 | OP_30_ | 1660.0 | -1010.0 |
| 91 | OP_31_ | 1660.0 | -900.0 |
| 92 | OP_32_ | 1660.0 | -790.0 |
| 93 | OP_33_ | 1660.0 | -685.0 |
| 94 | OP_34_ | 1660.0 | -580.0 |
| 95 | OP_35_ | 1660.0 | -475.0 |
| 96 | OP_36_ | 1660.0 | -370.0 |
| 97 | OP_37_ | 1660.0 | -265.0 |
| 98 | OP_38_ | 1660.0 | -160.0 |
| 99 | OP_39_ | 1660.0 | -55.0 |
| 100 | OP_40_ | 1660.0 | 50.0 |

* This specification are subject to be changed without notice.

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| Pad No. | Sym. | X | Y |
|---------|--------|---------|--------|
| 101 | OP_41_ | 1660.0 | 155.0 |
| 102 | OP_42_ | 1660.0 | 260.0 |
| 103 | OP_43_ | 1660.0 | 365.0 |
| 104 | OP_44_ | 1660.0 | 470.0 |
| 105 | OP_45_ | 1660.0 | 575.0 |
| 106 | OP_46_ | 1660.0 | 680.0 |
| 107 | OP_47_ | 1660.0 | 785.0 |
| 108 | OP_48_ | 1660.0 | 895.0 |
| 109 | OP_49_ | 1660.0 | 1005.0 |
| 110 | OP_50_ | 1660.0 | 1115.0 |
| 125 | OP_51_ | 1535.0 | 1240.0 |
| 126 | OP_52_ | 1425.0 | 1240.0 |
| 127 | OP_53_ | 1315.0 | 1240.0 |
| 128 | OP_54_ | 1205.0 | 1240.0 |
| 129 | OP_55_ | 1100.0 | 1240.0 |
| 130 | OP_56_ | 995.0 | 1240.0 |
| 131 | OP_57_ | 890.0 | 1240.0 |
| 132 | OP_58_ | 785.0 | 1240.0 |
| 133 | OP_59_ | 680.0 | 1240.0 |
| 134 | OP_60_ | 575.0 | 1240.0 |
| 135 | OP_61_ | 470.0 | 1240.0 |
| 136 | OP_62_ | 365.0 | 1240.0 |
| 137 | OP_63_ | 260.0 | 1240.0 |
| 138 | OP_64_ | 155.0 | 1240.0 |
| 139 | OP_65_ | 50.0 | 1240.0 |
| 140 | OP_66_ | -55.0 | 1240.0 |
| 141 | OP_67_ | -160.0 | 1240.0 |
| 142 | OP_68_ | -265.0 | 1240.0 |
| 143 | OP_69_ | -370.0 | 1240.0 |
| 144 | OP_70_ | -475.0 | 1240.0 |
| 145 | OP_71_ | -580.0 | 1240.0 |
| 146 | OP_72_ | -685.0 | 1240.0 |
| 147 | OP_73_ | -790.0 | 1240.0 |
| 148 | OP_74_ | -895.0 | 1240.0 |
| 149 | OP_75_ | -1000.0 | 1240.0 |
| 150 | OP_76_ | -1105.0 | 1240.0 |
| 151 | OP_77_ | -1210.0 | 1240.0 |
| 152 | OP_78_ | -1320.0 | 1240.0 |
| 153 | OP_79_ | -1430.0 | 1240.0 |
| 154 | MAIN | -1540.0 | 1240.0 |
| 155 | M1 | -1660.0 | 1172.5 |

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DESIGN NOTE : APPLICATION CIRCUIT WITH EXTERNAL CHARGE PUMP

