POWER MANAGEMENT CONTROLLER WITH MULTI-CELL SOLAR HARVESTING

Description

The EM8502 is an integrated power management solution for low power applications. It is designed to simplify the design of application using multiple solar cells in series that can be directly connected to the application and storage elements.

The device is designed to speed-up system start-up time when the main energy storage element (aka Long Term Storage – LTS) is completely discharged or insufficiently charged to supply the application, by using a secondary energy storage element (Short Term Storage - STS).

When solar energy is high enough the device connects the solar cell to STS or LTS to maintain the supply of the application, while charging the rechargeable element.

The EM8502 is capable of working with a variety of energy elements as secondary storage, namely re-chargeable batteries, super-capacitors or conventional capacitors. In all cases the EM8502 maintains its fast start-up capability that depends only on the harvester conditions and the STS capacitor value.

A USB connection to an external power source is available on the EM8502 for fast charge of the long term storage element.

The EM8502 integrates voltage supervisory functions. Minimum and maximum voltages are controlled on the LTS element to prevent damage to the energy storage element. Harvester minimum voltage monitoring allows disconnecting the solar cell from the storage elements to avoid leakages. Output voltages are kept in a safe range for the application.

To perform granular power management of the application, the EM8502 integrates four independent supply outputs and a sleep mode offering the capability to switch off part or all the supplies.

The EM8502 is available in QFN24 package.

Features

- Flexible operation with different energy banks
  - Secondary cell battery
  - Capacitors (gold-cap, super-cap)
- Fast start-up on any energy storage
  - Dual energy storage elements
  - Start-up on solar cell or on battery
- Power management control
  - Multiple independent supply outputs
  - Sleep mode and wake-up functions
  - User programmable under-voltage and over-voltage levels
- Configurable application voltage
  - Battery voltage
  - LDO
- Limited external components
  - Device configurations are stored in on-chip E^2PROM
  - Dynamic configuration through a SPI or I^2C interface
- Extended power management status
  - Battery on protection mode
  - LTS/STS connection status
  - Minimum/Maximum voltage warning
  - USB connected

Applications

- Multi-Solar cell platforms
- Wearable systems
- Beacons and wireless sensor networks
- Industrial and environmental monitoring
- Battery operated platforms

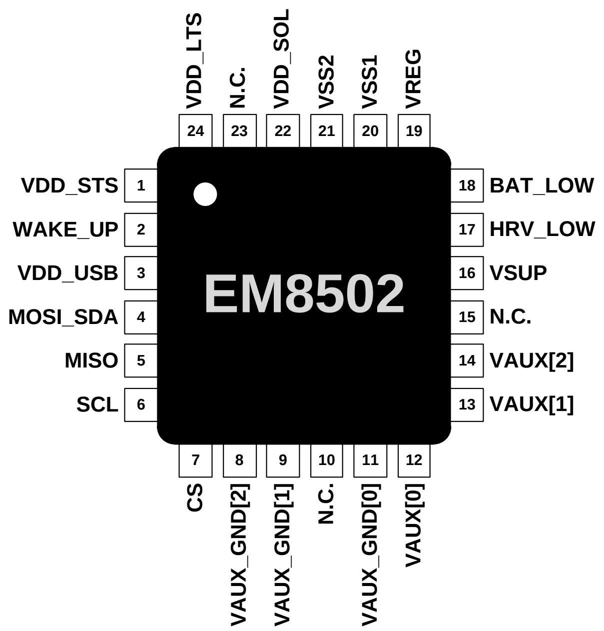

Figure 1 EM8502 QFN24 pins location

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1. ORDERING INFORMATION

Part Nb	Package form	Delivery form	Quantity
EM8502-A005-LF24B+	QFN24 4x4 mm	Tape & Reel	2500 p/reel

Table 1 Ordering Information

For other delivery format please contact EM Microelectronics representative.

2. PRODUCT DESCRIPTION

The EM8502 is a power management IC with battery charger function. It manages different energy source elements: a multi-cell solar harvester element through VDD_SOL, external supply through VDD_USB, a battery or a Long Term Storage (LTS) through VDD_LTS. It generates a local supply on a Short Term Storage (STS), visible through VDD_STS. The EM8502 provides the supply to the application from the energy sources. Surplus energy is stored in a LTS element.

Features and benefits include:

- **Power management controller, extending application battery life:** the EM8502 supplies the external application through the pins VSUP and VAUX[i]. The voltage is delivered directly from VDD_STS or through a regulator. On the VSUP pin a wake-up function allows to automatically re-enable the supply after a given time. For external devices using an I^2C serial interface, it is possible to disconnect their ground through the use of the auxiliary ground pins (VAUX_GND). This solution avoids supplying the devices connected to a switched-off output supply through the pull-up of I^2C bus. Overall power consumption is reduced by turning off peripheral ICs through the EM8502.

- **Battery charger from solar source:** EM8502 manages energy harvesting from a multiple solar cell in series by connecting to LTS and/or STS to maintain the application supply. With its dual storage architecture, application start-up is fast and independent of the battery (LTS) voltage.

- **Battery charger from USB source:** Fast charging is supported through a USB compatible supply input on the EM8502 (system start-up and battery charging to maximum voltage with configurable speed).

- **Voltage and current supervisor:** The EM8502 includes supervisory functions to detect harvester energy levels detecting (visible through the HRV_LOW pin) – and to monitor low battery voltage levels (visible through the BAT_LOW pin).
  The EM8502 protects the battery against over voltage conditions and automatically stops charging when a configurable threshold level is reached.

- **Configuration with E^2PROM, no additional external components:** The mode and functional configuration of the EM8502 is controlled by the host MCU through a SPI or an I^2C interface. Voltage supervision thresholds are set by registers. Configuration parameters are held in on-chip non-volatile memory (E^2PROM). The EM8502 default configuration parameter values can be modified by the user.

2.1. OPERATING MODES

The EM8502 operates in three main modes:

1) Normal mode (STS and LTS Connected)
   - V_{LTS} is inside battery operating range.
   - LTS is connected to STS.
   - The system can be configured to disconnect VAUX or/and VAUX_GND pins.

2) LTS protection mode (STS and LTS disconnected)
   - EM8502 enters this mode when V_{LTS} drops below minimum battery operation (v_bat_min_lo).
   - BAT_LOW pin is set to '1'.
   - LTS and STS are disconnected to protect LTS against under voltage condition.
   - VSUP and VAUX are maintained by the multiple solar cells connected on VDD_SOL or by VDD_USB through a LDO.

3) Sleep mode
   - VSUP is not supplied – no communication on SPI/I^2C interface.
   - VSUP can be re-activated by WAKE_UP pin or internal timer.

2.2. VOLTAGE NAMING CONVENTIONS

To describe the operation of this product, the following set of voltage naming conventions is adopted throughout this document, Table 2:

NAME	DESCRIPTION
v_bat_max_hi	Maximum battery voltage. High level of hysteresis.
v_bat_min_hi_dis	Minimum STS maintenance voltage – acts as v_bat_min_hi when STS and LTS are disconnected
v_bat_min_hi_con	Minimum battery maintenance voltage – acts as v_bat_min_hi when STS and LTS are connected
v_bat_min_hi	Minimum battery voltage. High level of hysteresis Equal to **v_bat_min_hi_dis** or **v_bat_min_hi_con** according to the connection state in between STS and LTS. The term “**v_bat_min_hi**” is used here whenever there is no specific usage of the connected and disconnected values
v_bat_min_lo	Minimum battery voltage. Low level of hysteresis
v_apl_max_hi	Maximum application voltage. High level of hysteresis
v_apl_max_lo	Maximum application voltage. Low level of hysteresis
$\mathbf{V_{cs\_hi}}$	Cold start voltage level
v_ulp_ldo	Regulated voltage on VSUP pin

Table 2 Voltage Naming Conventions

2.3. BLOCK DIAGRAM

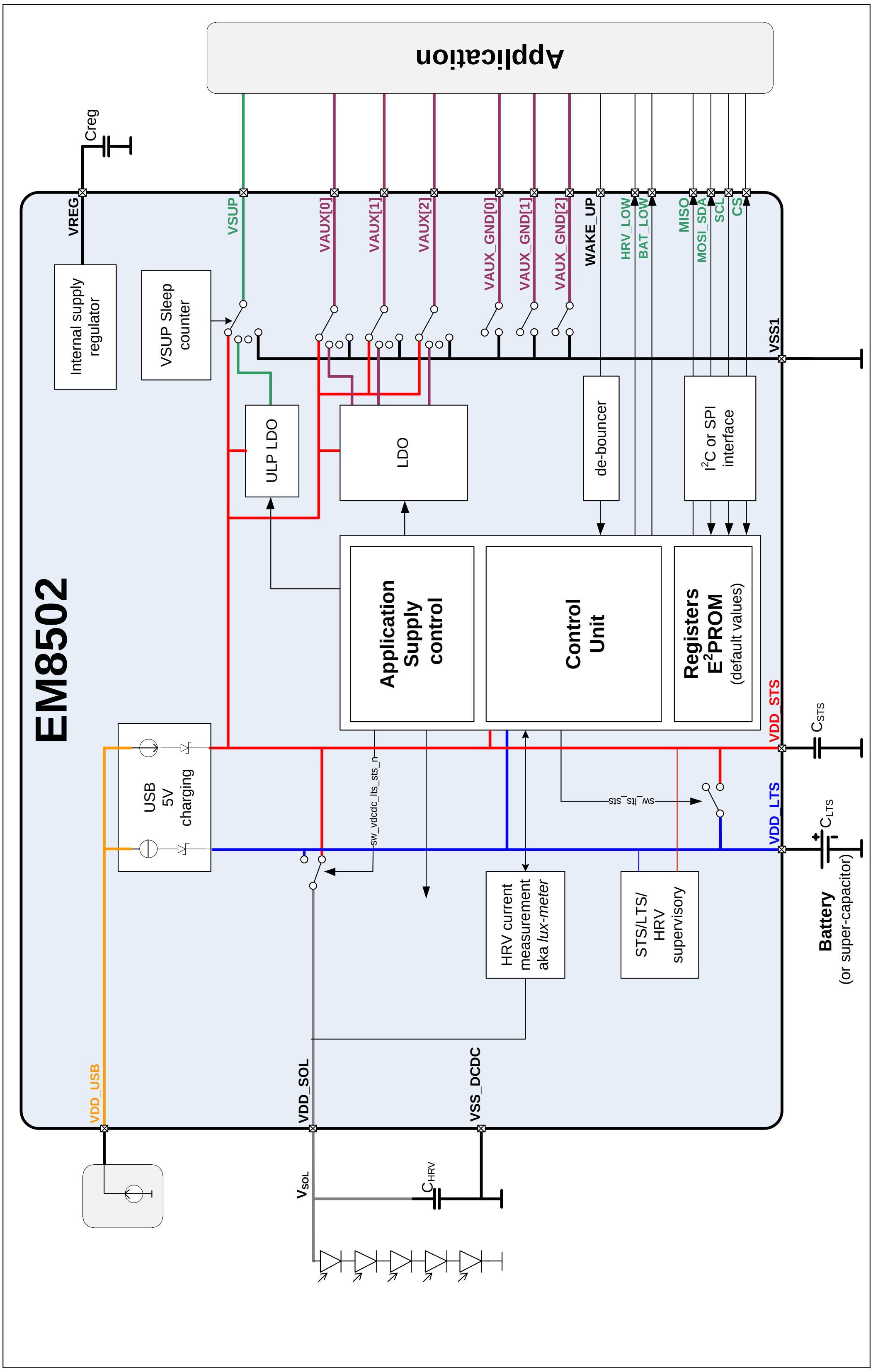


Figure 2-1 EM8502 Block Diagram

3. HANDLING PROCEDURES

This device has built-in protection against high static voltages or electric fields; however, anti-static precautions must be taken as for any other CMOS component. Unless otherwise specified, proper operation can only occur when all terminal voltages are kept within the voltage range. Unused inputs must always be tied to a defined logic voltage level.

4. PIN DESCRIPTION

PIN		I/O TYPE		DESCRIPTION
NO.	NAME	DIRECTION	SUPPLY	
1	VDD_STS	I/O	–	Connection for the Short Term energy Storage element (STS)
2	WAKE_UP	Input	up to 3.6V	Wake-up pin
3	VDD_USB	Input	–	USB power supply connection
4	MOSI_SDA	Input	VSUP	SPI MOSI or I2C SDA connection
5	MISO	Output	VSUP	SPI MISO connection
6	SCL	Input	VSUP	SPI or I2C clock
7	CS	Input	VSUP	SPI chip select and SPI/I2C selection mode(when at '1')
8	VAUX_GND[2]	Output	–	Auxiliary 2 ground connection
9	VAUX_GND[1]	Output	–	Auxiliary 1 ground connection
10	N.C.			
11	VAUX_GND[0]	Output	–	Auxiliary 0 ground connection
12	VAUX[0]	Output	–	Auxiliary 0 supply output connection
13	VAUX[1]	Output	–	Auxiliary 1 supply output connection
14	VAUX[2]	Output	–	Auxiliary 2 supply output connection
15	N.C.			
16	VSUP	Output	–	Main supply output
17	HRV_LOW	Output	VSUP	Energy harvester cell low indicator (when at '1')
18	BAT_LOW	Output	VSUP	Battery low indicator (when at '1')
19	VREG	Output	–	Regulated voltage connection
20	VSS1	Supply	–	Device ground connection
21	VSS2	Supply	–	Device ground connection
22	VDD_SOL	Input	–	Direct connection from the solar cell
23	N.C.			
24	VDD_LTS	I/O	–	Connection for the Long Term energy Storage element (LTS)

Table 3 Pin-out description

The digital pads are all supplied by VSUP, with the exception of the WAKE_UP pad whose trigger levels are independent of the supply voltages. When VSUP is disabled these pads are floating therefore the communication interface is off. All digital pads are active HIGH.

5. ELECTRICAL SPECIFICATIONS

5.1. ABSOLUTE MAXIMUM RATINGS

PARAMETER	VALUE MIN	VALUE MAX	UNIT
Power supply VDD_STS, VDD_LTS, VDD_SOL	-0.2	4.2	V
Power supply VDD_USB	-0.2	8.0	V
Input voltage	VSS-0.2	V_{SUP}+0.2	V
Input voltage (pin WAKE_UP)	-0.2	3.8	V
Storage Temperature Range (T_{STG})	-65	150	°C
Electrostatic discharge to ANSI/ESDA/JEDEC JS-001-2014 for HBM	-2000	2000	V

Table 4 Absolute maximum ratings

Stresses at or above these listed under Absolute Maximum Ratings may cause permanent damages to the device. Exposure beyond specified operating conditions may affect device reliability or cause malfunction.

Warning: The device is not functional when exposed to light. When a non-packaged version is used, it is mandatory to protect the device from light (e.g. glob-top, non-transparent package, metal shield on the PCB …)

5.2. OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Solar input	V_{SOL}			3.8	V
Long Term energy Storage bank voltage	V_{LTS}		3.0	3.6	V
Short Term energy Storage bank voltage	V_{STS}		3.0	3.6	V
VDD_USB voltage	V_{USB}		5	5.5	V
Long term capacitor(1)	C_{LTS}	0.001			F
Short term capacitor(2)	C_{STS}	47			µF
Regulated voltage capacitor	C_{REG}	470			nF
Harvester capacitor (nominal value)	C_{HRV}		1		µF
VSUP capacitor	C_{SUP}	1		0.1*C_{STS}	µF
VAUX capacitor	C_{AUX}	1		0.1*C_{STS}	µF
Input inductance	L_1	37.6	47	56.4	µH

(1) When using a super-capacitor
(2) C_{STS} shall be greater than 10 times C_{HRV} to avoid drops on STS when switching back and forth in between connection to LTS and STS

Table 5 Operating Conditions

5.3. ELECTRICAL CHARACTERISTICS

Unless otherwise specified: T_A=-40 to +85°C for min max specifications and T_A= 25°C for typical specifications.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
CURRENT CONSUMPTIONS ON LTS						
IDD in “LTS protection mode” and “HRV low mode”	I_{LTS_prot1}	Battery supervisory at 4Hz; VSUP and VAUX LDOs disabled		65		nA
IDD in “LTS protection mode”	I_{LTS_prot2}	Battery supervisory at 4Hz; VSUP and VAUX LDOs disabled		15		nA
IDD in “HRV low mode” STS and LTS connected	I_{HRV_lo2}	Battery supervisory at 4Hz; VSUP and VAUX LDOs disabled		145		nA
IDD in “HRV low mode” STS and LTS connected	I_{HRV_lo3}	Battery supervisory at 4Hz; ULP LDO enabled and VAUX LDO disabled		170		nA
IDD in “HRV low mode” STS and LTS connected	I_{HRV_lo4}	Battery supervisory at 4Hz; VSUP and VAUX[0] LDO enabled		285		nA
IDD in “HRV low mode” STS and LTS connected	I_{HRV_lo5}	Battery supervisory at 4Hz; VSUP and VAUX[1] LDO enabled		265		nA
IDD in “HRV low mode” STS and LTS connected	I_{HRV_lo6}	Battery supervisory at 4Hz; VSUP and VAUX[2] LDO enabled		250		nA
IDD in “HRV low mode” STS and LTS connected	I_{HRV_lo6}	Battery supervisory at 4Hz; VSUP and all VAUX LDO enabled		380		nA
IDD in “normal mode” STS and LTS disconnected	I_{NORM}	Battery supervisory at 4Hz; VSUP and VAUX LDOs disabled (VDD_STS < VDD_LTS)		45		nA
QUIESCENT CURRENT AND LEAKAGE ON STS (WHEN LTS IS NOT CONNECTED TO STS)						
IDD in “HRV low mode”	I_{STS_hrvlo}	Battery supervisory at 4Hz; VSUP and VAUX LDOs disabled		65		nA
VSUP AND VAUX LDO VOLTAGE LEVEL						
ULP/VAUX LDO level 0		$V_{STS} – V_{SUP}$> 0.3V	1.08	1.2	1.32	V
ULP/VAUX LDO level 1		$V_{STS} – V_{SUP}$> 0.3V	1.39	1.55	1.71	V
ULP/VAUX LDO level 2		$V_{STS} – V_{SUP}$> 0.3V	1.48	1.65	1.82	V
ULP/VAUX LDO level 3		$V_{STS} – V_{SUP}$> 0.3V	1.62	1.8	1.98	V
ULP/VAUX LDO level 4		$V_{STS} – V_{SUP}$> 0.3V	1.8	2	2.2	V
ULP/VAUX LDO level 5		$V_{STS} – V_{SUP}$> 0.3V	1.98	2.2	2.42	V
ULP/VAUX LDO level 6		$V_{STS} – V_{SUP}$> 0.3V	2.16	2.4	2.64	V
ULP/VAUX LDO level 7		$V_{STS} – V_{SUP}$> 0.3V	2.34	2.6	2.86	V
MAXIMUM CURRENT ON THE ULP AND VAUX LDO						
Maximum current on ULP LDO		Drop from open voltage is 100 mV, LDO level at 1.8V		10		mA
Maximum current on VAUX[0] LDO		Drop from open voltage is 100 mV, LDO level at 1.8V		20		mA
Maximum current on VAUX[1] LDO		Drop from open voltage is 100 mV, LDO level at 1.8V		10		mA
Maximum current on VAUX[2] LDO		Drop from open voltage is 100 mV, LDO level at 1.8V		5		mA
SWITCH RESISTOR						
VDD_LTS to VDD_STS	$R_{sw\_LTS\_STS}$	VDD_STS at 3V		3.1		Ω
VDD_STS to VSUP	R_{sw_VSUP}	VDD_STS at 3V		7.4		Ω
VDD_STS to VAUX[0]	R_{sw_VAUX0}	VDD_STS at 3V		4.4		Ω
VDD_STS to VAUX[1]	R_{sw_VAUX1}	VDD_STS at 3V		5.8		Ω
VDD_STS to VAUX[2]	R_{sw_VAUX2}	VDD_STS at 3V		6.4		Ω
VAUX_GND[0] to VSS	R_{sw_GND0}	VDD_STS at 3V		4.74		Ω
VAUX_GND[1,2] to VSS	$R_{sw\_GND1,2}$	VDD_STS at 3V		5.62		Ω
SUPERVISORY LEVELS ON STS, LTS AND HRV(1)						
Maximum voltage					3.6	V
Level step from lvl0 to lvl15	V_{M_15}			73		mV

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Level step from lvl16 to lvl30 (1.24V to 2.26V)	V_{lvl_30}		67.9	73	78.1	mV
Level step from lvl31 to lvl54 (2.34V to 4.2V)	V_{lvl_54}		69.4	73	76.7	mV
Differential non linearity				±0.5		LSB
Number of levels				50		
HARVESTER CURRENT LEVEL DETECTOR – LUX METER						
Harvester current level step	$I_{hrv\_check\_lvl}$			1		µA
Luxmeter current detection level "lvl" = level used for the measurement [0..15]	I_{lux_lvl}			2^{lvl}		µA
Short circuit voltage	V_{hrv_scv}			70		mV
USB POWER						
Minimum voltage for USB charging detection	V_{usb_min}			3.5		V
Regulated voltage on VDD_STS	V_{USB_REG}			2.1		V
Current source level 0 on LTS	I_{USB_lvl0}			0		mA
Current source level 1 on LTS	I_{USB_lvl1}			6.9		mA
Current source level 2 on LTS	I_{USB_lvl2}			12.7		mA
Current source level 3 on LTS	I_{USB_lvl3}			20.6		mA
E2PROM PARAMETERS						
E^2PROM write time	T_{ee_wr}				8	ms
E^2PROM read time	T_{ee_rd}				0.9	ms
E2PROM maximum write cycle	N_{ee_cyc}		1000			
E2PROM read hold time	T_{hd_rd}				10	µs
INTERFACE PARAMETERS						
Input WAKE_UP - low level	V_{il_wk}	V_{LTS}=1.2V to 3.6V			0.3	V
Input WAKE_UP - high level	V_{ih_wk}	V_{LTS} =1.2V to 3.6V	0.9			V
Wake-up rising edge reaction time	T_{r_wk}	Debouncer disabled		4.5		µs
Wake-up falling edge reaction time	T_{f_wk}	Debouncer disabled		120		µs
Input - low level	V_{il_si}	V_{SUP}=1.2V to 3.6V			0.2* V_{SUP}	V
Input - high level	V_{ih_si}	V_{SUP} =1.2V to 3.6V	0.8* V_{SUP}			V
Output – low level for I2C	I_{ol_sda}	V_{SUP} =1.8V, Vol=0.2* V_{SUP}	3			mA
Output – low level for I2C	$I_{ol\_sda\_1.2}$	V_{SUP} =1.20V, Vol=0.23*Vsup	3			mA
Output – low level	I_{ol}	V_{SUP} =1.8V, Vol=0.2*Vsup (MISO, MOSI_SDA, BAT_LOW, HRV_LOW)	1			mA
Output – low level	$I_{ol\_1.2}$	V_{SUP} =1.20V, Vol=0.23*Vsup (MISO, MOSI_SDA, BAT_LOW, HRV_LOW)	1			mA
Output – high level	I_{oh}	V_{SUP} =1.8V, Voh=0.8*Vsup (MISO, MOSI_SDA, BAT_LOW, HRV_LOW)			-1	mA
Output – high level	$I_{oh\_1.2}$	V_{SUP} =1.2V, Voh=0.8*Vsup (MISO, MOSI_SDA, BAT_LOW, HRV_LOW)			-1	mA
I^2C bus load capacitor	C_b	On MOSI_SDA and SCL			400	pF
SPI TIMINGS						
SPI clock input frequency	F_{spi}				5	MHz
SCL low pulse	T_{low_scl}		20			ns
SCL high pulse	T_{high_scl}		20			ns
MOSI_SDA setup time	T_{setup_mosi}		20			ns
MOSI_SDA hold time	T_{hold_mosi}		20			ns
MISO output delay	T_{delay_miso}	25pF load, V_{SUP} =1.6V min			30	ns
MISO output delay	T_{delay_miso}	25pF load, V_{SUP} =1.2V min			40	ns
CS setup time	T_{setup_cs}		50			ns
CS hold time	T_{hold_cs}		20			ns
I^2C TIMINGS(2)						
MOSI_SDA setup time	t_{sudat}	Standard & Fast Modes	160			ns
		High Speed Mode	30			ns
MOSI_SDA hold time	t_{hddat}	Standard & Fast Modes with C_b =100pF Max.	80			ns
		Standard & Fast Modes with C_b =400pF Max	90			ns
		High Speed Mode with C_b=100pF Max.	18		115	ns
		High Speed Mode with C_b=400pF Max.	24		150	ns
SCL low pulse	t_{low}	High Speed Mode with C_b=100pF Max. V_{SUP} =1.62V	160			ns
SCL low pulse	t_{low}	High Speed Mode with C_b=100pF Max. V_{SUP} =1.2V	210			ns

(1) The **v_bat_min**, **v_bat_max**, **v_apl_min** with their hysteresis can be set according to the supervising levels. E.g. for **v_bat_max**, both **v_bat_max_lo** and **v_bat_max_hi** will have to be set accordingly.
(2) Refers to I^2C specification 2.1 (January 2000)

Table 6 Electrical Specifications

5.4. TIMING DIAGRAMS

5.4.1. SPI INTERFACE

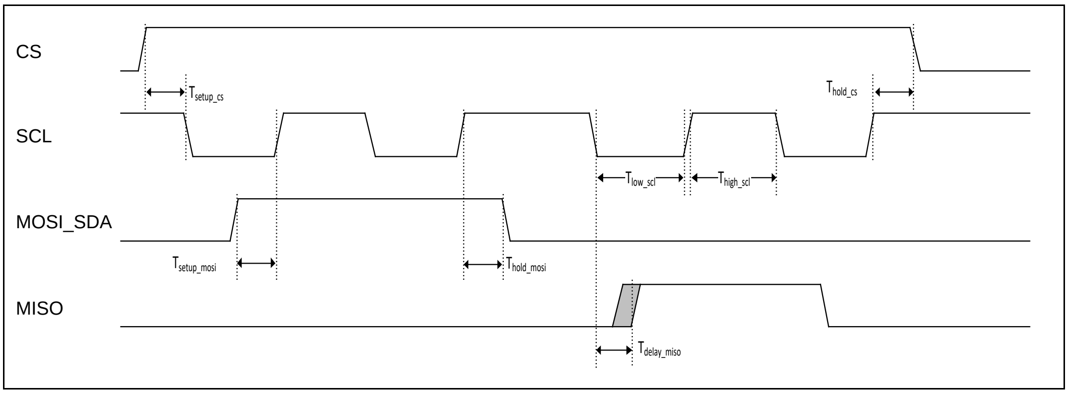


Figure 5-1 4-wire SPI Timing Diagram

5.4.2. I2C INTERFACE

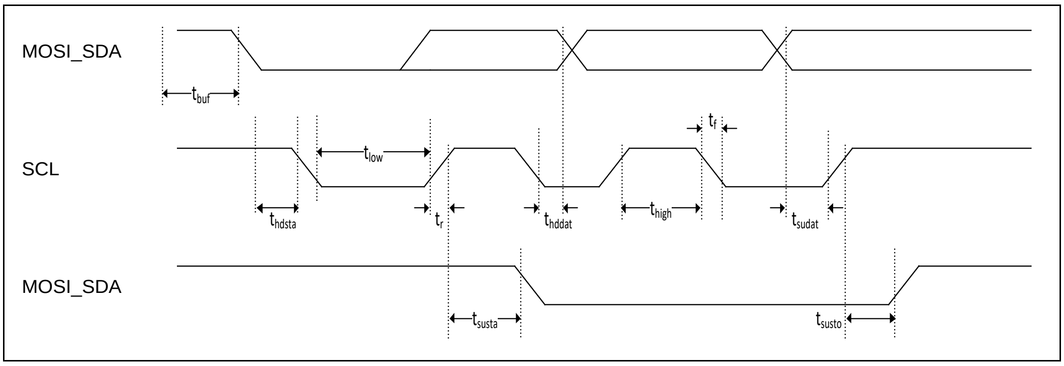


Figure 5-2 I^{2}C Timing Diagram

6. PRODUCT CONFIGURATION

The EM8502 is an autonomous power management system able to manage power domains, power sources and storage elements.

At start-up the device enters a boot sequence. It controls the state of both energy storage elements, and sets the default configuration parameters of the device by retrieving the corresponding values from the on-chip E^2PROM.

Upon completion of the boot sequence the system enters the supervising and harvester controller state ("normal mode"). It is now possible to modify configuration parameters through the serial interface to change the behavior of the device. When updating the device configuration through the serial interface it is recommended to write the complete set of EM8502 configuration parameters in a single transaction (see §7).

EM8502 is able to operate autonomously by using default configuration values from the on-chip E^2PROM.

6.1. STATUS INFORMATION

EM8502 provides status feed-back as follows.

- To allow fast system response the pins HRV_LOW and BAT_LOW directly indicate the status of the harvester cell and the battery to the host MCU.
- Additional status information is provided through register *reg_status*. During an SPI transaction the *reg_status* value sent as the first byte (along with the indication from the MCU of the address to be accessed). In case of an I2C transaction the *reg_status* register has to be polled explicitly.

Register Name: reg_status				Address: 0x22
Bits	**Bit name**	**Type**	**Reset**	**Description**
7	eeprom_data_busy	RO	0	• '1' EEPROM being written. Wait for new configuration • '0' EEPROM ready to be written. New configuration can be written
6	hrv_lux_busy	RO	0	• '1' lux-meter or HRV current supervisory is running • '0' no current measurement on the harvester on-going.
5	hrv_low	RO	0	• '1' HRV energy level too low for harvesting • '0' HRV has enough energy to be harvested
4	bat_low	RO	0	• '1' LTS voltage **lower** than **v_bat_min_hi** in normal mode, **lower** than **v_bat_min_lo** in primary cell mode • '0' LTS voltage **higher** than **v_bat_min_hi** in normal mode, **higher** than **v_bat_min_lo** in primary cell mode
3	sw_solar_lts_nsts	RO	0	• '1' Solar cell connected to LTS • '0' Solar cell connected to STS
2	sw_lts_sts	RO	0	• '1' LTS and STS are connected • '0' STS is disconnected from LTS
1	usb_on	RO	0	• '1' USB power has been detected • '0' No USB power found
0	lts_protect	RO	0	• '1' LTS protection mode activated (V_{LTS} < **v_bat_min_lo**) • '0' LTS protection mode inactive (V_{LTS} > **v_bat_min_lo**)

Table 7 Status Register (0x22)

EM8502 offers great flexibility in being configured for different system applications and use cases. The following chapters provide detailed descriptions of all configuration parameters and registers available to the user.

6.2. SUPERVISING AND HARVESTER CONTROLLER BEHAVIOUR

6.2.1. STORAGE ELEMENT

Storage element voltage and state are available through the *reg_vld_status* register.

Reguster name: reg_vld_status				Address: 0x23
Bits	**Bit name**	**Type**	**Reset**	**Description**
7	lts_bat_min_hi	RO	0	• '1' V_{LTS} > **v_bat_min_hi** • '0' V_{LTS} <= **v_bat_min_hi**
6	lts_bat_min_lo	RO	0	• '1' V_{LTS} > **v_bat_min_lo** • '0' V_{LTS} <= **v_bat_min_lo**
5	sts_bat_max_hi	RO	0	• '1' V_{STS} > **v_bat_max_hi** • '0' V_{STS} <= **v_bat_max_hi**
4	sts_bat_max_lo	RO	0	• '1' V_{STS} > **v_bat_max_lo** • '0' V_{STS} <= **v_bat_max_lo**
3	sts_apl_max_hi	RO	0	• '1' V_{STS} > **v_apl_max_hi** • '0' V_{STS} <= **v_apl_max_hi**
2	sts_apl_max_lo	RO	0	• '1' V_{STS} > **v_apl_max_lo** • '0' V_{STS} <= **v_apl_max_lo**
1	sts_bat_min_hi	RO	0	• '1' V_{STS} > **v_bat_min_hi** • '0' V_{STS} <= **v_bat_min_hi**
0	sts_bat_min_lo	RO	0	• '1' V_{STS} > **v_bat_min_lo** • '0' V_{STS} <= **v_bat_min_lo**

Table 8 Voltage Status Register (0x23)

Operation of the two energy banks (LTS and STS) is performed through three key voltage threshold levels.

- Minimum battery level voltage **v_bat_min** (reg_v_bat_min_hi_con or *reg_v_bat_min_hi_dis* and *reg_v_bat_min_lo*)
- Maximum battery level voltage **v_bat_max** (*reg_v_bat_max_hi* and *reg_v_bat_max_lo*)
- Maximum application level voltage **v_apl_max** (*reg_ v_apl_max_hi* and *reg_v_apl_max_lo*)

The three levels include a hysteresis to avoid instability of the controller. The hysteresis values have to be carefully chosen according to the application and have to fulfill the following conditions:

- v_bat_min_hi_dis > v_bat_min_hi_con > v_bat_min_lo
- v_apl_max_hi > v_apl_max_lo
- v_bat_max_hi > v_bat_max_lo

If v_apl_max ≥ v_bat_max the application maximum level is considered to be the maximum battery level.

Supervising of the minimum battery level is performed through two registers for its highest control level (v_bat_min_hi). When the two battery banks are not connected **v_bat_min_hi_dis** is used to inform the system when it has to charge STS again (see phase 4 to 5 in **Error! Reference source not found.** on page **Error! Bookmark not defined.**). When LTS and STS are connected together **v_bat_min_hi_con** is used as supervising level.

The minimum value allowed for the **v_bat_min_hi_dis** register is 0x15 corresponding to typically 1.47 V. For any value lower than this minimum the system may shut-down without notification through the BAT_LOW pin.

All voltage levels with prefix "*v_*" are configured by register according to the following equation:

v_<*voltage name*> = V_{M} * (reg_<*voltage name*>+1)

Supervisory status of the battery is also visible through the pin BAT_LOW. When the V_{LTS} is below **v_bat_min_hi** for two consecutive measurements, BAT_LOW is asserted (set to VSUP level). When two measurements show that V_{LTS} is above **v_bat_min_hi**, BAT_LOW is de-asserted (set to VSS). The only exception is during the boot phase where the BAT_LOW signal is asserted after the first measurement of V_{LTS}.

The EM8502 protects the battery when its voltage is too low. This corresponding threshold level can be set through the **v_bat_min_lo** register. When V_{LTS} is falling below this value the EM8502 operates only on the harvester.

6.2.2. HARVESTER POWER SUPERVISORY FUNCTIONS

The EM8502 monitors harvester power to prevent reverse current from the energy storage (LTS). The detection is done regularly through a current sensor. The device is sensing the current at the voltage V_{hrv_scv} delivered by the solar cell. The current threshold of detection is set through the *reg_hrv_check_lvl.hrv_check_lvl* register to disconnect the solar cell from the energy banks. To return to the running state, the EM8502 detection is done with a different principle. The current measurement is done by connecting a resistance on VDD_SOL and sense voltage on this pin using **v_hrv_min** voltage level.

Resistances and currents are defined in *reg_hrv_check_lvl.hrv_check_lvl*:

reg_hrv_check_lvl.hrv_check_lvl	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F
Current (µA)	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Resistance (kΩ)	35	23.3	17.5	14	11.7	10	8.75	7.8	7	6.36	5.38	5.4	5	4.7	4.4	4.4

Table 9 HRV Current Detection Levels

Configuration example:

- *reg_hrv_check_lvl* =0x00; *reg_v_hrv_cfg* = 0x00

The system indicates HRV_LOW ='1' from 1µA at V_{hrv_scv} (70mV) and remains off until V_{lvl} is reached with 35 kΩ load on VDD_SOL (2 µA at V_{lvl}). A hysteresis of 1 µA is applied.

Register name: reg_v_hrv_cfg			Address: 0x04	Default value mapped in E²PROM
Bits	**Bit name**	**Type**	**Description**	
7	–	–	Reserved	
6	–	RW	To be written always to '0'	
5:0	v_hrv_min	RW	Minimum HRV open voltage required to generate energy. $V_{hrv\_min} = V_{lvl} * (reg\_v\_hrv\_min(5:0)+1)$ if $V_{HRV} < V_{hrv\_min}$ and *reg_v_hrv_cfg.hrv_check_vld* = '1' then *reg_status.hrv_low* = '1'	

Table 10 Minimum HRV voltage (0x04)

Register name: reg_hrv_check_lvl			Address: 0x05	Default value mapped in E²PROM
Bits	**Bit name**	**Type**	**Description**	
7:4	–	–	Reserved	
3:0	hrv_check_lvl	RW	Minimum HRV short-cut current level to generate energy. $I_{hrv\_check} = (hrv\_check\_lvl+1) * 1\mu A$ if $I_{HRV} < I_{hrv\_check}$ and *reg_v_hrv_cfg.hrv_check_vld* = '0' then *reg_status.hrv_low* = '1'	

Table 11 Minimum HRV short-cut current (0x05)

6.2.3. TIMING CONFIGURATION

In addition to voltage level supervision, the user can select independent values for the frequency of supervision on LTS, STS and the harvester. The frequency influences the overall EM8502 power consumption and therefore its efficiency.

The STS and LTS measurement periods are set through the registers *reg_t_sts_period* and *reg_t_lts_period*. The monitoring of the harvester however requires disconnecting the solar cell and the storages in order to measure the short-cut current. The duration of the disconnect time is configured through the *reg_t_hrv_meas* register, whereas the measurement period is configured through the *reg_t_hrv_period* register.

Register value	t_hrv_meas	t_hrv_period	t_sts_period	t_lts_period	t_hrv_low_period	t_lts_hrv_low_period
0x00	16 ms	256 ms	1 ms	1 ms	256 ms	2 ms
0x01	32 ms	512 ms	2 ms	4 ms	512 ms	8 ms
0x02	64 ms	1 s	8 ms	16 ms	1 s	32 ms
0x03	128 ms	2 s	16 ms	64 ms	2 s	128 ms
0x04	256 ms	4 s	32 ms	256 ms	4 s	512 ms
0x05	512 ms	8 s	64 ms	1 s	8 s	2 s
0x06	1 s	16 s	128 ms	4 s	16 s	8 s
0x07	2 s	32 s	256 ms	16 s	32 s	32 s

Table 12 Timing Configuration

When entering in "HRV low mode" the monitoring on LTS and the harvester remains active, however the monitoring frequency can be adapted to this situation where the system cannot take energy anymore from the harvester source. The measurement period is then set in parameter **t_hrv_low_period.** In this mode STS is not fed by the harvester anymore. If STS and LTS are not connected internally, STS will collapse. No monitoring is performed on STS.

6.3. POWER MANAGEMENT FUNCTIONS

The EM8502 controls four independent power supply outputs.

The VSUP power supply output is connected to STS when STS level is within the application voltage range ([**v_bat_min**:**v_apl_max**]) or to an LDO (when above **v_apl_max**) to regulate the output to a given value.

The three auxiliary supply outputs VAUX [0:2], are user configurable between STS and the internal LDO. It is possible to force the use of the LDO even though the STS voltage level is compatible with the application supply requirements.

During the boot phase – which corresponds to the set-up of the device – all the power supply outputs are floating. Once the set-up of the registers is completed the supply output values are determined by configuration registers *reg_ldo_cfg.vsup_tied_low* and *reg_vaux_cfg.vaux[x]_cfg*.

The main application power supply (VSUP) is intended to be connected to the application controller. When connected to the LDO its maximum power is limited as LDO is optimized for low consumption. The VSUP supply output is controlled by the *reg_ldo_cfg* register. The value of the LDO is configurable through *reg_ldo_cfg.v_ulp_ldo*. The LDO enable can be forced with *reg_ldo_cfg.frc_ulp_ldo*. In "sleep state", VSUP can be grounded (*reg_ldo_cfg.vsup_tied_low* = '1') or floating (*reg_ldo_cfg.vsup_tied_low* = '1') (see §6.4).

The individual configurability of the three auxiliary supply outputs allows the creation of different power domains for the external application. The auxiliary outputs are split into the supply and ground pins where all six outputs can be switched on/off independently. The behavior of the VAUX pins is controlled through the *reg_vaux_cfg* register. *reg_vaux_cfg*.v_aux_*ldo* controls the level of the single LDO connected to the three auxiliary supplies.

When switched on (*reg_pwr_mgt.vaux[i]_en* = '1') the auxiliary supply output is controlled by *reg_vaux_cfg.vaux[i]_cfg*.

Four possible settings are available to the user:

1) Force the connection to STS
2) Force the connection to the LDO
3) Use the automatic configuration permitting the auxiliary output to float when STS drops below **v_bat_min**
4) Use the automatic configuration grounding the auxiliary output when STS drops below **v_bat_min**

The automatic configuration of the auxiliary supplies is ensures that the auxiliary output voltage is kept within the application voltage range by auto-connecting the supply output to the LDO when STS voltage is exceeding the **v_apl_max** value.

When the power supply output is switched off (*reg_pwr_mgt.vaux[i]_en* = '0'), its configuration is also controlled by the *reg_pwr_mgt.vaux[i]_cfg* register. The output is grounded if *reg_pwr_mgt.vaux[i]_cfg* is set to 3 (b11), otherwise it is kept floating.

When the LDO is used on VSUP or VAUX pins, changing the LDO settings does not generate over or under shoots on the output power supply terminals.

EM8502 offers the possibility to control the ground pin as part of the application, by connecting it to the ground of the EM8502 or letting it float. It is of particular interest when involving applications that are using I^2C communication through the pulls of the I^2C lines. The configuration of the VAUX_GND pins is controlled through the *reg_pwr_mgt.vaux_gnd[i] en* register.

Register name: reg_ldo_cfg			Address: 0x0E	Default value mapped in E^2PROM
Bits	**Bit name**	**Type**	**Description**	
7	vsup_tied_low	RW	When set to '1', connects VSUP pin to ground when VSUP is disabled, otherwise VSUP remains floating.	
6:4	v_vaux_ldo	RW	VAUX LDO regulated voltage selection • "000" (0) 1.2 V • "001" (1) 1.55 V • "010" (2) 1.65 V • "011" (3) 1.8 V • "100" (4) 2.0 V • "101" (5) 2.2 V • "110" (6) 2.4 V • "111" (7) 2.6 V	
3	frc_ulp_ldo	RW	Force ULP LDO on as soon as V_{STS} > **v_bat_min_hi**	
2:0	v_ulp_ldo	RW	ULP LDO regulated voltage selection • "000" (0) 1.2 V • "001" (1) 1.55 V • "010" (2) 1.65 V • "011" (3) 1.8 V • "100" (4) 2.0 V • "101" (5) 2.2 V • "110" (6) 2.4 V • "111" (7) 2.6 V	

Table 13 VSUP output supply and LDOs configuration register (0x0E)

Register name: reg_pwr_cfg			Address: 0x0F	Default value mapped in E²PROM
Bits	**Bit name**	**Type**	**Description**	
7	usb_ldo_frc_dis	RW	• '1' Disable USB LDO after boot sequence even if usb_crt_src_sel is > 0x0 • '0' Keep the default behavior on USB LDO	
6	dis_vaux_gnd2_hrv_low	RW	• '1' open the VAUX_GND[2] (pin is floating) in "HRV low" mode. • '0' Keep the same behavior as in normal mode	
5	dis_vaux_gnd1_hrv_low	RW	"HRV low" mode VAUX_GND[1] behavior. same as for pin VAUX_GND[2]	
4	dis_vaux_gnd0_hrv_low	RW	"HRV low" mode VAUX_GND[0] behavior. same as for pin VAUX_GND[2]	
3	dis_vaux2_hrv_low	RW	• '1' Disable vaux[2] in "HRV low" mode. It is configured by *reg_vaux_cfg.vaux2_cfg* • '0' Keeps its normal mode configuration.	
2	dis_vaux1_hrv_low	RW	"HRV low" mode VAUX[1] behavior. same as for pin VAUX[2]	
1	dis_vaux0_hrv_low	RW	"HRV low" mode VAUX[0] behavior. same as for pin VAUX[2]	
0	dis_vsup_hrv_low	RW	• '1' Disable VSUP in "HRV low" mode. Its behavior is defined by *reg_ldo_cfg.vsup_tied_low* • '0' Keeps its normal mode configuration	

Table 14 "HRV low" mode power switch configuration register (0x0F)

Register name: reg_vaux_cfg			Address: 0x10	Default value mapped in E²PROM
Bits	**Bit name**	**Type**	**Description**	
7:6	–	–	Reserved	
5:4	vaux2_cfg	RW	Configuration of VAUX[2] pin • "00" (0) Constantly connected to STS • "01" (1) Constantly connected to the LDO • "10" (2) Automatic configuration – floating when below V_{STS} < **v_bat_min** • "11" (3) Automatic configuration – grounded when below V_{STS} < **v_bat_min** If VAUX[2] is disconnected – VAUX[2] is connected to ground if the value is "11", otherwise it is floating	
3:2	vaux1_cfg	RW	Configuration of VAUX[1] pin – same as for VAUX[2] pin	
1:0	vaux0_cfg	RW	Configuration of VAUX[0] pin – same as for VAUX[2] pin	

Table 15 Auxiliary supply configuration register (0x10)

Register name: reg_vaux_gnd_cfg			Address: 0x11	Default value mapped in E²PROM
Bits	**Bit name**	**Type**	**Description**	
7:3	–	–	Reserved	
2	vaux_gnd2_cfg	RW	• '1' Auto disconnect when V_{STS} not within [**v_bat_min**.. **v_apl_max]** • '0' Fully manual connection	
1	vaux_gnd1_cfg	RW	Configuration of VAUX_GND[1] pin – same as for VAUX_GND [2] pin	
0	vaux_gnd0_cfg	RW	Configuration of VAUX_GND[0] pin – same as for VAUX_GND[2] pin	

Table 16 Auxiliary ground pins configuration register (0x11)

Register name: reg_pwr_mgt			Address: 0x19	Value at start-up mapped in E^2PROM
Bits	**Bit name**	**Type**	**Description**	
7	–	–	To be written always to '0'	
6	vaux_gnd2_en	RW	Enable the VAUX_GND[2] connection (see *reg_vaux_gnd_cfg.vaux_gnd2_cfg*) when V_{STS} > **v_bat_min_hi**	
5	vaux_gnd1_en	RW	Enable the VAUX_GND[1] connection (see *reg_vaux_gnd_cfg.vaux_gnd0_cfg*) when V_{STS} > **v_bat_min_hi**	
4	vaux_gnd0_en	RW	Enable the VAUX_GND[0] connection (see *reg_vaux_gnd_cfg.vaux_gnd0_cfg*) when V_{STS} > **v_bat_min_hi**	
3	vaux2_en	RW	Enable the VAUX[2] connection (see *reg_vauxcfg.vaux2_cfg*) when V_{STS} > **v_bat_min_hi**	
2	vaux1_en	RW	Enable the VAUX[1] connection (see *reg_vauxcfg.vaux1_cfg*) when V_{STS} > **v_bat_min_hi**	
1	vaux0_en	RW	Enable the VAUX[0] connection (see *reg_vauxcfg.vaux0_cfg*) when V_{STS} > **v_bat_min_hi**	
0	sleep_vsup	RW	Enable the VSUP "sleep state" – disconnects VSUP for **t_sleep_vsup** interval	

Table 17 Power switch enable register (0x19)

6.4. SLEEP MODE AND WAKE-UP FUNCTIONS

In addition to the direct control of the power supply outputs the EM8502 supports stopping supplying the application (switching off VSUP) for a given time interval to allow very low consumption modes. When enabled, the auxiliary supplies are kept in the same state as before entering in the "sleep state". The "sleep state" is not a functional mode of the power management unit, as the device is still working according to the configuration parameters set and is only acting on the state of the VSUP supply output.

The "sleep state" can also be interrupted (VSUP is connected again on STS or on the LDO according to the settings of the VSUP power switch see Table 13) by setting the WAKE_UP pin to a level above V_{ih_wk}.

During "sleep state" the serial interface is disabled.

To avoid false wake-up detection, a debouncing logic is connected to the WAKE_UP pin. The debouncer function is enabled by default (factory default value on E^2PROM), and can be disabled by setting the *reg_ext_cfg. wake_up_deb_en* to '0'. The wake-up is sensitive to the edge configured in *reg_ext_cfg.wake_up_edge_cfg*. It is not permitted to set *reg_ext_cfg.wake_up_edge_cfg* = "00".

Register name: reg_ext_cfg			Address: 0x13	Default value mapped in E^2PROM
Bits	**Bit name**	**Type**	**Description**	
7	sda_slopectrl	RW	MOSI_SDA pad slope control • '0' for standard and fast I2C mode, and high speed mode if VSUP < 1.8V • '1' for high speed mode if VSUP > 1.8V	
6	wake_up_deb_en	RW	When at '1' the wake-up debouncer is enabled	
5:4	wake_up_edge_cfg	RW	"00" (0x0): Forbidden "01" (0x1): wake-up on falling edge "10" (0x2): wake-up on rising edge "11" (0x3): wake-up on both edge	
3	*usb_frc_hrv_low_hiz*	*RW*	See Table 24 USB Configuration Register (0x13)	
2	*usb_frc_bat_low_hiz*	*RW*	See Table 24 USB Configuration Register (0x13)	
1:0	*usb_crt_src_sel*	*RW*	See Table 24 USB Configuration Register (0x13)	

Table 18 Wake-up terminal configuration register (0x13)

The "sleep state" duration is controlled through a 24-bit counter (*reg_t_sleep_vsup*[23:0]). VSUP supply can be interrupted for up to 4 hours, with a granularity of 1 ms.

t_sleep_vsup = *reg_t_sleep_vsup[23:0]*/1000 seconds

When VSUP is in "sleep state" it is possible to ground VSUP to create a known voltage level on the main controller supply, by setting *reg_ldo_cfg.vsup_tied_low* to '1' (see above in page 13).

The VSUP "sleep state" is enabled by setting *reg_pwr_mgt.sleep_vsup* to '1' (see Table 17 bit 0).

Register name: reg_t_sleep_vsup_lo			Address: 0x14	Default value mapped in E^2PROM
Bits	Bit name	Type	Description	
7:0	t_sleep_vsup_lo	RW	Sleep counter duration – least significant byte	

Table 19 VSUP "sleep state" counter time-out Least significant byte (0x14)

Register name: reg_t_sleep_vsup_mid			Address: 0x15	Default value mapped in E^2PROM
Bits	Bit name	Type	Description	
7:0	t_sleep_vsup_mid	RW	Sleep counter duration – byte 2	

Table 20 VSUP "sleep state" counter time-out middle significant byte (0x15)

Register name: reg_t_sleep_vsup_hi			Address: 0x16	Default value mapped in E^2PROM
Bits	Bit name	Type	Description	
7:0	t_sleep_vsup_hi	RW	Sleep counter duration – most significant byte	

Table 21 VSUP "sleep state" counter time-out Most significant byte (0x16)

6.5. LUX-METER

The device contains a specific element to determine ranges of current supplied by the solar cell.

The lux-meter is able to run in three modes:

- Fully automatic mode
- Automatic range selection
- Fully manual mode

In fully automatic mode (selected by writing ‘1’ in *reg_lux_meter_cfg.lux_meter_auto_meas*) the device determines the value range for the current flowing in from the solar cell. The result is available in the reg_lux_meter_result.lux_meter_result register field. The *reg_lux_meter_result.lux_meter_busy* bit indicates that the measurement is still ongoing and that the result is not available yet.

In automatic range selection mode (selected by writing ‘1’ in *reg_lux_meter_cfg.lux_meter_auto_rng)* the EM8502 automatically determines the optimal range, and measures the voltage at VDD_SOL for maximum precision. The *reg_lux_meter_result.lux_meter_busy* bit indicates that the range search is complete. In this mode lux-meter continues to operate until user disabled by writing ‘0’ into the *reg_lux_meter_cfg.lux_meter_auto_rng*.

The full manual mode allows the user to select the range. The mode is selected by writing on the bit *reg_lux_meter_cfg.lux_meter_manu* – ‘1’ to activate the mode, and ‘0’ to deactivate it. The selection of the range is done through the *reg_lux_meter_cfg.lux_meter_rng* field.

In case a lux-meter action is requested with LTS and STS disconnected, V_{LTS} < **v_bat_min_lo** the action is disregarded and the result – in automatic mode – is invalid.

Register name: reg_lux_meter_cfg				Address: 0x1C
Bits	**Bit name**	**Type**	**Reset**	**Description**
7	–	–	0	Reserved
6	lux_auto_meas	OS	0	Start the automatic lux-meter measurement. The lux-meter is disabled automatically when the measure is finished
5	lux_auto_rng	RW	0	Enable the lux-meter, and search for the best range. It remains enabled
4	lux_manu	RW	0	Enable the lux-meter in manual mode (range forced by *reg_lux_meter_cfg.lux_lvl*)
3:0	lux_lvl	RW	0x0	Target current level to be detected • "0000" (0x0) 1 µA • "0001" (0x1) 2 µA • "0010" (0x2) 4 µA • "0011" (0x3) 8 µA • "0100" (0x4) 15 µA • "0101" (0x5) 30 µA • "0110" (0x6) 60 µA • "0111" (0x7) 120 µA • "1000" (0x8) 0.25 mA • "1001" (0x9) 0.5 mA • "1010" (0xA) 1 mA • "1011" (0xB) 1.8 mA • "1100" (0xC) 3.2 mA • "1101" (0xD) 6 mA • "1110" (0xE) 11 mA • "1111" (0xF) 17 mA

Table 22 Lux Meter Configuration Register (0x1C)

Register name: reg_lux_meter_result				Address: 0x1D
Bits	**Bit name**	**Type**	**Reset**	**Description**
7:5	–	–	'000'	Reserved
4	lux_meter_busy	RO	0	Indicates that the lux-meter is still searching for best range
3:0	lux_meter_result	RO	0x0	Lux-meter range status (result in automatic measurement mode) • "0000" (0x0) below 2 µA • "0001" (0x1) from 2 µA to 4 µA • "0010" (0x2) from 4 µA to 8 µA • "0011" (0x3) from 8 µA to 15 µA • "0100" (0x4) from 15 µA to 30 µA • "0101" (0x5) from 30 µA to 60 µA • "0110" (0x6) from 60 µA to 120 µA • "0111" (0x7) from 120 µA to 0.25 mA • "1000" (0x8) from 0.25 mA to 0.5 mA • "1001" (0x9) from 0.5 mA to 1 mA • "1010" (0xA) from 1 mA to 1.8 mA • "1011" (0xB) from 1.8 mA to 3.2 mA • "1100" (0xC) from 3.2 mA to 6 mA • "1101" (0xD) from 6 mA to 11 mA • "1110" (0xE) from 11 mA to 17 mA • "1111" (0xF) above 17 mA

Table 23 Lux-meter Result Register (0x1D)

6.6. USB CHARGING

The EM8502 is equipped with a USB power line input to supply the device and to charge has the energy bank elements.

When a voltage above V_{usb_min} is detected, a regulator between VDD_USB and VDD_STS is enabled. The regulated voltage is V_{USB_REG}. In addition to the regulator, a current source is activated between VDD_USB and VDD_LTS. This function is controlled by the *reg_ext_cfg* register. Four user selected level of charge current delivered to LTS are available (*reg_ext_cfg.usb_crt_src_sel*).

When VDD_USB is connected, pins HRV_LOW and BAT_LOW can be brought into HiZ state.

Register name: reg_ext_cfg			Address: 0x13	Default value mapped in E²PROM
Bits	**Bit name**	**Type**	**Description**	
7	*sda_slopectrl*	*RW*		
6	*wake_up_deb_en*	*RW*		
5:4	*wake_up_edge_cfg*	*RW*		
3	usb_frc_hrv_low_hiz	RW	• '1' force HRV_LOW in Hi-Z state if usb_on = '1' • '0' HRV_LOW pin standard configuration	
2	usb_frc_bat_low_hiz	RW	• '1' force BAT_LOW in Hi-Z state if usb_on = '1' • '0' BAT_LOW pin standard configuration	
1:0	usb_crt_src_sel	RW	USB power current source selection • "00" (0x0) 0 mA (do not charge) • "01" (0x1) 5 mA • "10" (0x2) 10 mA • "11" (0x3) 20 mA	

Table 24 USB Configuration Register (0x13)

Warning: *When VDD_LTS is to be disconnected from its load, the USB current injected into LTS must be set to 0 mA, otherwise the device could be damaged.*

6.7. MISCELLANEOUS FUNCTIONS

This chapter describes additional control functions related to the regulation loop.

6.7.1. SOFT RESET FUNCTION

The soft reset function restarts the EM8502 from its boot sequence. The behavior of the EM8502 is the same as in a normal boot sequence. A soft reset is generated by setting the register *reg_soft_res_word* to 0xAB. This register is enabled only if *reg_protect_key* is set to 0xE2. If the value of the *reg_protect_key* is different from 0xE2, the register *reg_soft_res_word* is set to 0x00.

The *reg_protect_key* register is reset by the soft reset. Creating a new soft sequence requires preloading the *reg_protect_key* again.

Register name: reg_soft_res_word				Address: 0x1A
Bits	**Bit name**	**Type**	**Reset**	**Description**
7:0	soft_res_word	RW	0x00	Force reset when set at 0xAB

Table 25 Soft reset register (0x1A)

Register name: reg_protect_key				Address: 0x1B
Bits	**Bit name**	**Type**	**Reset**	**Description**
7:0	protect_key	RW	0x00	Allow writing on *reg_soft_res_word* register when set at 0xE2 Allow writing on protected registers when set at 0x4B Allow writing on E2PROM when set at 0xA5

Table 26 Protected registers key (0x1B)

6.7.2. REGISTER PROTECTION

The EM8502 functionality is determined by the content of the configuration registers (like the supervising levels or periods). The registers are always accessible in read mode. Some registers are write protected against unwanted write operations.

The registers ranging is address space from 0x00 to 0x18 are write protected. Writing into these registers is enabled after setting *reg_protect_key* to 0x4B.

Note: The *reg_protect_key* is reset at the end of the communication transaction (see §7 on page 19). It is necessary to set it on the same communication transaction – on SPI keeping CS to '1' or on I²C before putting an I²C stop.

Write access to the on-chip E²PROM is controlled by the same mechanism. Prior to a write operation into the E²PROM *reg_protect_key* must be set to 0xA5.

6.7.3. LTS PROTECTION DISABLE

By default the EM8502's monitors voltage levels, namely lower voltage limit, to prevent damage to the LTS energy storage element.

This protection can be disabled by setting register *reg_lts_cfg.no_bat_protect* leaving the system connected to LTS even when the voltage level drops below **v_bat_min**. Disabling protection might be suitable for systems using super-caps or solid-state battery storage elements.

When LTS protection is active the EM8502 tries to start-up from LTS only once, if after booting it still detects that V_{LTS} < **v_bat_min** it enables the protection and never try to restart from LTS. The system will then re-start as from a standard cold-start.

Register name: reg_lts_cfg			Address: 0x06	Default value mapped in E²PROM
Bits	**Bit name**	**Type**	**Description**	
7:3	–	–	Reserved	
2	–	–	Shall be written to '0'	
1	–	–	Shall be written to '0'	
0	no_bat_protect	RW	• '1' disables the battery protection feature. (reg.status.lts_protect = '0') • '0' enables the battery protection feature.	

Table 27 Wake-up terminal configuration register (0x13)

7. SERIAL INTERFACE

The EM8502 offers SPI and I²C serial interfaces selected by the CS pin (see §7.2.1).

The configuration/function of the EM8502 is updated only after the end of a communication transaction. An SPI transaction is defined by all the bytes sent and received when the pad CS is kept to '1'. An I²C transaction is defined by all the data sent or received between a start and a stop or repeated start I²C patterns.

Data synchronization between the communication interface and the internal part of the device is done at the end of a supervising loop. New information is active two milliseconds after the end of the transaction. All write transactions sent before the end of this synchronization interval are ignored. It is recommended to perform the device configuration in one transaction. Read transactions are allowed at any time.

7.1. I2C INTERFACE

The I²C slave interface is compatible with Philips I²C Specification version 2.1 (see specific timings on electrical specifications chapter). All modes (standard, fast, high speed) are supported. MOSI_SDA and SCL pins are not strictly open-drain (they represent diodes to VSUP).

The 7-bit device address is defined in the E²PROM (at address 0x58). This address is copied at boot into the *reg_spi_i2c_cfg.ic2_addr* register field.

The I²C bus uses the 2 wires SCL (Serial Clock) and MOSI_SDA. CS has to be connected to VSS. MOSI_SDA is bi-directional with open drain to VSS: it must be externally connected to VSUP via a pull up resistor.

The I2C interface supports single and multiple read and write transactions.

In the following figures, "S" indicates the I²C transaction start, "P" indicates the I²C transaction stop.

The multi-read and multi write transactions are described in the following figures.

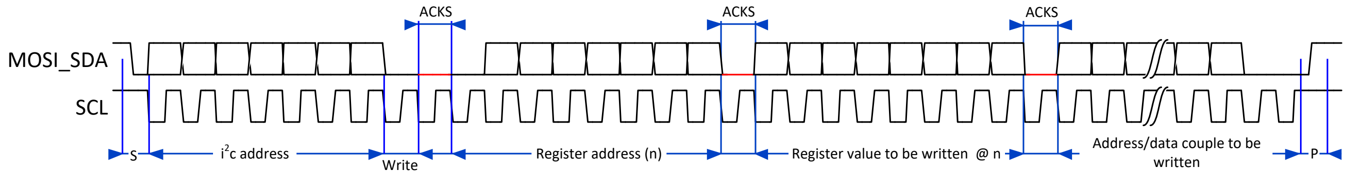


Figure 7-1: I2C write (multiple transactions)

To access registers in read mode, first address should first be send in write mode. Then a stop and a start conditions must be generated and data bytes are transferred with automatic address increment:

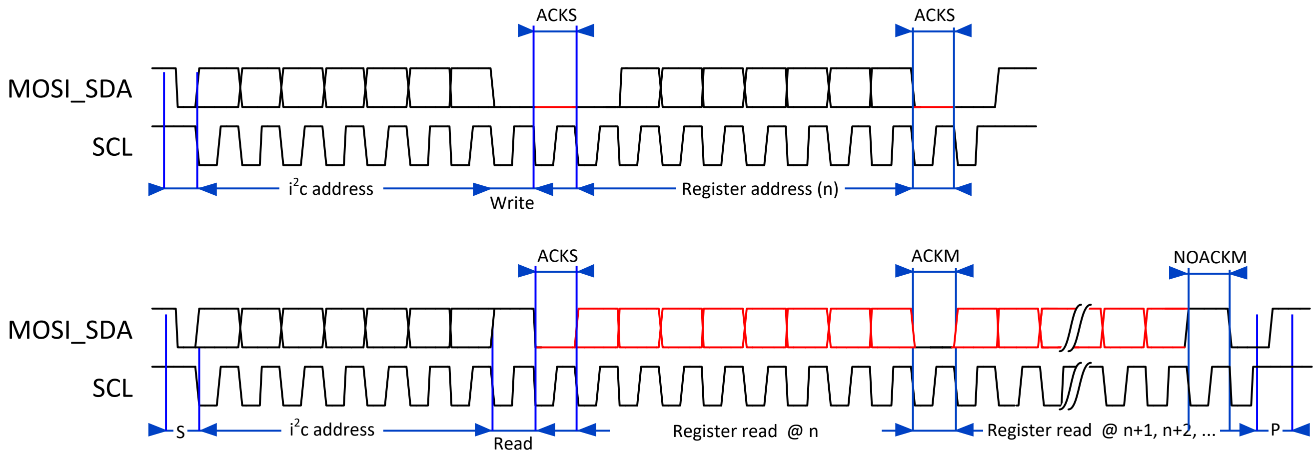


Figure 7-2: I2C read (multiple transactions)

In the case of a read transaction, it is possible to avoid stopping and starting again a new transaction by following the register address with a repeated start.

7.2. SPI INTERFACE

The SPI interface is a standard Serial to Peripheral Interface. It is compatible with two of the four standard transmission modes. The automatic selection between the two modes ([CPOL='0' and CPHA='0'] and [CPOL='1' and CPHA='1']) is determined by the value of SCL after the CS rising edge.

The SPI interface can be used in 4-wire or 3-wire. The 3-wire is selected by setting the register *reg_spi_i2c_cfg.spi_3w_en* to '1'. The pin MOSI is used as a data pin in 3-wire mode.

The SPI interface is a byte-oriented transmission interface. The first byte sent is contains the address of the register and access type of the transmission – on the first transmitted bit (reads register – '1' – or writes register – '0'). The following bytes contain register values. On read access the address read is incremented for each additional byte until the address 0x7F. When reaching this address, the devices internal address counter wraps to 0x00 and starts to read again from this address.

In case of a write transaction the protocol is based on an interleaved scheme of address and data. The first byte contains a 7-bit address and the write command (First sent bit of the first byte equal to '0'). The second byte contains data to be written to this address.

It is important to note that it is possible to send a set of write commands, followed by a multi read transaction within the same SPI transaction. Once in read mode, write accesses are not possible anymore in the same SPI transaction.

The following example shows a write of some registers followed by a check of the data.

0x00	0x05	0x01	0x03	0x06	0x02	0x80	0x00	0x00	0x00	0x00
Set hrv_period to 1/8 Hz		Set hrv_meas to 128ms		Set the system in primary cell mode		Read registers 0x00 to 0x03				

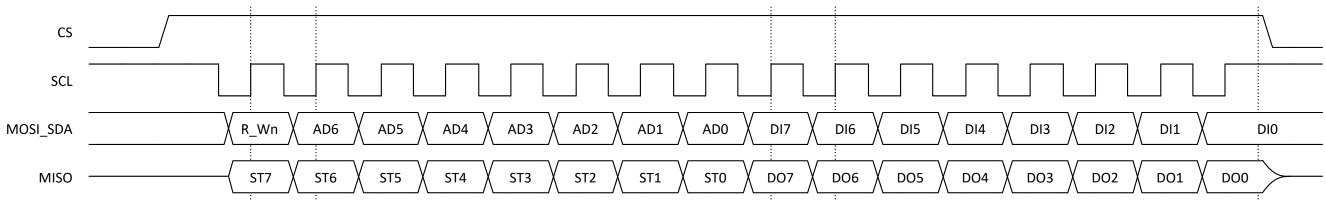


Figure 7-3 SPI transaction scheme CPOL=1, CPHA=1

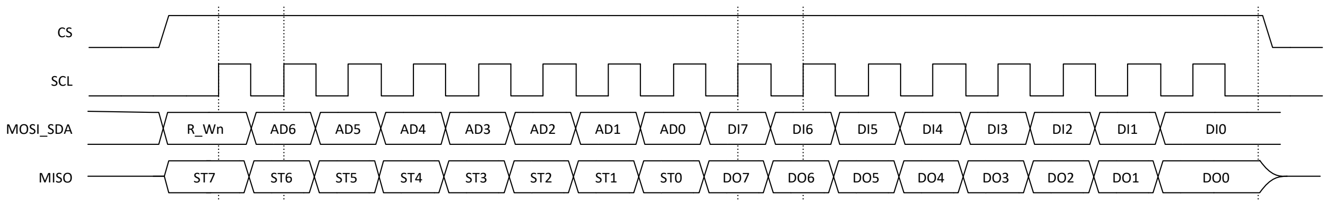


Figure 7-4 SPI transaction scheme CPOL=0, CPHA=0

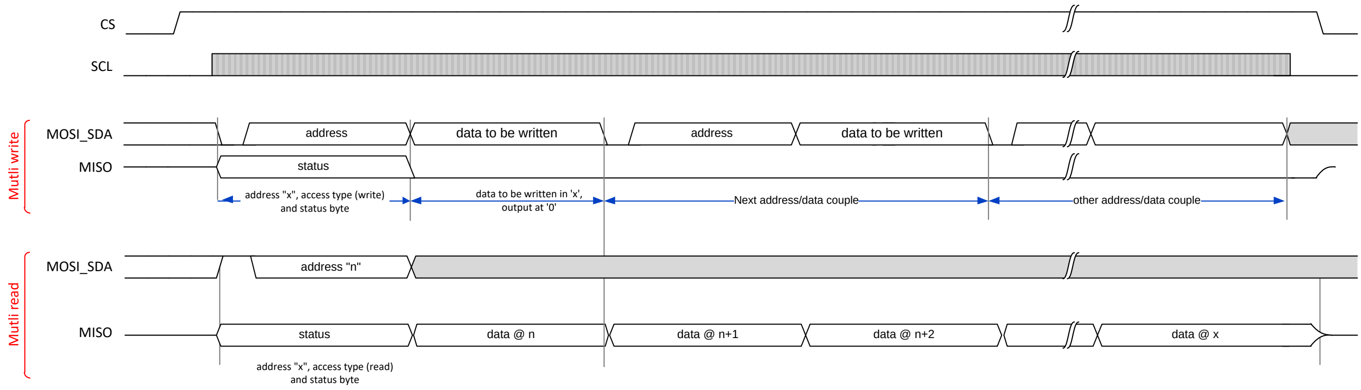


Figure 7-5 Multi register access transaction

Along with the address information the SPI interface sends the status register (*reg_status* – address 0x22) as the first response byte. In the case of the 3-wire mode the protocol is identical to the I²C interface, and doesn't allow having the status byte when sending the address to the device.

Interface signals are the following:

- CS chip select, active high
- SCL clock
- MOSI_SDA data input; data input/output in 3-wire mode
- MISO data output; Hi-Z level in 3-wire mode

7.2.1. INTERFACE SELECTION

The interface selection process is done through the use of the CS pin.

At reset (at the end of the boot sequence) the default interface selection is I²C. The SPI selection is done by asserting the CS pin. After CS assertion the SPI interface is selected until the device is shut-down (V_{STS} below V_{cs_lo}).

If the CS pin is continuously asserted (through a hard connection to VSUP) the SPI interface is permanently selected. I²C is not available in this case.

Register name: reg_spi_i2c_cfg			Address: 0x18	Default value mapped in E²PROM
Bits	**Bit name**	**Type**	**Description**	
7	spi_3w_en	RW	Set the SPI in its 3 wire mode (shared MOSI/MISO)	
6:0	i2c_addr	RW	i2c address	

Table 28 SPI/I2C configuration register (0x18)

7.3. E2PROM

7.3.1. ACCESSING THE E2PROM

The on-chip E²PROM contains the default working parameters of the device. The E²PROM address space is mapped into the EM8502 register map from address 0x40 (E²PROM address 0) to 0x7F ((E²PROM address 63). Some addresses are reserved (0x76 to 0x7F) and are accessible in read-only mode by the user; some contains the defaults values – as described on §8. All other addresses can be freely used.

The user can write on the E²PROM at any time. Note that no protection is built in to prevent incomplete write transaction caused by a lack of energy (STS too low). The user must ensure that the EM8502 is able to properly finish a write transaction.

Read and write accesses are performed through the serial interface. In difference to standard registers (addresses 0x00 to 0x3F), an E²PROM access requires a dead time. A read access needs a dead time between read address and the data. A write access requires a dead time after having sent the write data.

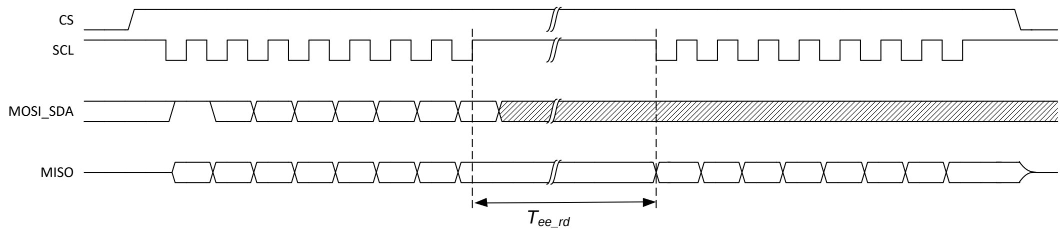


Figure 7-6 SPI transaction for reading the E²PROM (CPOL=1)

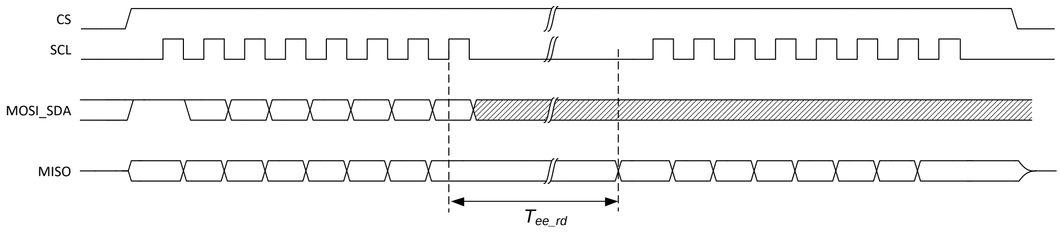


Figure 7-7 SPI transaction for reading the E²PROM (CPOL=0)

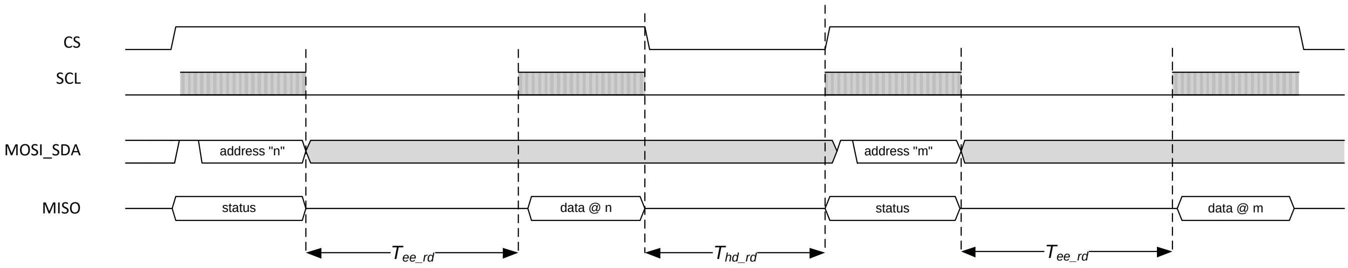


Table 29 SPI multiple E²PROM read transactions

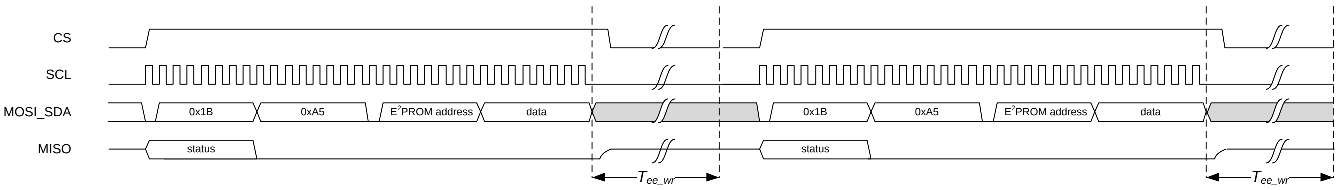


Figure 7-8 Two consecutive single E²PROM write SPI transactions

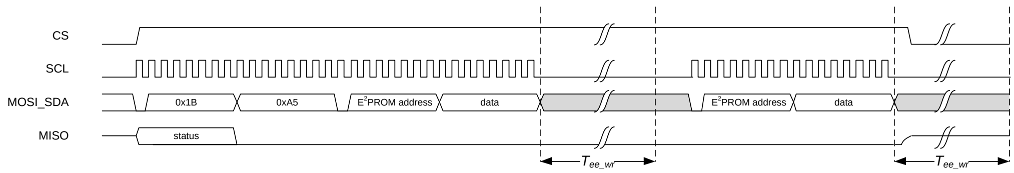


Figure 7-9 SPI multi-byte transaction for writing the E²PROM

When the I²C serial interface is used only single action per transaction is allowed when accessing the E²PROM. As for an SPI transaction a dead time are necessary. Prior to a write transaction into the E²PROM it is necessary to set the *reg_protection_key* register to 0xA5.

For a write transaction, no other I²C transaction into the E²PROM address area is allowed for T_{wr_ee} after the end of the write transaction. A transaction inside this time window is ignored by the device.

In the following diagram responses from EM8502 are shown in red, data from the I²C master in black.

The following abbreviations are used:

- W Write transaction request
- R Read transaction request
- S Start an I²C transaction
- P Stop an I²C transaction
- A I²C Acknowledge
- N I²C Non Acknowledge

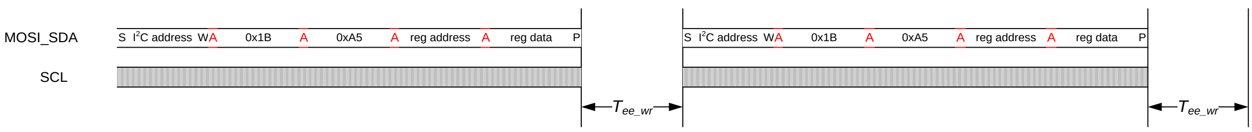


Figure 7-10 I²C transaction for writing on the E²PROM

For a read transaction a dead-time (T_{rd_ee}) has to be inserted in between the address setting transaction and the read action itself.

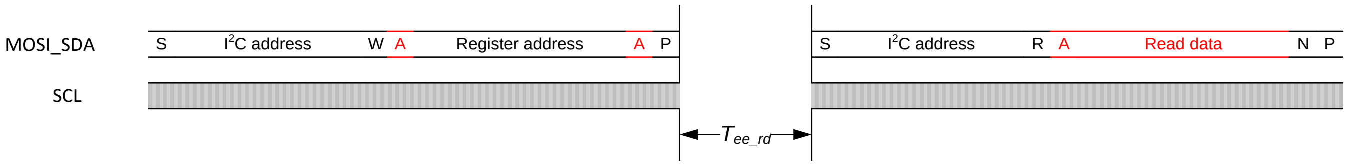


Figure 7-11 I²C transaction for reading the E²PROM

8. REGISTER MAP

Register Name	Address Hex	Address Dec	Factory Value	7	6	5	4	3	2	1	0
reg_t_hrv_period	0x00	0	0x05	-	-	-	-	-	t_hrv_period(2:0)		
reg_t_hrv_meas	0x01	1	0x03	-	-	-	-	-	t_hrv_meas(2:0)		
reg_t_sts_period	0x02	2	0x02	-	-	-	-	-	t_sts_period(2:0)		
reg_t_lts_period	0x03	3	0x05	-	-	-	-	-	t_lts_period(2:0)		
reg_v_hrv_cfg	0x04	4	0x01	-	0	v_hrv_min(5:0)					
reg_hrv_check_lvl	0x05	5	0x01	-	-	-	-	hrv_check_lvl(3:0)			
reg_lts_cfg	0x06	6	0x00	-	-	-	-	-	0	0	no_bat_protect
reg_v_bat_max_hi	0x07	7	0x29	-	-	v_bat_max_hi(5:0)					
reg_v_bat_max_lo	0x08	8	0x28	-	-	v_bat_max_lo(5:0)					
reg_v_bat_min_hi_dis	0x09	9	0x1E	-	-	v_bat_min_hi_dis(5:0)					
reg_v_bat_min_hi_con	0x0A	10	0x1E	-	-	v_bat_min_hi_con(5:0)					
reg_v_bat_min_lo	0x0B	11	0x1D	-	-	v_bat_min_lo(5:0)					
reg_v_apl_max_hi	0x0C	12	0x25	-	-	v_apl_max_hi(5:0)					
reg_v_apl_max_lo	0x0D	13	0x21	-	-	v_apl_max_lo(5:0)					
reg_ldo_cfg	0x0E	14	0x91	vsup_tied_low	v_vaux_ldo(2:0)			frc_ulp_ldo	v_ulp_ldo(2:0)		
reg_pwr_cfg	0x0F	15	0x00	usb_ldo_frc_dis	dis_vaux_gnd2_hrv_low	dis_vaux_gnd1_hrv_low	dis_vaux_gnd0_hrv_low	dis_vaux2_hrv_low	dis_vaux1_hrv_low	dis_vaux0_hrv_low	dis_vsup_hrv_low
reg_vaux_cfg	0x10	16	0x00	-	-	vaux2_cfg(1:0)		vaux1_cfg(1:0)		vaux0_cfg(1:0)	
reg_vaux_gnd_cfg	0x11	17	0x00	-	-	-	-	-	vaux_gnd2_cfg	vaux_gnd1_cfg	vaux_gnd0_cfg
reg_mppt_ratio	0x12	18	0x06	-	-	-	-	0x06			
reg_ext_cfg	0x13	19	0x61	sda_slopectrl	wake_up_deb_en	wake_up_edge_cfg(1:0)		usb_frc_hrv_low_hiz	usb_frc_bat_low_hiz	usb_crt_src_sel(1:0)	
reg_t_sleep_vsup_lo	0x14	20	0xE8	t_sleep_vsup_lo(7:0)							
reg_t_sleep_vsup_mid	0x15	21	0x03	t_sleep_vsup_mid(7:0)							
reg_t_sleep_vsup_hi	0x16	22	0x00	t_sleep_vsup_hi(7:0)							
reg_t_hrv_low_cfg	0x17	23	0x07	-	t_hrv_low_period(2:0)			-	t_lts_hrv_low_period(2:0)		
reg_spi_i2c_cfg	0x18	24	0x77	spi_3w_en	i2c_addr(6:0)						
reg_pwr_mgt	0x19	25	0x00	0	vaux_gnd2_en	vaux_gnd1_en	vaux_gnd0_en	vaux2_en	vaux1_en	vaux0_en	sleep_vsup

Note: *Italic-underlined* registers are protected against accidental write action. For writing those registers it is required to first write reg_protect_key to **0x4B**, before writing into them within the same communication transaction – see §6.7.2

Table 30 Register summary with default value defined in E^2PROM

Register Name	Address		Reset	Index							
	Hex	Dec	Value	7	6	5	4	3	2	1	0
reg_soft_res_word	0x1A	26	0x00	soft_res_word(7:0)							
reg_protect_key	0x1B	27	0x00	protect_key(7:0)							
reg_lux_meter_cfg	0x1C	28	0x00	-	lux_auto_meas	lux_auto_rng	lux_manu	lux_lvl(3:0)			
reg_lux_meter_result	0x1D	29	0x00	-	-	-	lux_meter_busy	lux_meter_result(3:0)			
reg_status	0x22	34	0x00	eeprom_data_busy	hrv_lux_busy	hrv_low	bat_low	sw_solar_lts_nsts	sw_lts_sts	usb_on	lts_protect
reg_vld_status	0x23	35	0x00	lts_bat_min_hi	lts_bat_min_lo	sts_bat_max_hi	sts_bat_max_lo	sts_apl_max_hi	sts_apl_max_lo	sts_bat_min_hi	sts_bat_min_lo

Note: *Italic-underlined* register (reg_soft_res_word) is protected against accidental write action. For writing it, it is required to first write reg_protect_key to **0xE2**, before writing into them within the same communication transaction – see §6.7.2

Table 31 Register summary – No E²PROM default values

Register Name	Address		Factory	Index							
	Hex	Dec	Value	7	6	5	4	3	2	1	0
eeprom0	0x40	64	0x05	-	-	-	-	-	t_hrv_period(2:0)		
eeprom1	0x41	65	0x03	-	-	-	-	-	t_hrv_meas(2:0)		
eeprom2	0x42	66	0x02	-	-	-	-	-	t_sts_period(2:0)		
eeprom3	0x43	67	0x05	-	-	-	-	-	t_lts_period(2:0)		
eeprom4	0x44	68	0x01	-	-	v_hrv_min(5:0)					
eeprom5	0x45	69	0x01	-	-	-	-	hrv_check_lvl(3:0)			
eeprom6	0x46	70	0x00	-	-	-	-	-	-	-	no_bat_protect
eeprom7	0x47	71	0x29	-	-	v_bat_max_hi(5:0)					
eeprom8	0x48	72	0x28	-	-	v_bat_max_lo(5:0)					
eeprom9	0x49	73	0x1E	-	-	v_bat_min_hi_dis(5:0)					
eeprom10	0x4A	74	0x1E	-	-	v_bat_min_hi_con(5:0)					
eeprom11	0x4B	75	0x1D	-	-	v_bat_min_lo(5:0)					
eeprom12	0x4C	76	0x25	-	-	v_apl_max_hi(5:0)					
eeprom13	0x4D	77	0x21	-	-	v_apl_max_lo(5:0)					
eeprom14	0x4E	78	0x91	vsup_tied_low	v_vaux_ldo(2:0)			frc_ulp_ldo	v_ulp_ldo(2:0)		
eeprom15	0x4F	79	0x00	usb_ldo_frc_dis	dis_vaux_gnd2_hrv_low	dis_vaux_gnd1_hrv_low	dis_vaux_gnd0_hrv_low	dis_vaux2_hrv_low	dis_vaux1_hrv_low	dis_vaux0_hrv_low	dis_vsup_hrv_low
eeprom16	0x50	80	0x00	-	-	vaux2_cfg(1:0)		vaux1_cfg(1:0)		vaux0_cfg(1:0)	
eeprom17	0x51	81	0x00	-	-	-	-	-	vaux_gnd2_cfg	vaux_gnd1_cfg	vaux_gnd0_cfg
eeprom18	0x52	82	0x06	-	-	-	-	-	-	-	-
eeprom19	0x53	83	0x61	sda_slopectrl	wake_up_deb_en	wake_up_edge_cfg(1:0)		usb_frc_hrv_low_hiz	usb_frc_bat_low_hiz	usb_crt_src_sel(1:0)	
eeprom20	0x54	84	0xE8	t_sleep_vsup_lo(7:0)							
eeprom21	0x55	85	0x03	t_sleep_vsup_mid(7:0)							
eeprom22	0x56	86	0x00	t_sleep_vsup_hi(7:0)							
eeprom23	0x57	87	0x07	-	t_hrv_low_period(2:0)			-	t_lts_hrv_low_period(2:0)		
eeprom24	0x58	88	0x77	spi_3w_en	i2c_addr(6:0)						
eeprom25	0x59	89	0x00	0	vaux_gnd2_en	vaux_gnd1_en	vaux_gnd0_en	vaux2_en	vaux1_en	vaux0_en	sleep_vsup

Note: All E²PROM is protected against accidental write action. For writing into the E²PROM it is required to first write into reg_protect_key the value **0xA5**, before writing into it within the same communication transaction see §6.7.2

Table 32 E²PROM default values memory mapping

9. TYPICAL APPLICATION

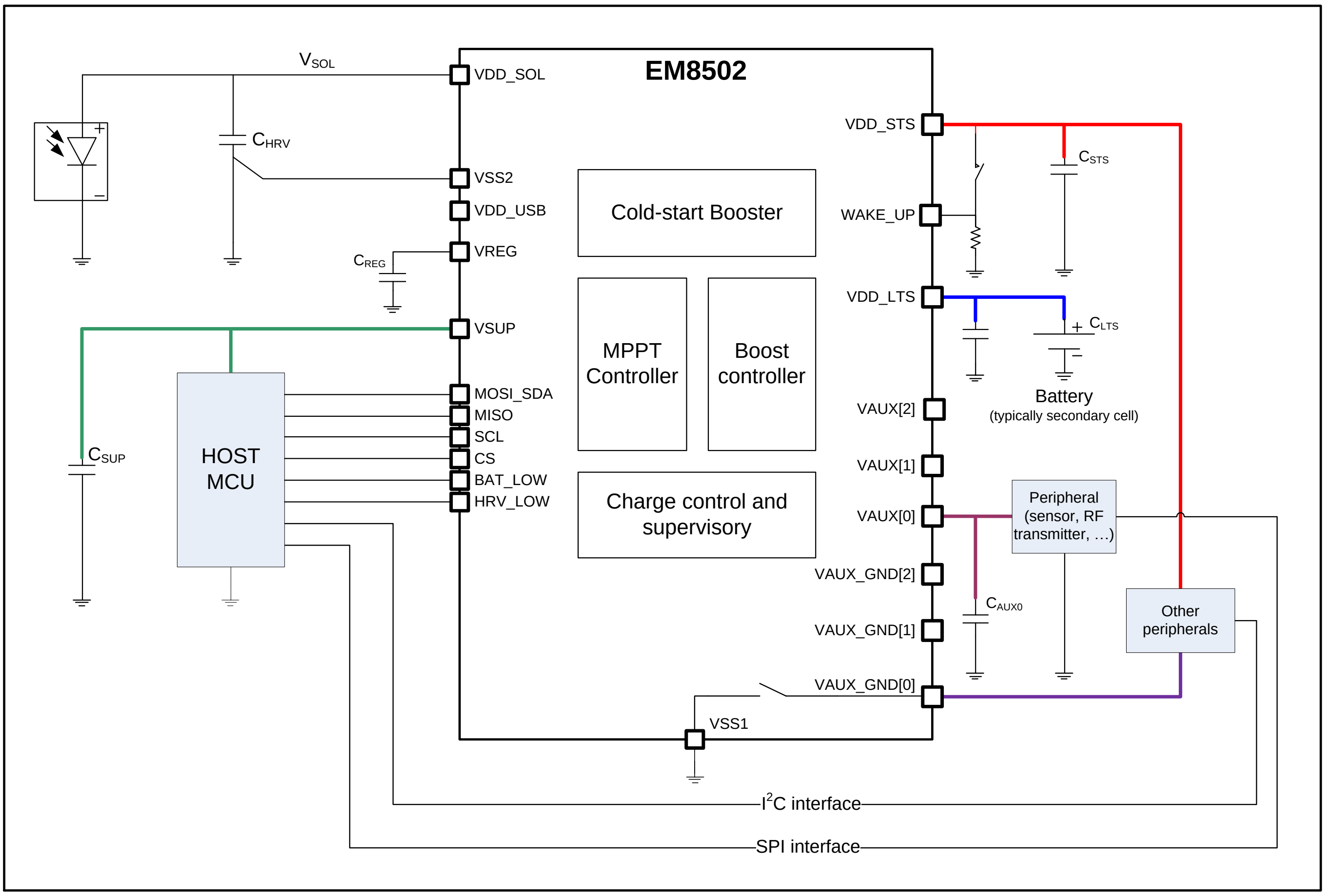


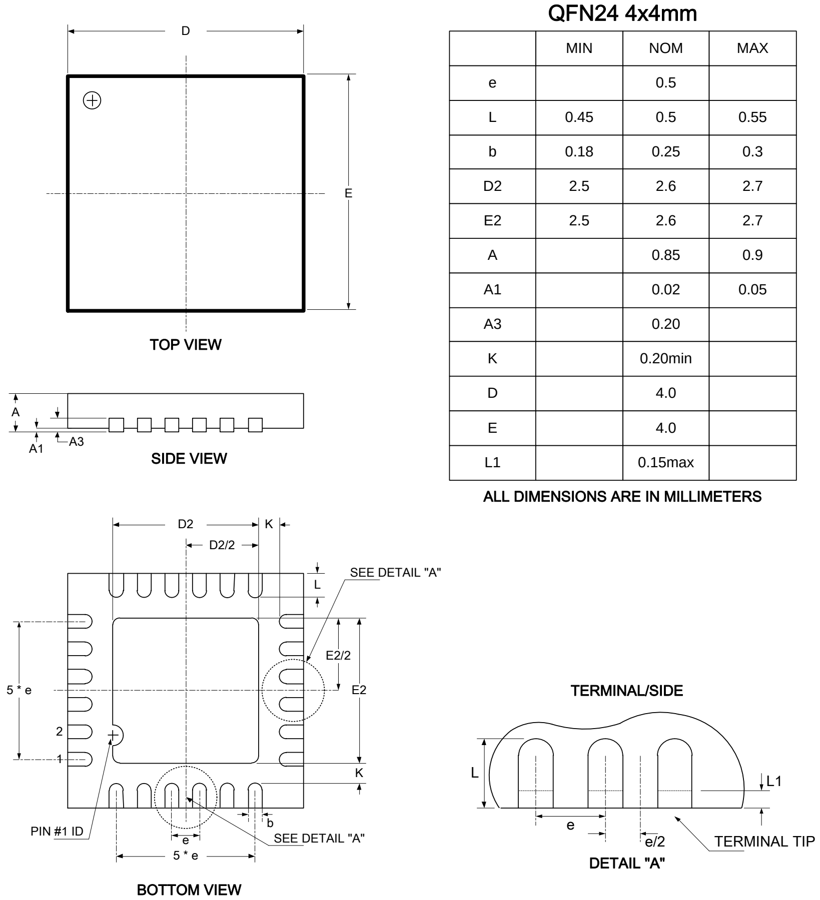
Figure 9-1 Example of Application with a Solar Cell Harvester

Component	Symbol	Value
Harvester capacitor	C_{HRV}	4.7µF
STS capacitor	C_{STS}	200µF
Regulator capacitor	C_{REG}	470 nF
Main supply output capacitor	C_{SUP}	1 µF
Auxiliary (2) supply output capacitor	C_{AUX2}	1 µF

Table 33 Component list for solar cell application

10. PACKAGING INFORMATION

10.1. QFN24 4X4 PACKAGE



QFN24 4x4mm

	MIN	NOM	MAX
e		0.5	
L	0.45	0.5	0.55
b	0.18	0.25	0.3
D2	2.5	2.6	2.7
E2	2.5	2.6	2.7
A		0.85	0.9
A1		0.02	0.05
A3		0.20	
K		0.20min	
D		4.0	
E		4.0	
L1		0.15max	

ALL DIMENSIONS ARE IN MILLIMETERS

Figure 10-1 QFN24 Mechanical Information

10.1.1. PACKAGE MARKING

This section reports the package marking for EM8502. Additional marking letters and numbers are used for lot traceability.

8	5	0	2	0
0	5			A