Green mode PWM Flyback Controller with External Over Temperature Protection

General Description

EM8633 is a high performance, low startup current, low cost, current mode PWM controller with green mode power saving. The EM8633 integrates functions of Soft Start(SS), Under Voltage Lockout(UVLO), Leading Edge Blanking(LEB), internal and external Over Temperature Protection(OTP), internal slope compensation. The EM8633 also features more protection like Over Load Protection(OLP) and Over Voltage Protection(OVP) to prevent circuit damage occurred under abnormal conditions.

The EM8633 provides the users a superior AC/DC power application of high efficiency, excellent EMI performance, low external component counts and lower cost solution.

Ordering Information

Part Number	Package	Remark
EM8633J	SOT-23-6	

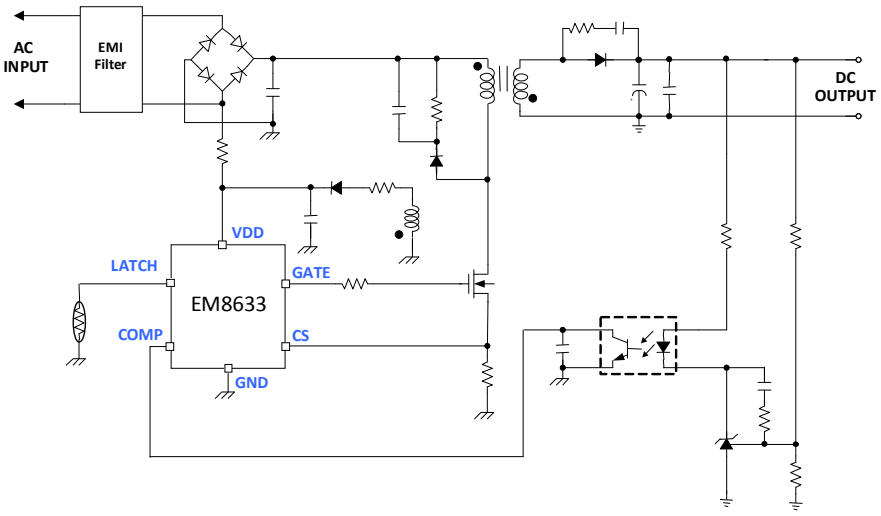
Features

- Ultra Low Start Up Current (6uA)
- Current Mode Control
- Soft Start Function
- Built-in Slope Compensation
- Internal Leading-edge Blanking
- Over Voltage Protection (OVP) on VDD pin
- Over Load Protection (OLP)
- Cycle-by-cycle Current Limit
- Feedback Open Protection
- External Over Temperature Protection (OTP)
- Internal Over Temperature Protection (OTP)
- Constant Output Power Limit (Full AC Input Range)
- Internal Frequency Jittering for Excellent EMI Performance
- Gate Voltage Clamping

Applications

- Switching AC/DC Adaptor and Charger
- Open-Frame SMP

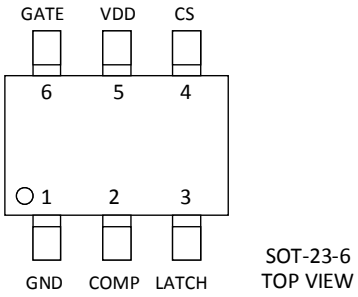
Typical Application Circuit



Protection Mode

VDD OVP	OLP	Latch Pin
Auto-Recovery	Auto-Recovery	Latch

Pin Configuration

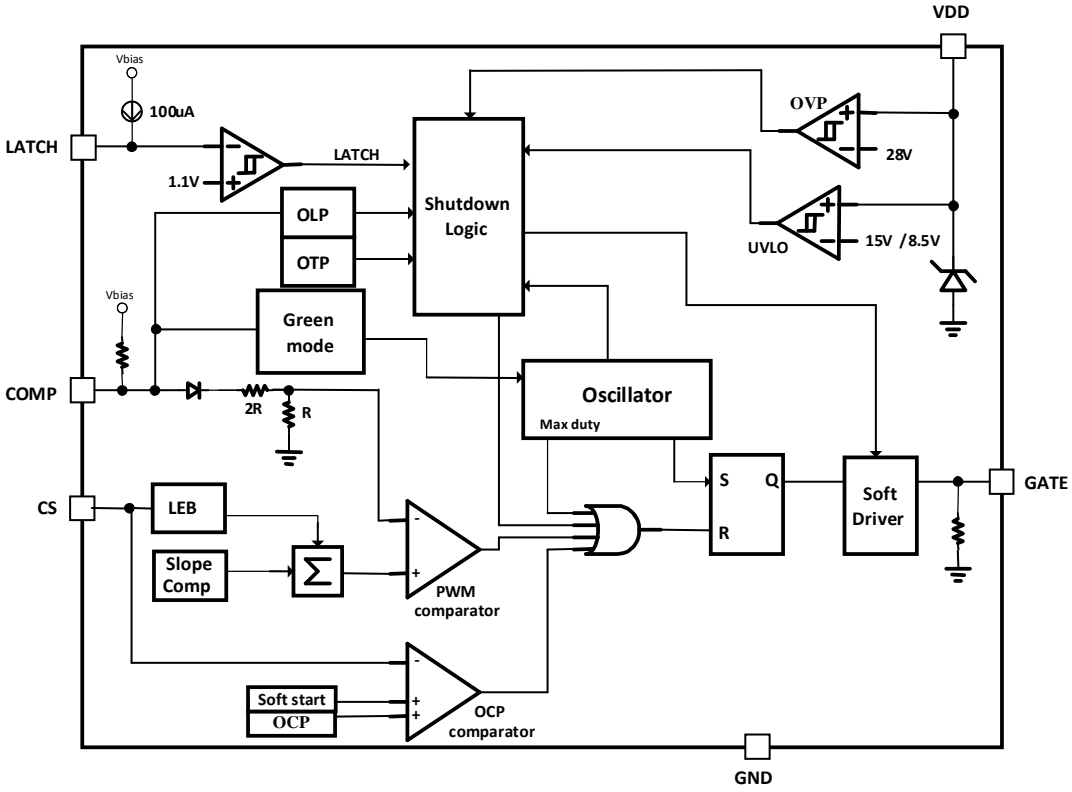


SOT-23-6
TOP VIEW

Pin Assignment

Pin Name	Pin Number	Pin Function
	SOT-23-6	
GND	1	Ground.
COMP	2	Voltage feedback pin. By connecting a photo-coupler to close the control loop and achieve the regulation.
LATCH	3	This pin provides an internal sourcing current of 100uA, used for external latch circuit. When this pin < 1.1V and after 160uS, IC is latch off. By connecting a NTC resistor to GND, it can achieve the OTP protection function. Keep this pin floating to disable the latch protection.
CS	4	Senses the primary current.
VDD	5	IC Power Supply Pin.
GATE	6	Gate drive output to drive the external MOSFET.

Function Block Diagram



Absolute Maximum Ratings (Note1)

- Supply Input Voltage, VDD ---------- 30V
- Gate pin---------- 30V
- LATCH, COMP, CS Pin ---------- - 0.3V to 6.5V
- Power Dissipation, PD @ TA = 25℃
  SOT-23-6 ---------- 0.4W
- Package Thermal Resistance
  SOT-23-6 ---------- 250℃/W
- Junction Temperature ---------- 150℃
- Lead Temperature (Soldering, 10 sec.) ---------- 260℃
- Storage Temperature Range ---------- -65℃ to 150℃
- ESD Susceptibility (Note2)
  HBM (Human Body Mode) ---------- 2KV
  MM (Machine Mode) ---------- 200V
- Gate Output Current---------- 300mA

Recommended Operating Conditions (Note3)

- Supply Input Voltage, VDD ---------- 11V to 26V
- Junction Temperature Range---------- -40℃ to 125℃
- Ambient Temperature Range---------- -40℃ to 85℃

Electrical Characteristics

(V_{DD}=15V, T_A=25℃, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
VDD Section						
VDD OVP Protect voltage	V_{OVP}		27	28	29	V
Start up Current	I_{START1}	VDD=7V	-	1	2	uA
	I_{START2}	VDD= V_{TH-ON} -0.5V	-	6	15	uA
VDD On Threshold Voltage	V_{TH-ON}		13.5	15	16.5	V
VDD Off Threshold Voltage	V_{TH-OFF}		7.5	8.5	9.5	V
VDD Reset Threshold Voltage	V_{RESET}			6		V
Operating Supply Current 1	I_{DD-OP1}	VDD=15V, V_{COMP}=0V,	-	2	3	mA
Operating Supply Current 2	I_{DD-OP2}	VDD=15V, V_{COMP}=3V, C_{GATE}=1nF	-	2.5	-	mA
Operating Supply Current 3	I_{DD-OP3}	VDD=15V, Protection triggerred	-	0.75	-	mA
Gate Section						
Rising Time	T_R	C_L = 1nF	-	150	200	nS
Falling Time	T_F	C_L = 1nF	-	30	100	nS
Current-Sense Section						
Maximum Internal Current Setpoint	V_{CSLim}		0.8	0.85	0.9	V
Leading Edge Blanking Time	T_{LEB}		200	300	400	nS
Propagation Delay Time	T_{PD}			100		nS
Soft-Start Period	T_{SS}			2		mS
Internal Oscillator						
Oscillation Frequency	f_{OSC}		60	65	70	KHz
Maximum Duty	D_{max}	V_{COMP}=3V, V_{CS}=0V	70	75	80	%
Green mode Minimum Frequency				22		KHz
Frequency Jittering	f_{jitter}			±6		%
Frequency Variation vs. VDD		VDD=11V to 25V			3	%
Frequency Variation vs. Temperature		-20℃ to 105℃ (Note4)			3	%

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
COMP Section						
COMP short to GND Current	I_{COMP}	V_{COMP}=0V		0.25	0.55	mA
Open loop COMP Voltage	V_{COMP}	COMP pin open		5.2		V
Green mode COMP Threshold Voltage	V_{Green}			1.8		V
Zero Duty COMP Threshold Voltage	V_{Zero}			1.1		V
Zero Duty COMP Hysteresis Voltage	V_{Zero_hy}			0.1		V
LATCH Section						
LATCH Pin Source Current	I_{LATCH}		95	100	105	uA
Turn-on Voltage	V_{LATCH_ON}			1.2		V
Turn-off Voltage	V_{LATCH_OFF}		1.05	1.10	1.15	V
LATCH Debounce Time	T_{LATCH}		100	160	220	uS
Protection Section						
Open loop Protection Delay Time	T_{Delay}			56	76	mS
Gate Clampping Voltage	V_{GATE}	VDD=20V		16		V
Open loop Protection COMP Trip Voltage	V_{OLP}			4.2		V
Internal Temperature Shutdown	T_{SD}			160		℃

Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. Devices are ESD sensitive. Handling precaution is recommended.

Note 3. The device is not guaranteed to function outside its operating conditions.

Note 4. Guaranteed by design.

Typical Operating Characteristics

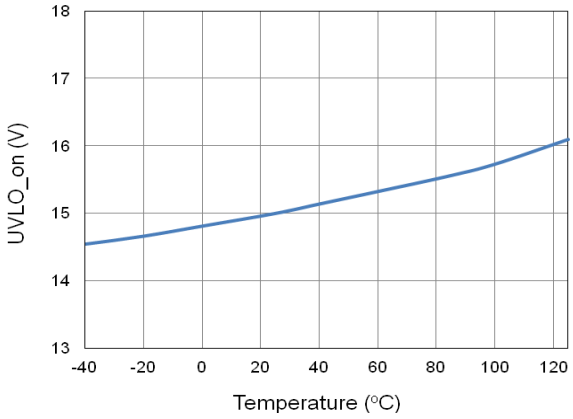


Fig1. UVLO_ON vs. Temperature

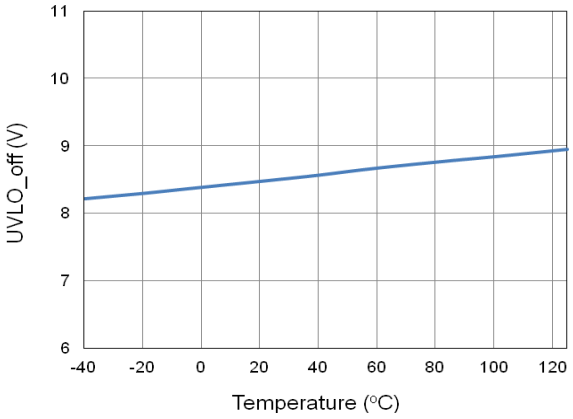
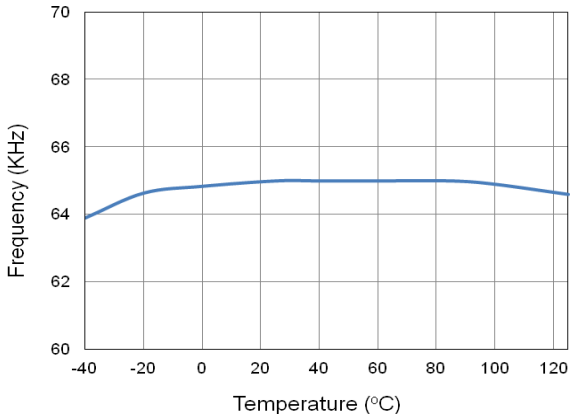


Fig2. UVLO_OFF vs. Temperature



Fg3. Frequency vs. Temperature

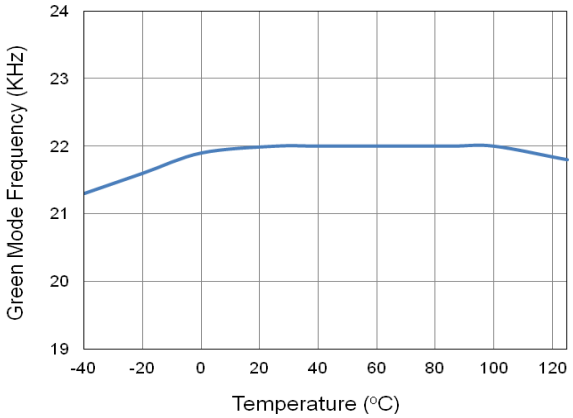


Fig4. Green Mode Frequency vs. Temperature

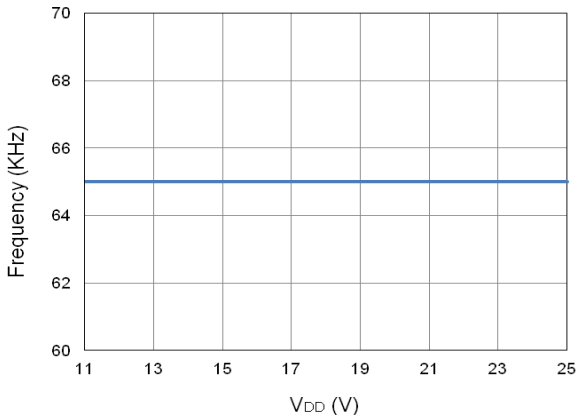


Fig5. Frequency vs. V_{DD}

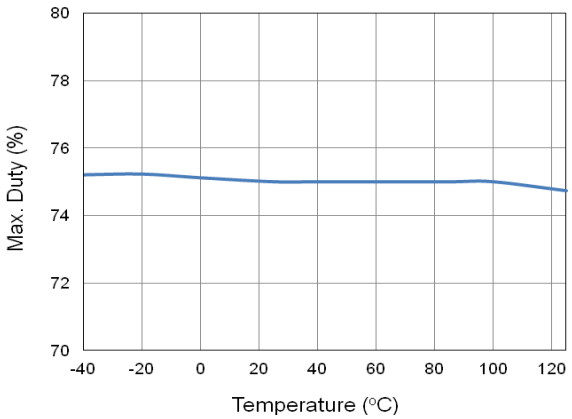


Fig6. Maximum Duty vs. Temperature

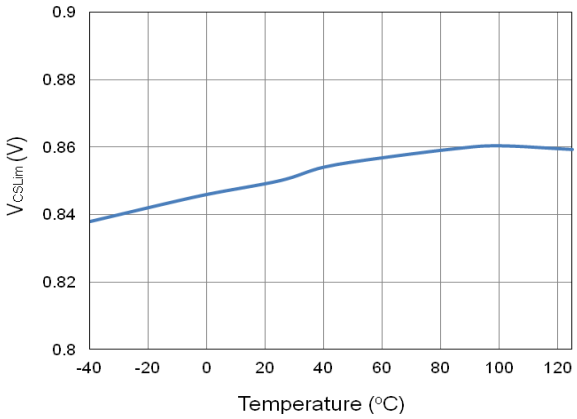


Fig7. V_{CSLim} vs. Temperature

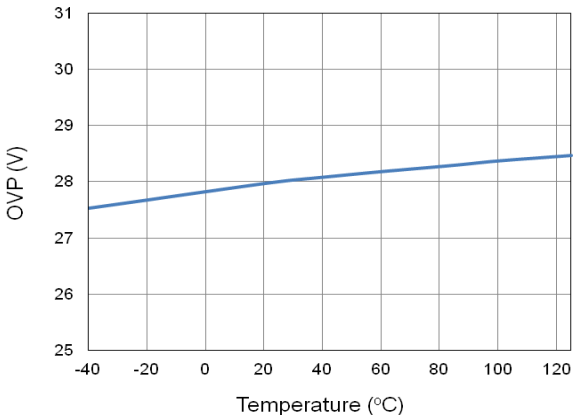


Fig8. OVP vs. Temperature

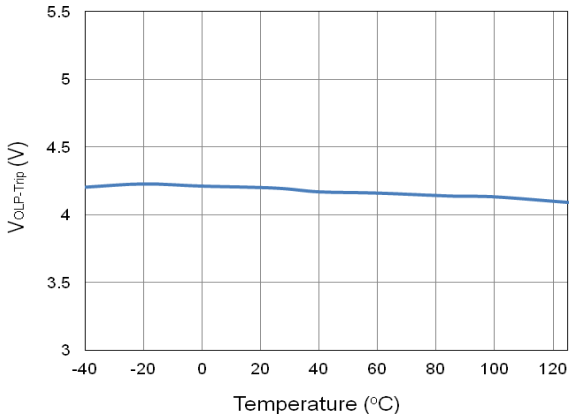


Fig9. $V_{OLP-Trip}$ vs. Temperature

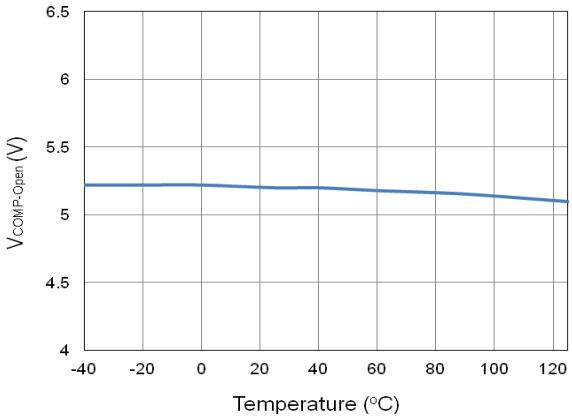


Fig10. $V_{COMP-Open}$ vs. Temperature

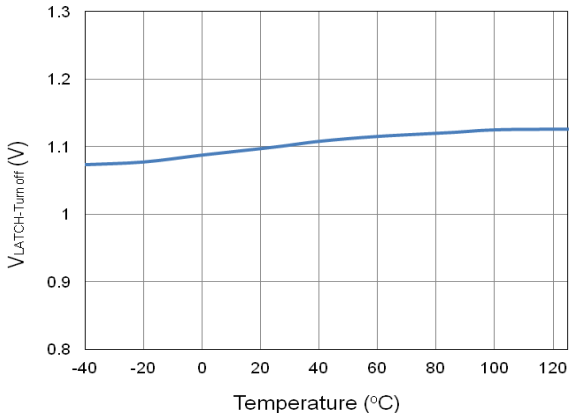


Fig11. $V_{LATCH-Turn\ off}$ vs. Temperature

Functional Description

UVLO

An UVLO comparator is implemented in EM8633 to monitor the VDD pin voltage. As shown in Fig. 12, a hysteresis is built in to prevent the shutdown from the voltage drop during startup. The UVLO (on) and UVLO (off) are setting at 15V and 8.5V, respectively.

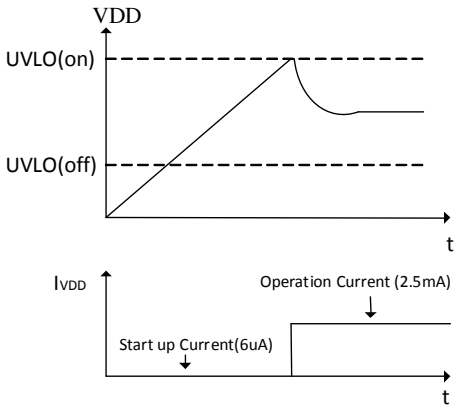


Fig. 12

Startup Operation

Fig. 13 shows a typical startup circuit and transformer auxiliary winding for the EM8633 application, it consumes only startup current (typical 6uA) and the current supplied through the startup resistor charges the VDD capacitor (C_{VDD}). When VDD reaches UVLO (on) voltage, EM8633 begins switching and the current consumed increases to 2.5mA. Then, the power required is supplied from the transformer auxiliary winding. The hysteresis of UVLO (off) provides more holdup time, which allows using a small capacitor for VDD. The ultra low startup current (typical 6uA) allow system using higher resistance value of R_{Start}. It provides a fast startup and low power dissipation solution.

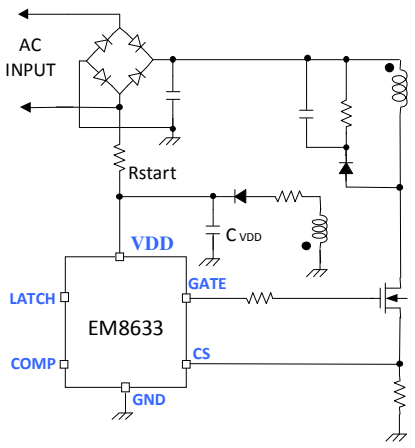


Fig. 13

Switching Frequency

To guarantee accurate frequency, EM8633 is trimmed to 7% tolerance. The switching frequency is 65KHz (Tpy.) with +-6% jitter range.The internal oscillator also generates slope compensation, 75% maximum duty limit.

Leading Edge Blanking (LEB)

Each time the power MOSFET turn on, the MOSFET C_{OSS}, secondary rectifier reverse recovery current and gate driver sourcing current comprise the current spike. To avoid premature termination of the switching pulse, a leading edge blanking time is built in. During the blanking time (300nS), the PWM comparator is off and cannot switch off the gate driver. It is recommended to adopt a smaller R-C filter (as show ad Fig.14) for high power application to avoid the total spike width over 300nS leading edge blanking time.

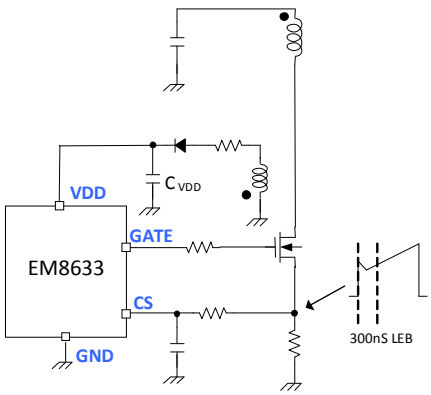


Fig. 14

Soft Start

The EM8633 has an internal soft-start circuit that increases cycle-by-cycle current limit comparator inverting input voltage slowly after it starts. The typical soft-start time is 2mS. The pulse width to the power MOSFET is progressively increased to establish the correct working conditions for transformers, rectifier diodes and capacitors. The voltage on the output capacitors is progressively increased with the intention of smoothly establishing the required output voltage. It also helps prevent transformer saturation and reduces the stress on the secondary diode during startup.

Slope compensation

In the conventional application, the problem of the stability is a critical issue for current mode controlling, when it operates in high than 50% of the duty cycle. The EM8633 built in saw-tooth slope compensation. So it requires no extra component.

Burst Mode Operation

At no load or light load condition, majority of the power dissipation in switching power supply is form switching loss on the power MOSFET, the core loss of the transformer and the loss on the snubber. The magnitude of power loss is in proportion to the number of switching events within a fixed period of time. Reducing switching events leads reduction on the power loss and conserves the energy.

The EM8633 adjusts the switching mode according to the load condition, the COMP pin voltage drops below burst mode threshold level. Device enters Burst Mode Control. The Gate drive output remains at off state to minimize the switching loss and reduces the standby power consumption.

Protection

The EM8633 provides many protection functions that intend to protect system from being damaged. All the protection functions are listed as below:

- **Cycle-by-cycle current limit**

  The EM8633 has over-current protection thresholds (0.85V). It is for cycle-by-cycle current limit, which turns off MOSFET for the remainder of the switching cycle when the sensing voltage of MOSFET current reaches the threshold.

- **Over-load / Open-loop Protection (OLP)**

  When feedback loop is open, as shown in Fig. 15, no current flows through the opto-coupler transistor, the EM8633 pulls up the COMP pin voltage to 5.2V.

  When the COMP pin voltage is above 4.2V longer than 56mS, OLP is triggered. This protection is also triggered when the SMPS output drops below the normal value longer than 56mS due to the overload condition.

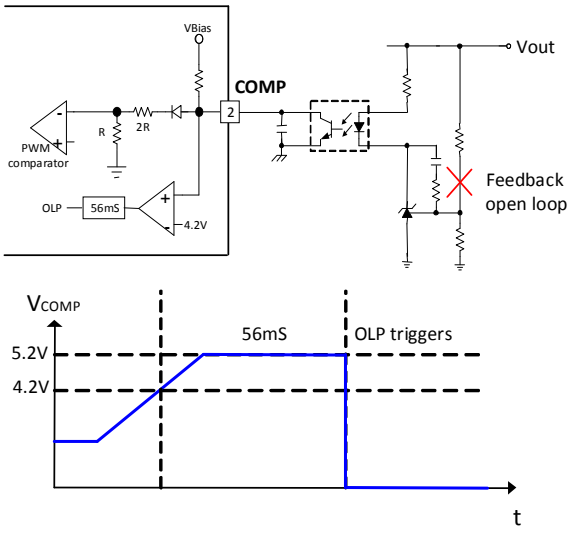


Fig. 15

- **Over Voltage Protection (OVP) on VDD**
  The EM8633 are implemented a Over-Voltage-Protection (OVP) on VDD. Whenever the VDD voltage is higher than the OVP threshold voltage (28V), the output gate drive will be shutdown to stop the switching of the power MOSFET until the next UVLO (on).
  The Over-Voltage-Protection on VDD function in EM8633 is an auto-restart type protection. If the OVP condition is not released, the VDD will tripped the OVP level again and re-shutdown the gate output. The VDD is working as a hiccup mode as shown in Fig. 16. On the other hand, if the OVP condition is removed, the VDD level will go back to normal level and the output will automatically return to the normal operation.

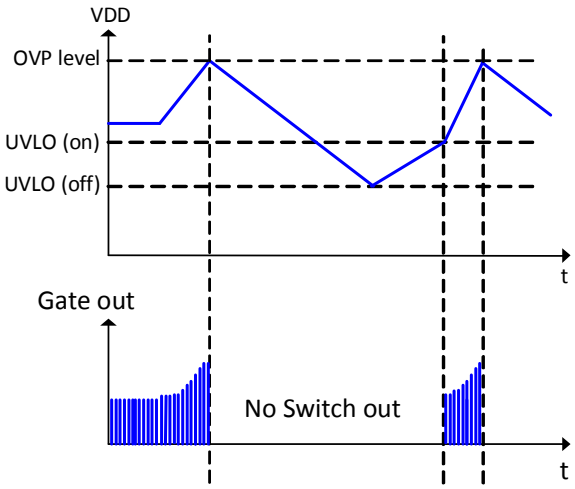


Fig. 16

- **Internal Over-Temperature Protection (OTP)**
  Internal 160℃ comparator will provide over temperature protection (OTP). OTP will shutdown system, until VDD below UVLO(low). The system will hiccup, if the internal temperature always higher than 160℃.

- **External Over-Temperature Protection (OTP)**
  The LATCH pin is equipped with a latch shutdown function. (Fig. 17) By decreasing the LATCH pin voltage to 1.1V or lower, the IC enters the latch mode. To reset latch mode, remove the AC power line, thus decreasing the VDD voltage to the Reset Threshold Voltage (6V) or lower. If the external latch shutdown function by the LATCH pin is not to be used, let this pin floating or connecting a capacitor only.
  Connect an NTC resistor to the LATCH pin to use the over-temperature protection. (Fig. 17)

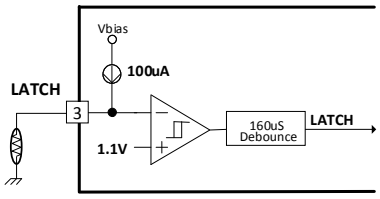
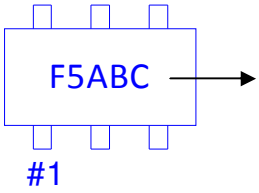


Fig.17

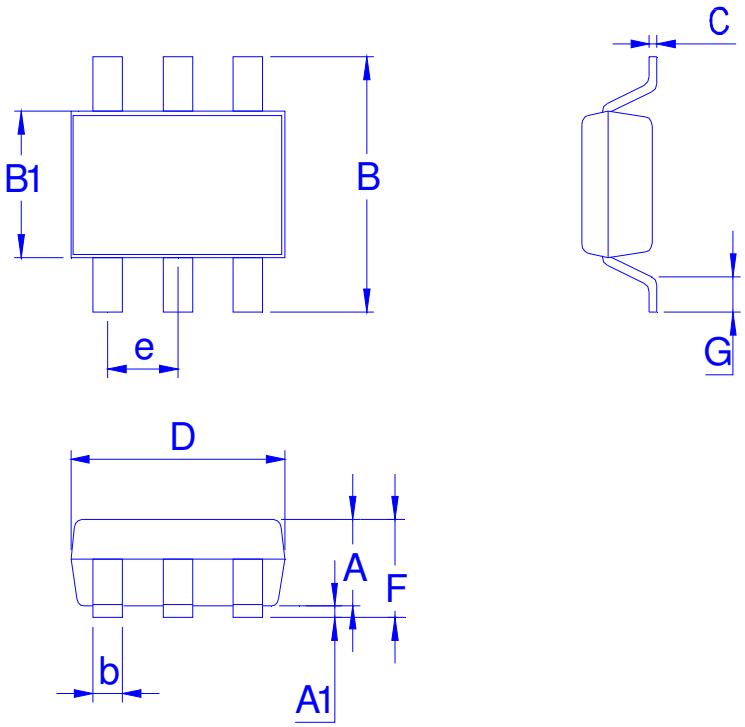
Ordering & Marking Information

Device Name: EM8633J for SOT-23-6



F5: Device Code, F5 for EM8633J
ABC: Date Code

Outline Drawing



Dimension in mm

Dimension	A	A1	B	B1	b	C	D	e	F	G
Min.	0.90	0.00			0.30	0.08				0.30
Typ.	1.15		2.80	1.60			2.90	0.95		0.45
Max.	1.30	0.15			0.50	0.22			1.45	0.60