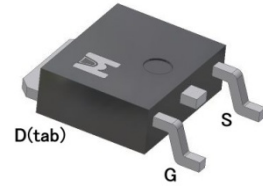
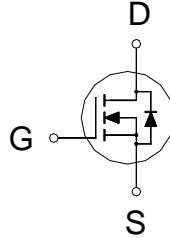


N-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

BV_{DSS}	25V
$R_{DS(on)}$ (MAX.)	4m Ω
I_D	80A



UIS, Rg 100% Tested

Pb-Free Lead Plating & Halogen Free



ABSOLUTE MAXIMUM RATINGS ($T_C = 25\text{ }^\circ\text{C}$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current	$T_C = 25\text{ }^\circ\text{C}$	I_D	80	A
	$T_C = 100\text{ }^\circ\text{C}$		50	
Pulsed Drain Current ¹		I_{DM}	170	
Avalanche Current		I_{AS}	53	
Avalanche Energy	$L = 0.1\text{mH}, I_D = 53\text{A}, R_G = 25\Omega$	E_{AS}	140	mJ
Repetitive Avalanche Energy ²	$L = 0.05\text{mH}$	E_{AR}	40	
Power Dissipation	$T_C = 25\text{ }^\circ\text{C}$	P_D	96	W
	$T_C = 100\text{ }^\circ\text{C}$		38	
Operating Junction & Storage Temperature Range		T_{j}, T_{stg}	-55 to 150	$^\circ\text{C}$

100% UIS testing in condition of $V_D = 15\text{V}, L = 0.1\text{mH}, V_G = 10\text{V}, I_L = 40\text{A}, \text{Rated } V_{DS} = 25\text{V N-CH}$

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	$R_{\theta JC}$		1.3	$^\circ\text{C} / \text{W}$
Junction-to-Ambient	$R_{\theta JA}$		75	

¹Pulse width limited by maximum junction temperature.

²Duty cycle $\leq 1\%$



ELECTRICAL CHARACTERISTICS ($T_c = 25\text{ }^\circ\text{C}$, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	25			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	1	1.5	3	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0V, V_{GS} = \pm 20V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 20V, V_{GS} = 0V$			1	μA
		$V_{DS} = 20V, V_{GS} = 0V, T_J = 125\text{ }^\circ\text{C}$			25	
On-State Drain Current ¹	$I_{D(ON)}$	$V_{DS} = 10V, V_{GS} = 10V$	80			A
Drain-Source On-State Resistance ¹	$R_{DS(ON)}$	$V_{GS} = 10V, I_D = 30A$		3.5	4	$m\Omega$
		$V_{GS} = 5V, I_D = 24A$		4.8	6	
Forward Transconductance ¹	g_{fs}	$V_{DS} = 5V, I_D = 24A$		30		S
DYNAMIC						
Input Capacitance	C_{iss}	$V_{GS} = 0V, V_{DS} = 15V, f = 1MHz$		3240		pF
Output Capacitance	C_{oss}			620		
Reverse Transfer Capacitance	C_{rss}			435		
Gate Resistance	R_g	$V_{GS} = 15mV, V_{DS} = 0V, f = 1MHz$		1.2		Ω
Total Gate Charge ^{1,2}	$Q_g(V_{GS}=10V)$	$V_{DS} = 15V, V_{GS} = 10V, I_D = 30A$		54		nC
	$Q_g(V_{GS}=5V)$			28		
Gate-Source Charge ^{1,2}	Q_{gs}			6.5		
Gate-Drain Charge ^{1,2}	Q_{gd}			15.5		
Turn-On Delay Time ^{1,2}	$t_{d(on)}$		$V_{DS} = 15V, I_D = 25A, V_{GS} = 10V, R_{GS} = 2.7\Omega$		22	
Rise Time ^{1,2}	t_r			16		
Turn-Off Delay Time ^{1,2}	$t_{d(off)}$			65		
Fall Time ^{1,2}	t_f			20		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS ($T_c = 25\text{ }^\circ\text{C}$)						
Continuous Current	I_S				80	A
Pulsed Current ³	I_{SM}				170	
Forward Voltage ¹	V_{SD}	$I_F = I_S, V_{GS} = 0V$			1.3	V
Reverse Recovery Time	t_{rr}	$I_F = I_S, di_F/dt = 100A / \mu S$		32		nS
Peak Reverse Recovery Current	$I_{RM(REC)}$			200		A
Reverse Recovery Charge	Q_{rr}			12		nC

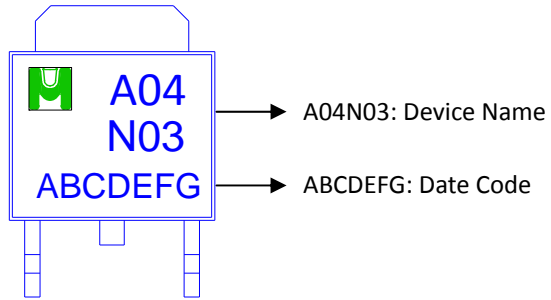
¹Pulse test : Pulse Width $\leq 300 \mu\text{sec}$, Duty Cycle $\leq 2\%$.

²Independent of operating temperature.

³Pulse width limited by maximum junction temperature.

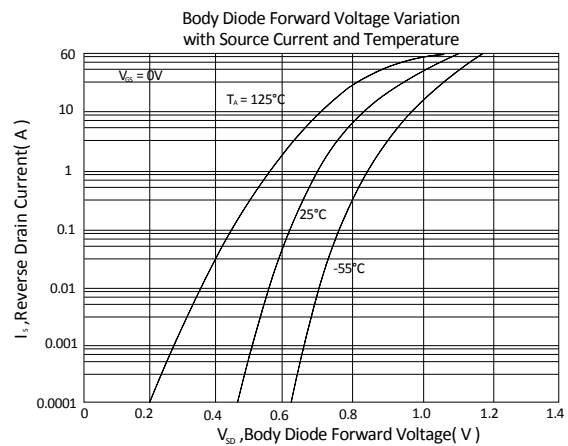
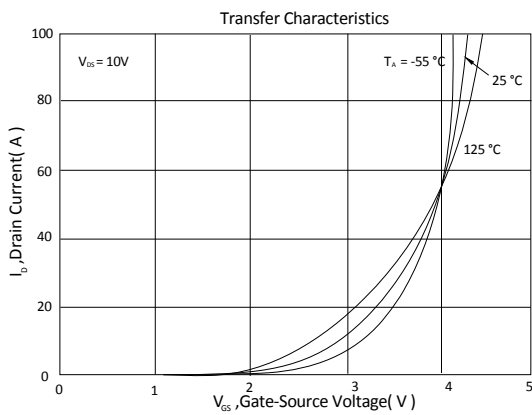
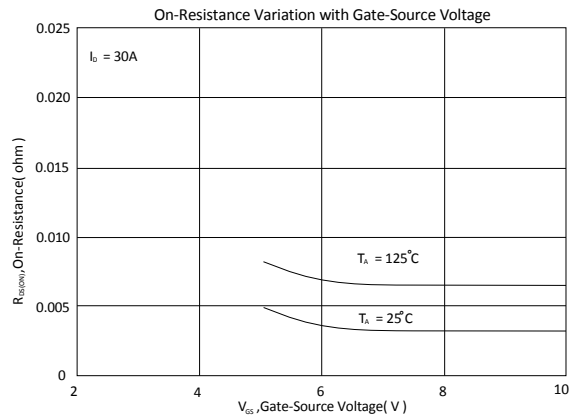
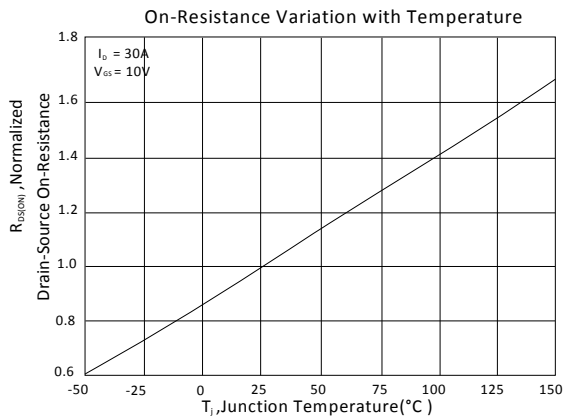
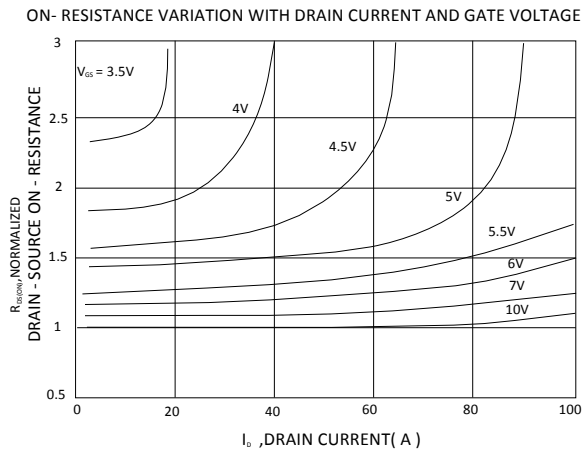
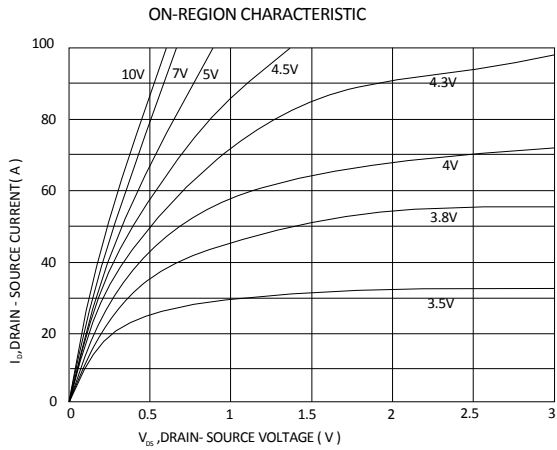
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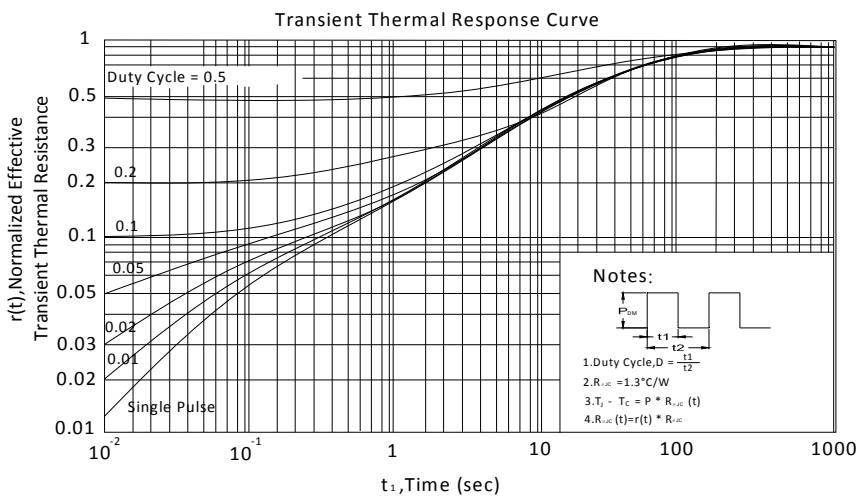
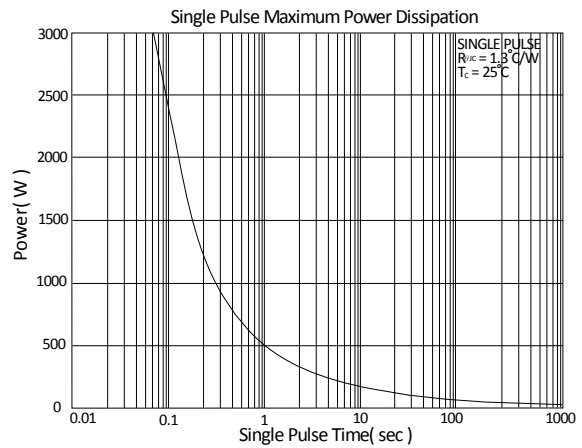
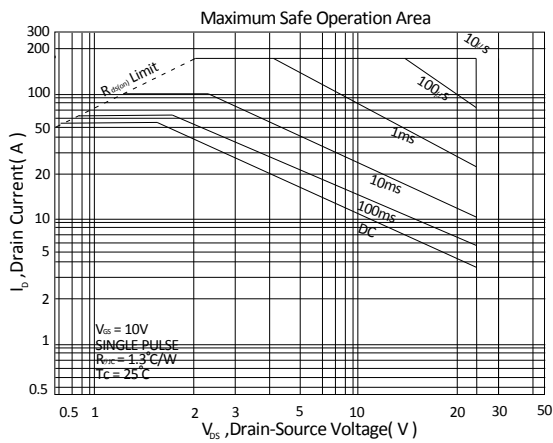
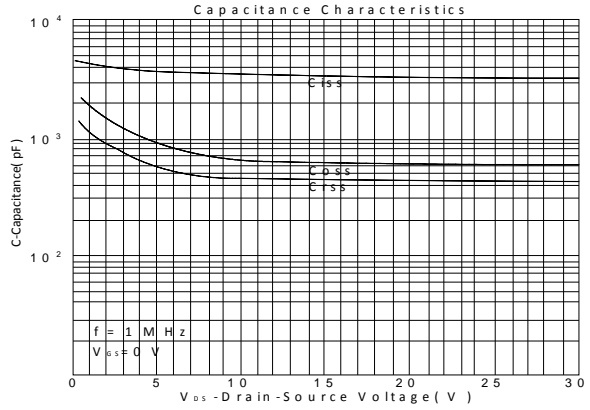
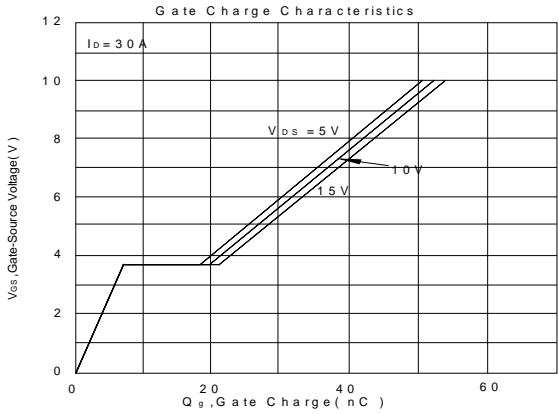
Device Name: EMA04N03A for DPAK (TO-252)





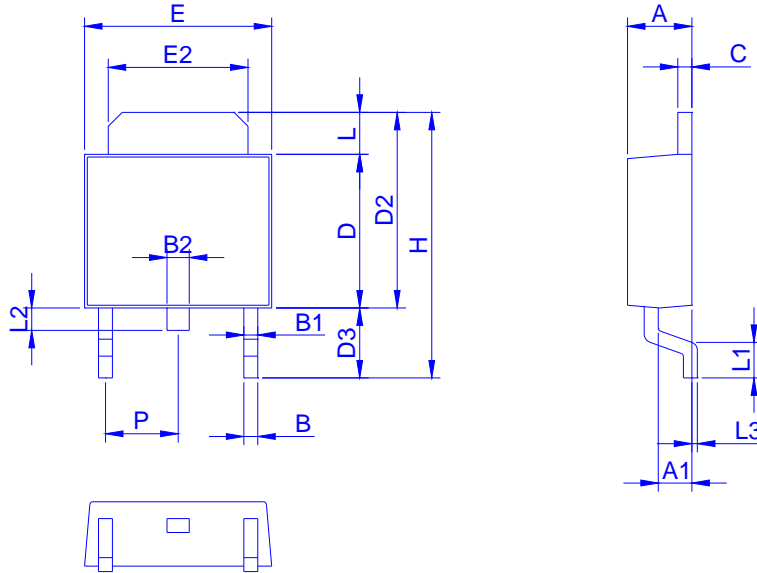
TYPICAL CHARACTERISTICS







Outline Drawing



Dimension	A	A1	B	B1	B2	C	D	D2	D3	E	E2	H	L	L1	L2	L3	P
Min.	2.10	0.95	0.30	0.40	0.60	0.40	5.30	6.70	2.20	6.40	4.80	9.20	0.89	0.90	0.50	0.00	2.10
Max.	2.50	1.30	0.85	0.94	1.00	0.60	6.20	7.30	3.00	6.70	5.45	10.15	1.70	1.65	1.10	0.30	2.50

Footprint

