1W Mono Audio Power Amplifier

General Description

The EMA1001 is an audio power amplifier primarily designed for portable communication applications such as mobile phones and portable multimedia players (PMP). To an 8Ω BTL load, it can deliver 1 watt of continuous average power with less than 1% distortion (THD+N) from a 5VDC supply.

The EMA1001 is pin-compatible to National Semi's LM4890 with a superior (THD+N). It does not require output coupling capacitors or bootstrap capacitors, and is ideal for mobile phone and other low voltage applications where minimal power consumption is a primary requirement.

The EMA1001 features a low-power consumption shutdown mode, and an internal thermal shutdown protection mechanism. Advanced pop & click circuitry is built in to eliminate noises that would otherwise occur during turn-on and turn-off transitions. The EMA1001 is unity-gain stable and can be configured by external gain-setting resistors.

EMP products are Pb-free and RoHS compliant.

Key Specifications

- PSRR at 217Hz, VDD = 5V (Fig. 1) 60dB(typ.)
- Power Output at 5.0V & 1% THD 1W(typ.)
- Power Output at 2.6V & 1% THD 250mW(typ.)
- Shutdown Current 0.1μA(typ.)

Features

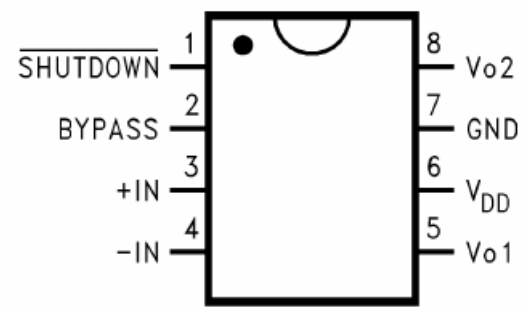
- Available in space-saving MSOP package
- Ultra low current shutdown mode
- BTL output driving capacitive loads
- Improved pop & click circuitry eliminating noises during turn-on and turn-off transitions
- 2.2 - 5.5V operation
- No output coupling capacitors, snubber networks or bootstrap capacitors required
- Thermal shutdown protection
- Unity-gain stable
- External gain configuration capability

Applications

- Mobile Phones
- PDAs and PMPs
- Portable Electronic Devices

Connection Diagram

MSOP/SOP Package



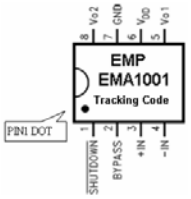
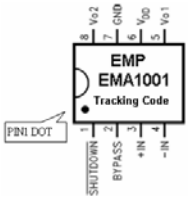
Order information

EMA1001-50MA08GRR/NRR

EMA1001-50SA08GRR/NRR

50	5.0V Operation
MA08	MSOP-8 Package
SA08	SOP-8 Package
GRR	RoHS (Pb Free)
	Rating: -40 to 85°C
	Package in Tape & Reel
NRR	RoHS & Halogen free (By Request)
	Rating: -40 to 85°C
	Package in Tape & Reel

Order, Mark & Packing Information

Package	Product ID	Marking	Packing
MSOP-8	EMA1001-50MA08GRR		3K units Tape & Reel
SOP-8	EMA1001-50SA08GRR		3K units Tape & Reel

Typical Application

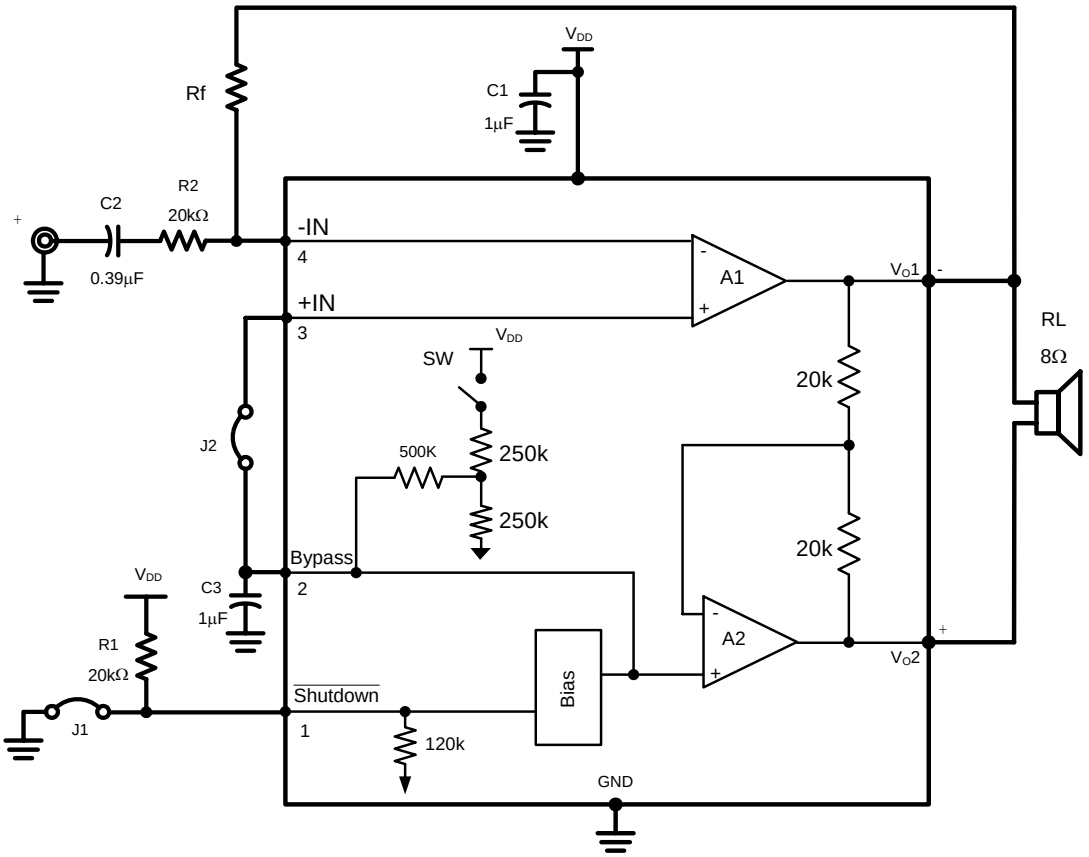


FIGURE 1. Typical Audio Amplifier Application Circuit

Absolute Maximum Ratings (Note 2)

Supply Voltage	6.0V
Storage Temperature	-65°C to +150°C
Input Voltage	-0.3V to VDD +0.3V
Power Dissipation (Note 3)	Internally Limited
ESD Susceptibility (Note 4)	2kV
Junction Temperature	150°C

Thermal Resistance	
θ_{JC} (MSOP)	56°C/W
θ_{JA} (MSOP)	190°C/W
θ_{JA} (DFN)	220°C/W
Operating Ratings	
Temperature Range	-40°C ≦ TA ≦ 85°C
Supply Voltage	2.0V ≦ VDD ≦ 5.5V

Electrical Characteristics V_{DD} = 5V (Notes 1, 2, 8)

The following specifications apply for the circuit shown in Figure 1 unless otherwise specified. Limits apply for TA = 25°C.

Symbol	Parameter	Conditions	Conditions		Units (Limits)
			Typical (Note 6)	Limit (Notes 7, 9)	
I_{DD}	Quiescent Power Supply Current	V_{IN} = 0V, Io = 0A, No Load	4	8	mA (max)
		V_{IN} = 0V, 8Ω Load	5	10	mA (max)
I_{SD}	Shutdown Current	$V_{SHUTDOWN}$ = 0V	0.1	1.0	µA (max)
V_{SDIH}	Shutdown Voltage Input high			1.2	V (min)
V_{SDIL}	Shutdown Voltage Input Low			0.4	V (max)
V_{OS}	Output Offset Voltage		5	25	mV (max)
P_O	Output Power (8Ω)	THD = 1% (max); f = 1 kHz	1.0	0.9	W
T_{WU}	Wake-up time	C_{bypass} = 1µF	100	220	ms (max)
T_{SD}	Thermal Shutdown Temperature		160	140	°C (min)
				180	°C (max)
THD+N	Total Harmonic Distortion + Noise	P_O = 0.4 Wrms; f = 1kHz	0.04		%
PSRR (Note 10)	Power Supply Rejection Ratio	V_{ripple} = 200mV sine p-p Input Terminated with 10 ohms to ground	60 (f =217Hz) 65 (f = 1kHz)	55	dB (min)
T_{SDT}	Shut Down Time	8Ω load	0.1		ms (max)

Electrical Characteristics V_{DD} = 2.6V (Notes 1, 2, 8)

The following specifications apply for the circuit shown in Figure 1 unless otherwise specified. Limits apply for TA = 25°C.

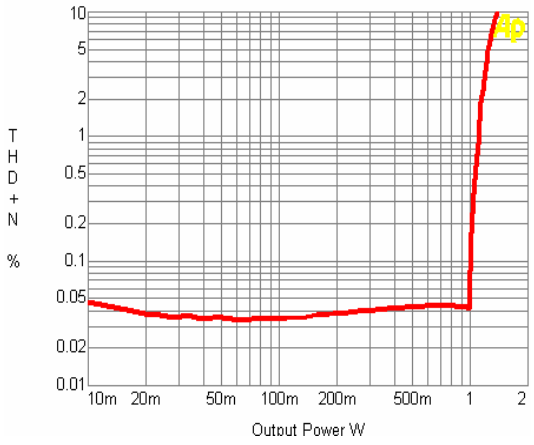
Symbol	Parameter	Conditions	Conditions		Units (Limits)
			Typical (Note 6)	Limit (Notes 7, 9)	
I_{DD}	Quiescent Power Supply Current	V_{IN} = 0V, Io = 0A, NoLoad	3	5	mA (max)
		V_{IN} = 0V, 8Ω Load	4	9	mA (max)
I_{SD}	Shutdown Current	$V_{SHUTDOWN}$ = 0V	0.1	1.0	µA (max)
V_{SDIH}	Shutdown Voltage Input High			1.2	V (min)
V_{SDIL}	Shutdown Voltage Input Low			0.4	V (max)
V_{OS}	Output Offset Voltage		5	25	mV (max)
P_O	Output Power (8Ω)	THD = 1% (max); f = 1 kHz	0.25	0.20	W(min)
T_{WU}	Wake-up time	C_{bypass} =1uF	100	220	ms (max)
T_{SD}	Thermal Shutdown Temperature		160	140	°C (min)
				180	°C (max)
THD+N	Total Harmonic Distortion + Noise	P_O = 0.2 Wrms; f = 1kHz	0.03		%
PSRR (Note 10)	Power Supply Rejection Ratio	V_{ripple} = 200mV sine p-p Input Terminated with 10 ohms to ground	60 (f =217Hz) 65 (f = 1kHz)	55	dB (min)
T_{SDT}	Shut Down Time	8 Ω load	0.1		ms (max)

Note 1: All voltages are measured with respect to the ground pin, unless otherwise specified.
Note 2: *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Operating Ratings* indicate conditions for which the device is functional, but do not guarantee specific performance limits. *Electrical Characteristics* state DC and AC electrical specifications under particular test conditions, which guarantee specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.
Note 3: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature T_A. The maximum allowable power dissipation is PDMAX = $(T_{JMAX}–T_A)/\theta JA$ or the number given in Absolute Maximum Ratings, whichever is lower. For the EMA1001, see power derating curves for additional information.
Note 4: Human body model, 100 pF discharged through a 1.5 kΩ resistor.
Note 5: Machine Model, 220 pF–240 pF discharged through all pins.
Note 6: Typicals are measured at 25°C and represent the parametric norm.
Note 7: Limits are guaranteed to EMP's AOQL (Average Outgoing Quality Level).
Note 8: Shutdown current is measured in a Normal Room Environment. Exposure to direct sunlight will increase ISD by a maximum of 2µA.
Note 9: Datasheet min/max specification limits are guaranteed by design, test, or statistical analysis.
Note 10: PSRR is a function of system gain. Specifications apply to the circuit in Figure 1 where A_V = 2. Higher system gains will reduce PSRR value by the amount of gain increase. A system gain of 10 represents a gain increase of 14dB. PSRR will be reduced by 14dB and applies to all operating voltages.

External Components Description (*Figure 1*)

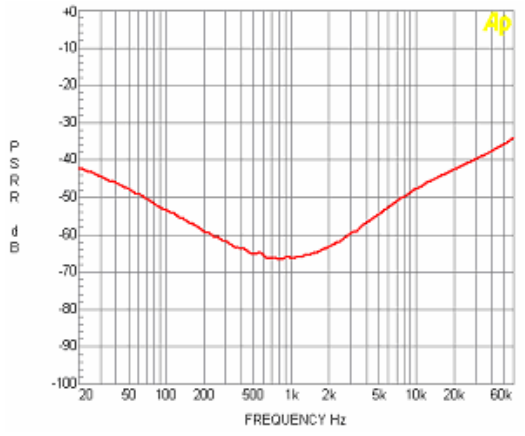
Components		Functional Description
1.	R_2	Inverting input resistance for setting the closed-loop gain in conjunction with R_f. This resistor also forms a high pass filter with C_2 at $f_C = 1/(2\pi R_2 C_2)$.
2.	C_2	Input coupling capacitor for blocking the DC voltage at the amplifier's input terminals. Also creates a high pass filter with C_2 at $f_C = 1/(2\pi R_2 C_2)$. Refer to the section, **Proper Selection of External Components**, for an explanation of how to determine the value of C_2.
3.	R_f	Feedback resistance for setting the closed-loop gain in conjunction with R_2.
4.	C_1	Supply bypass capacitor for providing power supply filtering. Refer to the section, **Power Supply Bypassing**, for information concerning proper placement and selection of the supply bypass capacitor, C_3.
5.	C_3	Bypass pin capacitor for providing half-supply filtering. Refer to the section, **Proper Selection of External Components**, for information concerning proper placement and selection of C_3.

Typical Performance Characteristics



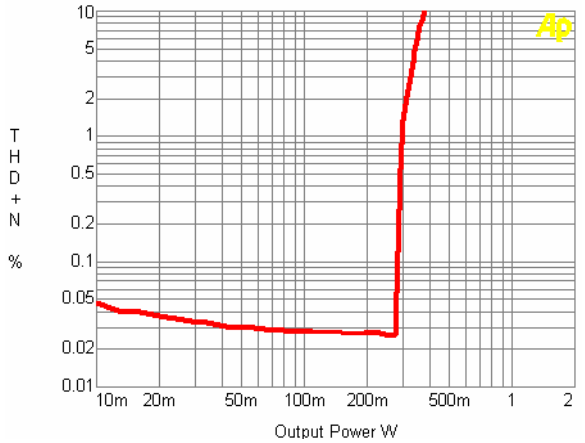
THD + Noise vs Output Power

@ V_{DD} = 5.0V, R_L = 8Ω, 1kHz, A_V = 2



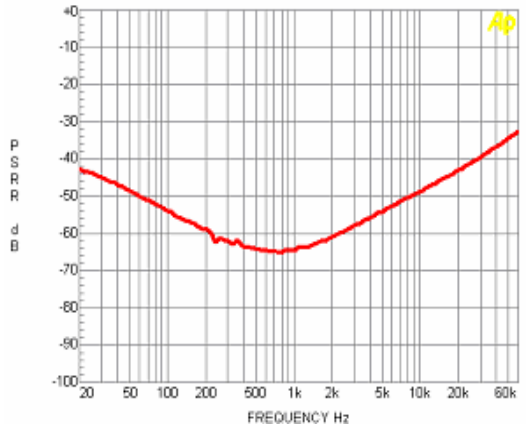
PSRR vs Frequency

@ V_{DD} = 5.0V, R_L = 8Ω, A_V = 2



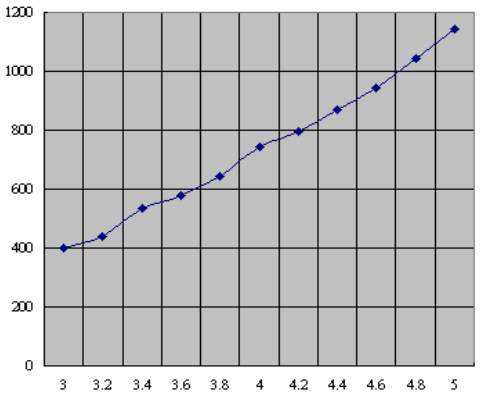
THD + Noise vs Output Power

@ V_{DD} = 2.6V, R_L = 8Ω, 1kHz, A_V = 2



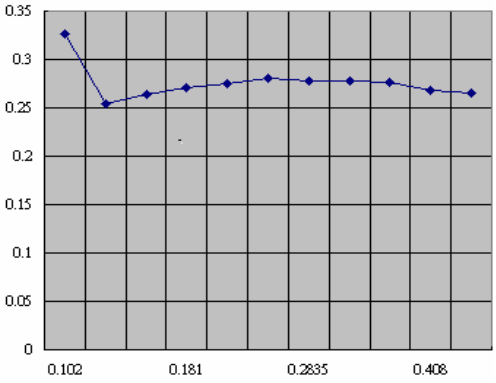
PSRR vs Frequency

@ V_{DD} = 2.6V, R_L = 8Ω, A_V = 2



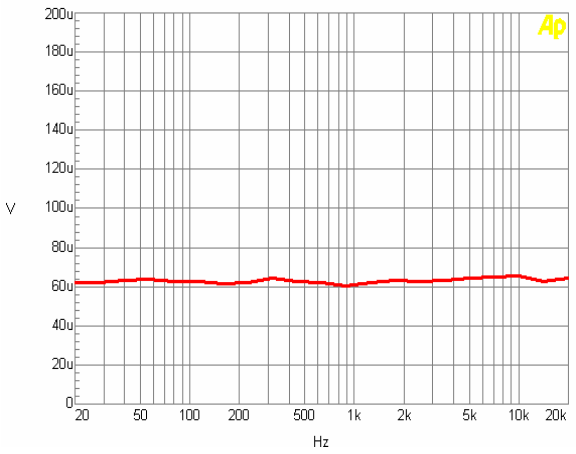
f=1KHz, RL=8ohm, Av=2, C3=C1=1uF, BW=60KHz

(X=Supply Voltage, Y=Power Out)

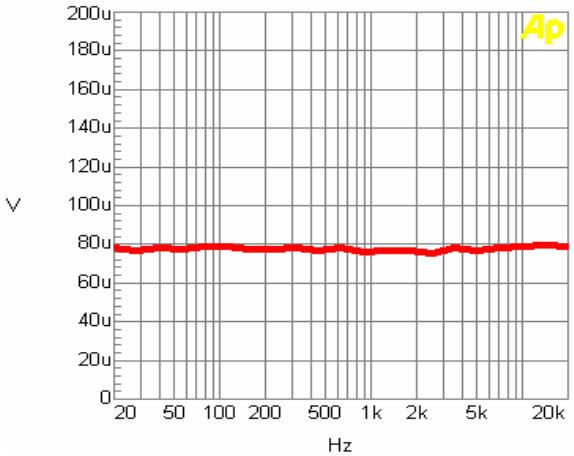


Vdd=3.3V, f=1KHz, RL=8ohm, Av=2,C3=C1=1uF,

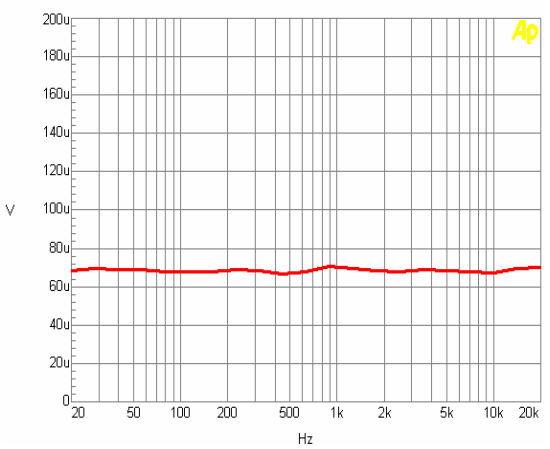
BW=60KHz (X=Output, Y=Power dissipation)



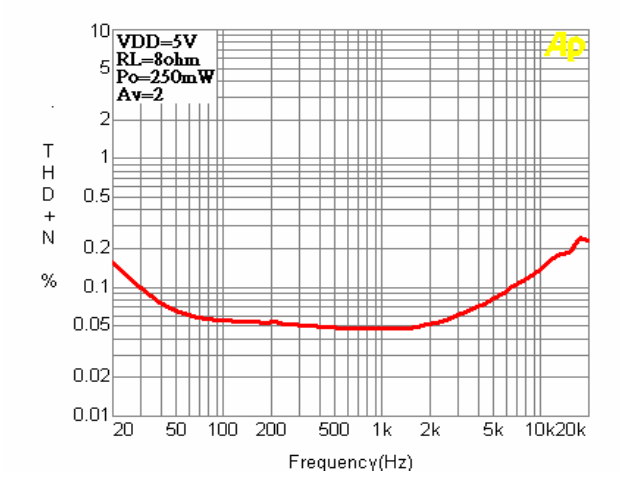
Output Noise @ 5V



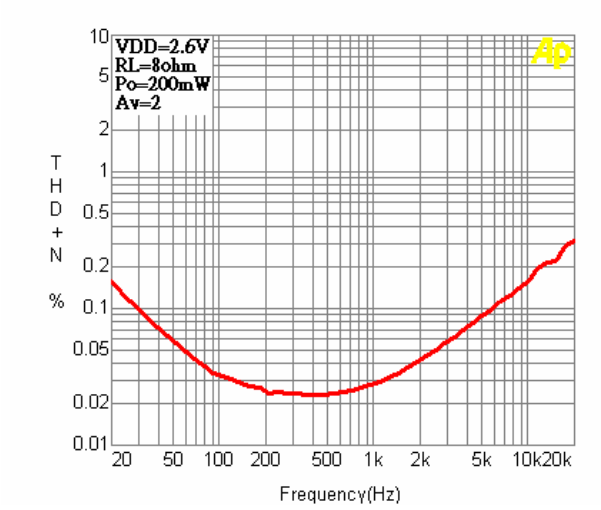
Output Noise @ 2.2V



Output Noise @ 2.6V



THD+Noise vs Frequency @ 5.0V



THD+Noise vs Frequency @ 2.6V

Application Information

BRIDGED CONFIGURATION EXPLANATION

As shown in *Figure 1*, the EMA1001 has two operational amplifiers internally, A1 and A2, allowing for a few different amplifier configurations. A1's gain is externally configurable, while A2 is internally fixed in a unity-gain, inverting configuration. The closed-loop gain of A1 is set by selecting the ratio of R_f to R_2, while A2's gain is fixed by the two internal 20kΩ resistors. *Figure 1* shows that the output of A1 serves as the input to A2, which results in both amplifiers producing signals identical in magnitude, but out of phase by 180°. Hence, the differential gain for the IC is

$$A_{VD} = 2 * (R_f / R_2)$$

By driving the load differentially through outputs V_{O1} and V_{O2}, a bridged mode amplifier configuration is established. Bridged mode operation is different from the single-ended amplifier configuration where one side of the load is connected to ground. A bridge amplifier design has a few distinct advantages over the single-ended configuration, as it provides differential drive to the load, thus doubling output swing for a specified supply voltage. Four times the output power is possible as compared to a single-ended amplifier under the same conditions. This increase in attainable output power assumes that the amplifier is not current limited or clipped. In order to choose an amplifier's closed-loop gain without causing excessive clipping, please refer to the **Audio Power Amplifier Design** section. A bridge configuration, such as the one used in the EMA1001, also creates a second advantage over single-ended amplifiers. Since the differential outputs, V_{O1} and V_{O2}, are biased at half-supply, no net DC voltage exists across the load. This eliminates the need for an output coupling capacitor, which is required in a single supply, single-ended amplifier configuration. Without an output coupling capacitor, the half-supply bias across the load would result in both increased internal IC power dissipation and also possible loudspeaker damage.

POWER DISSIPATION

Power dissipation is one of the major concerns in designing a quality amplifier -- the higher the power delivered to the load by a bridge amplifier, the higher the increase in internal power dissipation. Since the EMA1001 has two operational amplifiers in one package, the maximum internal power dissipation is 4 times that of a single-ended amplifier. The maximum power dissipation for a given application can be derived from the power dissipation graphs or from Equation 1.

$$P_{DMAX} = 4*(V_{DD})^2/(2\pi^2 R_L) \quad (1)$$

It is critical to maintain the maximum junction temperature T_{JMAX} below 150°C. T_{JMAX} can be determined from the power derating curves by using P_{DMAX} and the PC board foil area. By adding additional copper foil, the thermal resistance of the application can be reduced, resulting in higher P_{DMAX}. Additional copper foil can be added to any of the leads connected to the EMA1001. Refer to the **APPLICATION INFORMATION** on the EMA1001 reference design board for an example of good heat sinking. If T_{JMAX} still exceeds 150°C, then additional changes must be made. These changes can include reduced supply voltage, higher load impedance, or reduced ambient temperature. Internal power dissipation is a function of output power. Refer to the **Typical Performance Characteristics** curves for power dissipation information for different output powers and output loading.

POWER SUPPLY BYPASSING

As with any amplifier, proper supply bypassing is critical for low noise performance and high power supply rejection. The capacitor location on both the bypass and power supply pins should be as close to the device as possible. Typical applications employ a 5V regulator with 10µF tantalum or electrolytic capacitor and a ceramic bypass capacitor, which aids in supply stability. This does not eliminate the need for bypassing the supply nodes of the EMA1001. The selection of a bypass capacitor, especially C_3, is dependent upon PSRR requirements, click and pop performance (as in the section, **Proper Selection of External Components**), system cost, and size constraints.

SHUTDOWN FUNCTION

The EMA1001 contains a shutdown pin to externally turn off the amplifier's bias circuitry. When a logic low is placed on the shutdown pin, this shutdown feature turns the amplifier off. By switching the shutdown pin to ground, the EMA1001 supply current draw will be minimized in idle mode. The idle current may be greater than the typical value of 0.1µA while the device is disabled with shutdown pin voltages less than 0.5VDC. Idle current is measured with the shutdown pin grounded. In many applications, a microcontroller or microprocessor output is used to control the shutdown circuitry. They provide a quick, smooth transition into shutdown. Another solution is to use a single-pole, single-throw switch in conjunction with an external pull-up resistor. When the switch is closed, the shutdown pin is connected to ground and disables the amplifier. If the switch is open, then the external pull-up resistor will enable the EMA1001. This scheme guarantees that the shutdown pin will not float thus preventing unwanted state changes.

PROPER SELECTION OF EXTERNAL COMPONENTS

To optimize device and system performance, proper selection of external components is critical. While the EMA1001 can support a wide range of external component combinations, careful selection of component values can maximize overall system quality. The EMA1001 is unity-gain stable, which gives the designer maximum system flexibility. The EMA1001 should be used in low gain configurations to minimize THD+N values, and maximize the signal to noise ratio. Low gain configurations require large input signals to obtain a given output power. Input signals equal to or greater than 1Vrms are available from sources such as audio codecs. Please refer to the section, **Audio Power Amplifier Design**, for a more complete explanation of proper gain selection. Besides gain, one of the major considerations is the closed loop bandwidth of the amplifier. The bandwidth is primarily determined by the choice of external components shown in *Figure 1*. The input coupling capacitor, C_2, forms a first order high pass filter, which limits low frequency response. This value should be chosen based on needed frequency response for a few distinct reasons.

SELECTION OF INPUT CAPACITOR SIZE

For portable designs, large input capacitors are prohibited because they are both expensive and space hungry. To couple in low frequencies without severe attenuation, a certain sized capacitor is needed. But in many cases the speakers used in portable systems, whether internal or external, have little ability to reproduce signals below 100Hz to 150Hz. Thus, using a large input capacitor may not increase actual system performance. In addition to system cost and size, click and pop performance is affected by the size of the input coupling capacitor, C_2. A larger input coupling capacitor requires more charge to reach its quiescent DC voltage (nominally 1/2 V_{DD}). This charge comes from the output via the feedback and is apt to create pops upon device enable. Thus, by minimizing the capacitor size based on necessary low frequency response, turn-on pops can be minimized. Besides minimizing the input capacitor size, careful consideration should be paid to the bypass capacitor value. Bypass capacitor, C_3, is the most critical component to minimize turn-on pops since it determines how fast the EMA1001 turns on. The slower the EMA1001's outputs ramp to their quiescent DC voltage (nominally 1/2V_{DD}), the smaller the turn-on pop. Choosing C_3 equal to 1.0µF along with a small value of C_2, (in the range of 0.1µF to 0.39µF), should produce a virtually clickless and popless shutdown function. While the device will function properly, (no oscillations or motor-boating), with C_3 equal to 0.1µF, the device will be much more susceptible to turn-on clicks and pops. Thus, a value of C_3 equal to 1.0µF is recommended in all but the most cost sensitive designs.

AUDIO POWER AMPLIFIER DESIGN

A 1W/8 Audio Amplifier

Given:

Power Output	1 Wrms
Load Impedance	8Ω
Input Level	1 Vrms
Input Impedance	20 kΩ
Bandwidth	100 Hz–20 kHz ± 0.25 dB

A designer must first determine the minimum supply rail to

obtain the specified output power. By extrapolating from the Output Power vs Supply Voltage graphs in the **Typical Performance Characteristics** section, the supply rail can be easily found. In more applications, 5V is chosen as a standard voltage for the supply rail. Extra supply voltage creates headroom, which allows the EMA1001 to reproduce peaks in excess of 1W without producing audible distortion. At this stage, the designer must make sure that the power supply choice along with the output impedance does not violate the conditions described in the **Power Dissipation** section.

Once the power dissipation equations are addressed, the required differential gain can be determined from Equation 3.

$$A_{VD} \geqq (P_O R_L)^{1/2}/Vin = Vorms/Vinrms \quad (3)$$

$$R_f/R_2 = A_{VD}/2$$

From Equation 3, the minimum A_{VD} is 2.83; use A_{VD} = 3. Since the desired input impedance is 20 kΩ, and with an A_{VD} gain of 3, a ratio of 1.5:1 of R_f to R_2 results in an allocation of R_2 = 20 kΩ and R_f = 30 kΩ. The final design step is to address the bandwidth requirements, which must be stated as a pair of -3 dB frequency points. Five times away from a -3 dB point is 0.17 dB down from passband response, which is better than the required ±0.25 dB specified.

f_L = 100Hz/5 = 20Hz

f_H = 20kHz * 5 = 100kHz

As stated in the **External Components** section, R_2 and C_2 create a high-pass filter.

$C_2 \geq 1/(2\pi * 20\ k\Omega * 20Hz) = 0.397\mu F$; use 0.39µF.

The high frequency pole is the product of the desired frequency pole, f_H, and the differential gain, A_{VD}. With a AVD = 3 and f_H = 100kHz, the resulting GBWP = 300kHz which is much smaller than the EMA1001 GBWP of 2.5MHz. This calculation shows that if a designer has a need to design an amplifier with a higher differential gain, the EMA1001 can still be used without running into bandwidth limitations.

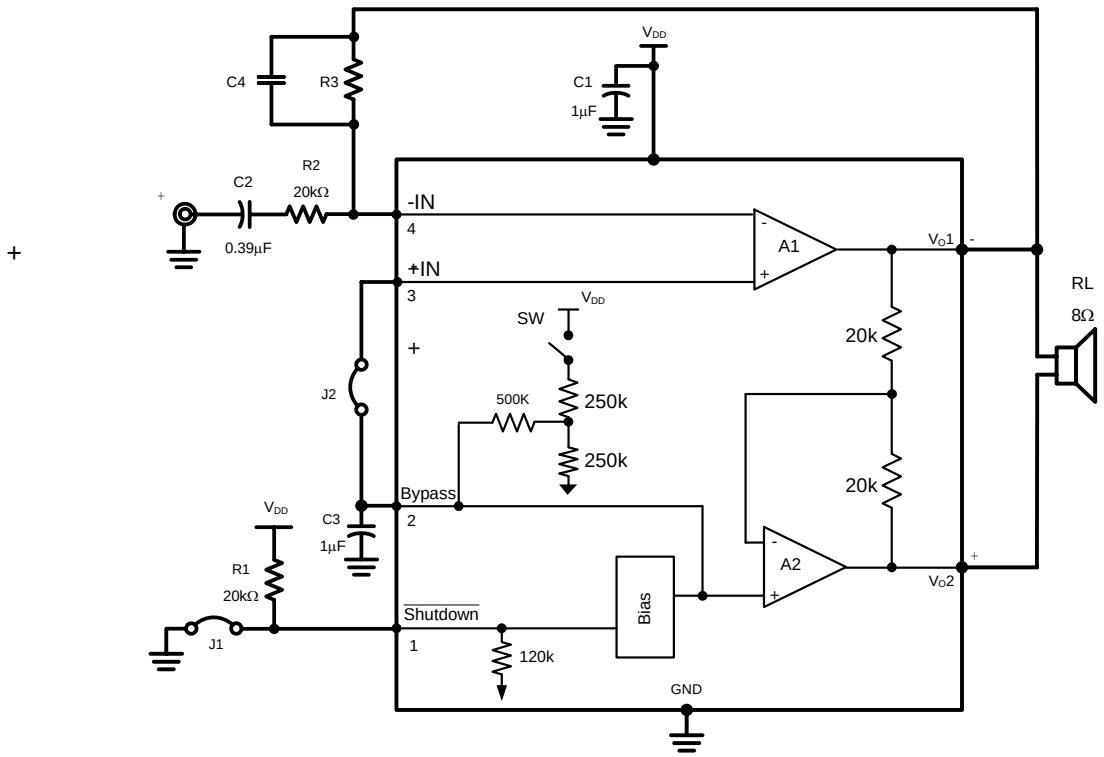


FIGURE 2. HIGHER GAIN AUDIO AMPLIFIER

The EMA1001 is unity-gain stable and requires only gain-setting resistors, an input coupling capacitor, and proper supply bypassing in the typical application. For a closed-loop differential gain of greater than 10, a feedback capacitor (C4) may be needed as shown in **Figure 2** to bandwidth limit the amplifier. This feedback capacitor creates a low pass filter that eliminates possible high frequency oscillations. Care should be taken when calculating the -3dB frequency in that an incorrect combination of R3 and C4 will cause rolloff before 20kHz. A typical combination of feedback resistor and capacitor that will not produce audio band high frequency rolloff is R3 = 20kΩ and C4 = 25pf. These components result in a -3dB point of approximately 320 kHz.

Reference Design Board and Layout

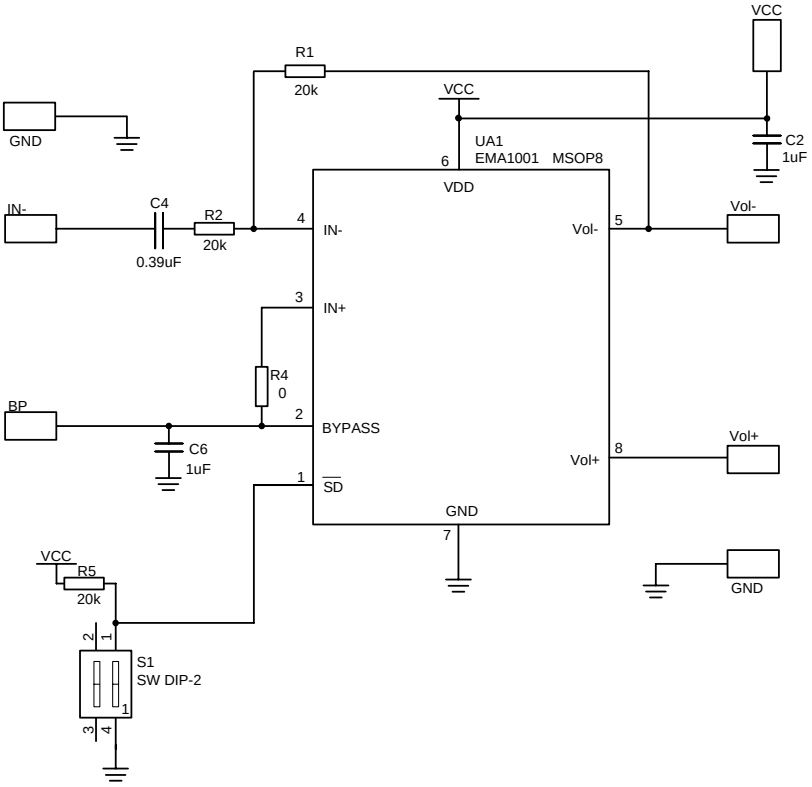


FIGURE 3. REFERENCE DESIGN

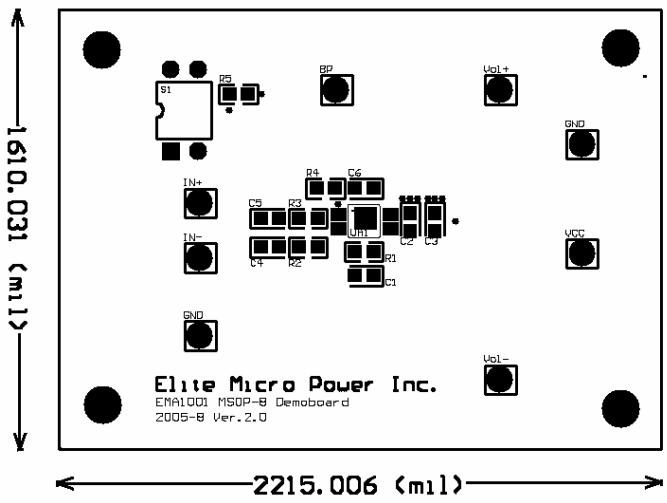


FIGURE 4. COMPONENT SIDE OF REFERENCE DESIGN

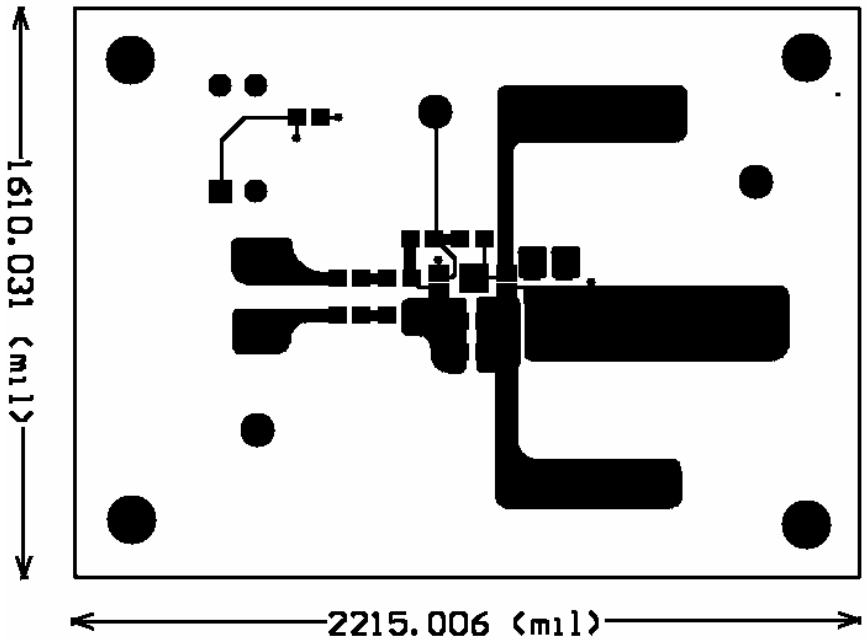


FIGURE 5. TOP LAYER OF REFERENCE DESIGN

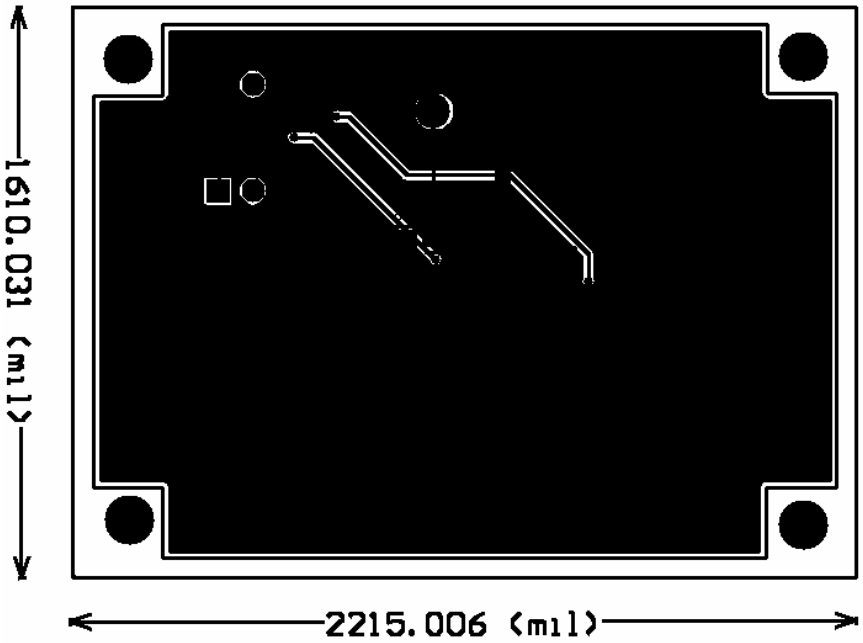


FIGURE 6. BOTTOM LAYER OF REFERENCE DESIGN

Bill of Materials of Figure 4

Description	Designator	Footprint	LibRef	Value
	UA1	MSOP-8	EMA1001 MSOP8	
DIP Switch	S1	DIP-4	SW DIP-2	
Capacitor (Semiconductor SIM Model)	C2	CC1608-0603	Cap Semi	0.1uF
Capacitor (Semiconductor SIM Model)	C4	CC1608-0603	Cap Semi	0.39uF
Capacitor (Semiconductor SIM Model)	C5	CC1608-0603	Cap Semi	0.39uF
Capacitor (Semiconductor SIM Model)	C3	CC1608-0603	Cap Semi	1uF
Capacitor (Semiconductor SIM Model)	C6	CC1608-0603	Cap Semi	1uF
Semiconductor Resistor	R1	CR1608-0603	Res Semi	20K
Semiconductor Resistor	R2	CR1608-0603	Res Semi	20K
Semiconductor Resistor	R3	CR1608-0603	Res Semi	20K
Semiconductor Resistor	R4	CR1608-0603	Res Semi	20K
Semiconductor Resistor	R5	CR1608-0603	Res Semi	20K
Capacitor (Semiconductor SIM Model)	C1	CC1608-0603	Cap Semi	22pF

PCB LAYOUT GUIDELINES

This section provides practical guidelines for mixed signal PCB layout that involves various digital/analog power and ground traces. Designers should note that these are only "rule-of-thumb" recommendations and the actual results will depend heavily on the final layout.

GENERAL MIXED SIGNAL LAYOUT RECOMMENDATIONS

Power and Ground Circuits

For 2 layer mixed signal design, it is important to isolate the digital power and ground trace paths from the analog power and ground trace paths. Star trace routing techniques (bringing individual traces back to a central point rather than daisy chaining traces together in a serial manner) can have a major impact on low level signal performance. Star trace routing refers to using individual traces to feed power and ground to each circuit or even device. This technique will require a greater amount of design time but will not increase the final price of the board. The only extra parts required will be some jumpers.

Single-Point Power / Ground Connections

The analog power traces should be connected to the digital traces through a single point (link). A "Pi-filter" can be helpful in minimizing High Frequency noise coupling between the analog and digital sections. It is further recommended to put digital and analog power traces over the corresponding digital and analog ground traces to minimize noise coupling.

Placement of Digital and Analog Components

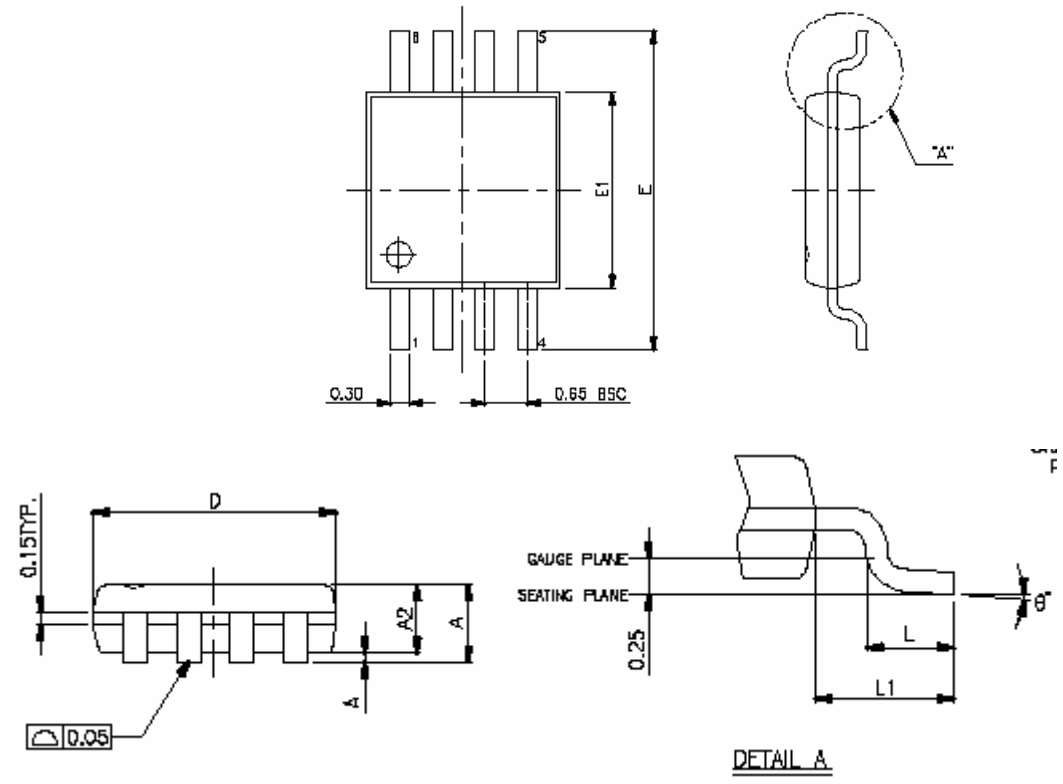
All digital components and high-speed digital signals traces should be located as far away as possible from analog components and circuit traces.

Avoiding Typical Design / Layout Problems

Avoid ground loops or running digital and analog traces parallel to each other (side-by-side) on the same PCB layer. When traces must cross over each other do it at 90 degrees. Running digital and analog traces at 90 degrees to each other from the top to the bottom side as much as possible will minimize capacitive noise coupling and cross talk.

Physical Dimensions

MSOP-8 Plastic Package

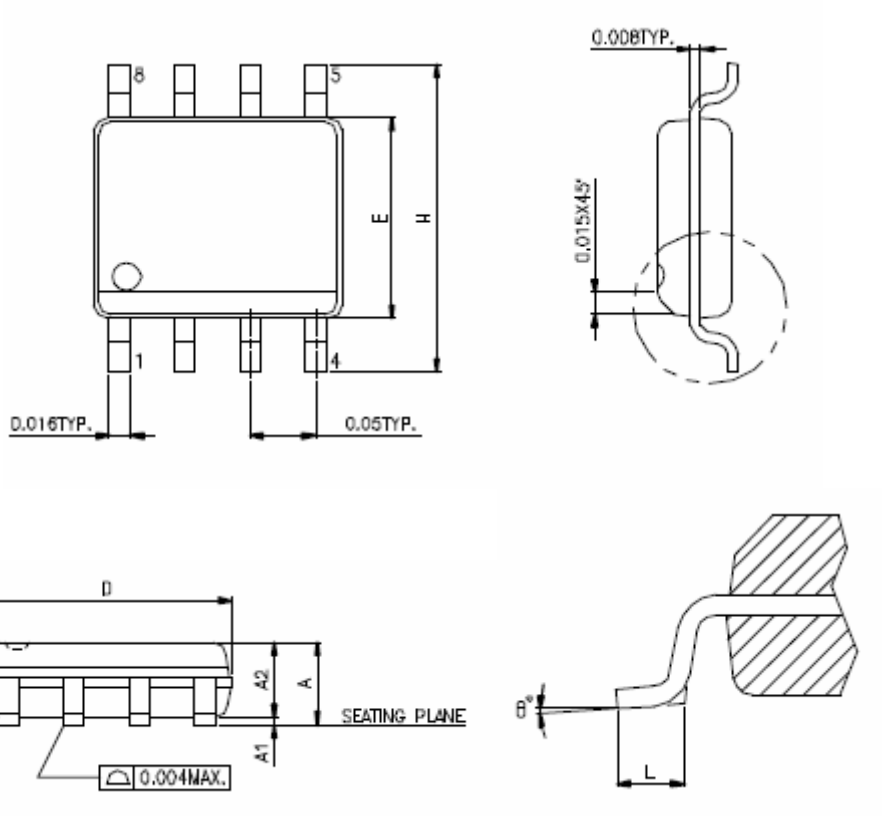


SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.10
A1	0.00	–	0.15
A2	0.75	0.85	0.95
D		3.00 BSC	
E		4.90 BSC	
E1		3.00 BSC	
L	0.40	0.60	0.80
L1		0.95 REF	
θ°	0	–	8

UNIT : MM

NOTES:
1. JEDEC OUTLINE : MO-187 AA
2. DIMENSION "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.
3. DIMENSION "E1" DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE.
4. DIMENSION "0.22" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 MM TOTAL IN EXCESS OF THE "0.22" DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT. MINIMUM SPAC BETWEEN PROTRUSION AND ADJACENT LEAD IS 0.07 MM.
5. DIMENSIONS "D" AND "E1" TO BE DETERMINED AT DATUM PLANE [H] .

SOP-8 Plastic Package



SYMBOLS	MIN.	MAX.
A	0.053	0.069
A1	0.004	0.010
A2	–	0.059
D	0.189	0.196
E	0.150	0.157
H	0.228	0.244
L	0.016	0.050
θ°	0	8

UNIT : INCH

NOTES:
1. JEDEC OUTLINE : MS-012 AA
2. DIMENSIONS "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .15mm (.006in) PER SIDE.
3. DIMENSIONS "E" DOES NOT INCLUDE INTER-LEAD FLASH, OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED .25mm (.010in) PER SIDE.

Revision History

Revision	Date	Description
5.0	2009.05.08	EMP transferred from version 4.0

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