



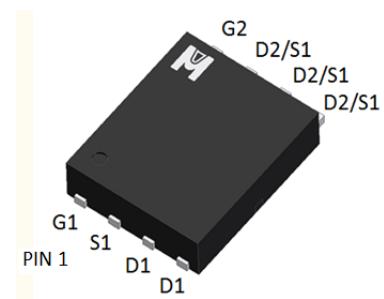
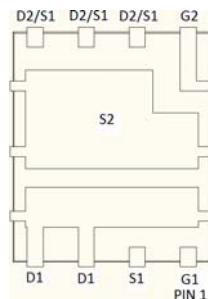
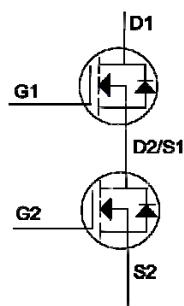
N-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

	N-CH-Q1	N-CH-Q2
BV_{DSS}	30V	30V
$R_{DS(on)}$ (MAX.)	5.0mΩ	2.0mΩ
I_D	53A	95A

UIS, R_g 100% Tested

Pb-Free Lead Plating & Halogen Free



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ C$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS		UNIT
			Q1	Q2	
Gate-Source Voltage		V_{GS}	± 20	± 20	V
Continuous Drain Current ³	$T_C = 25^\circ C$	I_D	53	95	A
	$T_C = 100^\circ C$		33	60	
Pulsed Drain Current ¹		I_{DM}	130	170	
Continuous Drain Current ³	$T_A = 25^\circ C$	I_D	21	37	
	$T_A = 70^\circ C$		17	30	
Avalanche Current		I_{AS}	30	65	
Avalanche Energy	$L = 0.1mH, R_G=25\Omega$	E_{AS}	45	211	mJ
Repetitive Avalanche Energy ²	$L = 0.05mH$	E_{AR}	22	105	
Power Dissipation	$T_C = 25^\circ C$	P_D	25	31	W
	$T_C = 100^\circ C$		10	12.5	
Power Dissipation	$T_A = 25^\circ C$	P_D	1.8	1.9	W
	$T_A = 70^\circ C$		1.1	1.2	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150		°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL		TYPICAL	MAXIMUM		UNIT
Junction-to-Case	$R_{\theta JC}$	Steady State		5	4	$^{\circ}\text{C} / \text{W}$
Junction-to-Ambient	$R_{\theta JA}$	Steady State		70	65	
	$R_{\theta JA}$	$t \leq 10 \text{ s}$		30	25	

¹Pulse width limited by maximum junction temperature.

²Duty cycle $\leq 1\%$

³Package limitation current, Q1=30A, Q2=36A

$R_{\theta JA}$ when mounted on a 1 in² pad of 2 oz copper.



ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(\text{BR})\text{DSS}}$	$V_{GS} = 0V, I_D = 250\mu\text{A}$	Q1	30		V
			Q2	30		
Gate Threshold Voltage	$V_{GS(\text{th})}$	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$	Q1	1	1.5	3
			Q2	1	1.5	3
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0V, V_{GS} = \pm 20V$	Q1		± 100	nA
			Q2		± 100	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 24V, V_{GS} = 0V$	Q1			1
			Q2			1
		$V_{DS} = 20V, V_{GS} = 0V, T_J = 125^\circ\text{C}$	Q1			25
			Q2			25
On-State Drain Current ¹	$I_{D(\text{ON})}$	$V_{DS} = 10V, V_{GS} = 10V$	Q1	53		A
			Q2	95		
Drain-Source On-State Resistance ¹	$R_{DS(\text{ON})}$	$V_{GS} = 10V, I_D = 16A$	Q1		4.0	5.0
		$V_{GS} = 10V, I_D = 25A$	Q2		1.6	2.0
		$V_{GS} = 4.5V, I_D = 10A$	Q1		6.0	7.8
		$V_{GS} = 4.5V, I_D = 15A$	Q2		2.3	3.0
Forward Transconductance ¹	g_{fs}	$V_{DS} = 5V, I_D = 16A$	Q1		50	S
		$V_{DS} = 5V, I_D = 25A$	Q2		70	
DYNAMIC						
Input Capacitance	C_{iss}	$V_{GS} = 0V, V_{DS} = 15V, f = 1\text{MHz}$	Q1		1508	pF
			Q2		3813	
Output Capacitance	C_{oss}		Q1		219	
			Q2		540	
Reverse Transfer Capacitance	C_{rss}		Q1		167	
			Q2		440	
Gate Resistance	R_g	$V_{GS} = 15\text{mV}, V_{DS} = 0V, f = 1\text{MHz}$	Q1		0.9	Ω
			Q2		1.5	
Total Gate Charge ^{1,2}	$Q_g(V_{GS}=10V)$	Q_1 $V_{DD} = 15V, V_{GS} = 10V,$ $I_D = 16A$	Q1		25	nC
			Q2		59	
			Q1		13	
			Q2		28	

Gate-Source Charge ^{1,2}	Q_{gs}	Q2 $V_{DD} = 15V, V_{GS} = 10V,$ $I_D = 25A$	Q1		5		
Gate-Drain Charge ^{1,2}	Q_{gd}		Q2		13		
Turn-On Delay Time ^{1,2}	$t_{d(on)}$	$V_{DD} = 15V,$ $I_D = 1A, V_{GS} = 10V, R_{GS} = 2.7\Omega$	Q1		20		nS
Rise Time ^{1,2}	t_r		Q2		25		
Turn-Off Delay Time ^{1,2}	$t_{d(off)}$	$V_{DD} = 15V,$ $I_D = 1A, V_{GS} = 10V, R_{GS} = 2.7\Omega$	Q1		15		
Fall Time ^{1,2}	t_f		Q2		16		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS ($T_J = 25^\circ C$)							
Continuous Current	I_S	$I_F = 10A, V_{GS} = 0V$	Q1			20	A
Forward Voltage ¹	V_{SD}		Q2			33	
Reverse Recovery Time	t_{rr}	$I_F = 16A, dI_F/dt = 100A/\mu S$	Q1			1.2	V
Reverse Recovery Charge	Q_{rr}		Q2			1.2	
		$I_F = 25A, dI_F/dt = 100A/\mu S$	Q1		30		nS
			Q2		35		
		$I_F = 25A, dI_F/dt = 100A/\mu S$	Q1		18		nC
			Q2		25		

¹Pulse test : Pulse Width $\leq 300 \mu sec$, Duty Cycle $\leq 2\%$.

²Independent of operating temperature.

³Pulse width limited by maximum junction temperature.



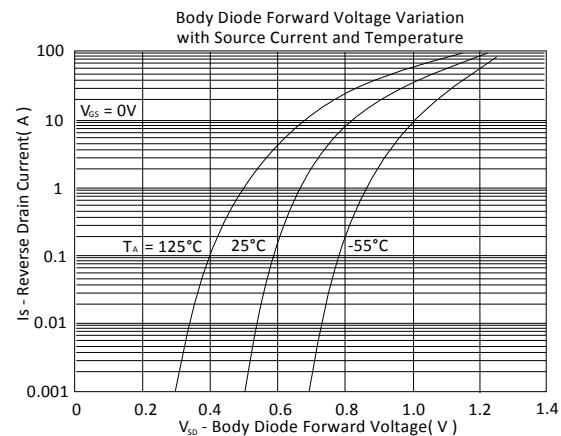
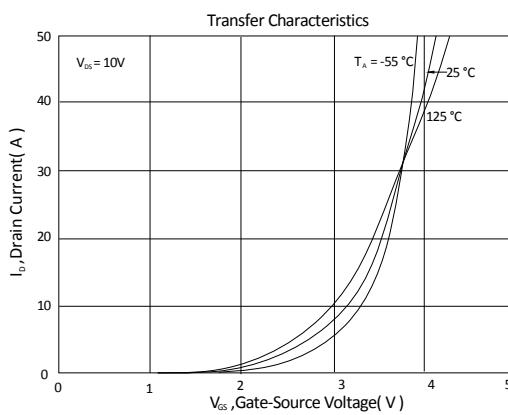
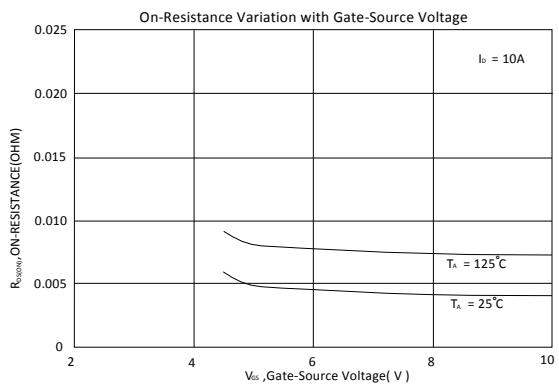
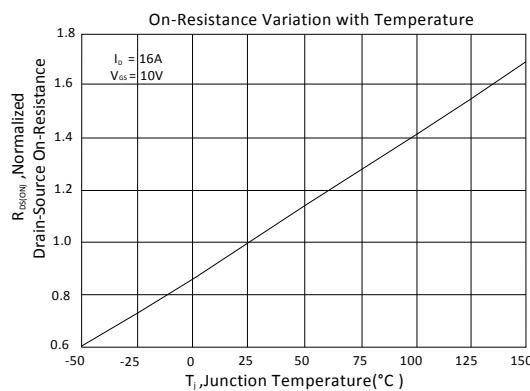
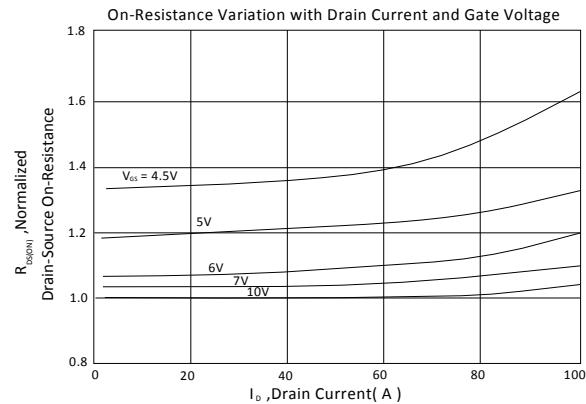
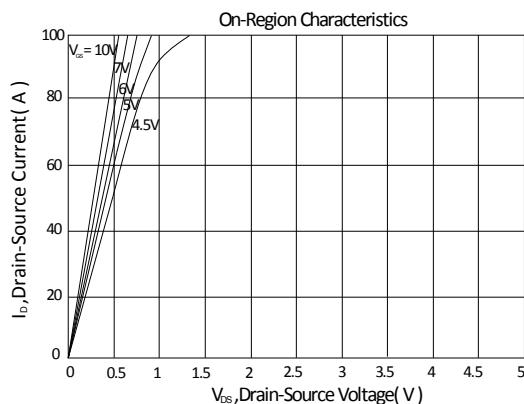
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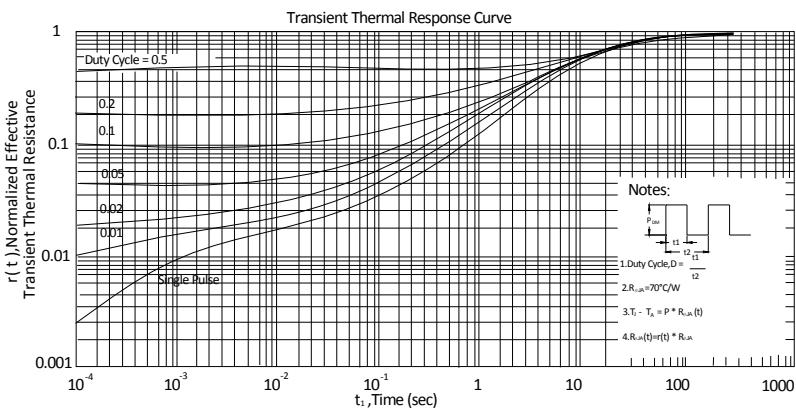
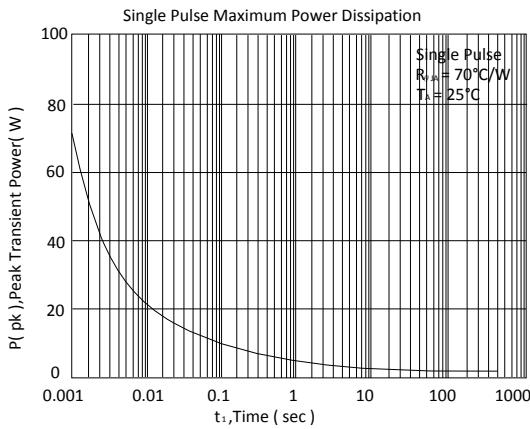
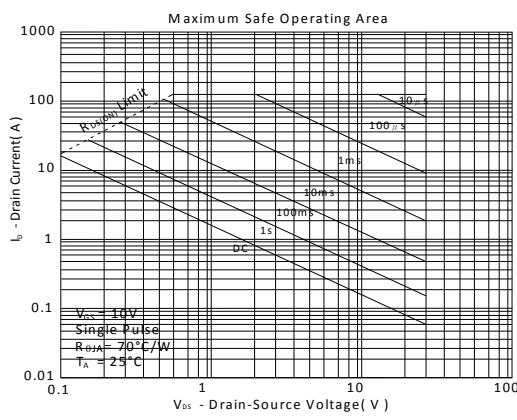
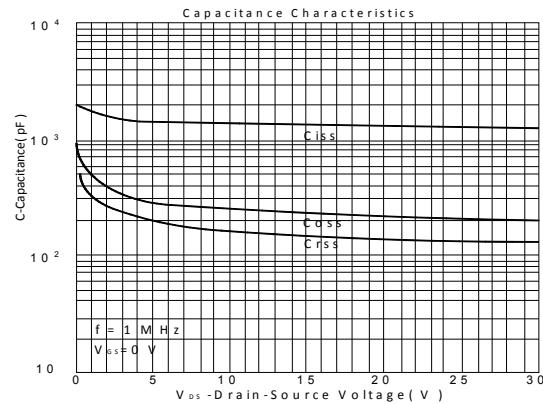
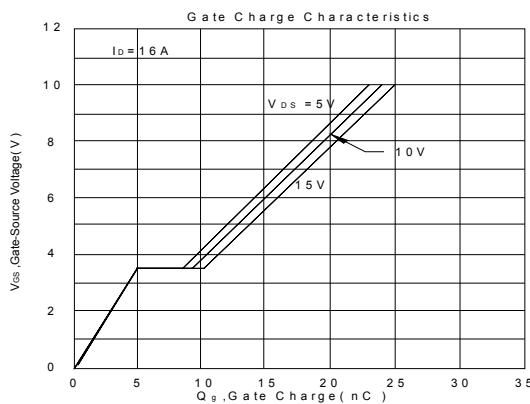
Ordering & Marking Information:

Device Name: EMB02Q03HP for Asymmetric Dual EDFN 5 x 6



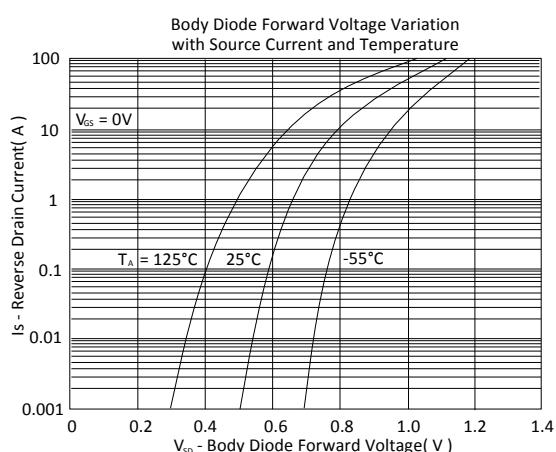
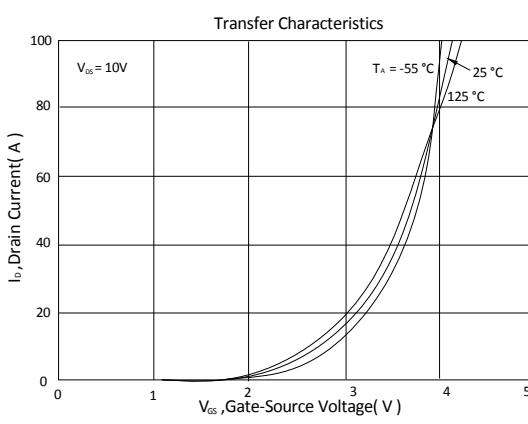
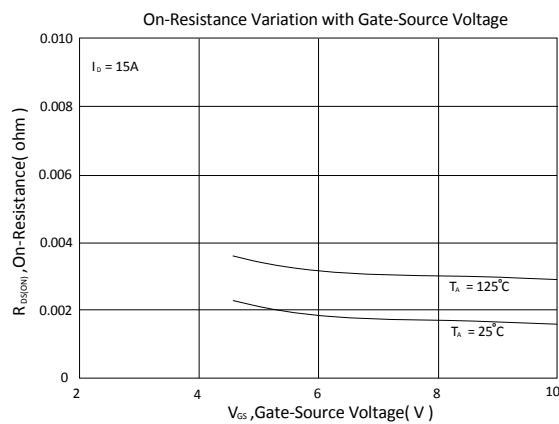
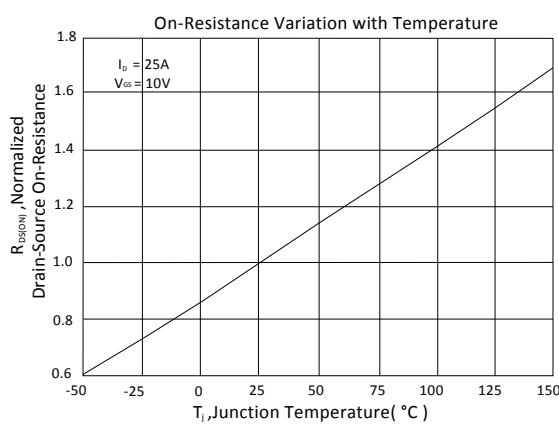
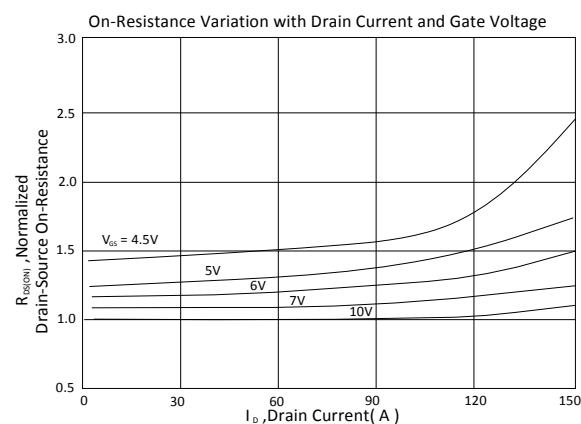
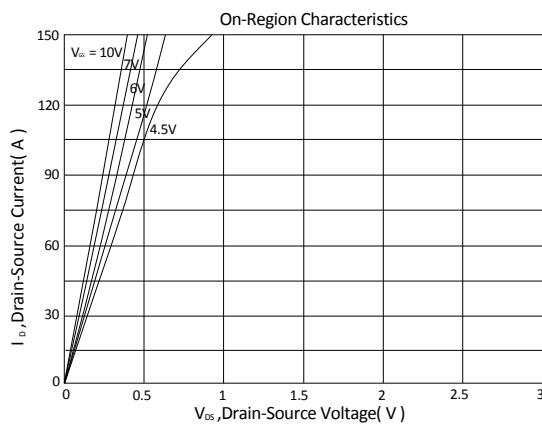
Q1 TYPICAL CHARACTERISTICS

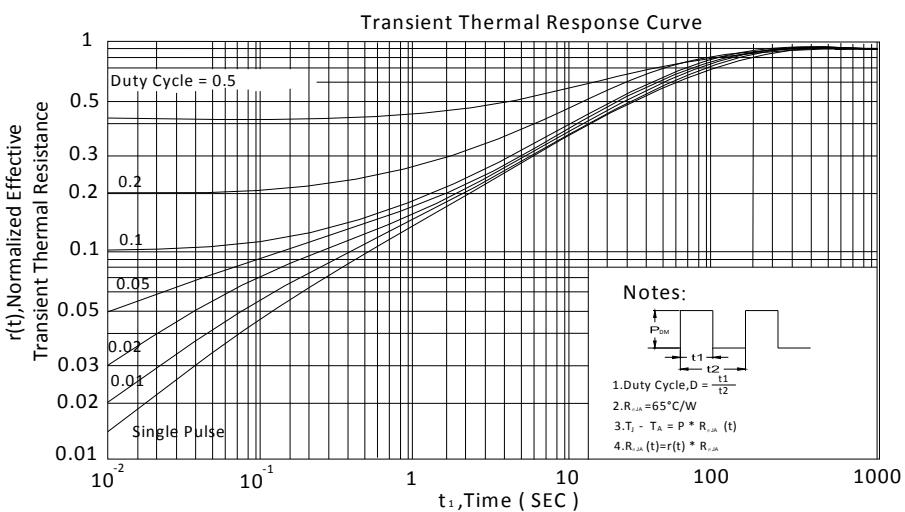
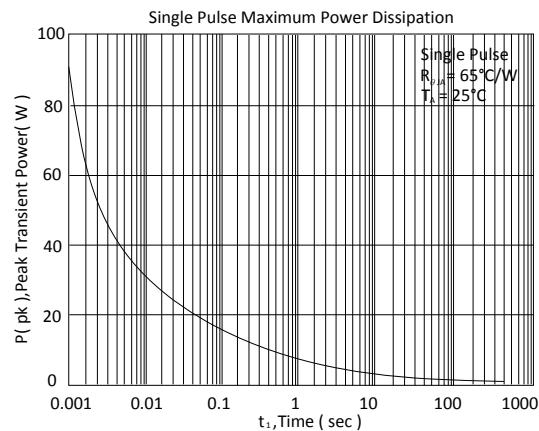
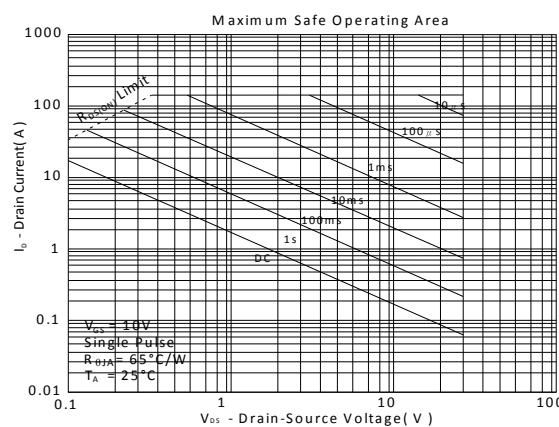
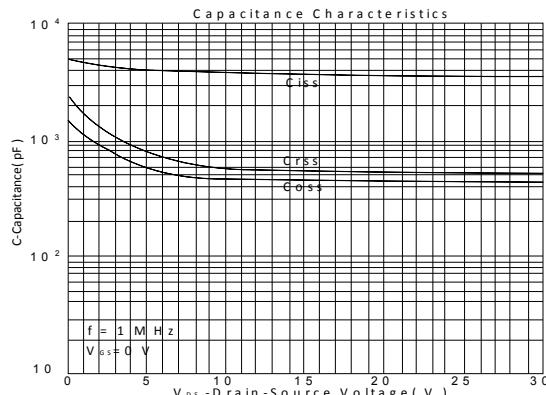
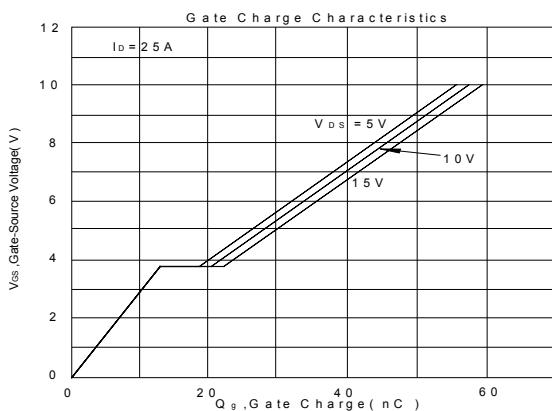






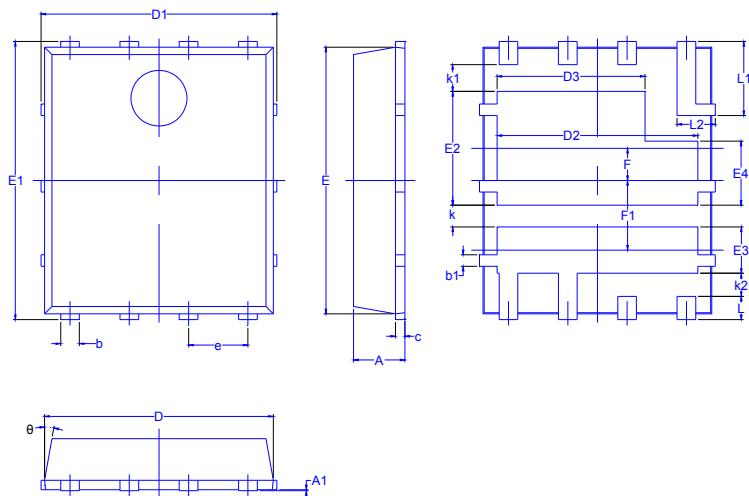
Q2 TYPICAL CHARACTERISTICS







Outline Drawing



Dimension in mm

Dimension	A	A1	b	b1	c	D	D1	D2	D3	E	E1	E2	E3	E4	e
Min.	1.00	0.00	0.30	0.15	0.15	4.80	5.05BSC	4.15	3.02	5.65	6.00BSC	2.3	0.85	1.23	1.27BSC
Typ.															
Max.	1.20	0.05	0.50	0.35	0.25	5.00		4.45	3.32	5.85		2.60	1.15	1.53	

Dimension	L	L1	L2	k	k1	k2	F	F1	θ
Min.	0.40	1.50	0.72	0.47BSC	0.58BSC	0.50BSC	0.695REF	1.50REF	10° REF
Typ.									
Max.	0.60	1.70	0.92						

Recommended minimum pads

