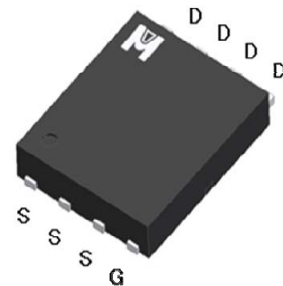
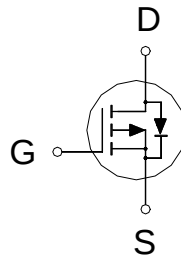


P-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

BV_{DSS}	-30V
$R_{DS(on)} (MAX.)$	$3.1m\Omega$
I_D	-85A



UIS, Rg 100% Tested

Pb-Free Lead Plating & Halogen Free



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current	$T_C = 25^\circ\text{C}$	I_D	-85	A
	$T_C = 100^\circ\text{C}$		-65	
Pulsed Drain Current ¹		I_{DM}	-260	
Avalanche Current		I_{AS}	-80	
Avalanche Energy	$L = 0.1\text{mH}, I_D = -80\text{A}, R_G = 25\Omega$	E_{AS}	320	mJ
Repetitive Avalanche Energy ²	$L = 0.05\text{mH}$	E_{AR}	160	
Power Dissipation	$T_C = 25^\circ\text{C}$	P_D	69	W
	$T_C = 100^\circ\text{C}$		27	
Operating Junction & Storage Temperature Range		T_{j}, T_{stg}	-55 to 150	$^\circ\text{C}$

100% UIS testing in condition of $V_D = -15\text{V}$, $L = 0.1\text{mH}$, $V_G = -10\text{V}$, $I_L = -50\text{A}$, Rated $V_{DS} = -30\text{V}$ P-CH

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	$R_{\theta JC}$		1.8	$^\circ\text{C} / \text{W}$
Junction-to-Ambient ³	$R_{\theta JA}$		62.5	

¹Pulse width limited by maximum junction temperature.

²Duty cycle $\leq 1\%$

ELECTRICAL CHARACTERISTICS ($T_J = 25\text{ }^{\circ}\text{C}$, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT	
			MIN	TYP	MAX		
STATIC							
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = -250\mu A$	-30			V	
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\mu A$	-1	-1.5	-3		
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0V, V_{GS} = \pm 20V$			± 100	nA	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -24V, V_{GS} = 0V$			-1	μA	
		$V_{DS} = -20V, V_{GS} = 0V, T_J = 125\text{ }^{\circ}C$			-10		
On-State Drain Current ¹	$I_{D(ON)}$	$V_{DS} = -5V, V_{GS} = -10V$	-85			A	
Drain-Source On-State Resistance ¹	$R_{DS(ON)}$	$V_{GS} = -10V, I_D = -30A$		2.7	3.1	m Ω	
		$V_{GS} = -4.5V, I_D = -30A$		4.0	5.0		
Forward Transconductance ¹	g_{fs}	$V_{DS} = -5V, I_D = -30A$		70		S	
DYNAMIC							
Input Capacitance	C_{iss}	$V_{GS} = 0V, V_{DS} = -15V, f = 1MHz$		6400		pF	
Output Capacitance	C_{oss}			913			
Reverse Transfer Capacitance	C_{rss}			656			
Gate Resistance	R_g	$V_{GS} = 15mV, V_{DS} = 0V, f = 1MHz$		3.4		Ω	
Total Gate Charge ^{1,2}	Q_g	$V_{DS} = -15V, V_{GS} = -10V,$ $I_D = -30A$		96.5		nC	
Gate-Source Charge ^{1,2}	Q_{gs}			24.8			
Gate-Drain Charge ^{1,2}	Q_{gd}			13.8			
Turn-On Delay Time ^{1,2}	$t_{d(on)}$	$V_{DS} = -15V,$ $I_D = -1A, V_{GS} = -10V, R_{GS} = 2.7\Omega$		15		nS	
Rise Time ^{1,2}	t_r			20			
Turn-Off Delay Time ^{1,2}	$t_{d(off)}$			130			
Fall Time ^{1,2}	t_f			55			
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T _C = 25 °C)							
Continuous Current	I_S				-85	A	
Pulsed Current ³	I_{SM}				-260		
Forward Voltage ¹	V_{SD}	$I_F = -30A, V_{GS} = 0V$			-1.2	V	
Reverse Recovery Time	t_{rr}	$I_F = I_S, dI_F/dt = 100A / \mu S$		26		nS	
Reverse Recovery Charge	Q_{rr}			80		nC	

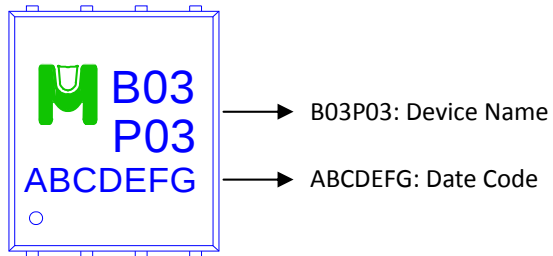
¹Pulse test : Pulse Width $\leq 300 \mu\text{sec}$, Duty Cycle $\leq 2\%$.

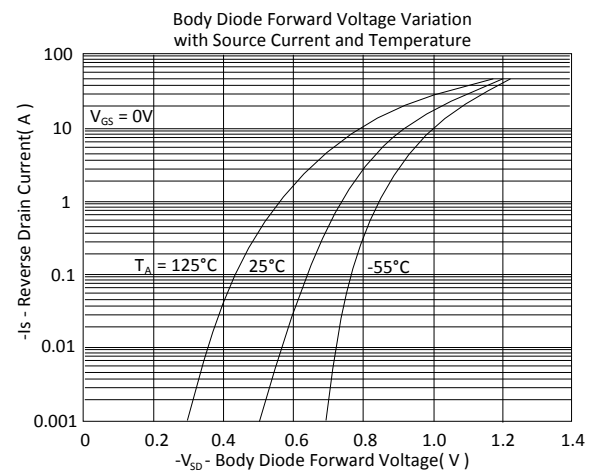
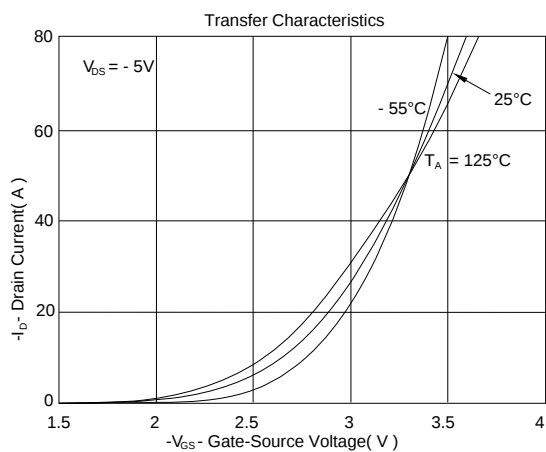
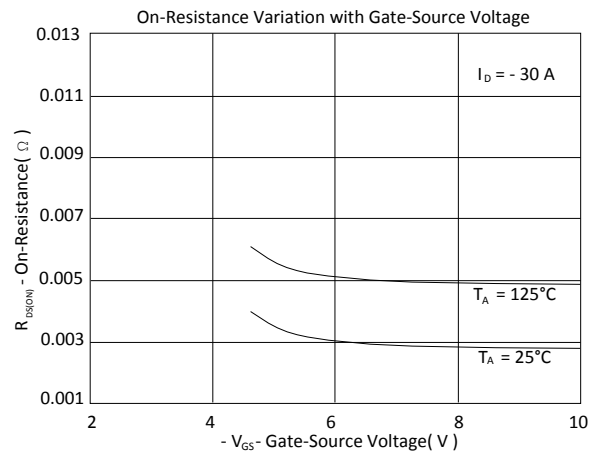
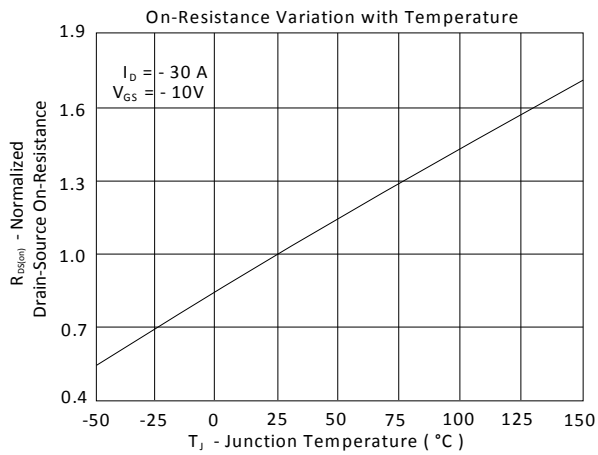
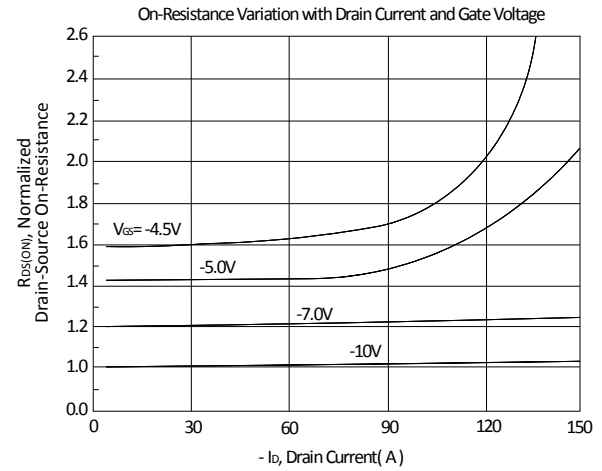
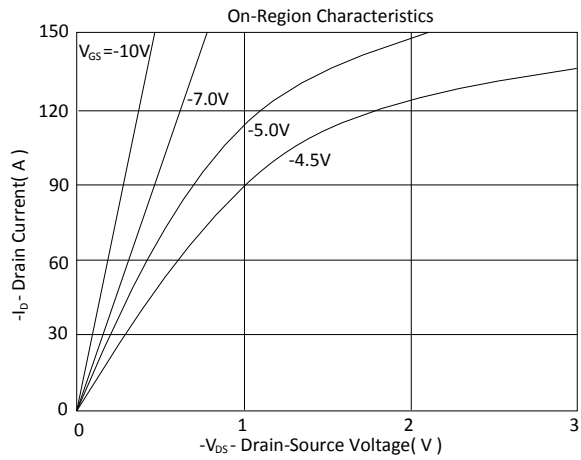
²Independent of operating temperature.

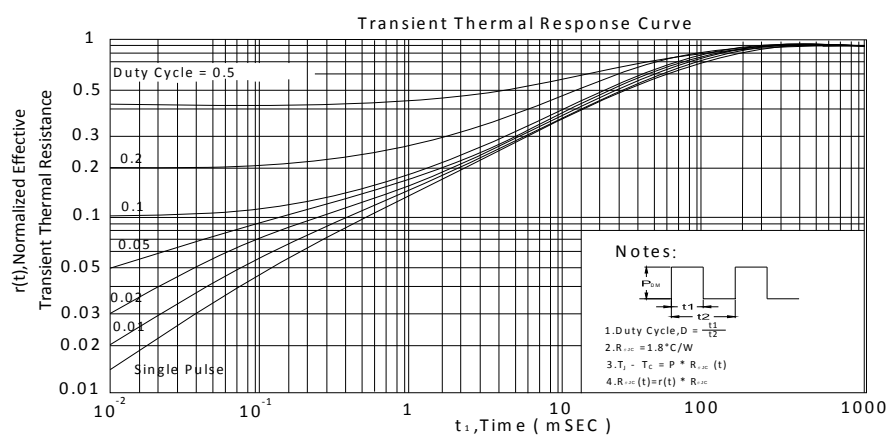
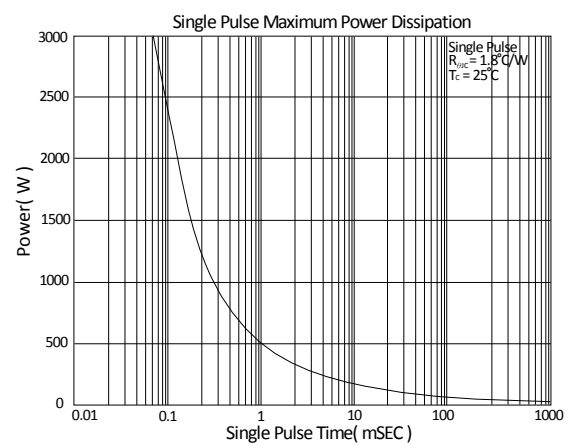
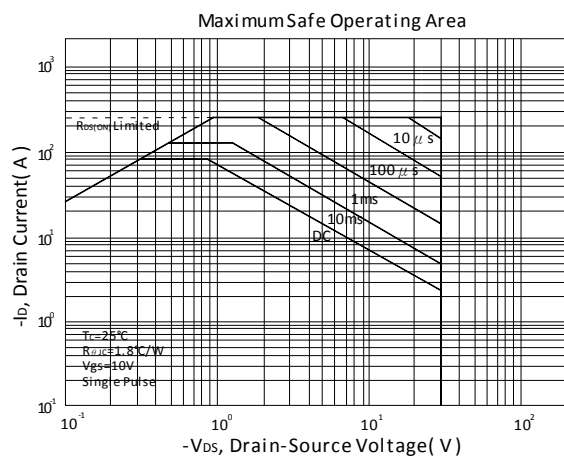
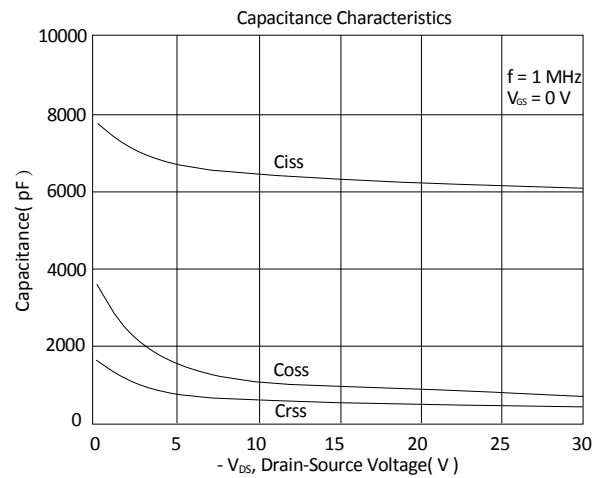
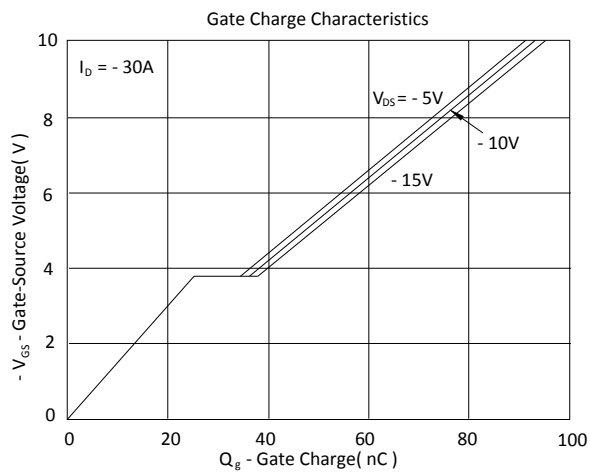
³Pulse width limited by maximum junction temperature.

Ordering & Marking Information:

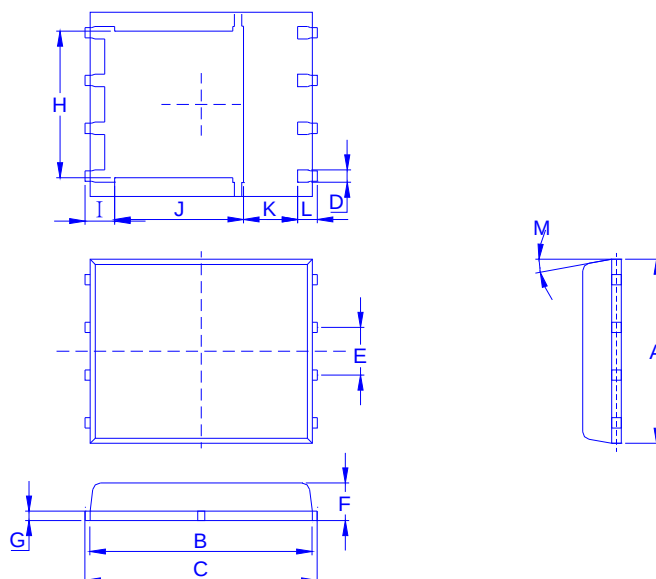
Device Name: EMB03P03H for EDFN 5 x 6







Outline Drawing



Dimension in mm

Dimension	A	B	C	D	E	F	G	H	I	J	K	L	M
Min.	4.80	5.50	5.90	0.3		0.85	0.15	3.67	0.41	3.00	0.94	0.45	0°
Typ.					1.27								
Max.	5.30	5.90	6.15	0.51		1.20	0.30	4.54	0.85	3.92	1.7	0.71	12°

Recommended minimum pads

