



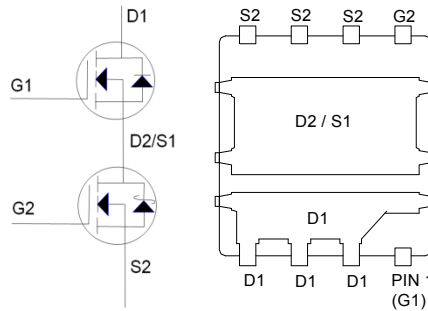
**N-Channel Logic Level Enhancement Mode Field Effect Transistor**

Product Summary:

	N-CH-Q1	N-CH-Q2
BV <sub>DSS</sub>	30V	30V
R <sub>DS(on)</sub> (MAX.)	9mΩ	4mΩ
I <sub>D</sub>	15A	25A

UIS, Rg 100% Tested

Pb-Free Lead Plating & Halogen Free



**ABSOLUTE MAXIMUM RATINGS (T<sub>C</sub> = 25 °C Unless Otherwise Noted)**

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS		UNIT
			Q1	Q2	
Gate-Source Voltage		V <sub>GS</sub>	±20	±20	V
Continuous Drain Current	T <sub>C</sub> = 25 °C	I <sub>D</sub>	15	25	A
	T <sub>C</sub> = 100 °C		12	18	
Pulsed Drain Current <sup>1</sup>		I <sub>DM</sub>	60	100	
Avalanche Current		I <sub>AS</sub>	15	25	
Avalanche Energy	L = 0.1mH, R <sub>G</sub> =25Ω	E <sub>AS</sub>	11.25	31.25	mJ
Repetitive Avalanche Energy <sup>2</sup>	L = 0.05mH	E <sub>AR</sub>	5.62	15.62	
Power Dissipation	T <sub>C</sub> = 25 °C	P <sub>D</sub>	48	100	W
	T <sub>C</sub> = 100 °C		19	40	
Operating Junction & Storage Temperature Range		T <sub>j</sub> , T <sub>stg</sub>	-55 to 150		°C

**THERMAL RESISTANCE RATINGS**

THERMAL RESISTANCE	SYMBOL		TYPICAL	MAXIMUM		UNIT
	R <sub>θJC</sub>	Steady State				
Junction-to-Case	R <sub>θJC</sub>	Steady State		2.6	1.25	°C / W
Junction-to-Ambient	R <sub>θJA</sub>	Steady State		62	55	
	R <sub>θJA</sub>	t ≤ 10 s		27	24	

<sup>1</sup>Pulse width limited by maximum junction temperature.

<sup>2</sup>Duty cycle ≤ 1%

R<sub>θJA</sub> when mounted on a 1 in<sup>2</sup> pad of 2 oz copper.



ELECTRICAL CHARACTERISTICS ( $T_c = 25\text{ }^\circ\text{C}$ , Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT	
			MIN	TYP	MAX		
<b>STATIC</b>							
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	Q1	30		V	
			Q2	30			
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	Q1	1	1.5	3	
			Q2	1	1.5	3	
Gate-Body Leakage	$I_{GSS}$	$V_{DS} = 0V, V_{GS} = \pm 20V$	Q1			$\pm 100$	nA
			Q2			$\pm 100$	
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 24V, V_{GS} = 0V$	Q1			1	$\mu A$
			Q2			1	
		$V_{DS} = 20V, V_{GS} = 0V, T_J = 125\text{ }^\circ\text{C}$	Q1			25	
			Q2			25	
On-State Drain Current <sup>1</sup>	$I_{D(ON)}$	$V_{DS} = 10V, V_{GS} = 10V$	Q1	15		A	
			Q2	25			
Drain-Source On-State Resistance <sup>1</sup>	$R_{DS(ON)}$	$V_{GS} = 10V, I_D = 12A$	Q1		7.6	9	m $\Omega$
		$V_{GS} = 10V, I_D = 20A$	Q2		3.3	4	
		$V_{GS} = 4.5V, I_D = 9A$	Q1		12	14.5	
		$V_{GS} = 4.5V, I_D = 15A$	Q2		4.8	6	
Forward Transconductance <sup>1</sup>	$g_{fs}$	$V_{DS} = 5V, I_D = 13A$	Q1		45	S	
		$V_{DS} = 5V, I_D = 20A$	Q2		105		
<b>DYNAMIC</b>							
Input Capacitance	$C_{iss}$	$V_{GS} = 0V, V_{DS} = 15V, f = 1MHz$	Q1		595	pF	
			Q2		1600		
Output Capacitance	$C_{oss}$		Q1		161		
			Q2		411		
Reverse Transfer Capacitance	$C_{rss}$		Q1		71		
			Q2		174		
Gate Resistance	$R_g$	$V_{GS} = 15mV, V_{DS} = 0V, f = 1MHz$	Q1		1.2	$\Omega$	
			Q2		2.5		
Total Gate Charge <sup>1,2</sup>	$Q_g(V_{GS}=10V)$	$V_{DD} = 15V, V_{GS} = 10V,$ $I_D = 10A$	Q1		8.4	nC	
			Q2		27		
	$Q_g(V_{GS}=4.5V)$		Q1		4.6		
			Q2		14		



Gate-Source Charge <sup>1,2</sup>	$Q_{gs}$	$V_{DD} = 15V, V_{GS} = 10V,$ $I_D = 10A$	Q1	1		
			Q2	3.9		
Gate-Drain Charge <sup>1,2</sup>	$Q_{gd}$		Q1	2.8		
			Q2	7.8		
Turn-On Delay Time <sup>1,2</sup>	$t_{d(on)}$	$V_{DD} = 15V,$ $I_D = 1A, V_{GS} = 10V, R_{GS} = 2.7\Omega$	Q1	8	nS	
			Q2	15		
Rise Time <sup>1,2</sup>	$t_r$		Q1	5		
			Q2	10		
Turn-Off Delay Time <sup>1,2</sup>	$t_{d(off)}$		Q1	15		
			Q2	20		
Fall Time <sup>1,2</sup>	$t_f$	Q1	8			
		Q2	10			
<b>SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (<math>T_c = 25^\circ C</math>)</b>						
Continuous Current	$I_S$		Q1	15	A	
			Q2	25		
Pulsed Current <sup>3</sup>	$I_{SM}$		Q1	60		
			Q2	100		
Forward Voltage <sup>1</sup>	$V_{SD}$		$I_F = 10A, V_{GS} = 0V$	Q1	1.2	V
			Q2	1.2		
Reverse Recovery Time	$t_{rr}$	Q1	22	nS		
		$I_F = 10A, di_F/dt = 100A / \mu S$	Q2		20	
Reverse Recovery Charge	$Q_{rr}$	Q2	6	nC		
		$I_F = 10A, di_F/dt = 100A / \mu S$	Q2		16	

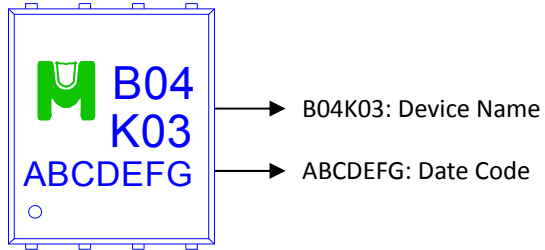
<sup>1</sup>Pulse test : Pulse Width  $\leq 300 \mu sec$ , Duty Cycle  $\leq 2\%$ .

<sup>2</sup>Independent of operating temperature.

<sup>3</sup>Pulse width limited by maximum junction temperature.

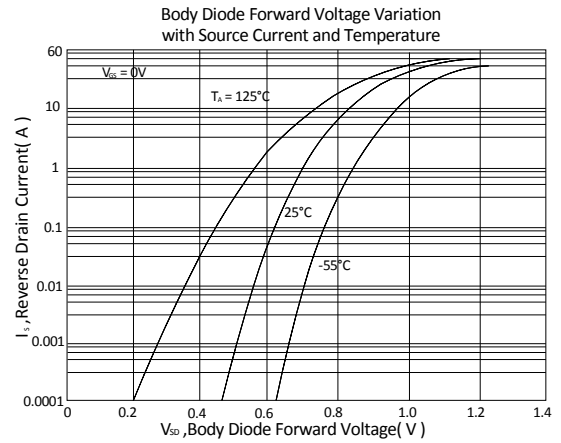
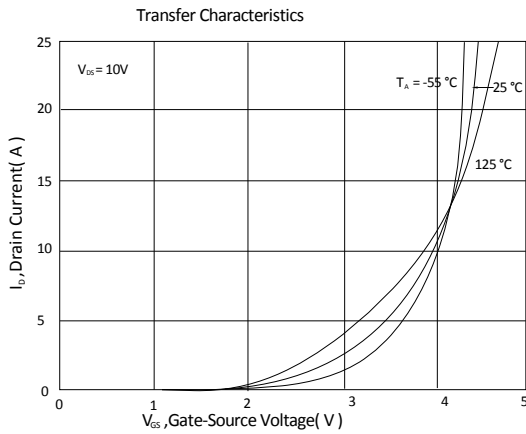
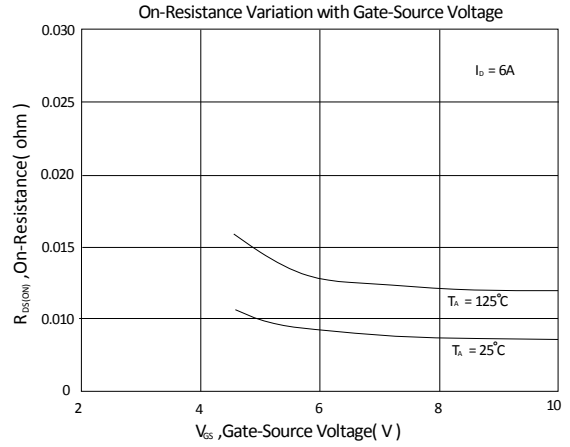
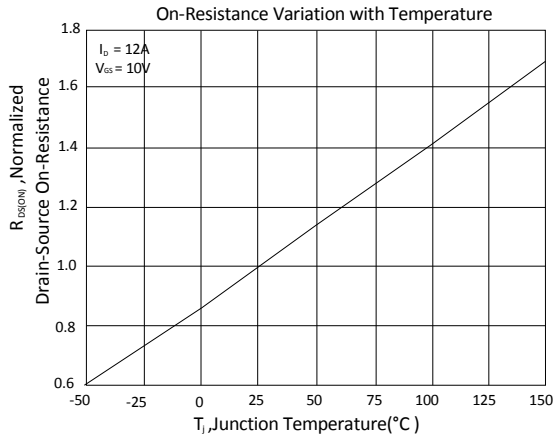
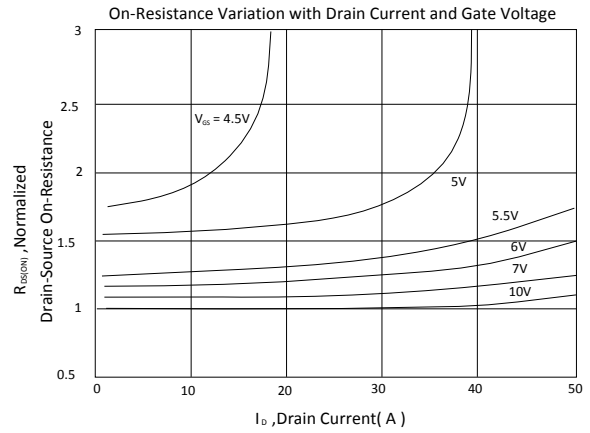
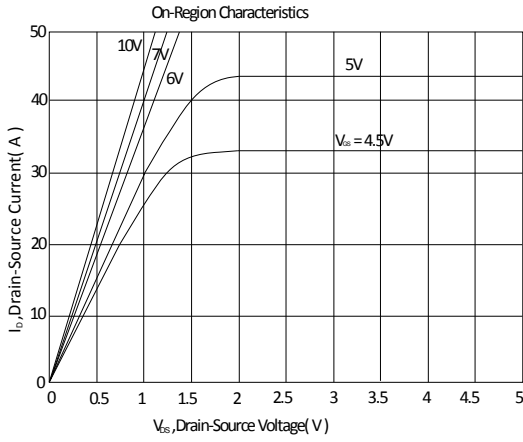
**Ordering & Marking Information:**

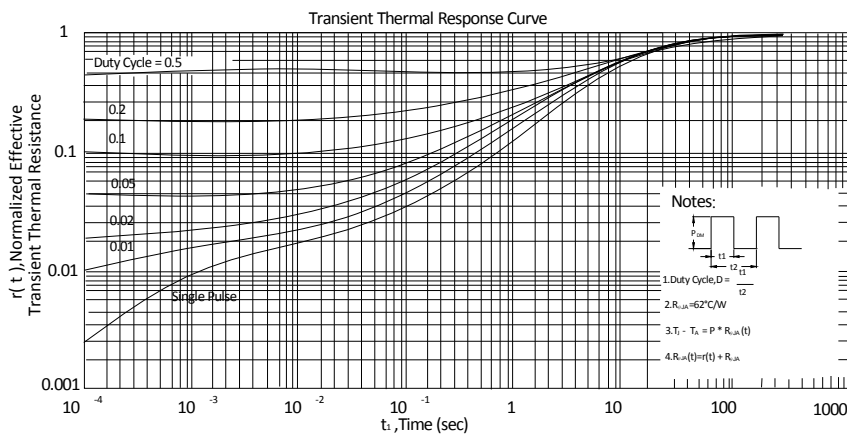
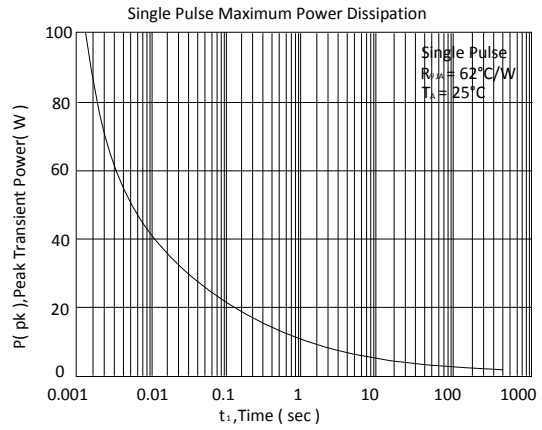
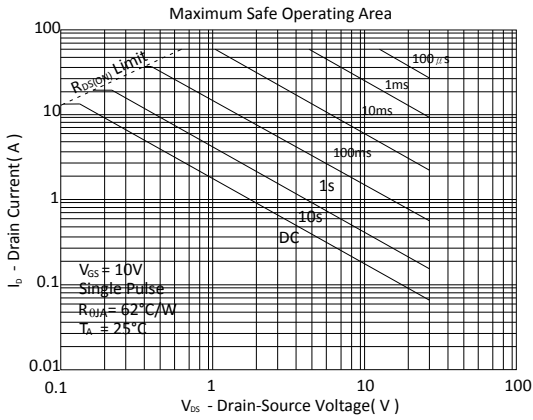
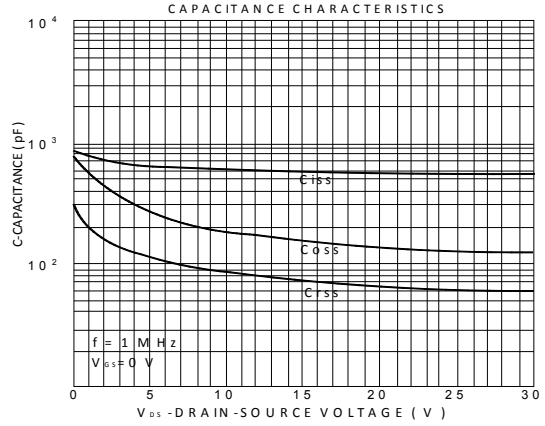
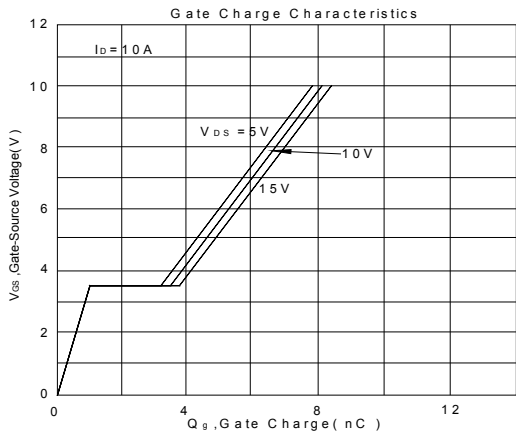
Device Name: EMB04K03HPF for Asymmetric Dual EDFN 5 x 6





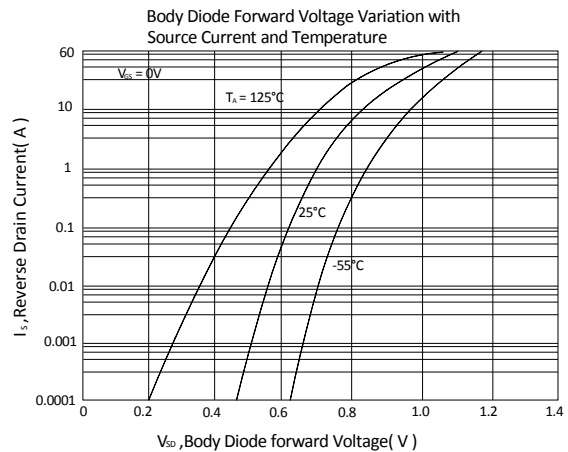
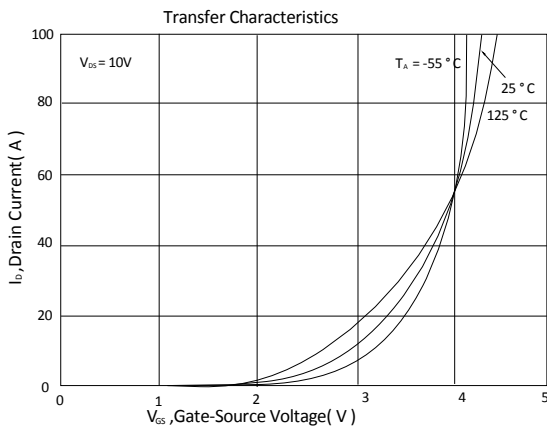
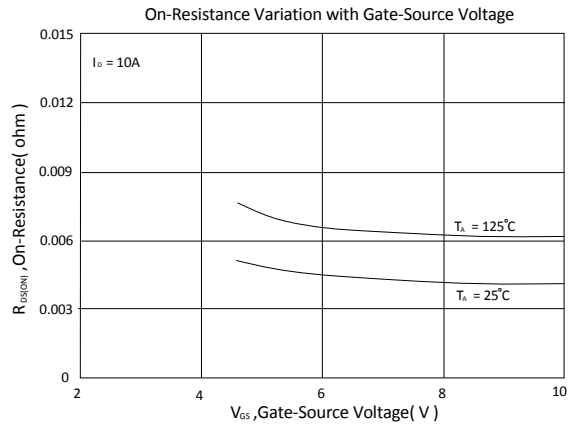
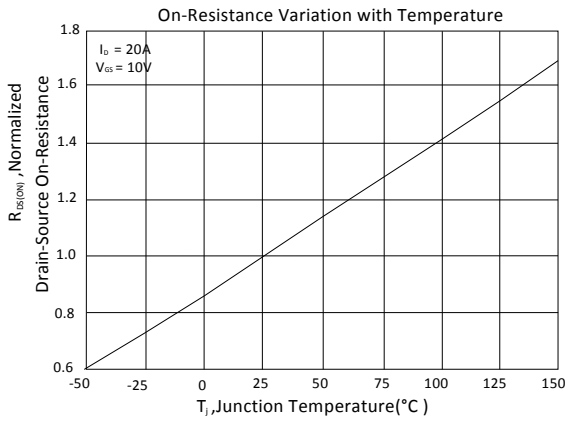
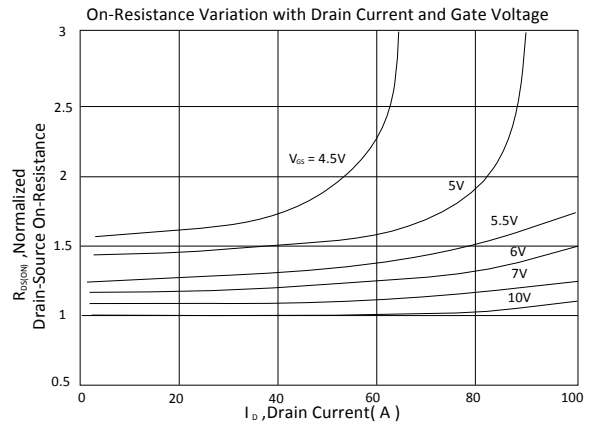
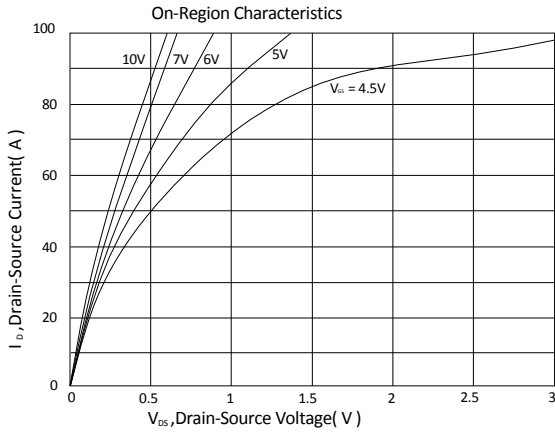
Q1 TYPICAL CHARACTERISTICS

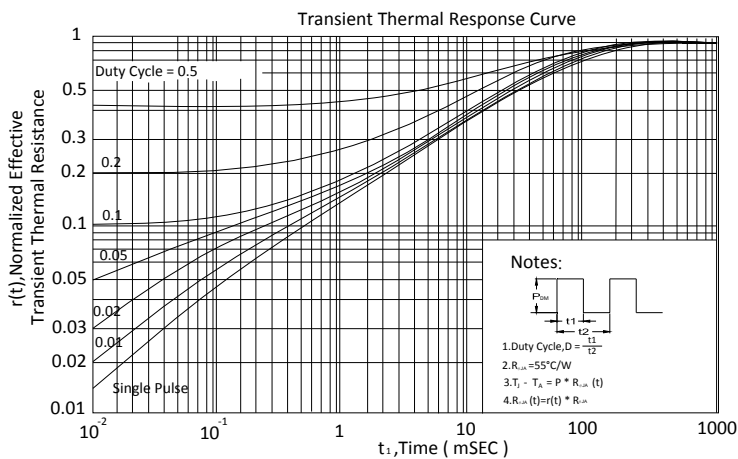
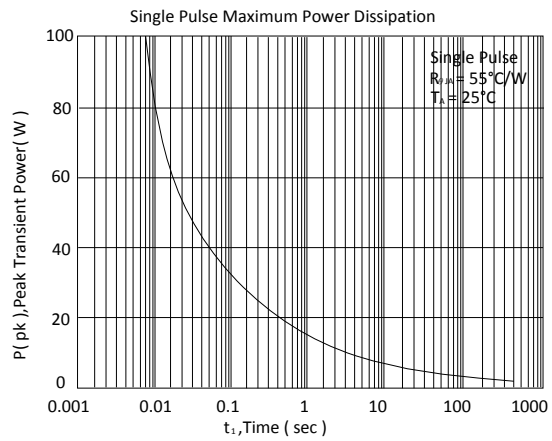
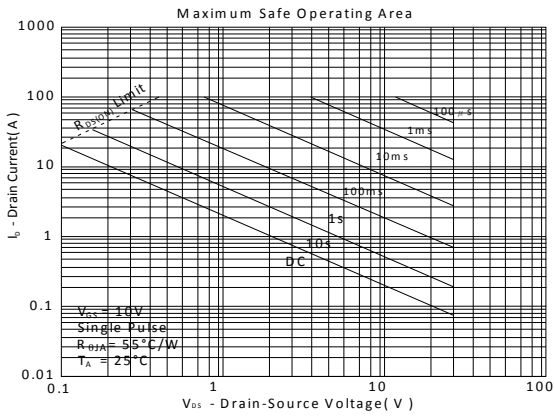
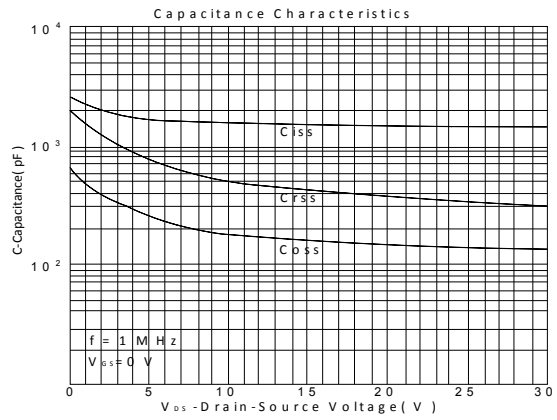
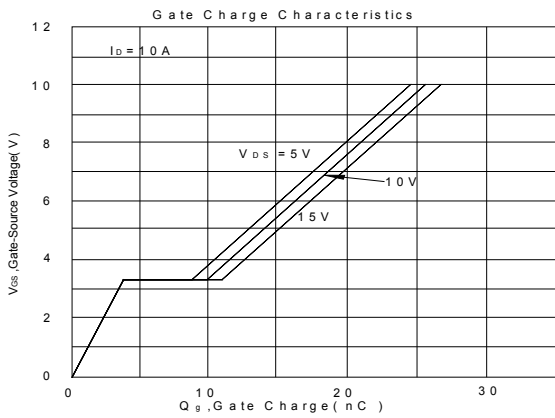






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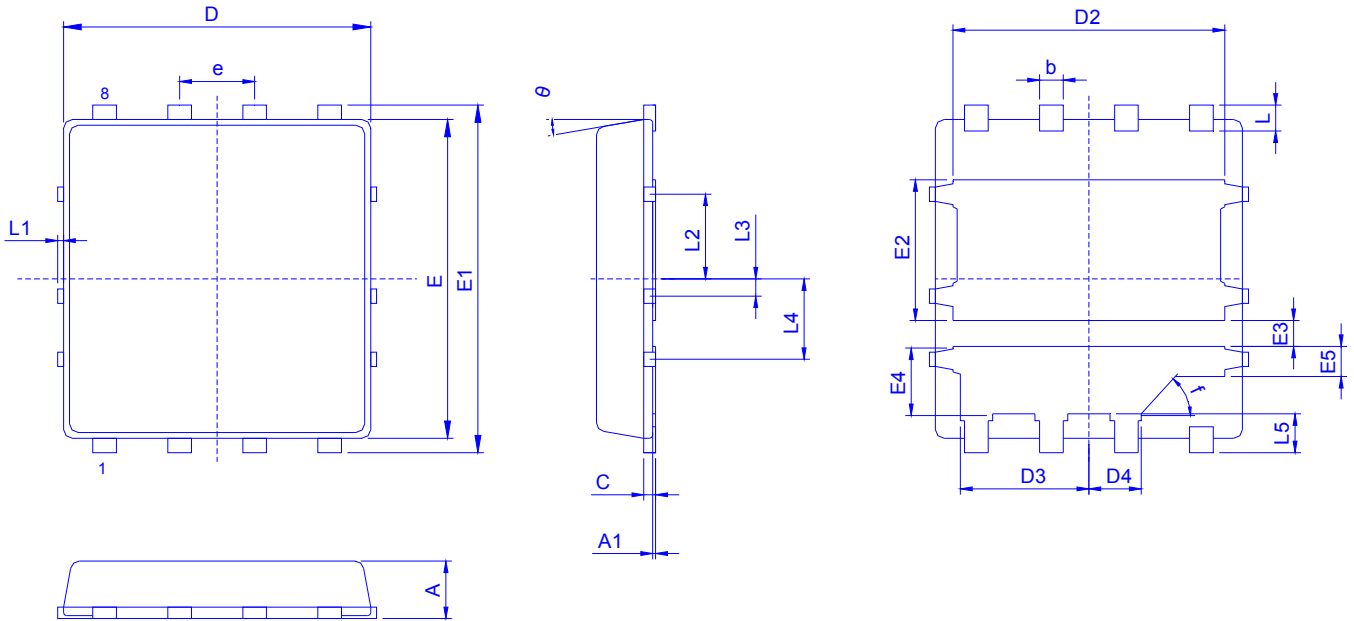








Outline Drawing



Dimension in mm

Dimension	A	A1	b	c	D	D2	D3	D4	E	E1	E2	E3	E4	E5
Min.	0.85	0.00	0.35	0.15		4.5	2.125	0.835			2.4	0.40	1.125	0.475
Typ.	0.90		0.40	0.20	5.2	4.6	2.175	0.885	5.55	6.05	2.45	0.45	1.175	0.525
Max.	1.00	0.05	0.45	0.25		4.7	2.225	0.935			2.5	0.50	1.225	0.575

Dimension	e	L	L1	L2	L3	L4	L5	F	θ
Min.		0.35	0	1.375	0.2	1.3	0.575		0°
Typ.	1.27	0.45		1.475	0.3	1.4	0.675	45°	
Max.		0.55	0.1	1.575	0.4	1.5	0.775		10°

Recommended minimum pads

