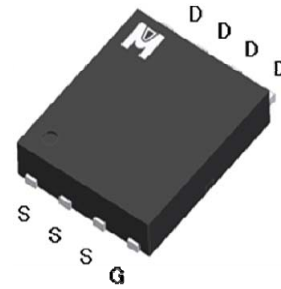
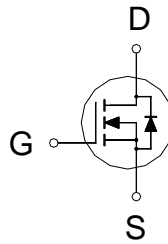


N-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

BV _{DSS}	30V
R _{DS(on)} (MAX.)	4mΩ
I _D	84A



UIS, Rg 100% Tested

Pb-Free Lead Plating & Halogen Free

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V _{GS}	±20	V
Continuous Drain Current ¹	T _C = 25 °C	I _D	84	A
	T _A = 25 °C (t ≤ 10s)		30	
	T _A = 25 °C (Steady-State)		19	
	T _C = 100 °C		53	
Pulsed Drain Current ²		I _{DM}	320	
Avalanche Current		I _{AS}	47	
Avalanche Energy	L = 0.1mH, I _{AS} = 47A, R _G = 25Ω	E _{AS}	110	mJ
Repetitive Avalanche Energy ³	L = 0.05mH	E _{AR}	55	
Power Dissipation	T _C = 25 °C	P _D	50	W
	T _C = 100 °C		20	
Operating Junction & Storage Temperature Range		T _J , T _{stg}	-55 to 150	°C

100% UIS testing in condition of V_D = 15V, L = 0.1mH, V_G = 10V, I_L = 30A, Rated V_{DS} = 30V N-CH

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE		SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case		R _{θJC}		2.5	°C / W
Junction-to-Ambient ³	t ≤ 10s	R _{θJA}		20	
Junction-to-Ambient ⁴	Steady-State	R _{θJA}		50	

¹Package Limited.

²Pulse width limited by maximum junction temperature.

³Duty cycle ≤ 1%



⁴50°C / W when mounted on a 1 in² pad of 2 oz copper.

ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0V, I _D = 250μA	30			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250μA	1	1.7	3	
Gate-Body Leakage	I _{GSS}	V _{DS} = 0V, V _{GS} = ±20V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 24V, V _{GS} = 0V			1	μA
		V _{DS} = 20V, V _{GS} = 0V, T _J = 125 °C			25	
On-State Drain Current ^{1,4}	I _{D(ON)}	V _{DS} = 10V, V _{GS} = 10V	84			A
Drain-Source On-State Resistance ¹	R _{DS(ON)}	V _{GS} = 10V, I _D = 30A		3.2	4.0	mΩ
		V _{GS} = 4.5V, I _D = 24A		4.8	6.0	
Forward Transconductance ¹	g _{fs}	V _{DS} = 5V, I _D = 30A		22		S
DYNAMIC						
Input Capacitance	C _{iss}	V _{GS} = 0V, V _{DS} = 15V, f = 1MHz		2328		pF
Output Capacitance	C _{oss}			672		
Reverse Transfer Capacitance	C _{rss}			66		
Gate Resistance	R _g	V _{GS} = 15mV, V _{DS} = 0V, f = 1MHz		1.6		Ω
Total Gate Charge ^{1,2}	Q _g (V _{GS} =10V)	V _{DS} = 15V, V _{GS} = 10V, I _D = 30A		35		nC
	Q _g (V _{GS} =4.5V)			17		
Gate-Source Charge ^{1,2}	Q _{gs}			4.8		
Gate-Drain Charge ^{1,2}	Q _{gd}			5.4		
Turn-On Delay Time ^{1,2}	t _{d(on)}		V _{DS} = 15V, I _D = 1A, V _{GS} = 10V, R _{GS} = 2.7Ω		20	
Rise Time ^{1,2}	t _r			15		
Turn-Off Delay Time ^{1,2}	t _{d(off)}			50		
Fall Time ^{1,2}	t _f			20		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25 °C)						
Continuous Current ^{1,4}	I _S				84	A
Pulsed Current ³	I _{SM}				320	
Forward Voltage ¹	V _{SD}	I _F = 30A, V _{GS} = 0V			1.2	V
Reverse Recovery Time	t _{rr}	I _F = 30A, dI _F /dt = 100A / μS		26		nS
Reverse Recovery Charge	Q _{rr}				30	

¹Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.

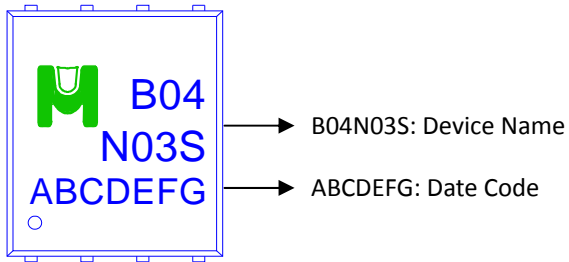
²Independent of operating temperature.

³Pulse width limited by maximum junction temperature.

⁴Package Limited.

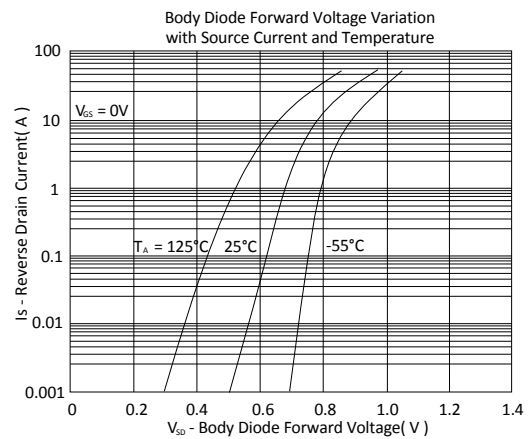
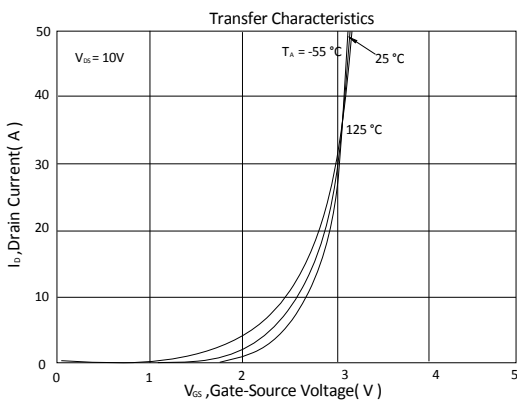
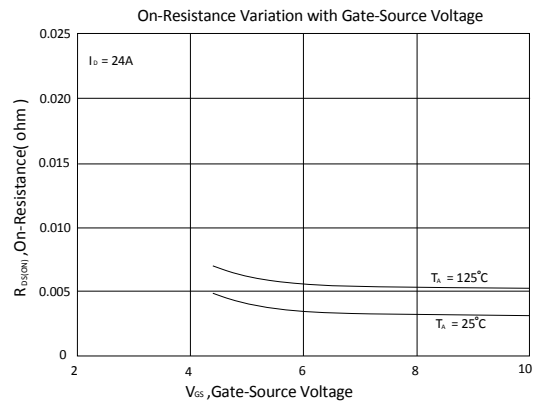
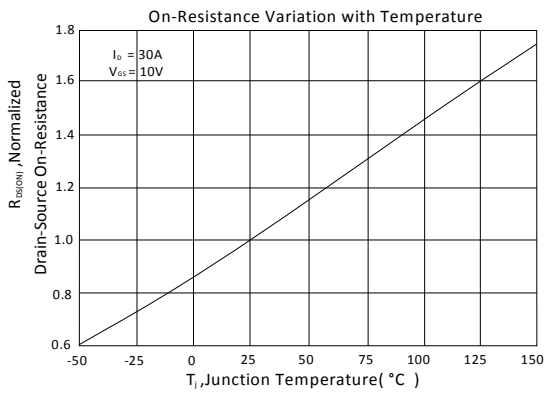
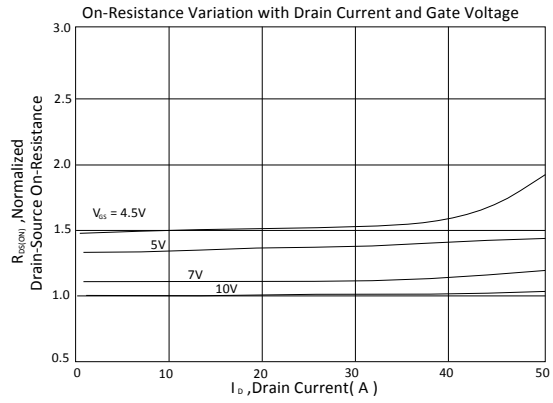
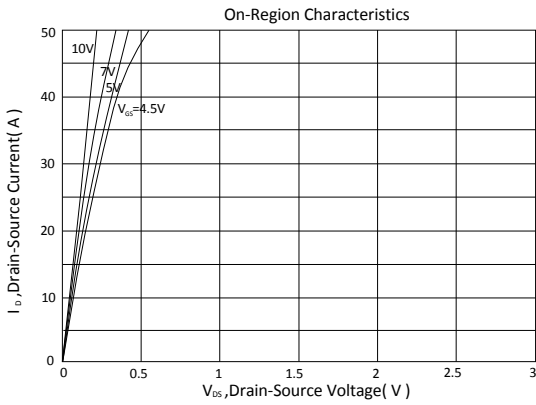
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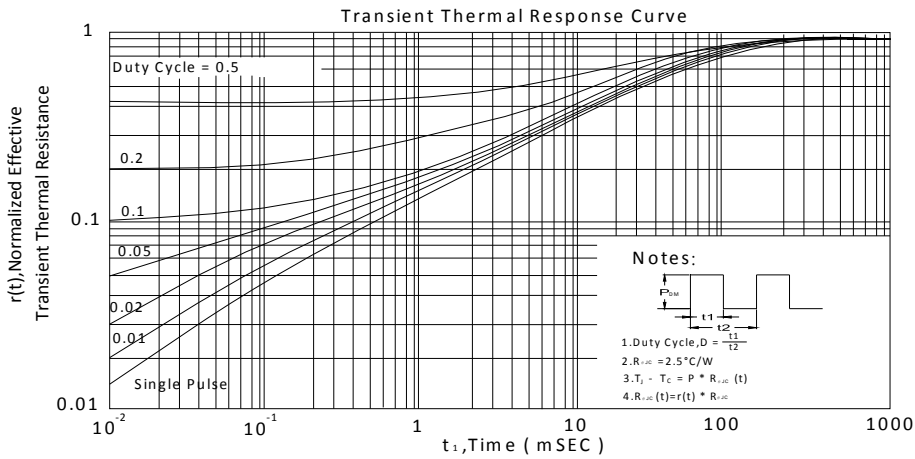
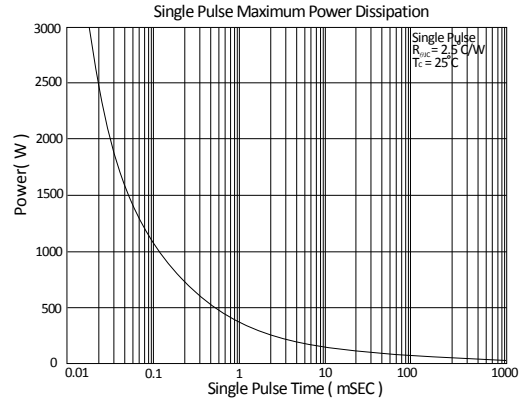
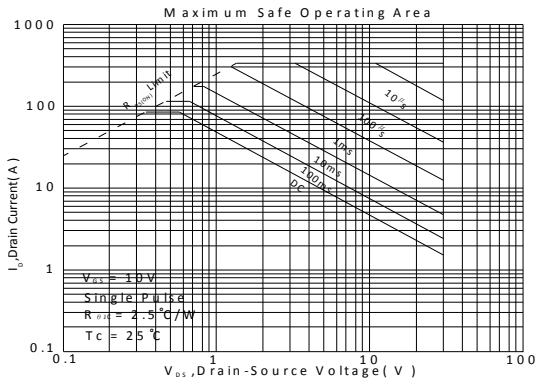
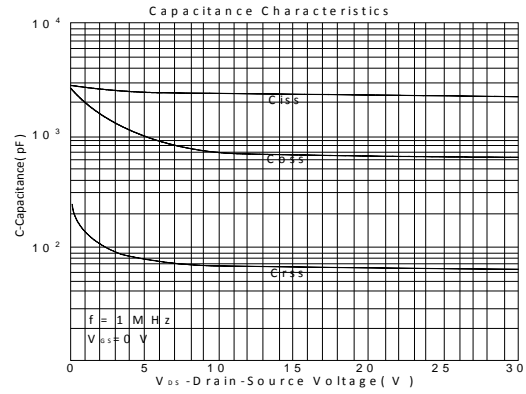
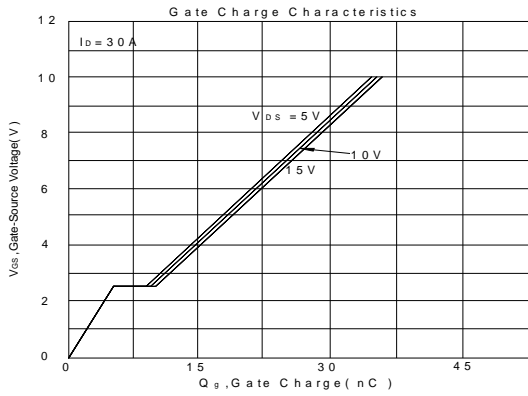
Device Name: EMB04N03HS for EDFN 5 x 6





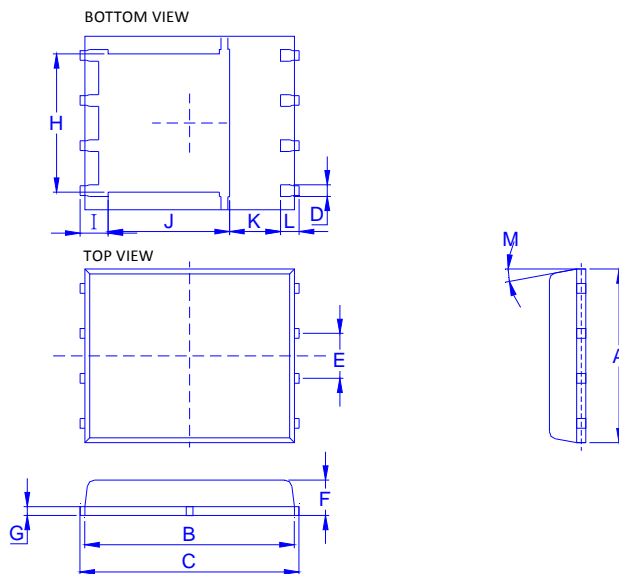
TYPICAL CHARACTERISTICS







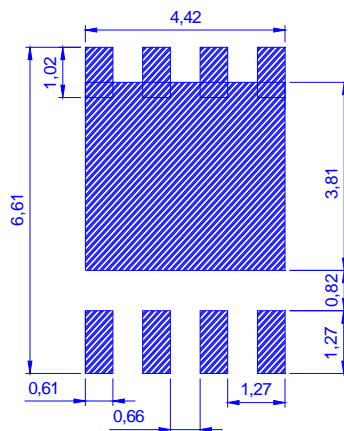
Outline Drawing



Dimension in mm

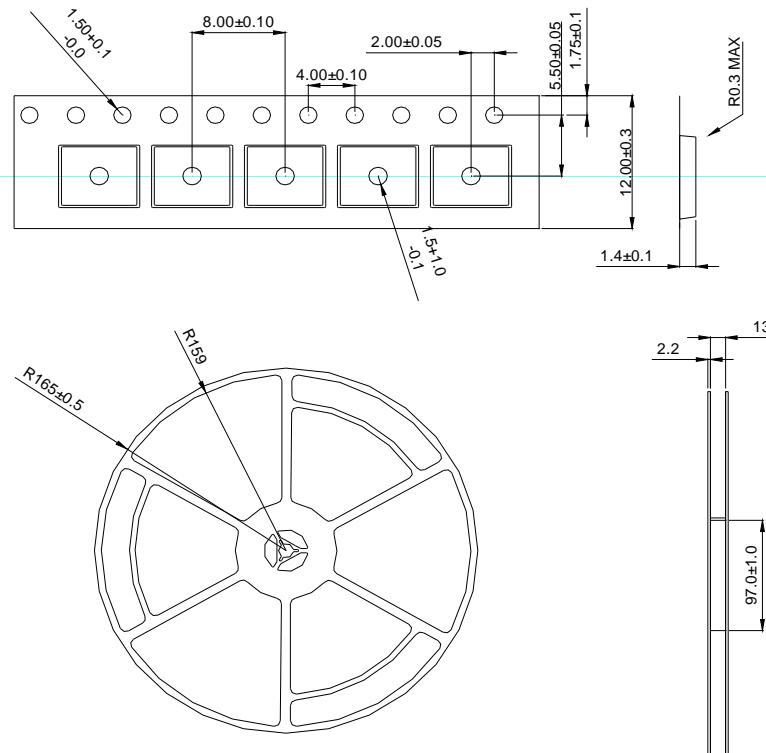
Dimension	A	B	C	D	E	F	G	H	I	J	K	L	M
Min.	4.80	5.50	5.90	0.3		0.85	0.15	3.67	0.41	3.00	0.94	0.45	0°
Typ.					1.27								
Max.	5.30	5.90	6.15	0.51		1.20	0.30	4.54	0.85	3.92	1.7	0.71	12°


Recommended minimum pads





◆ Tape&Reel Information:2500pcs/Reel(Dimension in millimeter)



產品別	EDFN 5*6
Reel 尺寸	13"
編帶方式	L-Type 
前空格	25
後空格	50
裝箱數	
滿捲數量	2.5K
捲/內盒比	1 : 1
內盒滿箱數	2.5K
內/外箱比	10 : 1
外箱滿箱數	25K