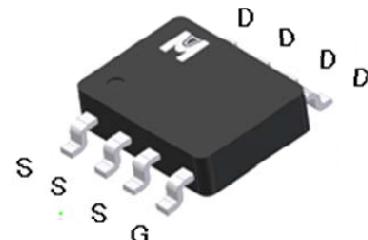
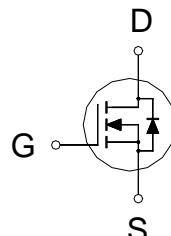


N-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

BV _{DSS}	30V
R _{DSON} (MAX.)	6mΩ
I _D	18A



UIS, R_G 100% Tested

Pb-Free Lead Plating



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V _{GS}	±20	V
Continuous Drain Current	T _A = 25 °C	I _D	18	A
	T _A = 100 °C		12	
Pulsed Drain Current ¹		I _{DM}	72	
Avalanche Current		I _{AS}	20	
Avalanche Energy	L = 0.1mH, ID=20A, RG=25Ω	E _{AS}	20	mJ
Repetitive Avalanche Energy ²	L = 0.05mH	E _{AR}	10	
Power Dissipation	T _A = 25 °C	P _D	2.5	W
	T _A = 100 °C		1	
Operating Junction & Storage Temperature Range		T _j , T _{stg}	-55 to 150	°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	R _{θJC}	25	50	°C / W
Junction-to-Ambient ³	R _{θJA}			

¹Pulse width limited by maximum junction temperature.

²Duty cycle ≤ 1%

³50°C / W when mounted on a 1 in² pad of 2 oz copper.

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(\text{BR})\text{DSS}}$	$V_{GS} = 0V, I_D = 250\mu\text{A}$	30			V
Gate Threshold Voltage	$V_{GS(\text{th})}$	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$	1	1.5	3	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0V, V_{GS} = \pm 20V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 24V, V_{GS} = 0V$			1	μA
		$V_{DS} = 20V, V_{GS} = 0V, T_J = 125^\circ\text{C}$			25	
On-State Drain Current ¹	$I_{D(\text{ON})}$	$V_{DS} = 10V, V_{GS} = 10V$	18			A
Drain-Source On-State Resistance ¹	$R_{DS(\text{ON})}$	$V_{GS} = 10V, I_D = 18\text{A}$		5.3	6	$\text{m}\Omega$
		$V_{GS} = 4.5V, I_D = 12\text{A}$		7.5	9.5	
Forward Transconductance ¹	g_{fs}	$V_{DS} = 5V, I_D = 18\text{A}$		25		S
DYNAMIC						
Input Capacitance	C_{iss}	$V_{GS} = 0V, V_{DS} = 15V, f = 1\text{MHz}$		1983		pF
Output Capacitance	C_{oss}			328		
Reverse Transfer Capacitance	C_{rss}			287		
Gate Resistance	R_g	$V_{GS} = 15\text{mV}, V_{DS} = 0V, f = 1\text{MHz}$		1.2		Ω
Total Gate Charge ^{1,2}	$Q_g(V_{GS}=10V)$	$V_{DS} = 15V, V_{GS} = 10V, I_D = 18\text{A}$		34.6		nC
	$Q_g(V_{GS}=4.5V)$			21		
Gate-Source Charge ^{1,2}	Q_{gs}			4.8		
Gate-Drain Charge ^{1,2}	Q_{gd}			9.7		
Turn-On Delay Time ^{1,2}	$t_{d(on)}$	$V_{DS} = 15V, I_D = 1\text{A}, V_{GS} = 10V, R_{GS} = 2.7\Omega$		9		nS
Rise Time ^{1,2}	t_r			20		
Turn-Off Delay Time ^{1,2}	$t_{d(off)}$			25		
Fall Time ^{1,2}	t_f			3		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS ($T_c = 25^\circ\text{C}$)						
Continuous Current	I_S	$I_F = I_S, V_{GS} = 0V$			4	A
Pulsed Current ³	I_{SM}				40	
Forward Voltage ¹	V_{SD}				1.2	
Reverse Recovery Time	t_{rr}			32		
Peak Reverse Recovery Current	$I_{RM(\text{REC})}$			40		
Reverse Recovery Charge	Q_{rr}			12		

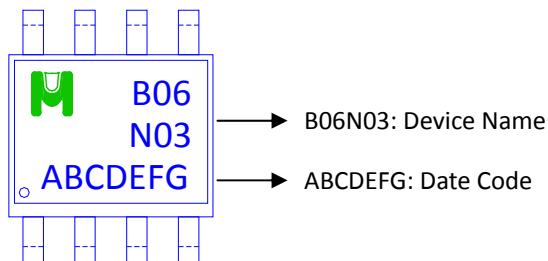
¹Pulse test : Pulse Width \leq 300 μ sec, Duty Cycle \leq 2%.

²Independent of operating temperature.

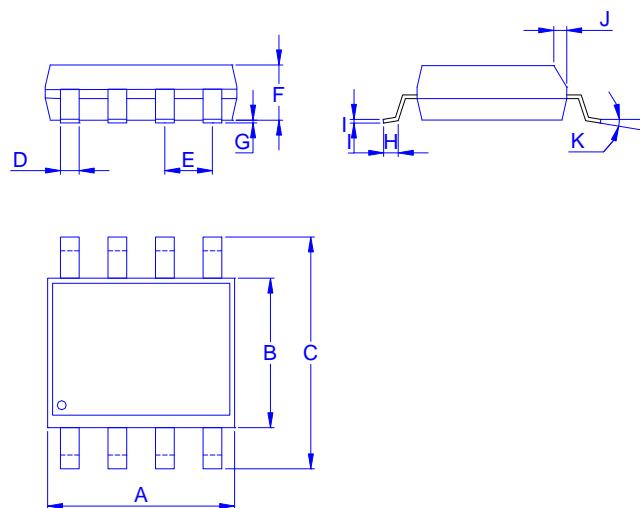
³Pulse width limited by maximum junction temperature.

Ordering & Marking Information:

Device Name: EMB06N03G for SOP-8



Outline Drawing



Dimension in mm

Dimension	A	B	C	D	E	F	G	H	I	J	K
in.	4.70	3.70	5.80	0.33		1.20	0.08	0.40	0.19	0.25	0°
Typ.					1.27						
Max.	5.10	4.10	6.20	0.51		1.62	0.28	0.83	0.26	0.50	8°

