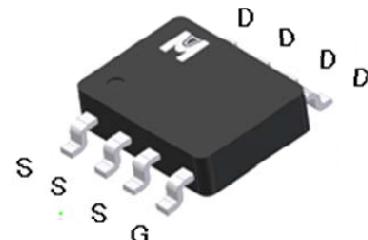


N-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

BV <sub>DSS</sub>	30V
R <sub>DSON</sub> (MAX.)	6mΩ
I <sub>D</sub>	18A



UIS, R<sub>G</sub> 100% Tested

Pb-Free Lead Plating & Halogen Free



ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$  Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V <sub>GS</sub>	±20	V
Continuous Drain Current	T <sub>A</sub> = 25 °C	I <sub>D</sub>	18	A
	T <sub>A</sub> = 100 °C		12	
Pulsed Drain Current <sup>1</sup>		I <sub>DM</sub>	72	
Avalanche Current		I <sub>AS</sub>	20	
Avalanche Energy	L = 0.1mH, ID=20A, RG=25Ω	E <sub>AS</sub>	20	mJ
Repetitive Avalanche Energy <sup>2</sup>	L = 0.05mH	E <sub>AR</sub>	10	
Power Dissipation	T <sub>A</sub> = 25 °C	P <sub>D</sub>	2.5	W
	T <sub>A</sub> = 100 °C		1	
Operating Junction & Storage Temperature Range		T <sub>j</sub> , T <sub>stg</sub>	-55 to 150	°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	R <sub>θJC</sub>	25	50	°C / W
Junction-to-Ambient <sup>3</sup>	R <sub>θJA</sub>			

<sup>1</sup>Pulse width limited by maximum junction temperature.

<sup>2</sup>Duty cycle ≤ 1%

<sup>3</sup>50°C / W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper.

ELECTRICAL CHARACTERISTICS ( $T_c = 25^\circ\text{C}$ , Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(\text{BR})\text{DSS}}$	$V_{GS} = 0V, I_D = 250\mu\text{A}$	30			V
Gate Threshold Voltage	$V_{GS(\text{th})}$	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$	1	1.5	3	
Gate-Body Leakage	$I_{GSS}$	$V_{DS} = 0V, V_{GS} = \pm 20V$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 24V, V_{GS} = 0V$			1	$\mu\text{A}$
		$V_{DS} = 20V, V_{GS} = 0V, T_J = 125^\circ\text{C}$			25	
On-State Drain Current <sup>1</sup>	$I_{D(\text{ON})}$	$V_{DS} = 10V, V_{GS} = 10V$	18			A
Drain-Source On-State Resistance <sup>1</sup>	$R_{DS(\text{ON})}$	$V_{GS} = 10V, I_D = 18\text{A}$		4.7	6	$\text{m}\Omega$
		$V_{GS} = 4.5V, I_D = 12\text{A}$		8.7	11	
Forward Transconductance <sup>1</sup>	$g_{fs}$	$V_{DS} = 5V, I_D = 18\text{A}$		26		S
DYNAMIC						
Input Capacitance	$C_{iss}$	$V_{GS} = 0V, V_{DS} = 15V, f = 1\text{MHz}$		1983		$\text{pF}$
Output Capacitance	$C_{oss}$			328		
Reverse Transfer Capacitance	$C_{rss}$			287		
Gate Resistance	$R_g$	$V_{GS} = 15\text{mV}, V_{DS} = 0V, f = 1\text{MHz}$		1.3		$\Omega$
Total Gate Charge <sup>1,2</sup>	$Q_g(V_{GS}=10V)$	$V_{DS} = 15V, V_{GS} = 10V, I_D = 18\text{A}$		34.6		$\text{nC}$
	$Q_g(V_{GS}=4.5V)$			21		
Gate-Source Charge <sup>1,2</sup>	$Q_{gs}$			4.8		
Gate-Drain Charge <sup>1,2</sup>	$Q_{gd}$			9.7		
Turn-On Delay Time <sup>1,2</sup>	$t_{d(on)}$	$V_{DS} = 15V, I_D = 1\text{A}, V_{GS} = 10V, R_{GS} = 2.7\Omega$		20		$\text{ns}$
Rise Time <sup>1,2</sup>	$t_r$			15		
Turn-Off Delay Time <sup>1,2</sup>	$t_{d(off)}$			60		
Fall Time <sup>1,2</sup>	$t_f$			10		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS ( $T_c = 25^\circ\text{C}$ )						
Continuous Current	$I_S$	$I_F = I_S, V_{GS} = 0V$			10	$\text{A}$
Pulsed Current <sup>3</sup>	$I_{SM}$				40	
Forward Voltage <sup>1</sup>	$V_{SD}$				1.2	
Reverse Recovery Time	$t_{rr}$			32		
Peak Reverse Recovery Current	$I_{RM(\text{REC})}$			40		
Reverse Recovery Charge	$Q_{rr}$			12		

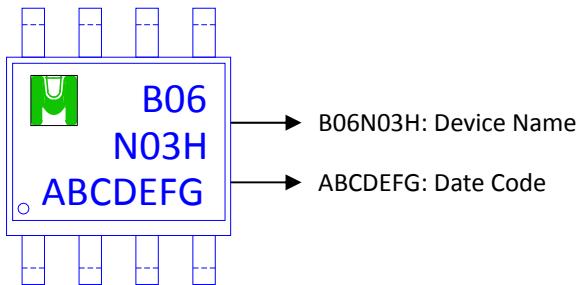
<sup>1</sup>Pulse test : Pulse Width  $\leq$  300  $\mu$ sec, Duty Cycle  $\leq$  2%.

<sup>2</sup>Independent of operating temperature.

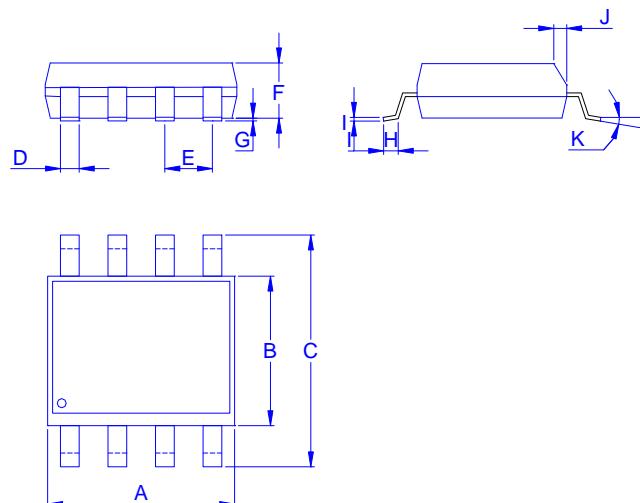
<sup>3</sup>Pulse width limited by maximum junction temperature.

#### Ordering & Marking Information:

Device Name: EMB06N03GH for SOP-8



#### Outline Drawing



Dimension in mm

Dimension	A	B	C	D	E	F	G	H	I	J	K
Min.	4.70	3.70	5.80	0.33		1.20	0.08	0.40	0.19	0.25	0°
Typ.					1.27						
Max.	5.10	4.10	6.20	0.51		1.62	0.28	0.83	0.26	0.50	8°

