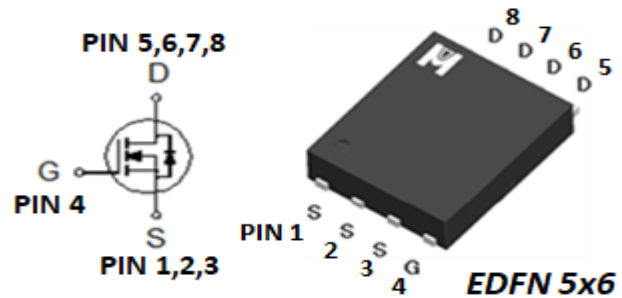


Single N-Channel Logic Level Enhancement Mode Field Effect Transistor

▪Product Summary:

	N-CH
BVDSS	30V
$R_{DS(ON)(MAX.)}@V_{GS}=10V$	7.0m Ω
$R_{DS(ON)(MAX.)}@V_{GS}=4.5V$	10.6m Ω
$I_D @T_C=25^\circ C$	51.0A
$I_D @T_A=25^\circ C$	14.0A

▪ Pin Description:



Single N Channel MOSFET

UIS, Rg 100% Tested

Pb-Free Lead Plating & Halogen Free

▪ABSOLUTE MAXIMUM RATINGS ($T_C = 25^\circ C$ Unless Otherwise Noted)



PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current	$T_C = 25^\circ C$	I_D	51	A
	$T_C = 100^\circ C$		46	
Continuous Drain Current	$T_A = 25^\circ C$	I_D	14	
	$T_A = 70^\circ C$		11	
Pulsed Drain Current ¹		I_{DM}	110	
Avalanche Current		I_{AS}	30	
Avalanche Energy	L = 0.1mH	EAS	45.0	mJ
Repetitive Avalanche Energy ²	L = 0.05mH	EAR	22.5	
Power Dissipation	$T_C = 25^\circ C$	P_D	56.8	W
	$T_C = 100^\circ C$		22.7	
Power Dissipation	$T_A = 25^\circ C$	P_D	2.3	W
	$T_A = 70^\circ C$		1.5	
Operating Junction & Storage Temperature Range		T_j, T_{stg}	-55 to 150	$^\circ C$

▪ 100% UIS testing in condition of $V_D=15V, L=0.1mH, V_G=10V, I_L=18A, \text{Rated } V_{DS}=30V \text{ N-CH}$

▪THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	$R_{\theta JC}$		2.2	$^\circ C/W$
Junction-to-Ambient ³	$R_{\theta JA}$		55	

¹Pulse width limited by maximum junction temperature.

²Duty cycle < 1%

³55 $^\circ C$ / W when mounted on a 1 in² pad of 2 oz copper.

⁴Guarantee by Engineering test

▪ ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage ⁴	V _{(BR)DSS}	V _{GS} = 0V, I _D = 250uA	30			V
Gate Threshold Voltage ⁴	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250uA	1.5	1.6	2.5	
Gate-Body Leakage ⁴	I _{GSS}	V _{DS} = 0V, V _{GS} = ±20V			±100	nA
Zero Gate Voltage Drain Current ⁴	I _{DSS}	V _{DS} = 30V, V _{GS} = 0V			1	uA
		V _{DS} = 30V, V _{GS} = 0V, T _J = 125 °C			100	
On-State Drain Current ¹	I _{D(ON)}	V _{DS} = 10V, V _{GS} = 10V	51			A
Drain-Source On-State Resistance ^{1,4}	R _{DS(ON)}	V _{GS} = 10V, I _D = 25A		5.9	7	mΩ
		V _{GS} = 4.5V, I _D = 20A		8.9	10.6	
Forward Transconductance ¹	g _{fs}	V _{DS} = 5V, I _D = 25A		18		S
DYNAMIC						
Input Capacitance ⁵	C _{iss}	V _{GS} = 0V, V _{DS} = 15V, f = 1MHz		970		pF
Output Capacitance ⁵	C _{oss}			428		
Reverse Transfer Capacitance ⁵	C _{rss}			46		
Gate Resistance ^{4,5}	R _g	f = 1MHz		1.0		Ω
Total Gate Charge ^{1,2,5}	Q _g (V _{GS} =10V)	V _{DS} = 15V, V _{GS} = 10V, I _D = 25A		16.9		nC
	Q _g (V _{GS} =4.5V)			8.5		
Gate-Source Charge ^{1,2,5}	Q _{gs}			2.6		
Gate-Drain Charge ^{1,2,5}	Q _{gd}			3.2		
Turn-On Delay Time ^{1,2,5}	t _{d(on)}	V _{DS} = 15V, V _{GS} = 10V, I _D = 5A, R _g = 6Ω		6.8		nS
Rise Time ^{1,2,5}	t _r			11.5		
Turn-Off Delay Time ^{1,2,5}	t _{d(off)}			15.4		
Fall Time ^{1,2,5}	t _f			2.8		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS						
Continuous Current	I _S				51	A
Pulsed Current ³	I _{SM}				110	
Forward Voltage ^{1,4}	V _{SD}	I _F = 25A, V _{GS} = 0V			1.3	V
Reverse Recovery Time ⁵	t _{rr}	I _F = 25A, dI _F /dt = 400A / uS		144.5		nS
Peak Reverse Recovery Current ⁵	I _{RM(REC)}			3.14		A
Reverse Recovery Charge ⁵	Q _{rr}			271.0		nC

¹ Pulse test : Pulse Width ≤ 300 usec, Duty Cycle ≤ 2%.

² Independent of operating temperature.

³ Pulse width limited by maximum junction temperature.

⁴ Guarantee by FT test Item

⁵ Guarantee by Engineering test

EMC will review datasheet by quarter, and update new version.

▪ TYPICAL CHARACTERISTICS

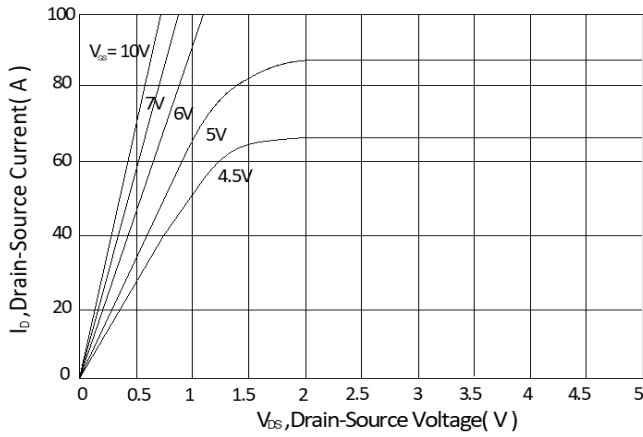


Fig.1 Typical Output Characteristics

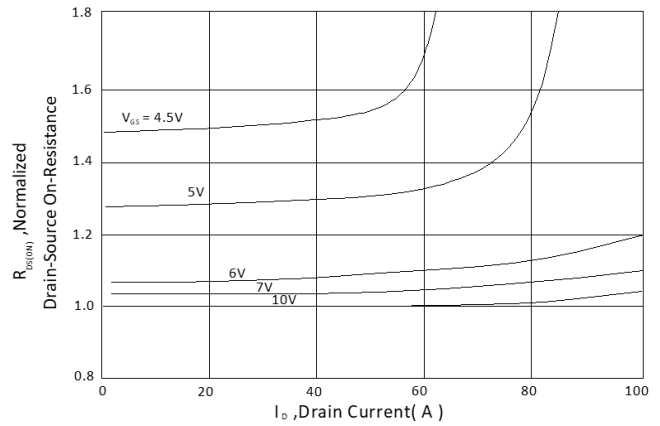


Fig.2 On-Resistance Variation with Drain Current and Gate Voltage

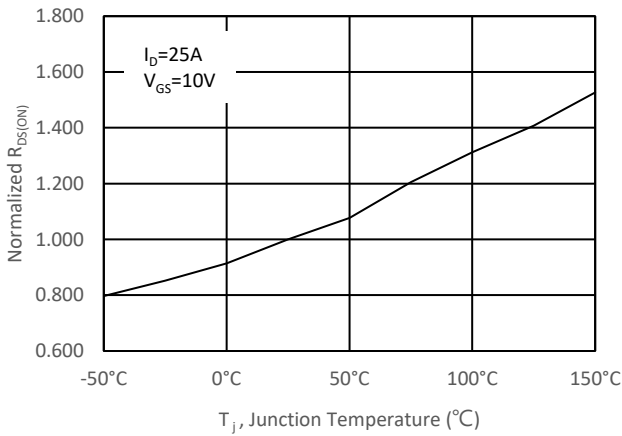


Fig.3 Normalized On-Resistance v.s. Junction Temperature

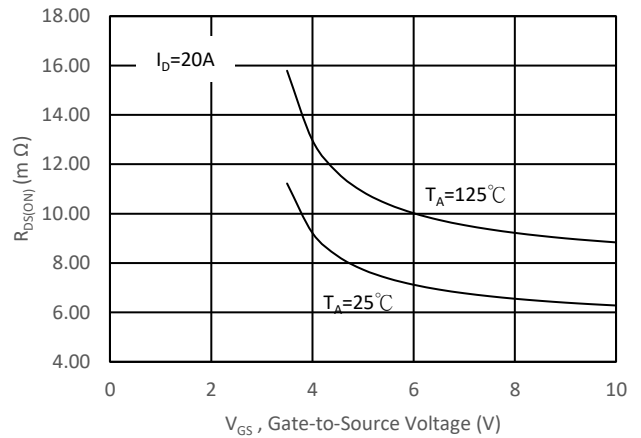


Fig.4 On-Resistance v.s. Gate Voltage

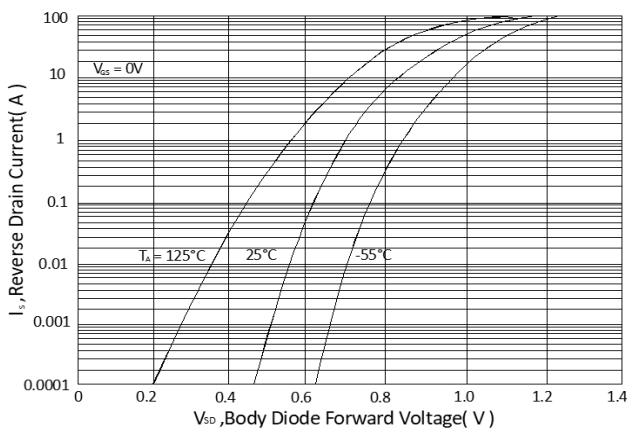


Fig.5 Forward Characteristic of Reverse Diode

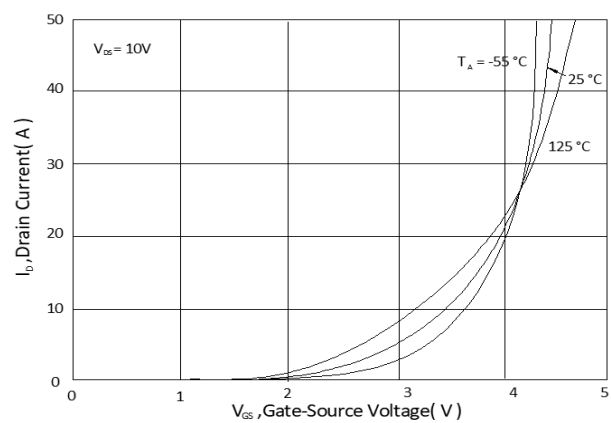


Fig.6 Transfer Characteristics

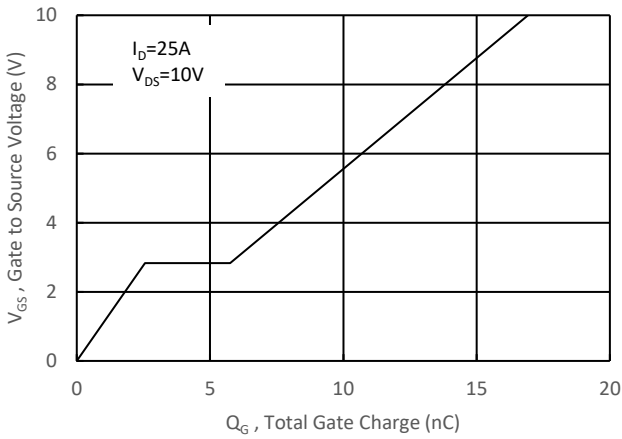


Fig.7 Gate Charge Characteristics

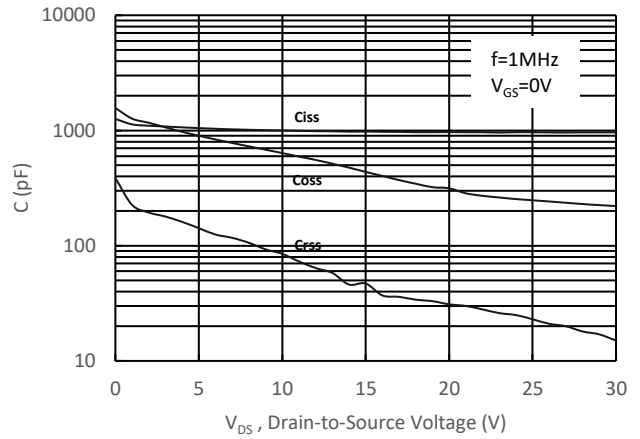


Fig.8 Typical Capacitance Characteristics

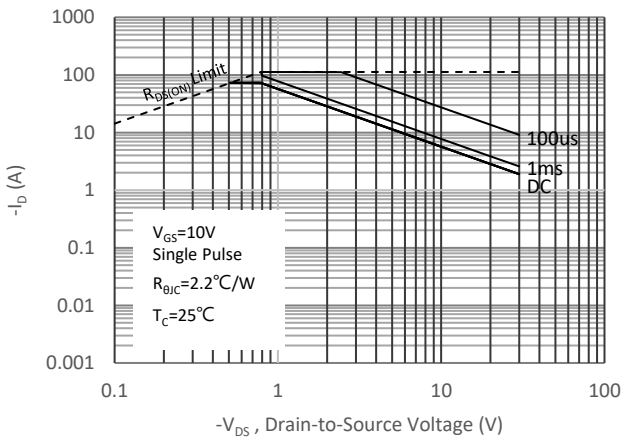


Fig.9. Maximum Safe Operating Area

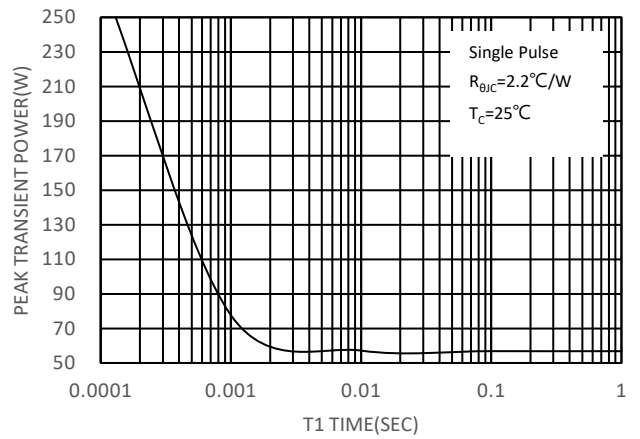


Fig.10. Single Pulse Maximum Power Dissipation

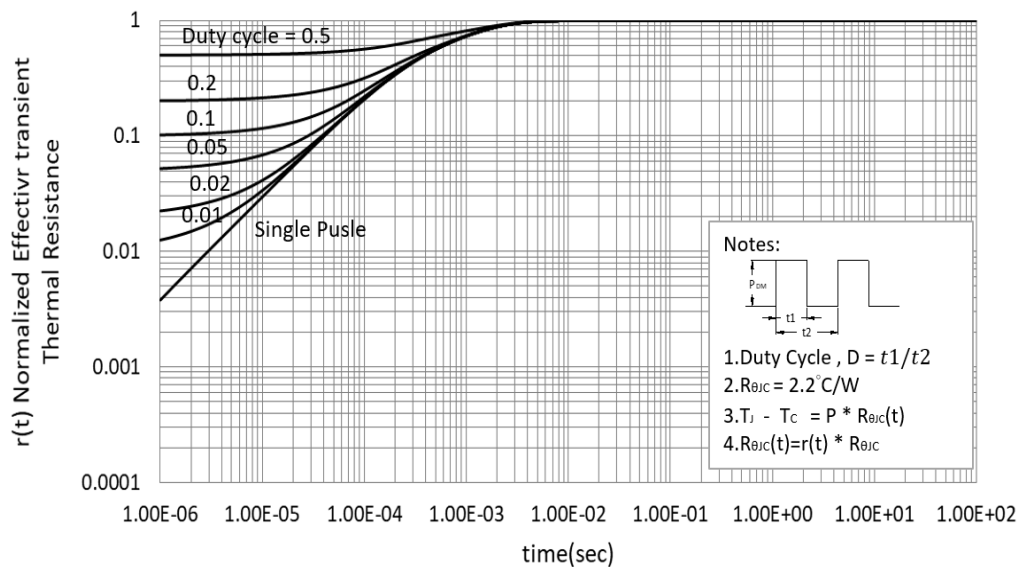


Fig.11. Effective Transient Thermal Impedance

Ordering & Marking Information:

Device Name: EMB07N03HS for EDFN 5x6



B07N03S: Device Name

ABCDEFGH: Date Code

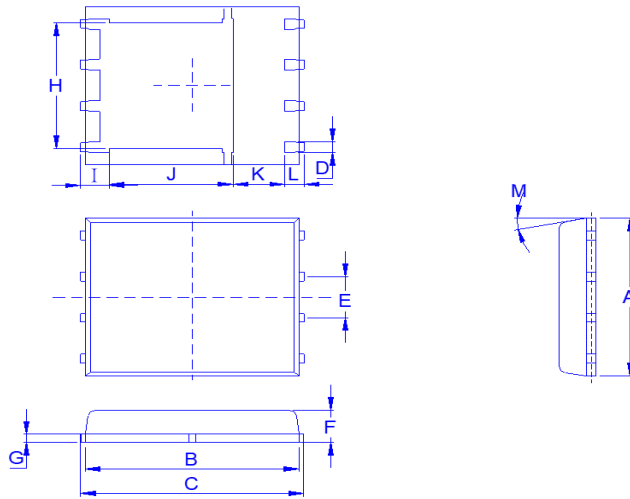
A: Assembly House

B: Year(A:2008 B:2009 C:2010....)

C: Month(A:01 B:02 C:03 D:04 E:05 F:06 G:07 H:08 I:09 J:10 K:11 L:12)

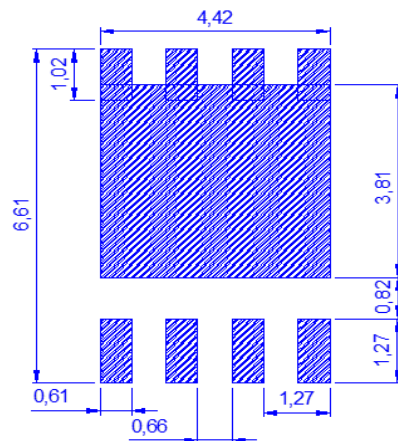
DEFG: Serial No.

Outline Drawing

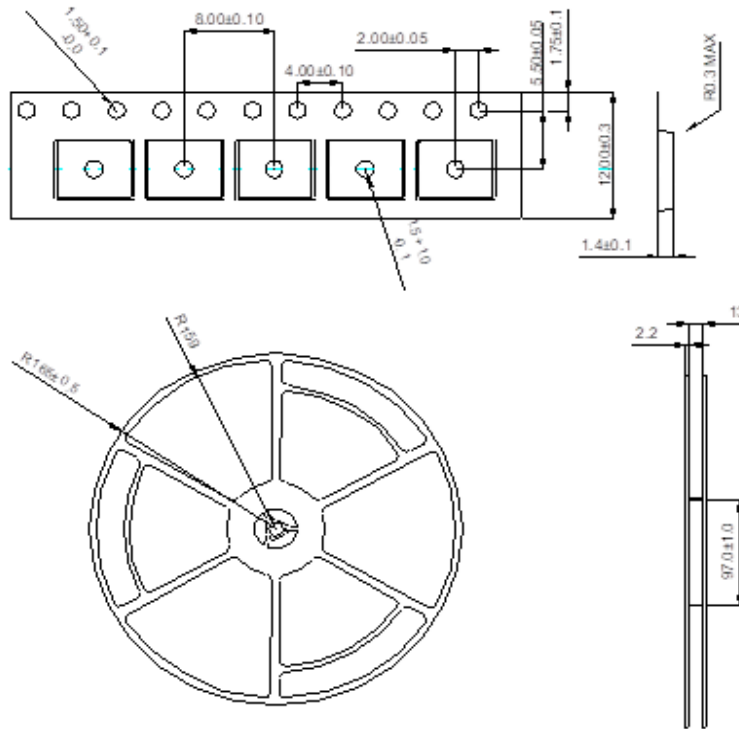


Dimension	A	B	C	D	E	F	G	H	I	J	K	L	M
Min.	4.8	5.55	5.9	0.3	1.17	0.85	0.15	3.61	0.38	3.18	1	0.38	0°
Typ.	4.9	5.7	6	0.4	1.27	0.95	0.2	3.87	0.4	3.44	1.2	0.4	
Max.	5.4	5.85	6.15	0.51	1.37	1.17	0.34	4.31	0.71	3.78	1.39	0.71	12°

Footprint



◆ Tape&Reel Information:2500pcs/Reel
 (Dimension in millimeter)



產品別	EDFN5X6
Reel尺寸	13"
編帶方式	FEED DIRECTION
前空格	25
後空格	50
裝箱數	
滿捲數量	2.5K
捲/內盒比	01:01
內盒滿箱數	2.5K
內/外箱比	10:01
外箱滿箱數	25K



★Datasheet Latest version specification :

	Revision History	Prepared	Approved	Date
A.0	Initial Datasheet	Jannie	Andy	2018/1/26
A.1	Update electrical specifications	Johnson	Sam	2020/8/26