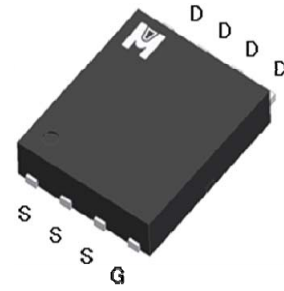
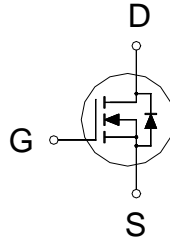


N-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

BV <sub>DSS</sub>	40V
R <sub>DS(on)</sub> (MAX.)	7mΩ
I <sub>D</sub>	55A



UIS, R<sub>g</sub> 100% Tested

Pb-Free Lead Plating & Halogen Free



ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub> = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V <sub>GS</sub>	±20	V
Continuous Drain Current	T <sub>C</sub> = 25 °C	I <sub>D</sub>	55	A
	T <sub>C</sub> = 100 °C		40	
Pulsed Drain Current <sup>1</sup>		I <sub>DM</sub>	150	
Avalanche Current		I <sub>AS</sub>	50	
Avalanche Energy	L = 0.1mH, I <sub>D</sub> =50A, R <sub>G</sub> =25Ω	E <sub>AS</sub>	125	mJ
Repetitive Avalanche Energy <sup>2</sup>	L = 0.05mH	E <sub>AR</sub>	62.5	
Power Dissipation	T <sub>C</sub> = 25 °C	P <sub>D</sub>	50	W
	T <sub>C</sub> = 100 °C		20	
Operating Junction & Storage Temperature Range		T <sub>j</sub> , T <sub>stg</sub>	-55 to 150	°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	R <sub>θJC</sub>		2.5	°C / W
Junction-to-Ambient	R <sub>θJA</sub>		50	

<sup>1</sup>Pulse width limited by maximum junction temperature.

<sup>2</sup>Duty cycle ≤ 1%



ELECTRICAL CHARACTERISTICS ( $T_J = 25\text{ }^\circ\text{C}$ , Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
<b>STATIC</b>						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	40			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	1.0	1.9	3.0	
Gate-Body Leakage	$I_{GSS}$	$V_{DS} = 0V, V_{GS} = \pm 20V$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 32V, V_{GS} = 0V$			1	$\mu A$
		$V_{DS} = 30V, V_{GS} = 0V, T_J = 125\text{ }^\circ\text{C}$			25	
On-State Drain Current <sup>1</sup>	$I_{D(ON)}$	$V_{DS} = 10V, V_{GS} = 10V$	55			A
Drain-Source On-State Resistance <sup>1</sup>	$R_{DS(ON)}$	$V_{GS} = 10V, I_D = 24A$		6	7	$m\Omega$
		$V_{GS} = 4.5V, I_D = 16A$		8	11	
Forward Transconductance <sup>1</sup>	$g_{fs}$	$V_{DS} = 5V, I_D = 24A$		28		S
<b>DYNAMIC</b>						
Input Capacitance	$C_{iss}$	$V_{GS} = 0V, V_{DS} = 20V, f = 1MHz$		1977		$pF$
Output Capacitance	$C_{oss}$			257		
Reverse Transfer Capacitance	$C_{rss}$			230		
Gate Resistance	$R_g$	$V_{GS} = 15mV, V_{DS} = 0V, f = 1MHz$		1.5		$\Omega$
Total Gate Charge <sup>1,2</sup>	$Q_g$	$V_{DS} = 20V, V_{GS} = 10V,$ $I_D = 24A$		47		$nC$
Gate-Source Charge <sup>1,2</sup>	$Q_{gs}$			5.7		
Gate-Drain Charge <sup>1,2</sup>	$Q_{gd}$			14.5		
Turn-On Delay Time <sup>1,2</sup>	$t_{d(on)}$	$V_{DS} = 20V,$ $I_D = 1A, V_{GS} = 10V, R_{GS} = 6\Omega$		10		$nS$
Rise Time <sup>1,2</sup>	$t_r$			15		
Turn-Off Delay Time <sup>1,2</sup>	$t_{d(off)}$			30		
Fall Time <sup>1,2</sup>	$t_f$			20		
<b>SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (<math>T_C = 25\text{ }^\circ\text{C}</math>)</b>						
Continuous Current	$I_S$				55	A
Pulsed Current <sup>3</sup>	$I_{SM}$				150	
Forward Voltage <sup>1</sup>	$V_{SD}$	$I_F = I_S, V_{GS} = 0V$			1.3	V
Reverse Recovery Time	$t_{rr}$	$I_F = 24A, dI_F/dt = 100A / \mu S$		75		nS
Reverse Recovery Charge	$Q_{rr}$			50		nC

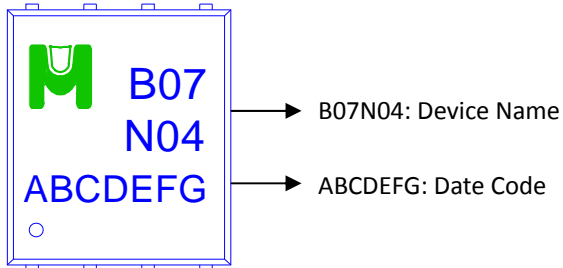
<sup>1</sup>Pulse test : Pulse Width  $\leq 300\text{ }\mu\text{sec}$ , Duty Cycle  $\leq 2\%$ .

<sup>2</sup>Independent of operating temperature.

<sup>3</sup>Pulse width limited by maximum junction temperature.

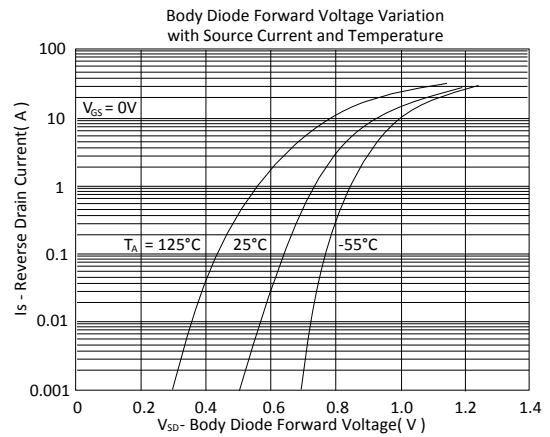
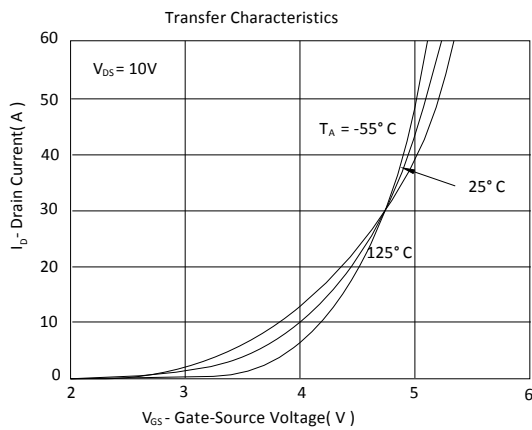
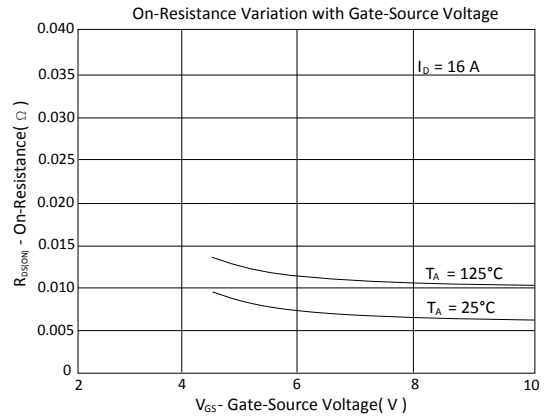
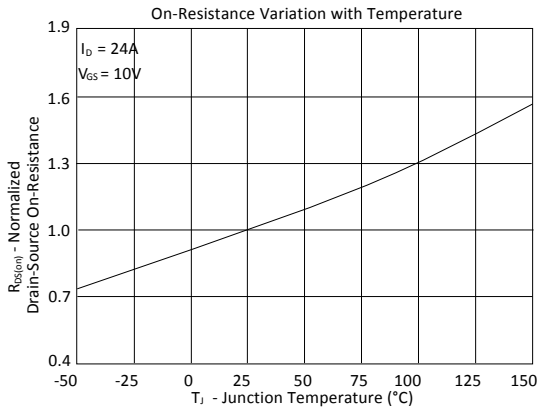
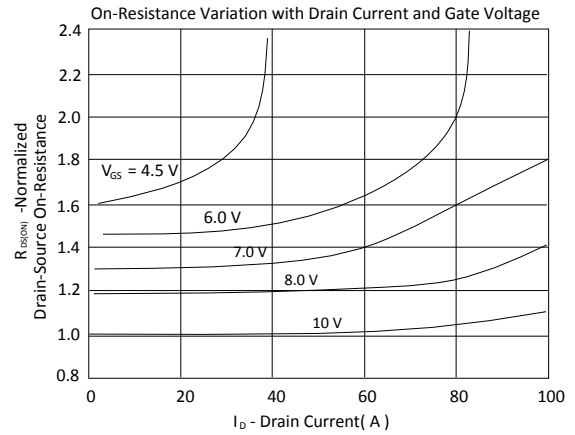
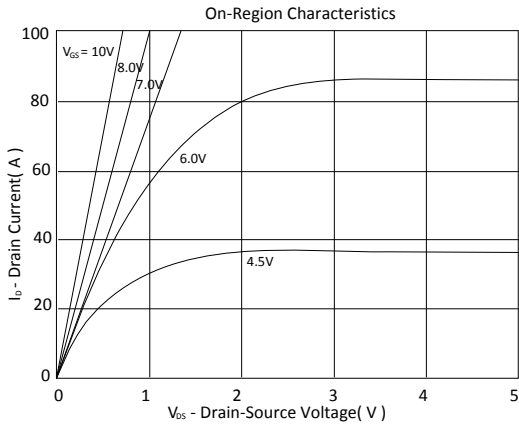
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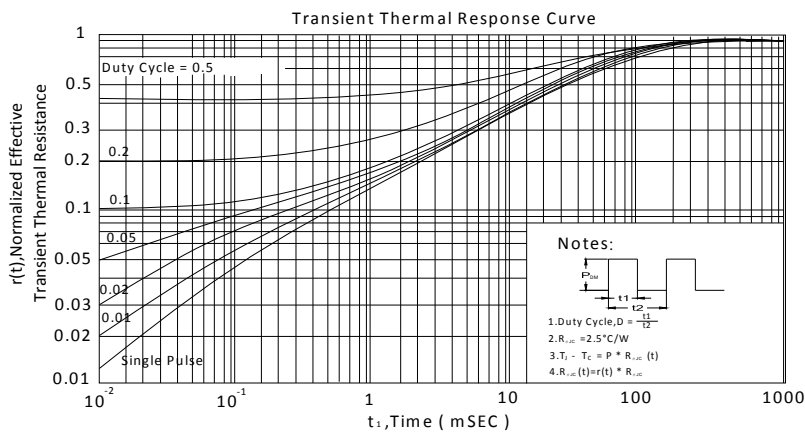
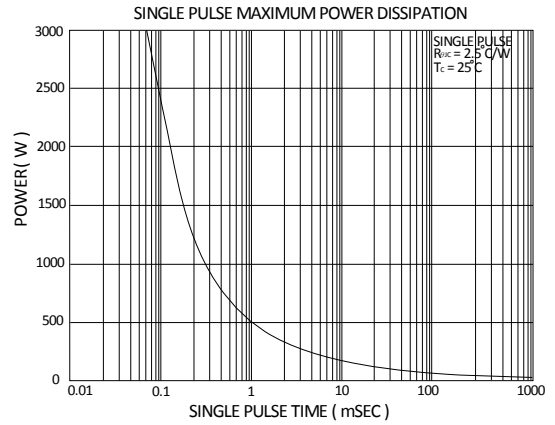
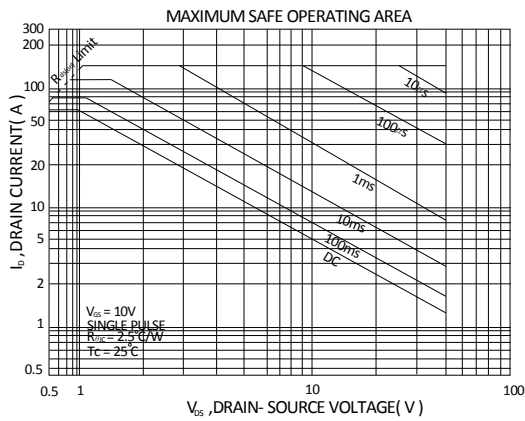
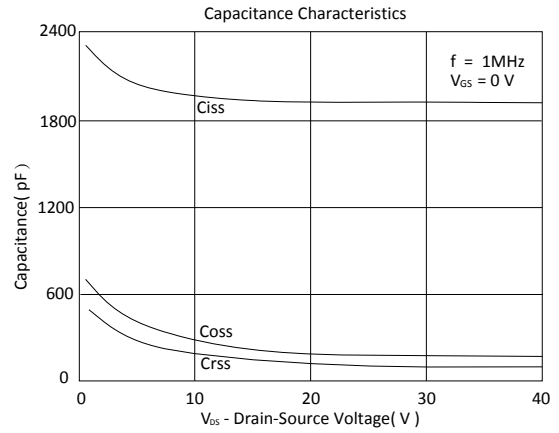
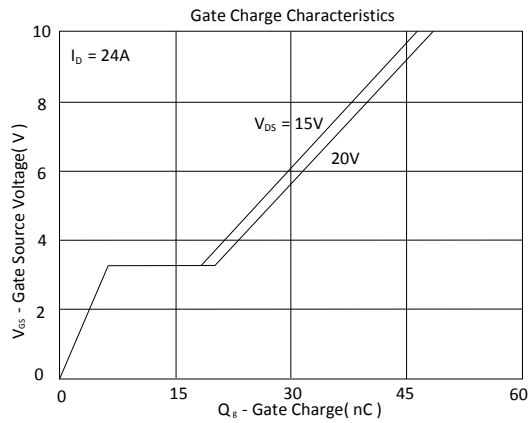
Device Name: EMB07N04H for EDFN 5 x 6





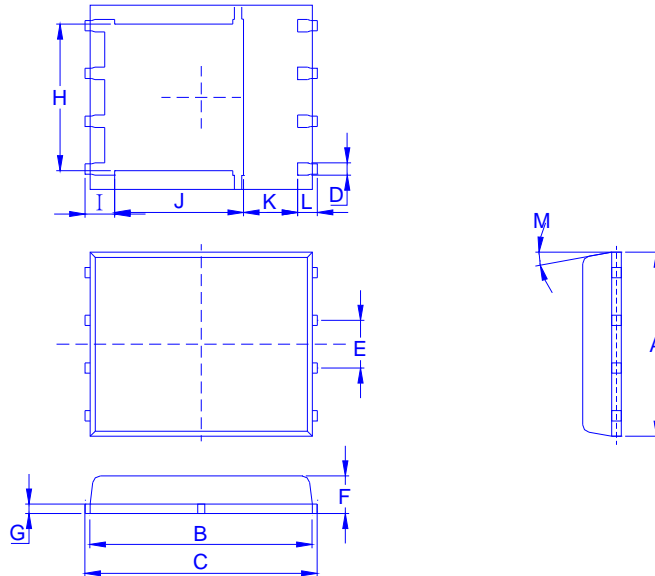
TYPICAL CHARACTERISTICS







Outline Drawing



Dimension in mm

Dimension	A	B	C	D	E	F	G	H	I	J	K	L	M
Min.	4.80	5.50	5.90	0.3		0.85	0.15	3.67	0.41	3.00	0.94	0.45	0°
Typ.					1.27								
Max.	5.30	5.90	6.15	0.51		1.20	0.30	4.54	0.85	3.92	1.7	0.71	12°

Recommended minimum pads

