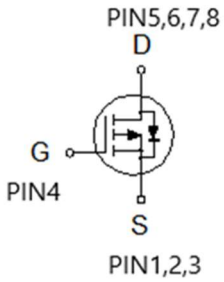
杰力科技股份有限公司
Excelliance MOS Corporation

EMB07P03V

P-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

BV_{DSS}	-30V
$R_{DSON\ (MAX.)}$	7.8mΩ
I_D	-26A



P-Channel MOSFET

UIS, Rg 100% Tested

Pb-Free Lead Plating & Halogen Free

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V_{GS}	±25	V
Continuous Drain Current	T_C = 25 °C	I_D	-26	A
	T_A = 25 °C		-15	
	T_C = 100 °C		-19	
Pulsed Drain Current[1]		I_{DM}	-100	
Avalanche Current		I_{AS}	-26	
Avalanche Energy	L = 0.1mH, I_{AS}=-26A, RG=25Ω	E_{AS}	33.8	mJ
Repetitive Avalanche Energy[2]	L = 0.05mH	E_{AR}	16.9	
Power Dissipation	T_C = 25 °C	P_D	21	W
	T_C = 100 °C		8.3	
Power Dissipation	T_A = 25 °C	P_D	2.5	W
	T_A = 100 °C		1	
Operating Junction & Storage Temperature Range		T_j, T_{stg}	-55 to 150	°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	$R_{\theta JC}$		6	°C / W
Junction-to-Ambient[3]	$R_{\theta JA}$		50	

[1]Pulse width limited by maximum junction temperature.

[2]Duty cycle ≤ 1%

[3]50°C / W when mounted on a 1 in^2 pad of 2 oz copper.

ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = -250μA	-30			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -250μA	-1	-1.5	-3	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0V, V_{GS} = ±20V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -24V, V_{GS} = 0V			-1	μA
		V_{DS} = -20V, V_{GS} = 0V, T_J = 125 °C			-10	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = -5V, V_{GS} = -10V	-26			A
Drain-Source On-State Resistance[1]	$R_{DS(ON)}$	V_{GS} = -10V, I_D = -15A		6.9	7.8	mΩ
		V_{GS} = -4.5V, I_D = -10A		8.5	11.5	
Forward Transconductance[1]	g_{fs}	V_{DS} = -5V, I_D = -15A		24		S
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS} = 0V, V_{DS} = -15V, f = 1MHz		4294		pF
Output Capacitance	C_{oss}			634		
Reverse Transfer Capacitance	C_{rss}			566		
Gate Resistance	R_g	V_{GS} = 15mV, V_{DS} = 0V, f = 1MHz		3.0		Ω
Total Gate Charge[1,2]	Q_g	V_{DS} = -15V, V_{GS} = -10V, I_D = -15A		62.4		nC
Gate-Source Charge[1,2]	Q_{gs}			8.5		
Gate-Drain Charge[1,2]	Q_{gd}			13		
Turn-On Delay Time[1,2]	$t_{d(on)}$	V_{DS} = -15V, I_D = -1A, V_{GS} = -10V, R_{GS} = 2.7Ω		18		nS
Rise Time[1,2]	t_r			26		
Turn-Off Delay Time[1,2]	$t_{d(off)}$			22		
Fall Time[1,2]	t_f			75		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25 °C)						
Continuous Current	I_S				-26	A
Pulsed Current[3]	I_{SM}				-100	
Forward Voltage[1]	V_{SD}	I_F = -15A, V_{GS} = 0V			-1.2	V
Reverse Recovery Time	t_{rr}	I_F = I_S, dI_F/dt = 100A / μS		55		nS
Reverse Recovery Charge	Q_{rr}			62		nC

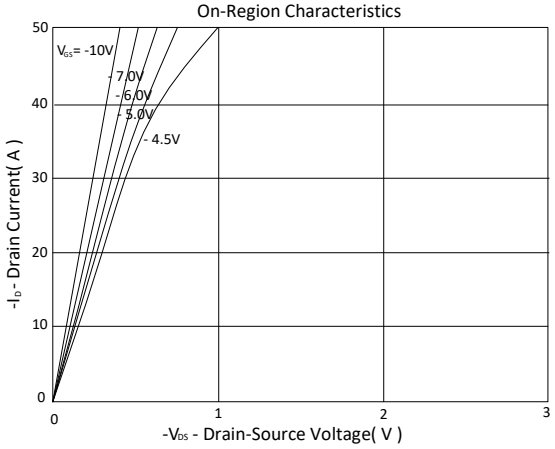
[1]Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.

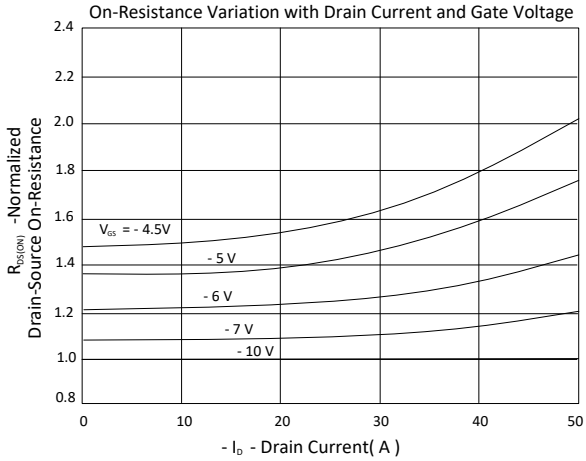
[2]Independent of operating temperature.

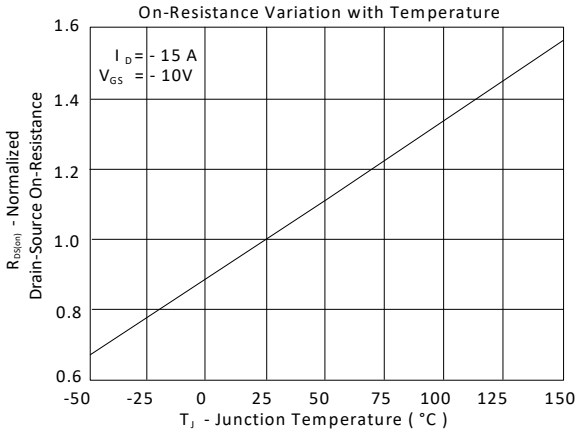
[3]Pulse width limited by maximum junction temperature.

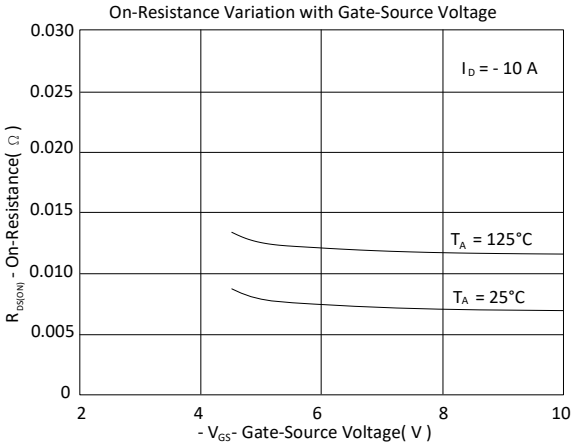
EMC will review datasheet by quarter, and update new version.

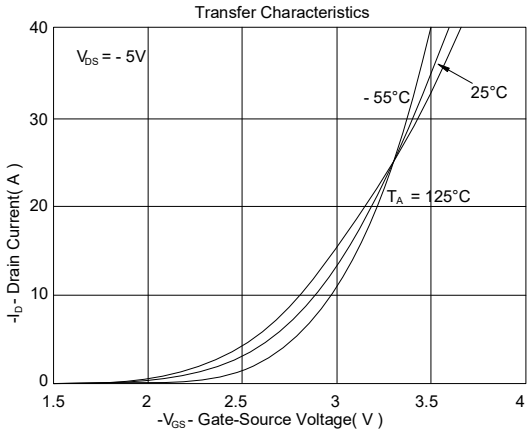
TYPICAL CHARACTERISTICS

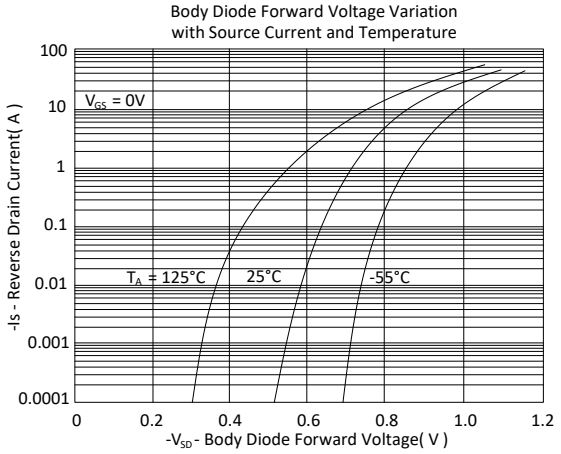




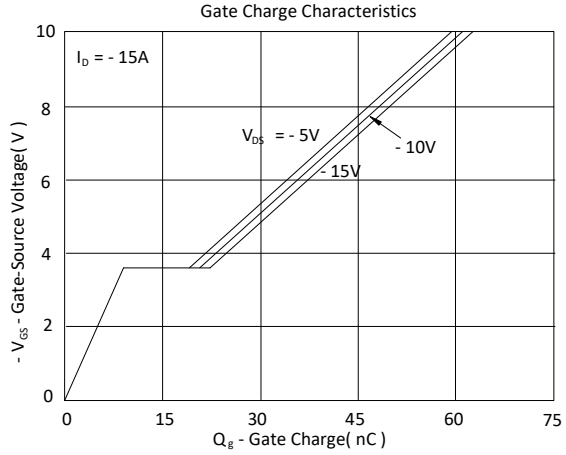




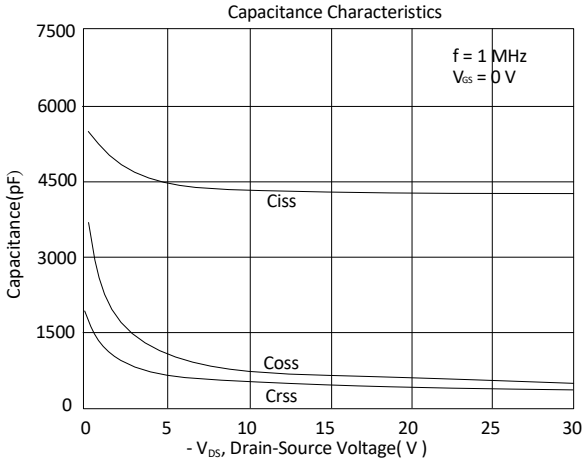




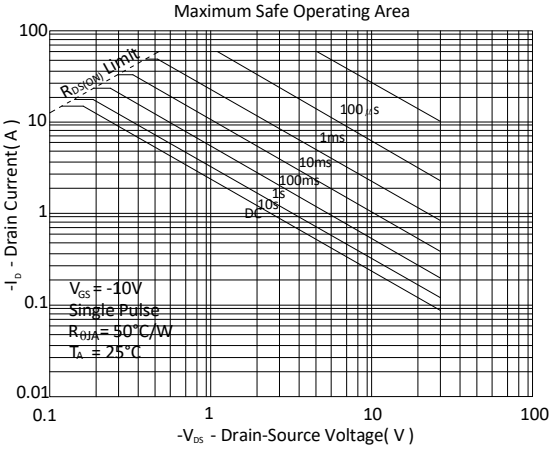
Gate Charge Characteristics



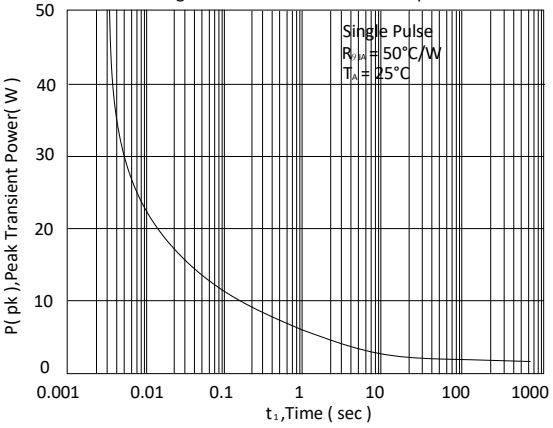
Capacitance Characteristics



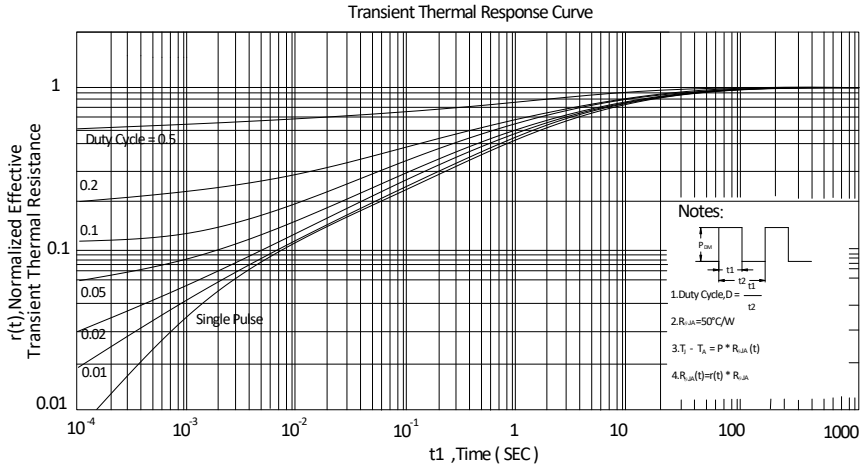
Maximum Safe Operating Area



Single Pulse Maximum Power Dissipation

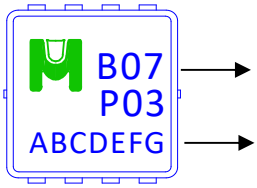


Transient Thermal Response Curve



Ordering & Marking Information:

Device Name: EMB07P03V for EDFN 3 x 3



B07P03: Device Name

ABCDEFG: Date Code

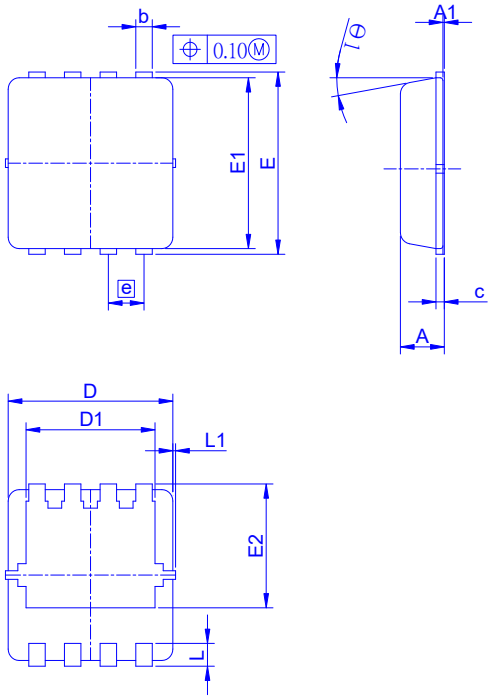
A: Assembly House

B: Year(A:2008 B:2009 C:2010….)

C: Month(A:01 B:02 C:03 D:04 E:05 F:06 G:07 H:08 I:09 J:10 K:11 L:12)

DEFG: Serial No.

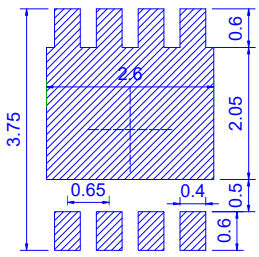
Outline Drawing



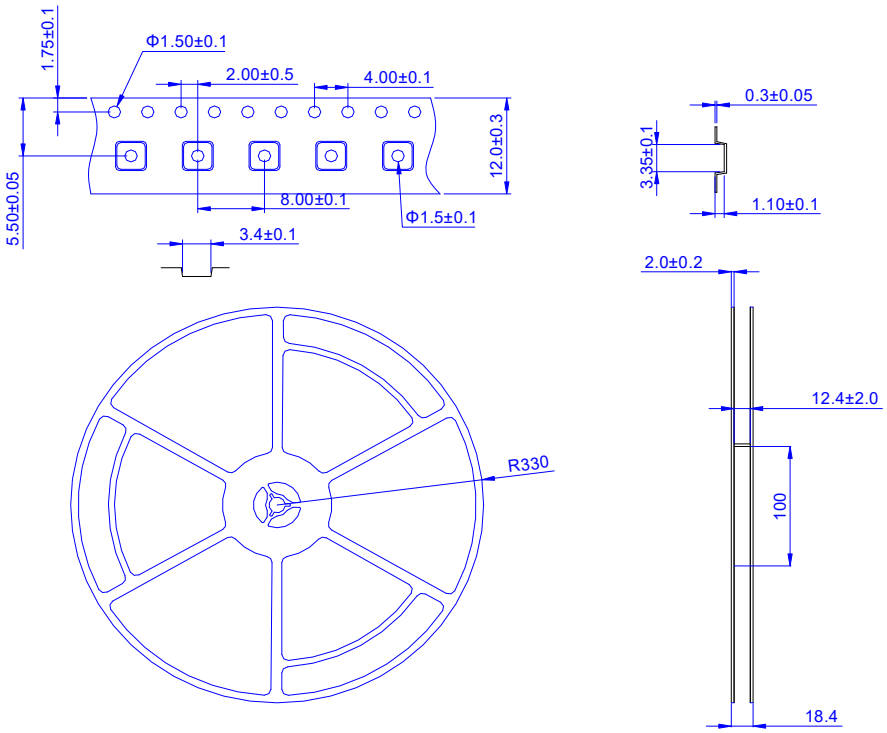
Dimension in mm

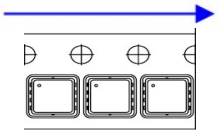
Dimension	A	A1	b	c	D	D1	E	E1	E2	e	L	L1	Θ1
Min.	0.65	0	0.20	0.10	2.90	2.15	3.10	2.90	1.53	0.55	0.25	-	0°
Typ.	0.75	-	0.30	0.15	3.00	2.45	3.20	3.00	1.97	0.65	0.40	0.075	10°
Max.	0.90	0.05	0.40	0.25	3.30	2.74	3.50	3.30	2.59	0.75	0.60	0.150	14°

Recommended minimum pads



Tape&Reel Information: 5000pcs/Reel



產品別	EDFN3X3
Reel 尺寸	13”
編帶方式	FEED DIRECTION 
前空格	50
後空格	50
裝箱數	
滿捲數量	5K
捲/內盒比	1 : 1
內盒滿箱數	5K
內/外箱比	10 : 1
外箱滿箱數	50K