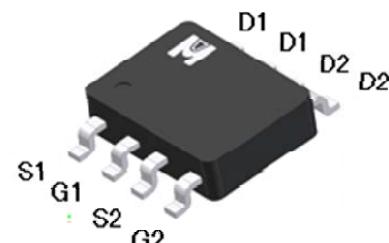
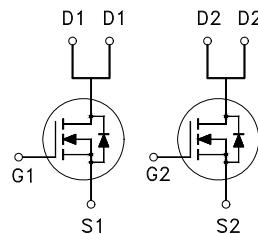




N-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

	N-CH-Q1	N-CH-Q2
BV _{DSS}	40V	40V
R _{DSON} (MAX.)	17.5mΩ	8.8mΩ
I _D	7.4A	10.5A



UIS, Rg 100% Tested

Pb-Free Lead Plating & Halogen Free



ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS		UNIT
			Q1	Q2	
Gate-Source Voltage		V _{GS}	±20	±20	V
Continuous Drain Current	T _A = 25 °C	I _D	7.4	10.5	A
	T _A = 70 °C		5.6	8.4	
Pulsed Drain Current ¹		I _{DM}	30	42	
Avalanche Current		I _{AS}	7.5	10.5	
Avalanche Energy	L = 0.1mH, RG=25Ω	E _{AS}	2.8	5.5	mJ
Repetitive Avalanche Energy ²	L = 0.05mH	E _{AR}	1.4	2.7	
Power Dissipation	T _A = 25 °C	P _D	2		W
	T _A = 100 °C		0.8		
Operating Junction & Storage Temperature Range		T _j , T _{stg}	-55 to 150		°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	R _{θJC}		25	°C / W
Junction-to-Ambient ³	R _{θJA}		62.5	

¹Pulse width limited by maximum junction temperature.

²Duty cycle ≤ 1%

³62.5°C / W when mounted on a 1 in² pad of 2 oz copper.

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(\text{BR})\text{DSS}}$	$V_{GS} = 0V, I_D = 250\mu\text{A}$	Q1	40		V
			Q2	40		
Gate Threshold Voltage	$V_{GS(\text{th})}$	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$	Q1	1	1.7	3
			Q2	1	1.7	3
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0V, V_{GS} = \pm 20V$	Q1			± 100
			Q2			± 100
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 32V, V_{GS} = 0V$	Q1		1	μA
			Q2		1	
		$V_{DS} = 30V, V_{GS} = 0V, T_J = 125^\circ\text{C}$	Q1		25	
			Q2		25	
On-State Drain Current ¹	$I_{D(\text{ON})}$	$V_{DS} = 10V, V_{GS} = 10V$	Q1	7.4		A
			Q2	10.5		
Drain-Source On-State Resistance ¹	$R_{DS(\text{ON})}$	$V_{GS} = 10V, I_D = 6A$	Q1		15.5	17.5
		$V_{GS} = 10V, I_D = 10A$	Q2		8.0	8.8
		$V_{GS} = 4.5V, I_D = 4A$	Q1		22	32
		$V_{GS} = 4.5V, I_D = 8A$	Q2		11	15
Forward Transconductance ¹	g_{fs}	$V_{DS} = 5V, I_D = 6A$	Q1		15	S
		$V_{DS} = 5V, I_D = 10A$	Q2		18	
DYNAMIC						
Input Capacitance	C_{iss}	$V_{GS} = 0V, V_{DS} = 20V, f = 1\text{MHz}$	Q1		707	pF
			Q2		1962	
Output Capacitance	C_{oss}		Q1		98	
			Q2		245	
Reverse Transfer Capacitance	C_{rss}		Q1		81	
			Q2		225	
Gate Resistance	R_g	$V_{GS} = 15\text{mV}, V_{DS} = 0V, f = 1\text{MHz}$	Q1		1.5	Ω
			Q2		1.4	

Total Gate Charge ^{1,2}	$Q_g(V_{GS}=10V)$	$V_{DD} = 20V, V_{GS} = 10V,$ $I_D = 6A$ Q_2 $V_{DD} = 20V, V_{GS} = 10V,$ $I_D = 10A$	Q1		18		nC
	$Q_g(V_{GS}=4.5V)$		Q2		47		
Gate-Source Charge ^{1,2}	Q_{gs}	$V_{DD} = 20V, V_{GS} = 10V,$ $I_D = 10A$	Q1		10		
Gate-Drain Charge ^{1,2}	Q_{gd}		Q2		24		
Turn-On Delay Time ^{1,2}	$t_{d(on)}$		Q1		2.4		
Rise Time ^{1,2}	t_r		Q2		6.8		
Turn-Off Delay Time ^{1,2}	$t_{d(off)}$	$V_{DD} = 20V,$ $I_D = 1A, V_{GS} = 10V, R_{GS} = 2.7\Omega$	Q1		6.0		nS
Fall Time ^{1,2}	t_f		Q2		16		

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS ($T_c = 25^\circ C$)

Continuous Current	I_S	$I_F = 6A, V_{GS} = 0V$ $I_F = 10A, V_{GS} = 0V$	Q1		7.5	A	
Pulsed Current ³	I_{SM}		Q2		10.5		
Forward Voltage ¹	V_{SD}		Q1		30	V	
			Q2		42		
Reverse Recovery Time	t_{rr}	$I_F = 6A, dI_F/dt = 100A/\mu S$	Q1		1.3	nS	
			Q2		1.3		
		$I_F = 10A, dI_F/dt = 100A/\mu S$	Q1		18		
			Q2		22		
Reverse Recovery Charge	Q_{rr}	Q1		5		nC	
		Q2		6			

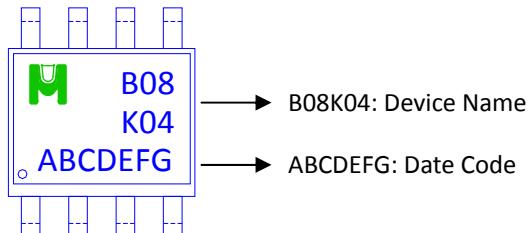
¹Pulse test : Pulse Width $\leq 300 \mu sec$, Duty Cycle $\leq 2\%$.

²Independent of operating temperature.

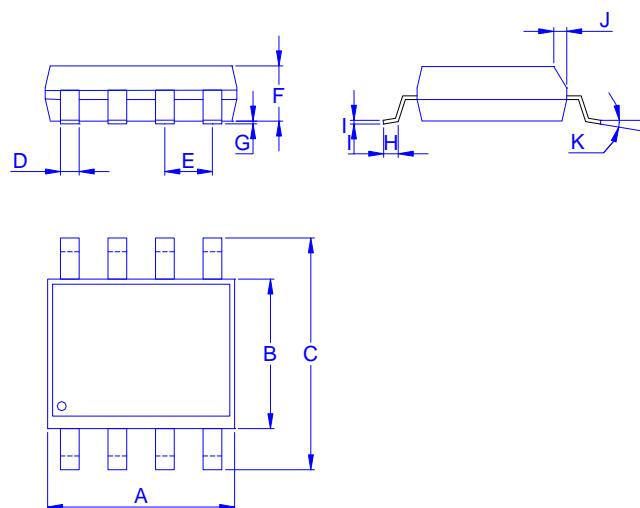
³Pulse width limited by maximum junction temperature.

Ordering & Marking Information:

Device Name: EMB08K04G for SOP-8



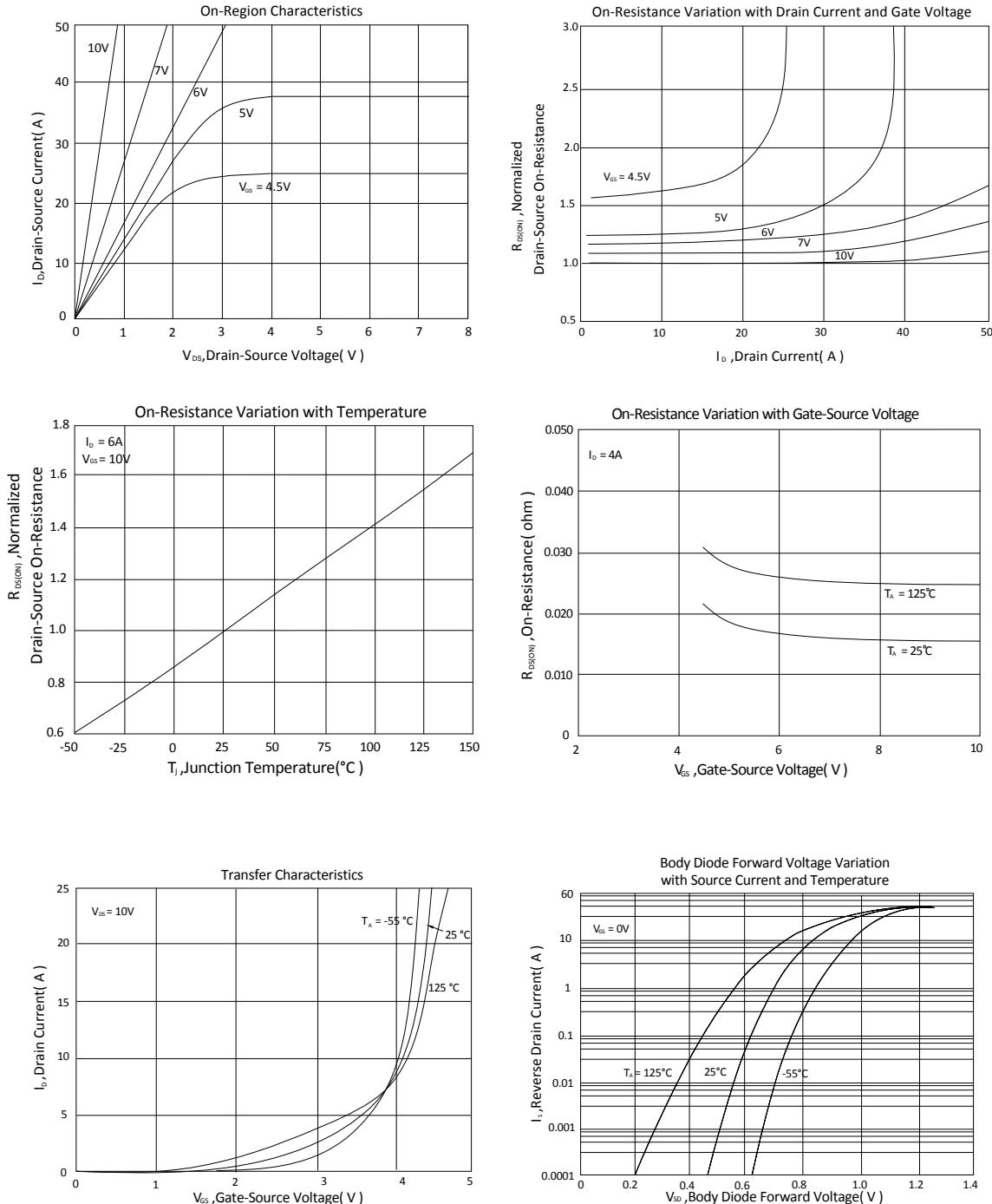
Outline Drawing

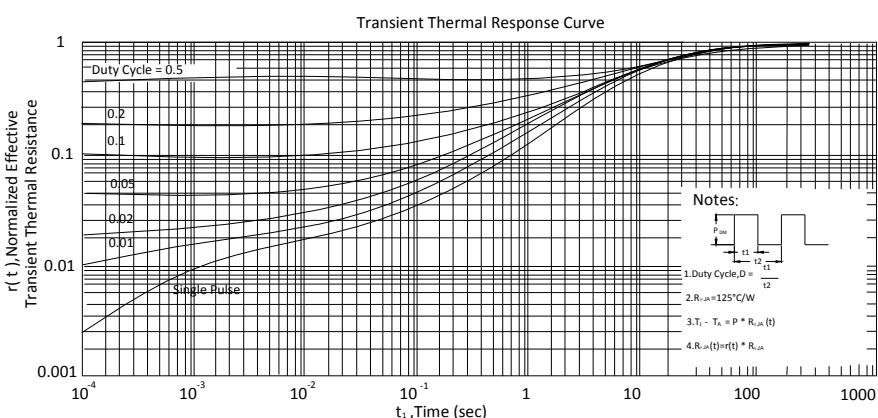
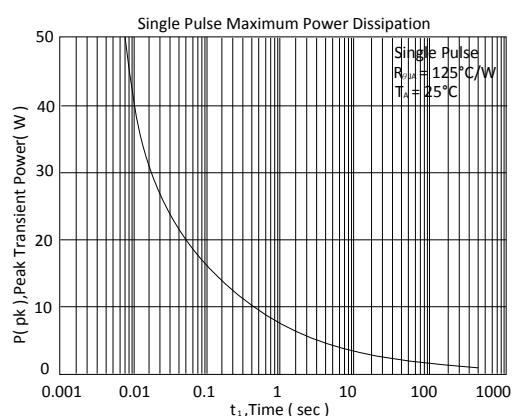
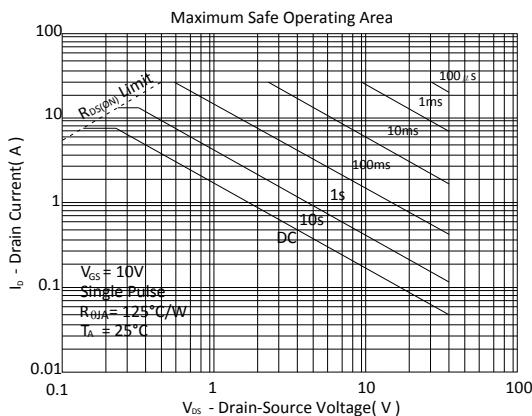
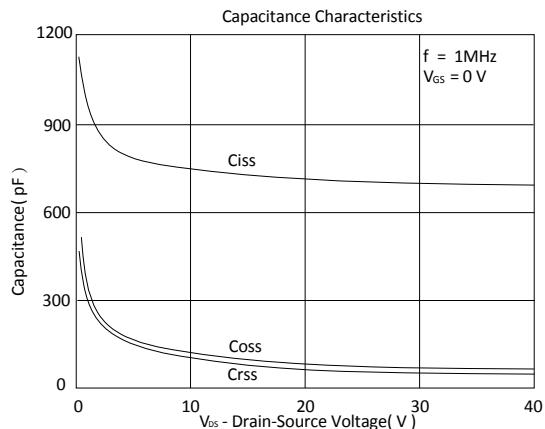
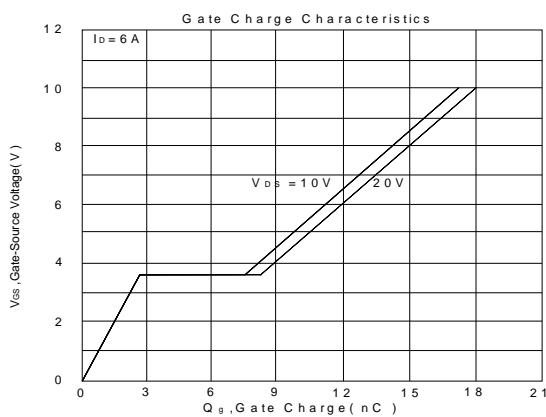


Dimension in mm

Dimension	A	B	C	D	E	F	G	H	I	J	K
Min.	4.70	3.70	5.80	0.33		1.20	0.08	0.40	0.19	0.25	0°
Typ.					1.27						
Max.	5.10	4.10	6.20	0.51		1.62	0.28	0.83	0.26	0.50	8°

Q1 TYPICAL CHARACTERISTICS





Q2 TYPICAL CHARACTERISTICS

