杰力科技股份有限公司
Excelliance MOS Corporation

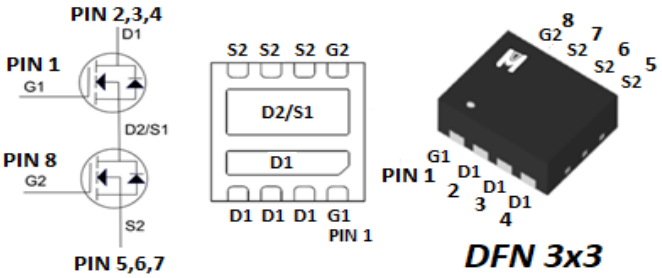
EMB09K03VP

Dual N-Channel Logic Level Enhancement Mode Field Effect Transistor

▪Product Summary:

	Q1	Q2
BVDSS	30V	30V
$R_{DSON\ (MAX.)}$@V_{GS}=10V	20.0mΩ	9.0mΩ
$R_{DSON\ (MAX.)}$@V_{GS}=4.5V	30.0mΩ	15.0mΩ
I_D @T_C=25°C	32.0A	49.0A
I_D @T_A=25°C	8.0A	13.0A

▪ Pin Description:



Dual N Channel MOSFET
UIS, Rg 100% Tested
Pb-Free Lead Plating & Halogen Free

▪ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS Q1	LIMITS Q2	UNIT
Gate-Source Voltage		V_{GS}	±20	±20	V
Continuous Drain Current	T_C = 25 °C	I_D	32	49	A
	T_C = 100 °C		20	31	
Continuous Drain Current	T_A = 25 °C	I_D	8	13	
	T_A = 70 °C		6	10	
Pulsed Drain Current[1]		I_{DM}	85	127	
Avalanche Current		I_{AS}	16	21	
Avalanche Energy	L = 0.1mH	EAS	12.8	22.1	mJ
Repetitive Avalanche Energy[2]	L = 0.05mH	EAR	6.4	11.0	
Power Dissipation	T_C = 25 °C	P_D	35.7	35.7	W
	T_C = 100 °C		14.3	14.3	
Power Dissipation	T_A = 25 °C	P_D	2.5	2.5	W
	T_A = 70 °C		1.6	1.6	
Operating Junction & Storage Temperature Range		T_j, T_{stg}	-55 to 150		°C

▪THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE		SYMBOL	TYPICAL	MAXIMUM Q1	MAXIMUM Q2	UNIT
Junction-to-Case		$R_{\theta JC}$		3.5	3.5	°C/W
Junction-to-Ambient[3]	t≦10s	$R_{\theta JA}$		50	50	
	Steady-State	$R_{\theta JA}$		90	90	

[1]Pulse width limited by maximum junction temperature.
[2]Duty cycle < 1%
[3]90°C / W when mounted on a 1 in^2 pad of 2 oz copper.
[4]Guarantee by Engineering test

▪ **Q1_ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)**

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage[4]	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = 250uA	30			V
Gate Threshold Voltage[4]	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250uA	1	1.6	3	V
Gate-Body Leakage[4]	I_{GSS}	V_{DS} = 0V, V_{GS} = ±20V			±100	nA
Zero Gate Voltage Drain Current[4]	I_{DSS}	V_{DS} = 24V, V_{GS} = 0V			1	uA
		V_{DS} =20V, V_{GS} =0V, T_J =125 °C			25	uA
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 10V, V_{GS} = 10V	32			A
Drain-Source On-State Resistance[1,4]	$R_{DS(ON)}$	V_{GS} = 10V, I_D = 8A		12.5	20	mΩ
		V_{GS} = 4.5V, I_D = 5A		18.9	30	mΩ
Forward Transconductance[1]	g_{fs}	V_{DS} = 5V, I_D = 5A		15		S
DYNAMIC						
Input Capacitance[5]	C_{iss}	V_{GS} = 0V, V_{DS} = 15V, f = 1MHz		401		pF
Output Capacitance[5]	C_{oss}			73		pF
Reverse Transfer Capacitance[5]	C_{rss}			60		pF
Gate Resistance[4,5]	R_g	f = 1MHz		1.5		Ω
Total Gate Charge[1,2,5]	Q_g(V_{GS}=10V)	V_{DS} = 15V, V_{GS} = 10V, I_D = 8A		8.9		nC
	Q_g(V_{GS}=4.5V)			4.9		nC
Gate-Source Charge[1,2,5]	Q_{gs}			1.3		nC
Gate-Drain Charge[1,2,5]	Q_{gd}			2.6		nC
Turn-On Delay Time[1,2,5]	$t_{d(on)}$	V_{DS} = 15V, V_{GS} = 10V, I_D = 5A , Rg = 6Ω		4.9		nS
Rise Time[1,2,5]	t_r			11.0		nS
Turn-Off Delay Time[1,2,5]	$t_{d(off)}$			13.0		nS
Fall Time[1,2,5]	t_f			12.8		nS
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS						
Continuous Current	I_S				32	A
Pulsed Current[3]	I_{SM}				85	A
Forward Voltage[1,4]	V_{SD}	I_F = 10A, V_{GS} = 0V			1.3	V
Reverse Recovery Time[5]	t_{rr}	I_F = 10A, dI_F/dt = 400A / uS		8.0		nS
Reverse Recovery Charge[5]	Q_{rr}			9.8		nC

[1]Pulse test : Pulse Width ≦ 300 usec, Duty Cycle ≦ 2%.

[2]Independent of operating temperature.

[3]Pulse width limited by maximum junction temperature.

[4]Guarantee by FT test Item

[5]Guarantee by Engineering test

EMC will review datasheet by quarter, and update new version.

▪ Q1_TYPICAL CHARACTERISTICS

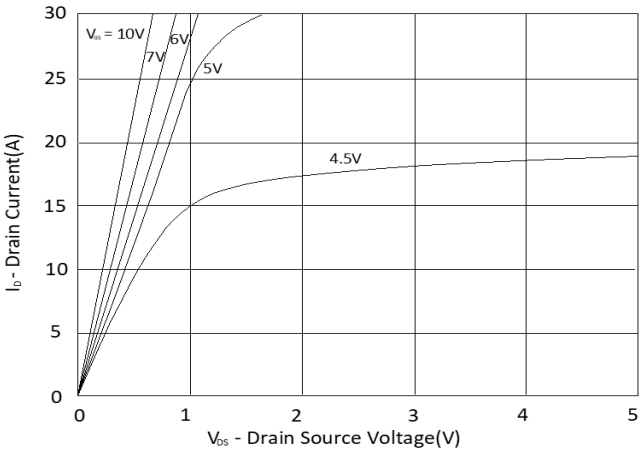


Fig.1 Typical Output Characteristics

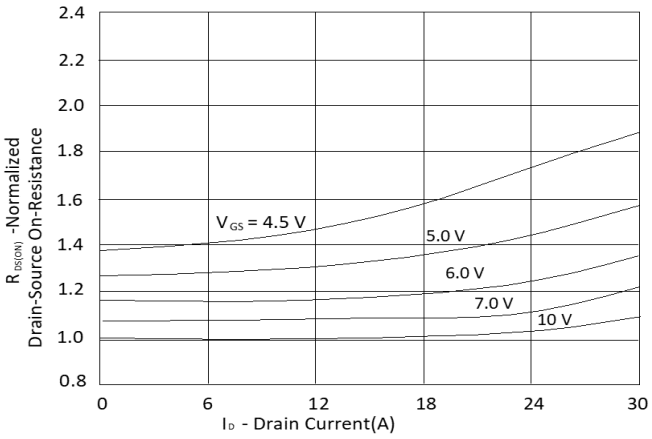


Fig.2 On-Resistance Variation with Drain Current and Gate Voltage

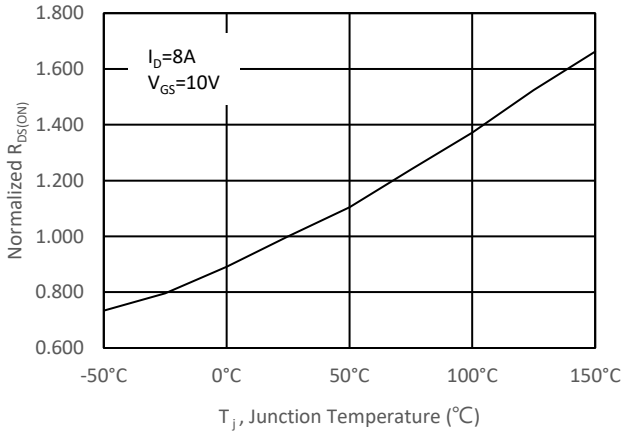


Fig.3 Normalized On-Resistance v.s. Junction Temperature

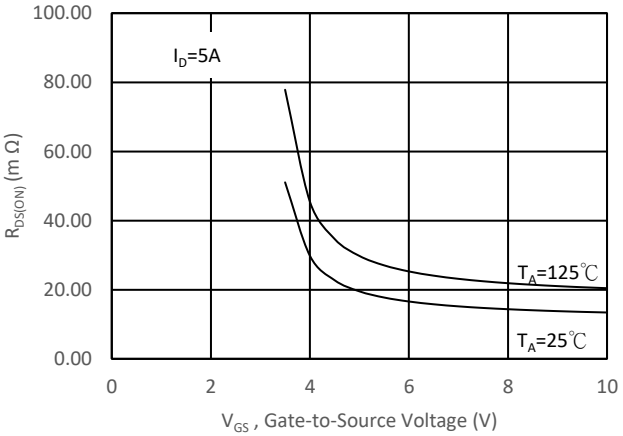


Fig.4 On-Resistance v.s. Gate Voltage

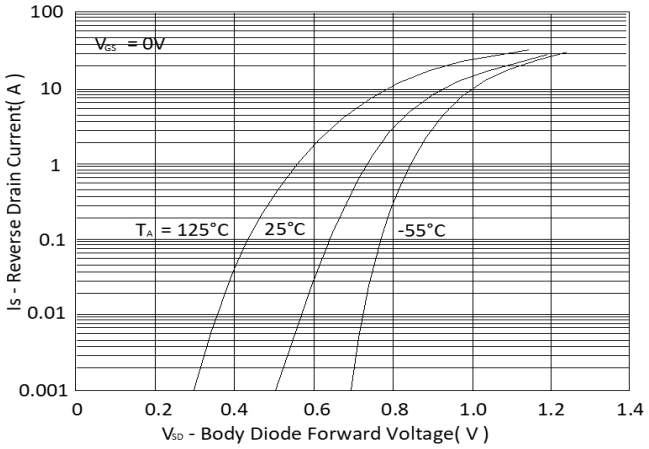


Fig.5 Forward Characteristic of Reverse Diode

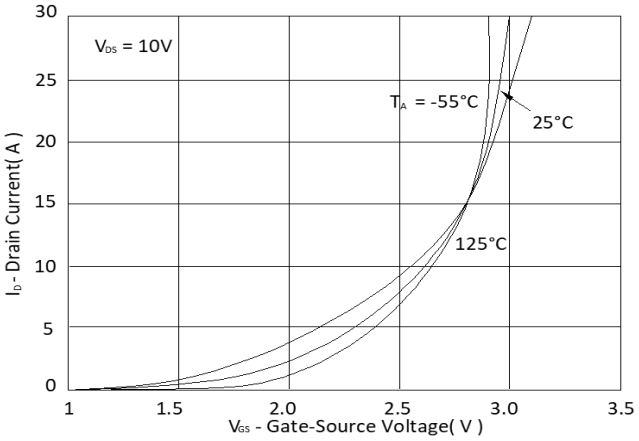


Fig.6 Transfer Characteristics

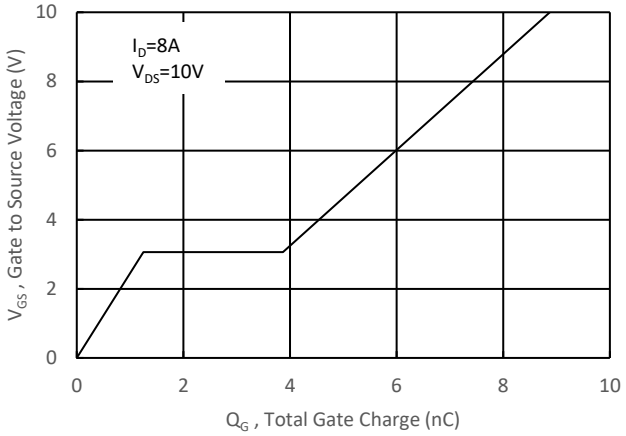


Fig.7 Gate Charge Characteristics

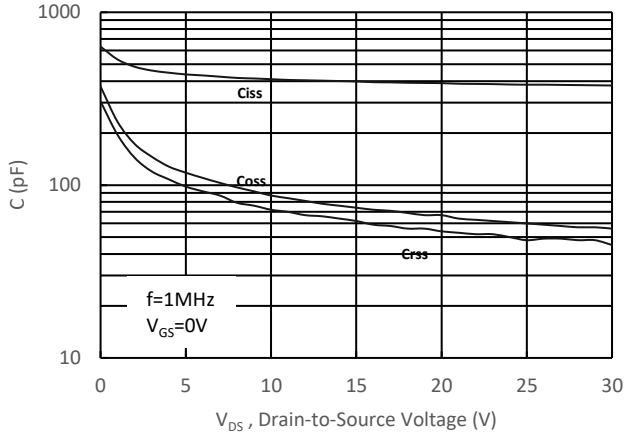


Fig.8 Typical Capacitance Characteristics

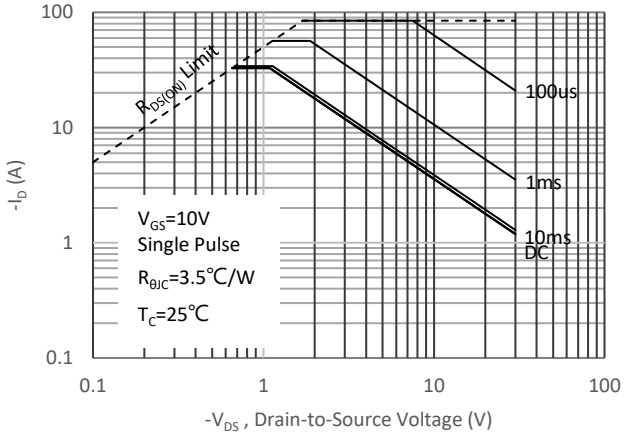


Fig 9. Maximum Safe Operating Area

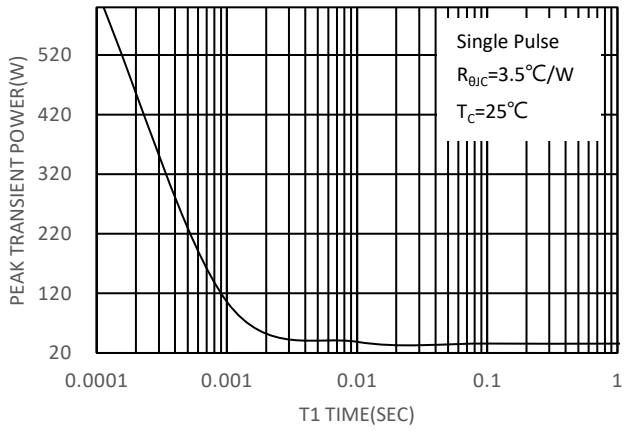


Fig 10. Single Pulse Maximum Power Dissipation

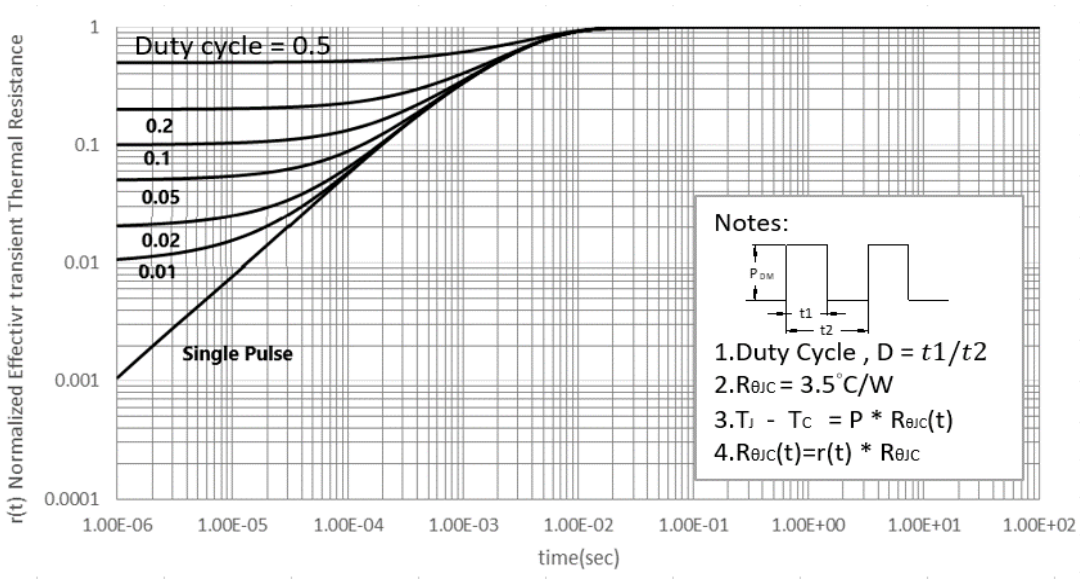


Fig 11. Effective Transient Thermal Impedance

▪ **Q2_ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)**

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage[4]	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = 250uA	30			V
Gate Threshold Voltage[4]	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250uA	1	1.6	3	
Gate-Body Leakage[4]	I_{GSS}	V_{DS} = 0V, V_{GS} = ±20V			±100	nA
Zero Gate Voltage Drain Current[4]	I_{DSS}	V_{DS} = 24V, V_{GS} = 0V			1	uA
		V_{DS} =20V, V_{GS} =0V, T_J =125 °C			25	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 10V, V_{GS} = 10V	49			A
Drain-Source On-State Resistance[1,4]	$R_{DS(ON)}$	V_{GS} = 10V, I_D = 10A		7	9	mΩ
		V_{GS} = 4.5V, I_D = 6A		11	15	
Forward Transconductance[1]	g_{fs}	V_{DS} = 5V, I_D = 6A		18		S
DYNAMIC						
Input Capacitance[5]	C_{iss}	V_{GS} = 0V, V_{DS} = 15V, f = 1MHz		976		pF
Output Capacitance[5]	C_{oss}			150		
Reverse Transfer Capacitance[5]	C_{rss}			99		
Gate Resistance[4,5]	R_g	f = 1MHz		1.4		Ω
Total Gate Charge[1,2,5]	Q_g(V_{GS}=10V)	V_{DS} = 15V, V_{GS} = 10V, I_D = 10A		16.5		nC
	Q_g(V_{GS}=4.5V)			8.5		
Gate-Source Charge[1,2,5]	Q_{gs}			2.1		
Gate-Drain Charge[1,2,5]	Q_{gd}			3.4		
Turn-On Delay Time[1,2,5]	$t_{d(on)}$	V_{DS} = 15V, V_{GS} = 10V, I_D = 5A , Rg = 6Ω		7.0		nS
Rise Time[1,2,5]	t_r			14.8		
Turn-Off Delay Time[1,2,5]	$t_{d(off)}$			13.0		
Fall Time[1,2,5]	t_f			12.8		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS						
Continuous Current	I_S				49	A
Pulsed Current[3]	I_{SM}				127	
Forward Voltage[1,4]	V_{SD}	I_F = 15A, V_{GS} = 0V			1.3	V
Reverse Recovery Time[5]	t_{rr}	I_F = 15A, dI_F/dt = 400A / uS		6.9		nS
Reverse Recovery Charge[5]	Q_{rr}			6.2		nC

[1]Pulse test : Pulse Width ≦ 300 usec, Duty Cycle ≦ 2%.

[2]Independent of operating temperature.

[3]Pulse width limited by maximum junction temperature.

[4]Guarantee by FT test Item

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▪ Q2_TYPICAL CHARACTERISTICS

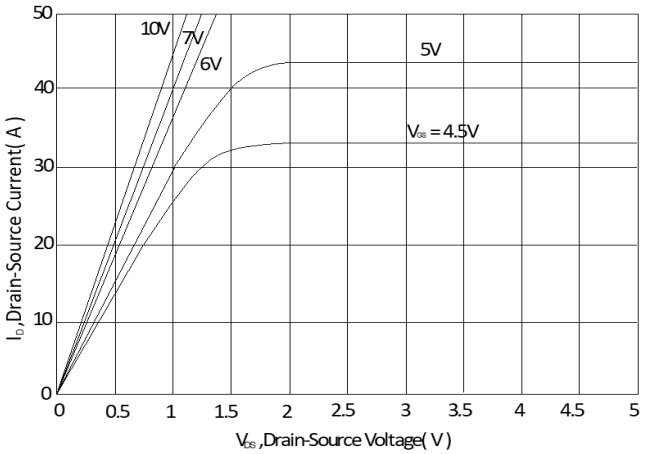


Fig.1 Typical Output Characteristics

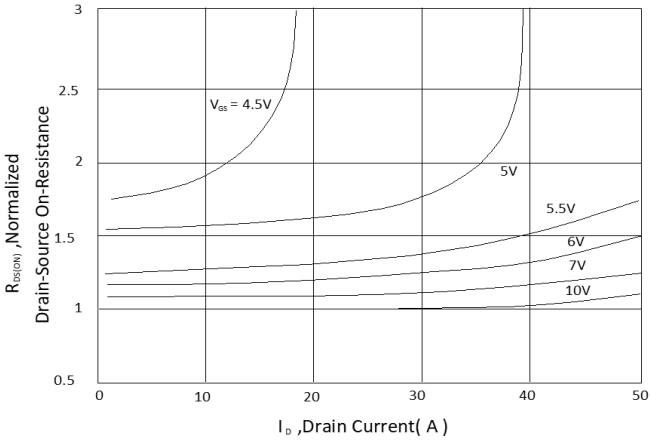


Fig.2 On-Resistance Variation with Drain Current and Gate Voltage

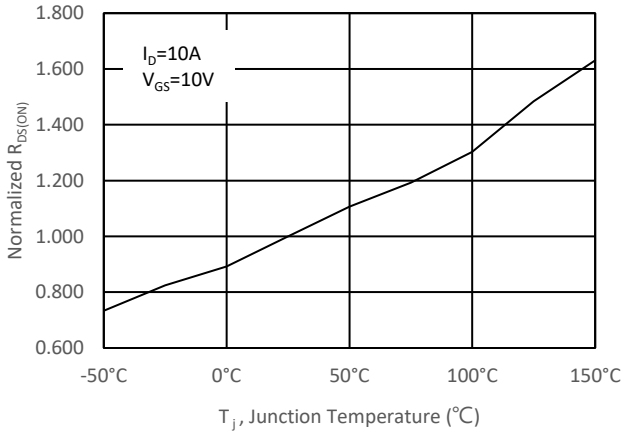


Fig.3 Normalized On-Resistance v.s. Junction Temperature

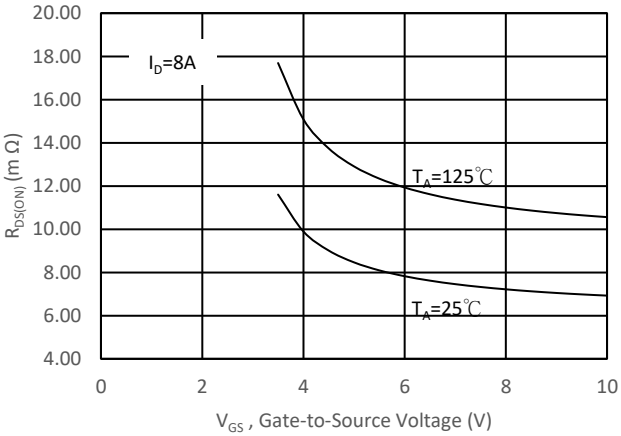


Fig.4 On-Resistance v.s. Gate Voltage

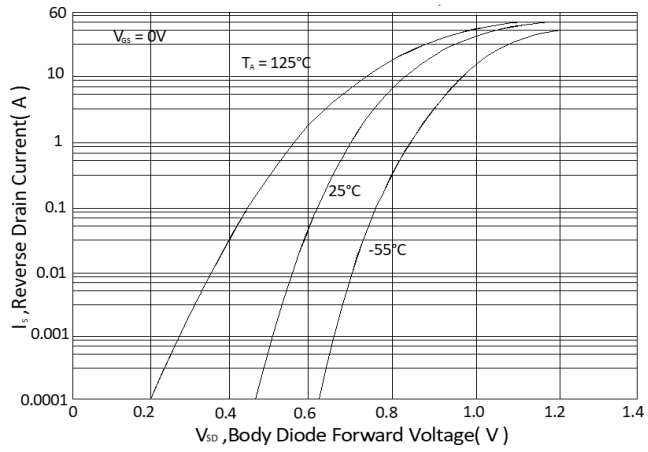


Fig.5 Forward Characteristic of Reverse Diode

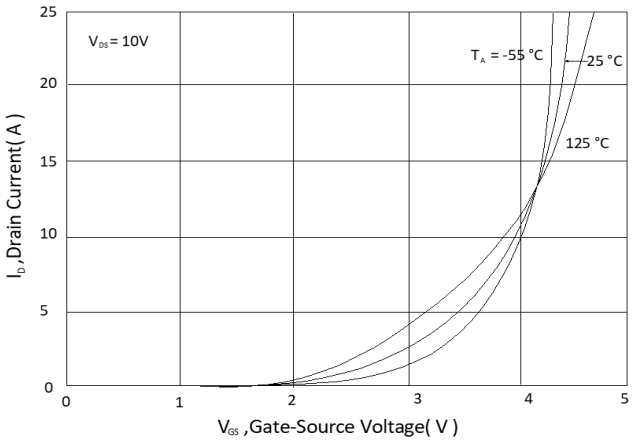


Fig.6 Transfer Characteristics

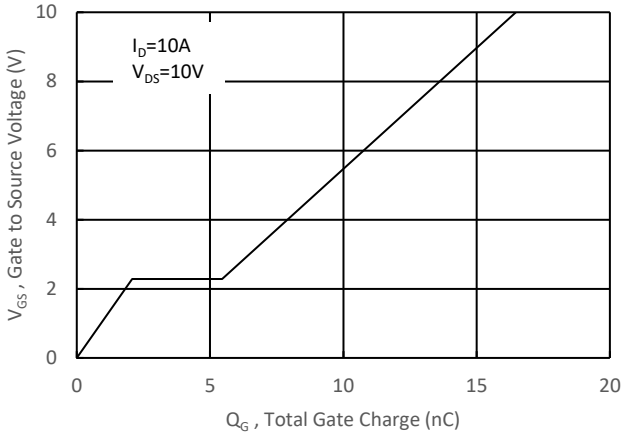


Fig.7 Gate Charge Characteristics

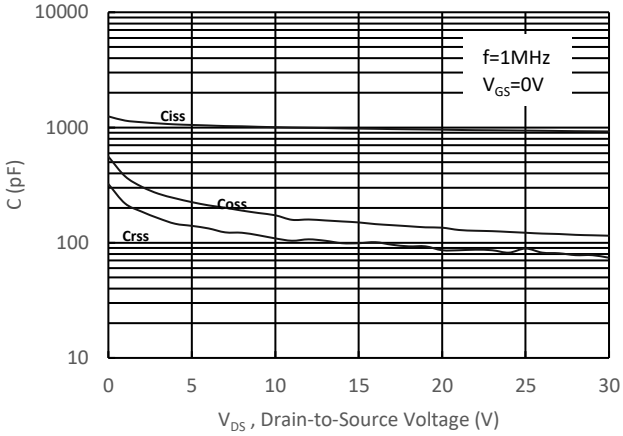


Fig.8 Typical Capacitance Characteristics

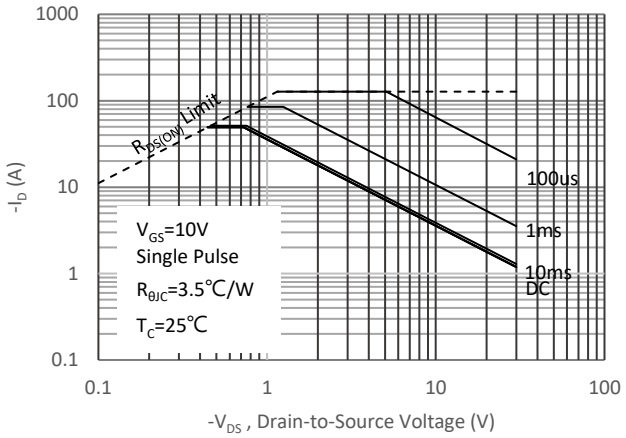


Fig 9. Maximum Safe Operating Area

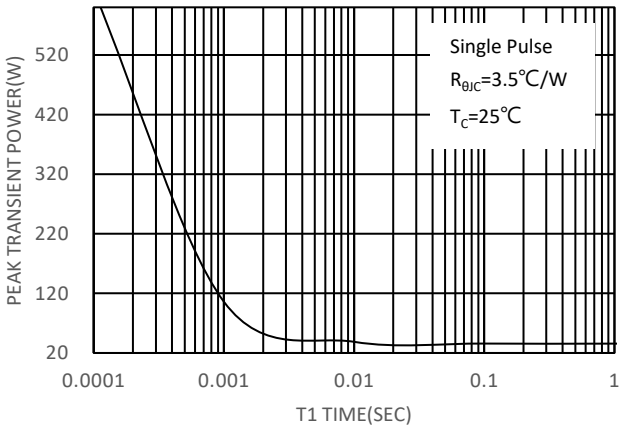


Fig 10. Single Pulse Maximum Power Dissipation

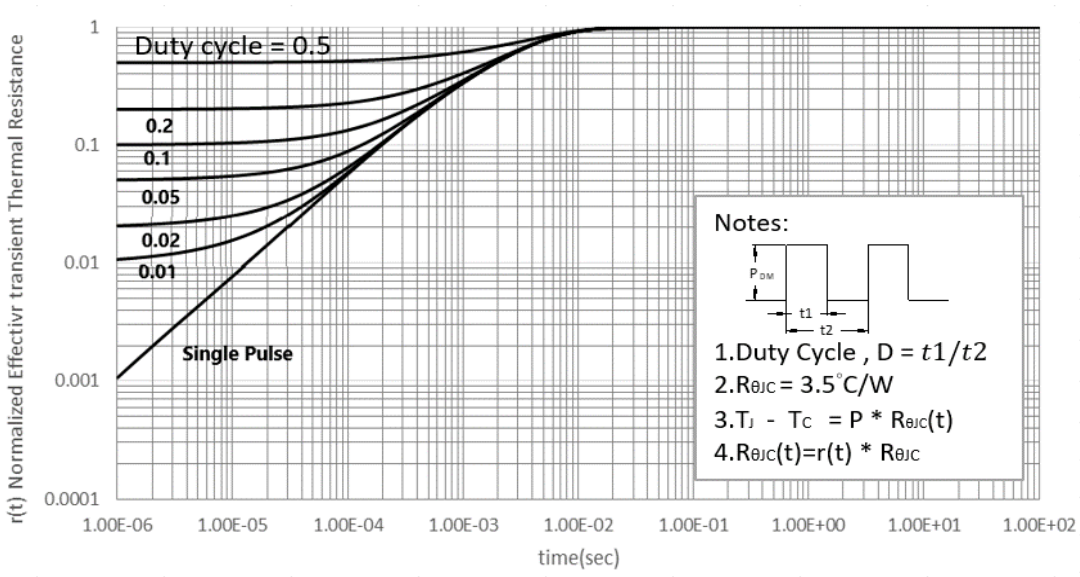


Fig 11. Effective Transient Thermal Impedance

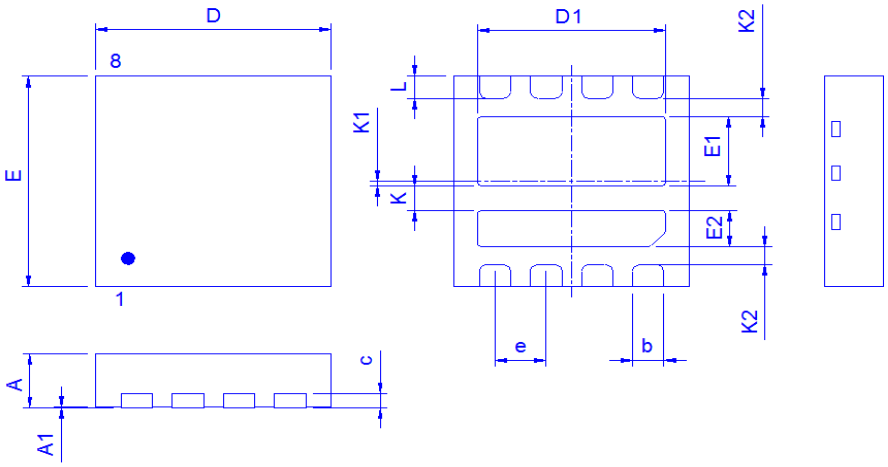
Ordering & Marking Information:

Device Name: EMB09K03VP for Asymmetric Dual DFN3X3

B09K03: Device Name

ABCDEFG: Date Code
A: Assembly House
B: Year(A:2008 B:2009 C:2010….)
C: Month(A:01 B:02 C:03 D:04 E:05 F:06 G:07 H:08 I:09 J:10 K:11 L:12)
DEFG: Serial No.

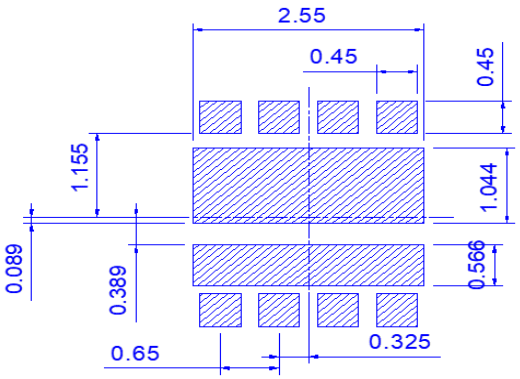
Outline Drawing



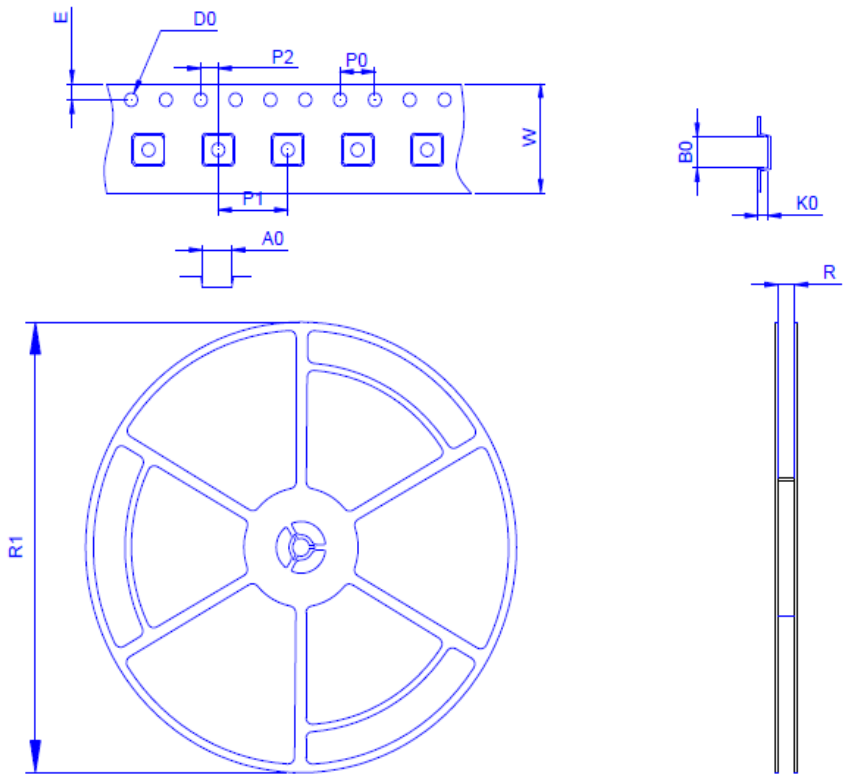
Dimension	A	A1	b	c	D	D1	E	E1	E2	e	L	K	K1
Min.	0.7	0	0.35		2.9	2.3	2.9	0.89	0.42		0.27		
Typ.	0.75		0.4	0.203	3	2.4	3	0.99	0.52	0.65	0.32	0.35	0.06
Max.	0.8	0.05	0.45		3.1	2.5	3.1	1.09	0.62		0.37		

Dimension	K2
Min.	
Typ.	0.25
Max.	

Footprint



◆ **Tape&Reel Information:5000pcs/Reel**



產品別	DFN3*3-8L
Reel 尺寸	13"
編帶方式	FEED DIRECTION

Dimension in mm

Dimension	Carrier tape									Reel	
	A0	B0	D0	E	K0	P0	P1	P2	W	R	R1
Typ.	3.30	3.30	1.50	1.75	1.10	4.00	8.00	2.00	12.00	12.40	330.00
±	0.30	0.20	0.20	0.20	0.40	0.20	0.20	0.20	0.50	REF	REF