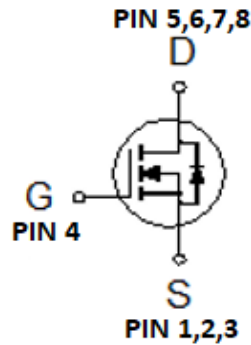


Single N-Channel Logic Level Enhancement Mode Field Effect Transistor

•Product Summary:

	N-CH
BV_{DSS}	30V
$R_{DSON (MAX.)@V_{GS}=10V}$	9.0m Ω
$R_{DSON (MAX.)@V_{GS}=4.5V}$	13.5m Ω
$I_D @T_C=25^\circ C$	44A

• Pin Description:



Single N Channel MOSFET

UIS, Rg 100% Tested

Pb-Free Lead Plating & Halogen Free



• ABSOLUTE MAXIMUM RATINGS ($T_C = 25^\circ C$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current ¹	$T_C = 25^\circ C$	I_D	44	A
	$T_A = 25^\circ C$		12	
	$T_C = 100^\circ C$		44	
Pulsed Drain Current ¹		I_{DM}	127	A
Avalanche Current ^{1,4}		I_{AS}	28	
Avalanche Energy ^{1,4}	$L = 0.1mH$	E_{AS}	39.2	mJ
Repetitive Avalanche Energy ^{2,4}	$L = 0.05mH$	E_{AR}	19.6	
Power Dissipation ¹	$T_C = 25^\circ C$	P_D	83.3	W
	$T_C = 100^\circ C$		33.3	
Power Dissipation ¹	$T_A = 25^\circ C$	P_D	2.3	W
	$T_A = 100^\circ C$		0.9	
Operating Junction & Storage Temperature Range		T_j, T_{stg}	-55 to 150	$^\circ C$

•THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	$R_{\theta JC}$		1.5	$^\circ C / W$
Junction-to-Ambient ³	$R_{\theta JA}$		55	

¹Pulse width limited by maximum junction temperature.

²Duty cycle $\leq 1\%$

³55 $^\circ C / W$ when mounted on a 1 in² pad of 2 oz copper.

⁴Guarantee by Engineering test

▪ ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage ⁴	V _{(BR)DSS}	V _{GS} = 0V, I _D = 250uA	30			V
Gate Threshold Voltage ⁴	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250uA	1.2	1.8	2.5	
Gate-Body Leakage ⁴	I _{GSS}	V _{DS} = 0V, V _{GS} = ±20V			±100	nA
Zero Gate Voltage Drain Current ⁴	I _{DSS}	V _{DS} = 30V, V _{GS} = 0V			1	uA
		V _{DS} = 30V, V _{GS} = 0V, T _J = 125 °C			25	
On-State Drain Current ¹	I _{D(ON)}	V _{DS} = 10V, V _{GS} = 10V	44			A
Drain-Source On-State Resistance ^{1,4}	R _{DS(ON)}	V _{GS} = 10V, I _D = 12A		7.5	9	mΩ
		V _{GS} = 4.5V, I _D = 8A		10	13.5	
Forward Transconductance ¹	g _{fs}	V _{DS} = 5V, I _D = 12A		20		S
DYNAMIC						
Input Capacitance ⁵	C _{iss}	V _{GS} = 0V, V _{DS} = 15V, f = 1MHz		890		pF
Output Capacitance ⁵	C _{oss}			130		
Reverse Transfer Capacitance ⁵	C _{rss}			90		
Gate Resistance ^{4,5}	R _g	V _{GS} = 15mV, V _{DS} = 0V, f = 1MHz		3.3	5.3	Ω
Total Gate Charge ^{1,2,5}	Q _g (V _{GS} =10V)	V _{DS} = 15V, V _{GS} = 10V, I _D = 12A		15.6		nC
	Q _g (V _{GS} =4.5V)			8		
Gate-Source Charge ^{1,2,5}	Q _{gs}			2		
Gate-Drain Charge ^{1,2,5}	Q _{gd}			3.1		
Turn-On Delay Time ^{1,2,5}	t _{d(on)}	V _{DS} = 15V, V _{GS} = 10V, I _D = 1A, R _g = 6Ω		5.5		nS
Rise Time ^{1,2,5}	t _r			2.4		
Turn-Off Delay Time ^{1,2,5}	t _{d(off)}			28.8		
Fall Time ^{1,2,5}	t _f			15.5		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS						
Continuous Current	I _S				44	A
Pulsed Current ³	I _{SM}				127	
Forward Voltage ^{1,4}	V _{SD}	I _F = I _S =12A, V _{GS} = 0V			1.2	V
Reverse Recovery Time ⁵	t _{rr}	I _F = I _S =20A, dI _F /dt = 400A / mS		7.7		nS
Peak Reverse Recovery Current ⁵	I _{RM(REC)}			2.18		A
Reverse Recovery Charge ⁵	Q _{rr}			9		nC

¹Pulse test : Pulse Width ≤ 300 usec, Duty Cycle ≤ 2%.

²Independent of operating temperature.

³Pulse width limited by maximum junction temperature.

⁴Guarantee by FT test Item

⁵Guarantee by Engineering test

EMC will review datasheet by quarter, and update new version.

▪ TYPICAL CHARACTERISTICS

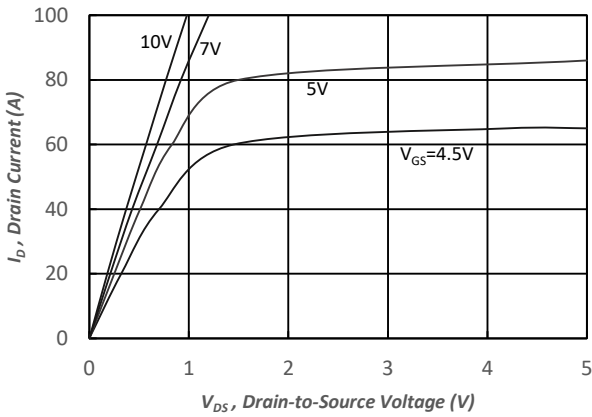


Fig.1 Typical Output Characteristics

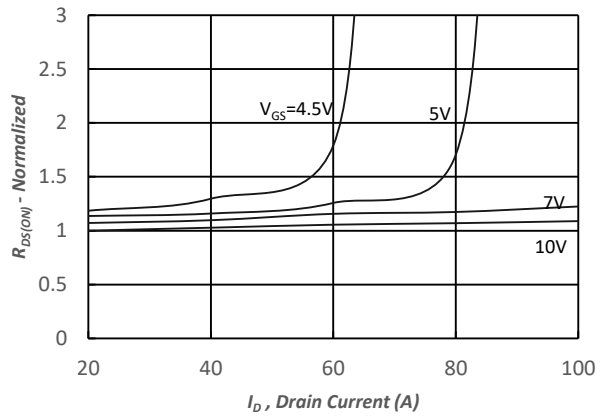


Fig.2 On-Resistance Variation with Drain Current and Gate Voltage

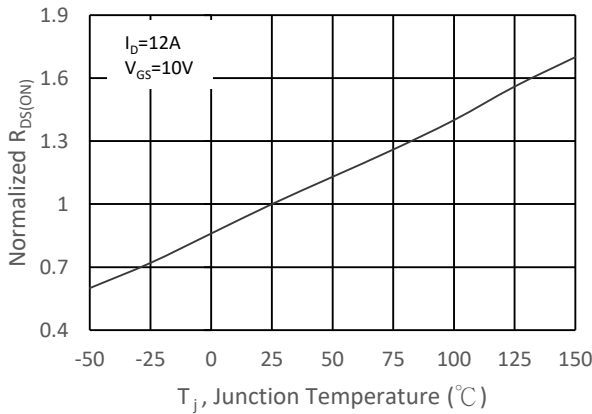


Fig.3 Normalized On-Resistance v.s. Junction Temperature

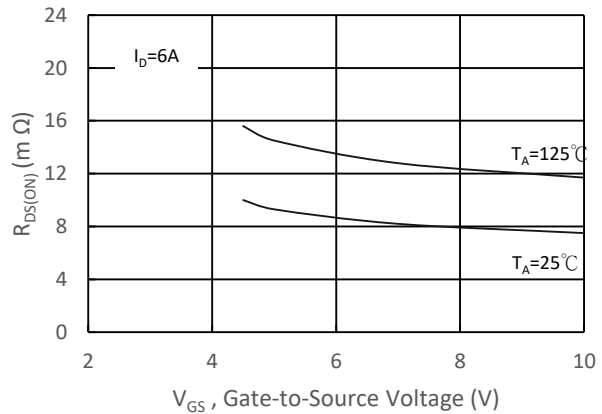


Fig.4 On-Resistance v.s. Gate Voltage

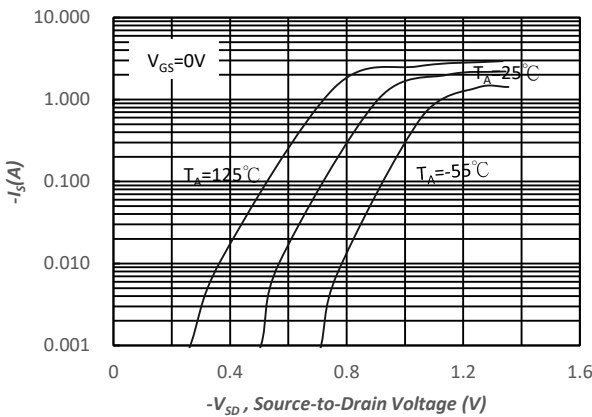


Fig.5 Forward Characteristic of Reverse Diode

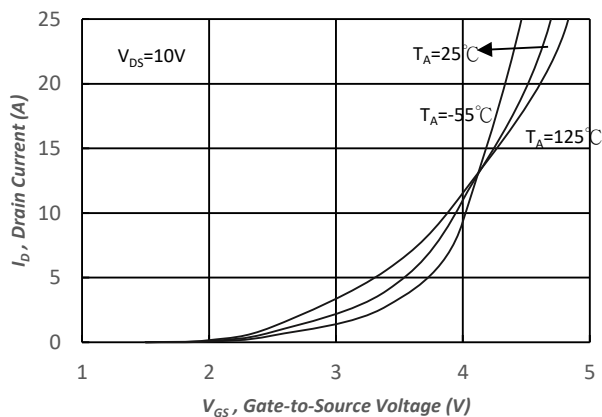


Fig.6 Transfer Characteristics

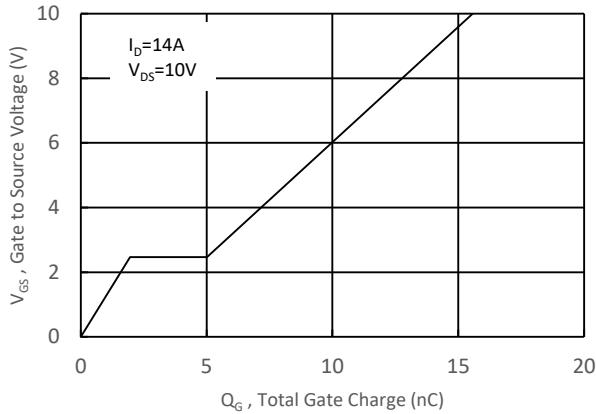


Fig.7 Gate Charge Characteristics

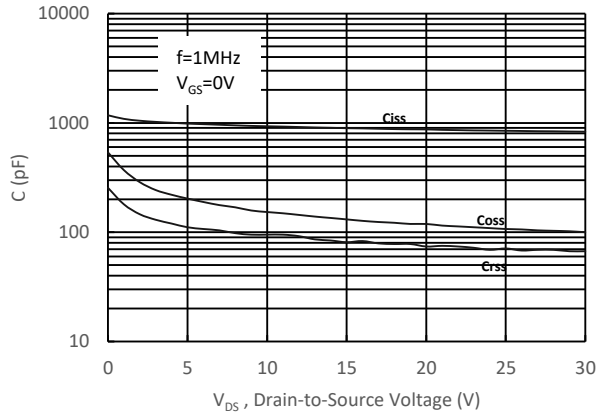


Fig.8 Typical Capacitance Characteristics

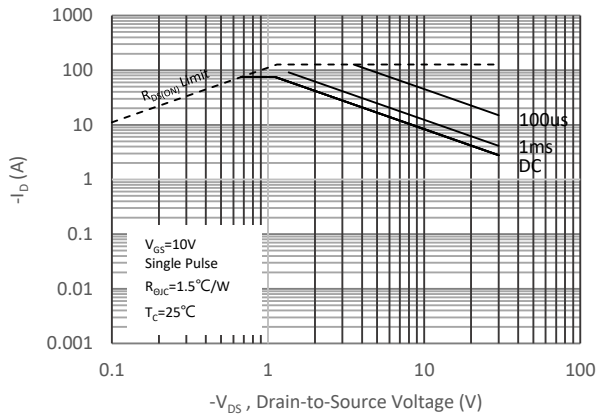


Fig 9. Maximum Safe Operating Area

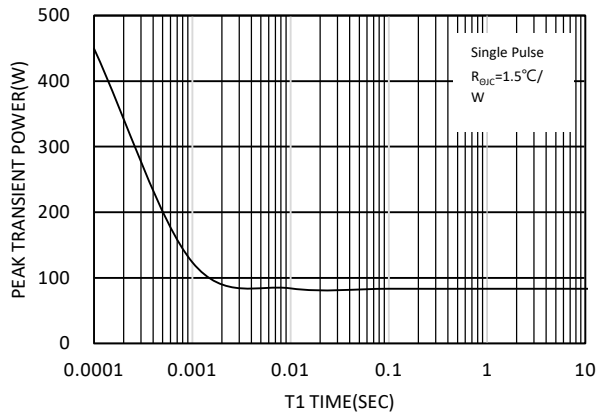


Fig 10. Single Pulse Maximum Power Dissipation

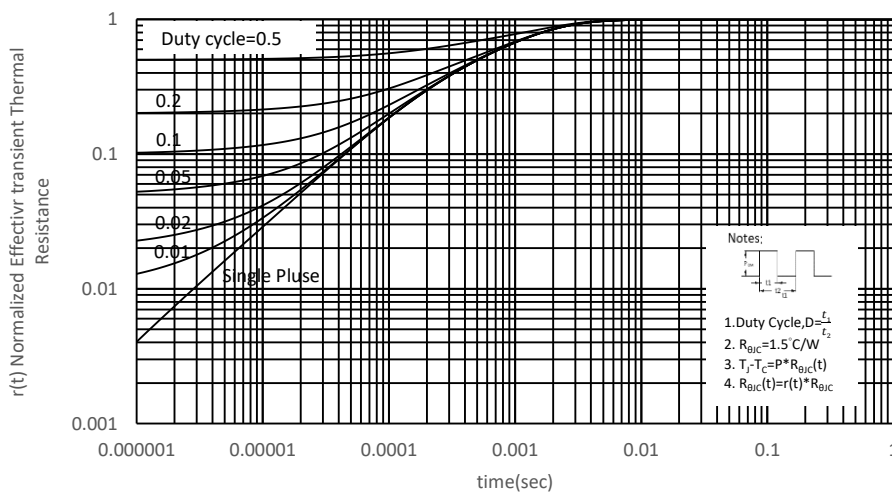


Fig 11. Effective Transient Thermal Impedance

Ordering & Marking Information:

Device Name: EMB09N03V for EDFN 3x3



B09N03: Device Name

ABCDEFGH: Date Code

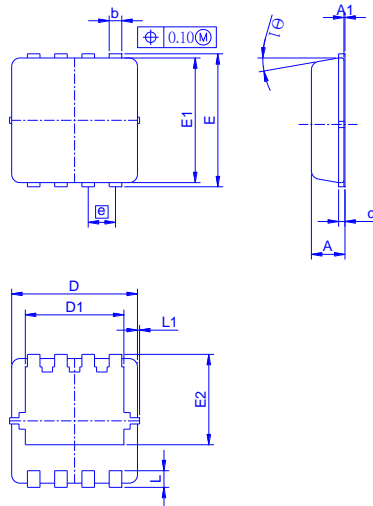
A: Assembly House

B: Year(A:2008 B:2009 C:2010....)

C: Month(A:01 B:02 C:03 D:04 E:05 F:06 G:07 H:08 I:09 J:10 K:11 L:12)

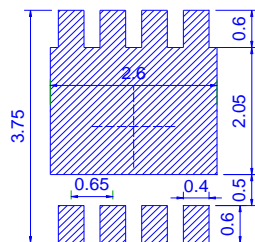
DEFG: Serial No.

Outline Drawing

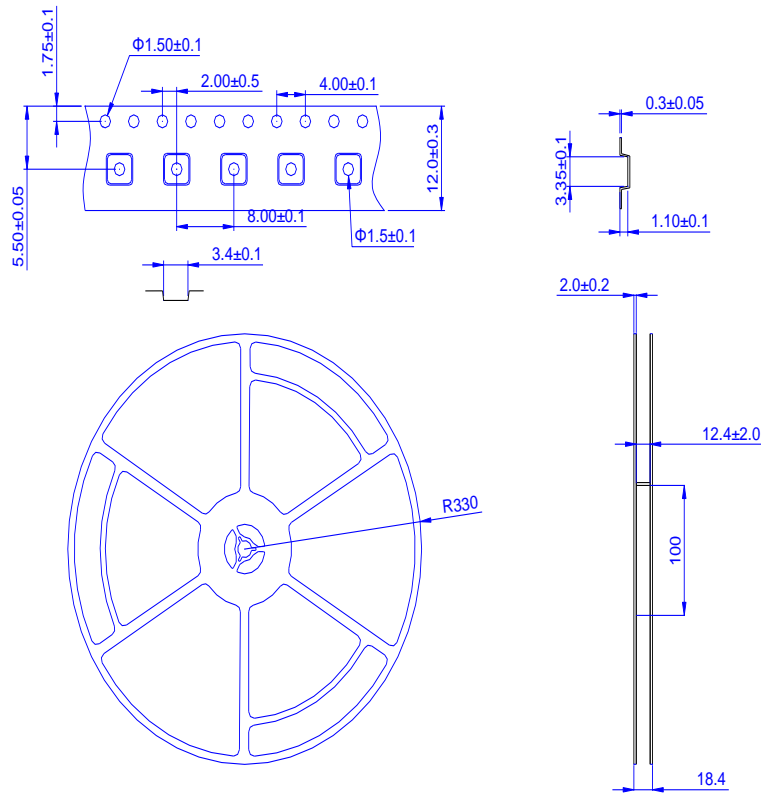


Dimension	A	A1	b	c	D	D1	E	E1	E2	e	L	L1	θ1
Min.	0.65	0	0.2	0.1	2.9	2.15	3.1	2.9	1.53	0.55	0.25	-	0°
Typ.	0.75	-	0.3	0.15	3	2.45	3.2	3	1.97	0.65	0.4	0.075	10°
Max.	0.9	0.05	0.4	0.25	3.3	2.74	3.5	3.3	2.59	0.75	0.6	0.15	14°

Footprint



◆ **Tape&Reel Information:5000pcs/Reel(Dimension in millimeter)**



產品別	EDFN 3x3
Reel尺寸	13"
編帶方式	<p>FEED DIRECTION</p>
前空格	50
後空格	50
裝箱數	
滿捲數量	5K
捲/內盒比	01:01
內盒滿箱數	5K
內/外箱比	10:01
外箱滿箱數	50K



★Datasheet Latest version specification :

	Revision History	Prepared	Approved	Date
A.0	Initial Datasheet	Jannie	Andy	2015/9/25
A.1	Add revision elements as required by Compal	Johnson	Andy	2019/10/23
A.2	Update thermal resistance coefficient and related information	Johnson	Sam	2020/3/2