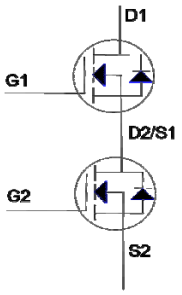
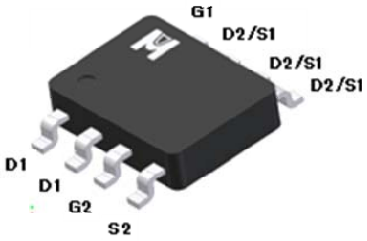
Dual Asymmetric N-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

	N-CH-Q1	N-CH-Q2
BV_{DSS}	30V	30V
$RD_{SON\ (MAX.)}$	15.5mΩ	12.5mΩ
ID	9A	10A





UIS, Rg 100% Tested

Pb-Free Lead Plating & Halogen Free

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS		UNIT
Gate-Source Voltage		V_{GS}	±20	±20	V
Continuous Drain Current	T_C = 25 °C	I_D	9	10	A
	T_C = 100 °C		6	7	
Pulsed Drain Current[1]		I_{DM}	36	40	
Avalanche Current		I_{AS}	12	12	
Avalanche Energy	L = 0.1mH, ID=10A, RG=25Ω	E_{AS}	5	5	mJ
Repetitive Avalanche Energy[2]	L = 0.05mH	E_{AR}	2.5	2.5	
Power Dissipation	T_C = 25 °C	P_D	2		W
	T_C = 100 °C		1.1		
Operating Junction & Storage Temperature Range		T_j, T_{stg}	-55 to 150		°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	$R_{\theta JC}$		25	°C / W
Junction-to-Ambient[3]	$R_{\theta JA}$		62.5	

[1]Pulse width limited by maximum junction temperature.

[2]Duty cycle ≤ 1%

[3]62.5°C / W when mounted on a 1 in^2 pad of 2 oz copper.

ELECTRICAL CHARACTERISTICS (T_C = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS		LIMITS			UNIT
				MIN	TYP	MAX	
STATIC							
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = 250μA	Q1	30			V
			Q2	30			
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250μA	Q1	1	1.5	3	
			Q2	1	1.7	3	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0V, V_{GS} = ±20V	Q1			±100	nA
			Q2			±100	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 24V, V_{GS} = 0V	Q1			1	μA
			Q2			1	
		V_{DS} = 20V, V_{GS} = 0V, T_J = 125 °C	Q1			25	
			Q2			25	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 10V, V_{GS} = 10V	Q1	9			A
			Q2	10			
Drain-Source On-State Resistance[1]	$R_{DS(ON)}$	V_{GS} = 10V, I_D = 9A	Q1		13	15.5	mΩ
		V_{GS} = 10V, I_D = 10A	Q2		10.6	12.5	
		V_{GS} = 4.5V, I_D = 5A	Q1		21	26	
		V_{GS} = 4.5V, I_D = 6A	Q2		17	23	
Forward Transconductance[1]	g_{fs}	V_{DS} = 5V, I_D = 9A	Q1		15		S
		V_{DS} = 5V, I_D = 10A	Q2		18		
DYNAMIC							
Input Capacitance	C_{iss}	V_{GS} = 0V, V_{DS} = 15V, f = 1MHz	Q1		597		pF
			Q2		762		
Output Capacitance	C_{oss}		Q1		111		
			Q2		150		
Reverse Transfer Capacitance	C_{rss}		Q1		96		
			Q2		130		
Gate Resistance	R_g	V_{GS} = 15mV, V_{DS} = 0V, f = 1MHz	Q1		2.0		Ω
			Q2		2.0		

Total Gate Charge[1,2]	Q_g(V_{GS}=10V)	V_{DS} = 15V, V_{GS} = 10V, I_D = 10A	Q1		14		nC
			Q2		15.2		
	Q_g(V_{GS}=4.5V)		Q1		7.2		
			Q2		9.1		
Gate-Source Charge[1,2]	Q_{gs}		Q1		1.8		
			Q2		2.1		
Gate-Drain Charge[1,2]	Q_{gd}		Q1		4.7		
			Q2		6.5		
Turn-On Delay Time[1,2]	$t_{d(on)}$	V_{DS} = 15V, I_D = 1A, V_{GS} = 10V, R_{GS} = 6Ω	Q1		8		nS
			Q2		11		
Rise Time[1,2]	t_r		Q1		6		
			Q2		16		
Turn-Off Delay Time[1,2]	$t_{d(off)}$		Q1		18		
			Q2		36		
Fall Time[1,2]	t_f		Q1		3		
			Q2		20		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25 °C)							
Continuous Current	I_S		Q1			2.3	A
			Q2			2.5	
Pulsed Current[3]	I_{SM}		Q1			9.2	
			Q2			10	
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0V	Q1			1.2	V
			Q2			1.2	
Reverse Recovery Time	t_{rr}	I_F = I_S, dI_F/dt = 100A / μS	Q1		18		nS
			Q2		18		
Peak Reverse Recovery Current	$I_{RM(REC)}$		Q1		30		A
			Q2		40		
Reverse Recovery Charge	Q_{rr}		Q1		5		nC
			Q2		10		

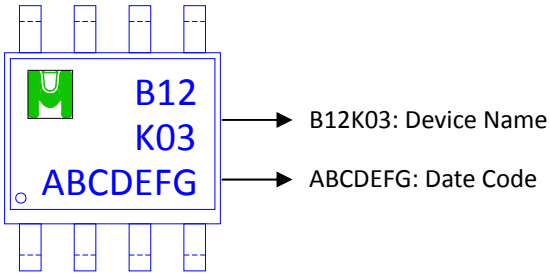
[1]Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.

[2]Independent of operating temperature.

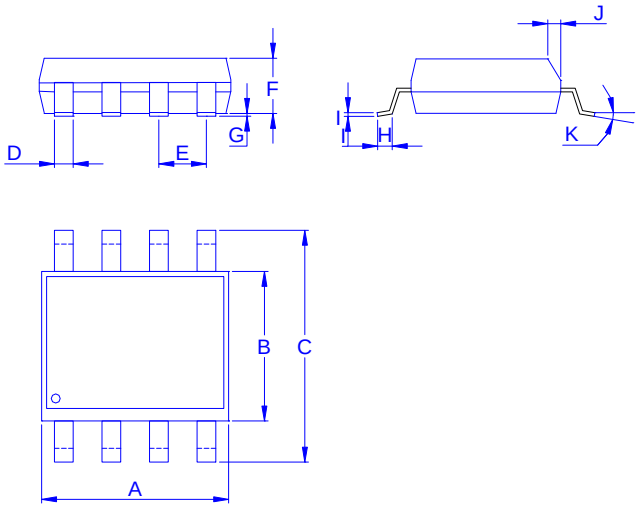
[3]Pulse width limited by maximum junction temperature.

Ordering & Marking Information:

Device Name: EMB12K03GP for Asymmetric SOP-8



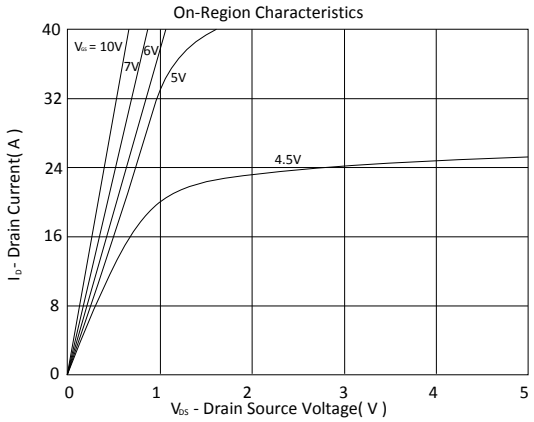
Outline Drawing

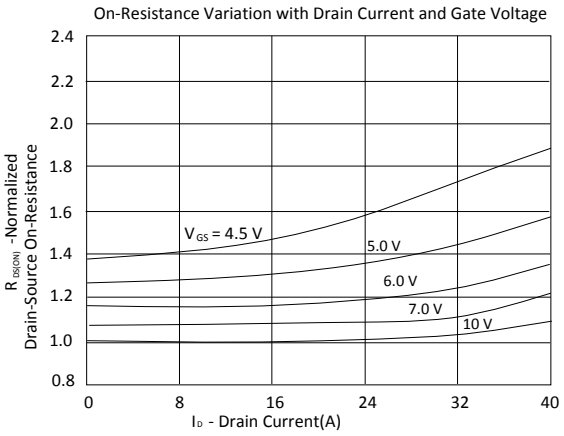


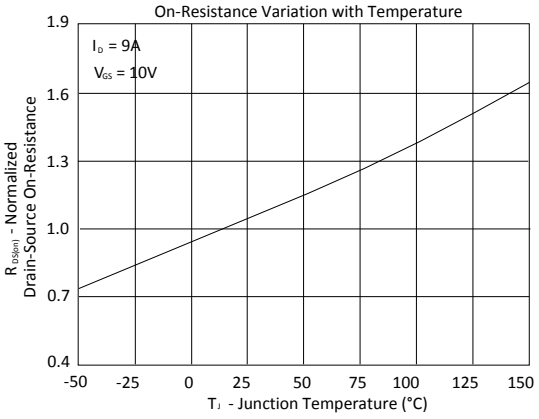
Dimension in mm

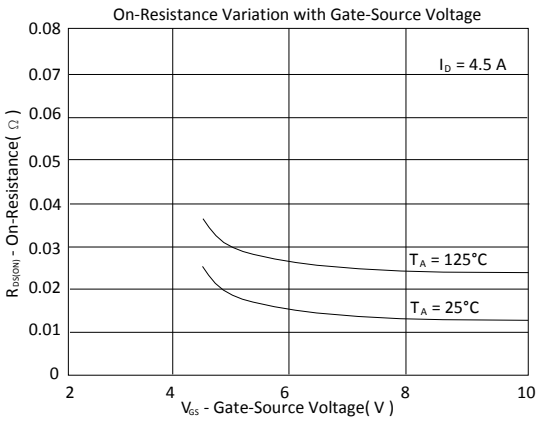
Dimension	A	B	C	D	E	F	G	H	I	J	K
Min.	4.70	3.70	5.80	0.33		1.20	0.08	0.40	0.19	0.25	0°
Typ.					1.27						
Max.	5.10	4.10	6.20	0.51		1.62	0.28	0.83	0.26	0.50	8°

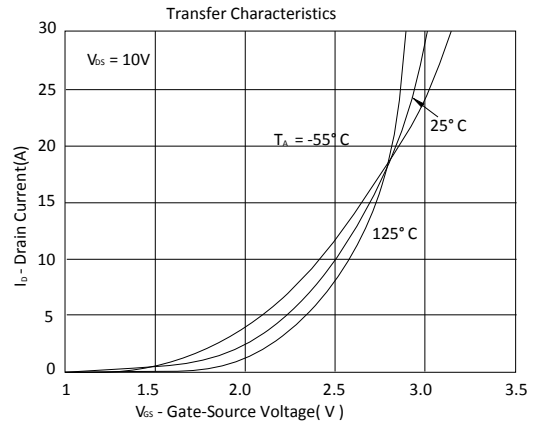
N-Channel-Q1

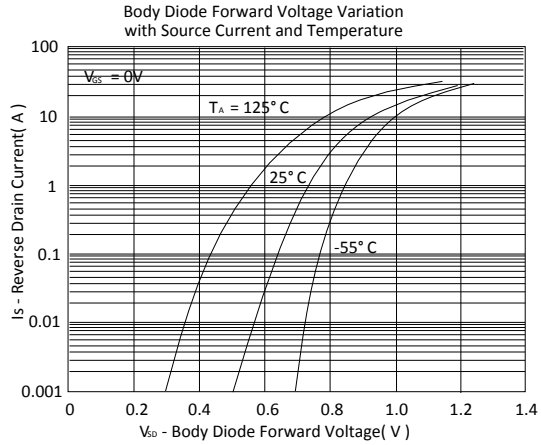

On-Region Characteristics
V_{GS} = 10V
7V
6V
5V
4.5V
I_D - Drain Current(A)
V_{DS} - Drain Source Voltage(V)


On-Resistance Variation with Drain Current and Gate Voltage
$R_{DS(ON)}$ -Normalized
Drain-Source On-Resistance
V_{GS} = 4.5 V
5.0 V
6.0 V
7.0 V
10 V
I_D - Drain Current(A)

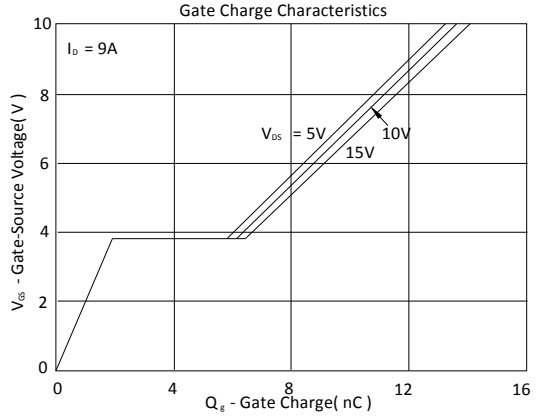

On-Resistance Variation with Temperature
I_D = 9A
V_{GS} = 10V
$R_{DS(ON)}$ - Normalized
Drain-Source On-Resistance
T_J - Junction Temperature (°C)


On-Resistance Variation with Gate-Source Voltage
I_D = 4.5 A
T_A = 125°C
T_A = 25°C
$R_{DS(ON)}$ - On-Resistance(Ω)
V_{GS} - Gate-Source Voltage(V)

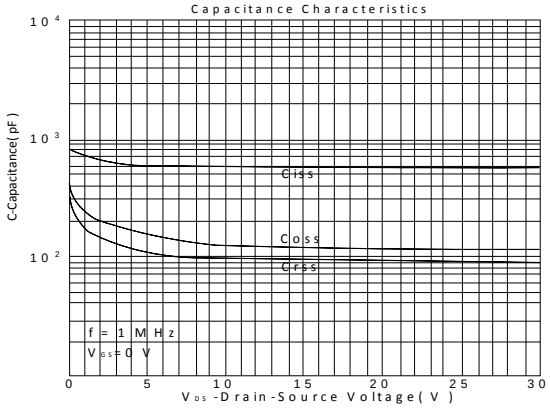

Transfer Characteristics
V_{DS} = 10V
T_A = -55° C
25° C
125° C
I_D - Drain Current(A)
V_{GS} - Gate-Source Voltage(V)


Body Diode Forward Voltage Variation
with Source Current and Temperature
V_{GS} = 0V
T_A = 125° C
25° C
-55° C
Is - Reverse Drain Current(A)
V_{SD} - Body Diode Forward Voltage(V)

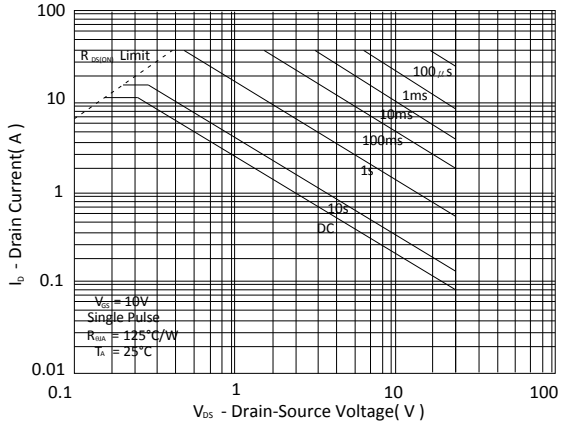
Gate Charge Characteristics



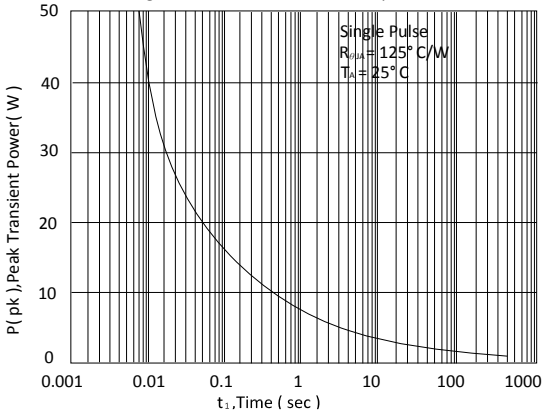
Capacitance Characteristics



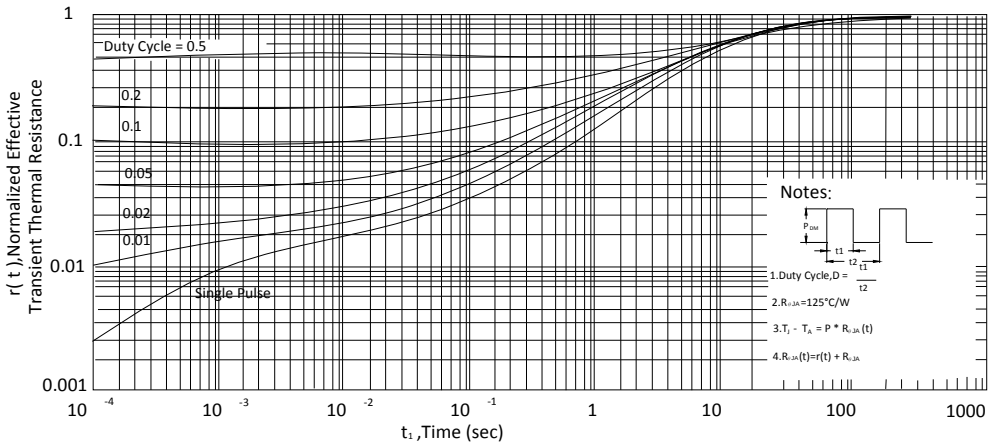
Maximum Safe Operating Area



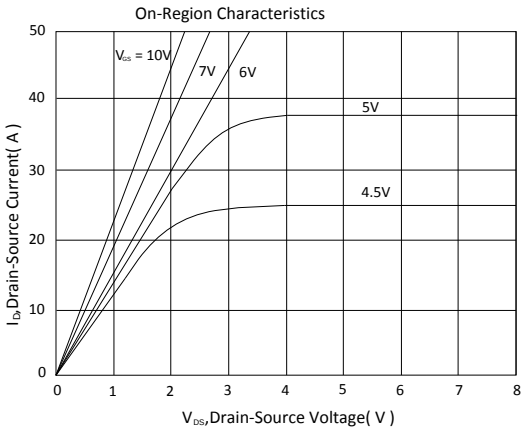
Single Pulse Maximum Power Dissipation

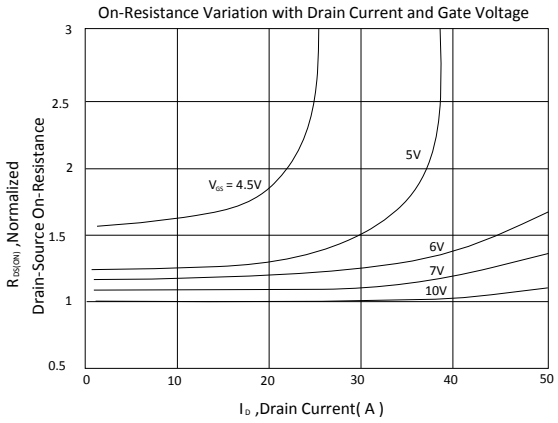


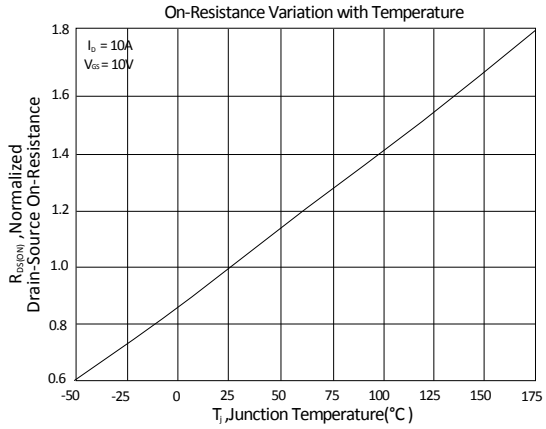
Transient Thermal Response Curve

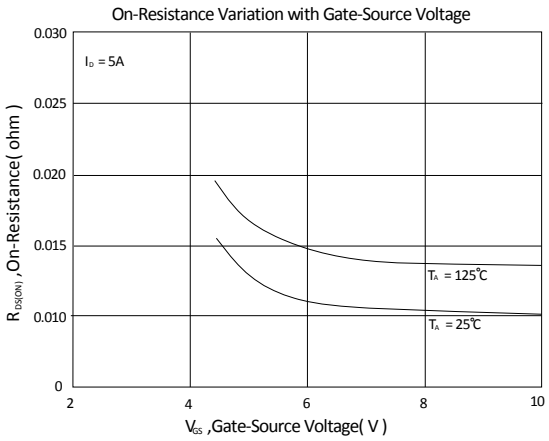


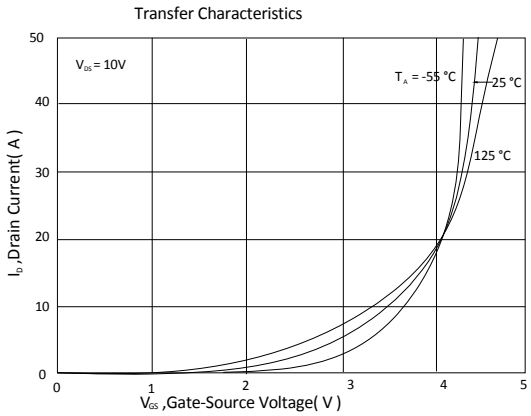
N-Channel-Q2

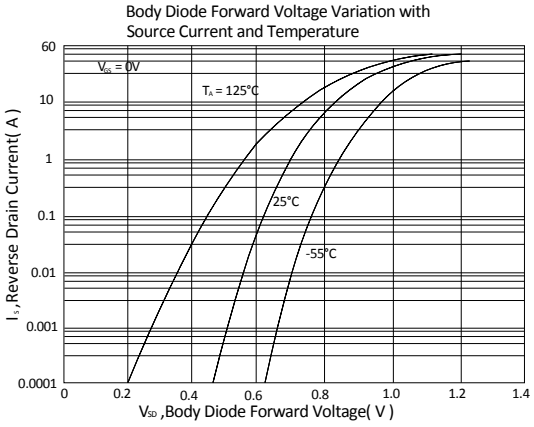

On-Region Characteristics
V_{GS} = 10V
7V
6V
5V
4.5V
I_D,Drain-Source Current(A)
V_{DS},Drain-Source Voltage(V)

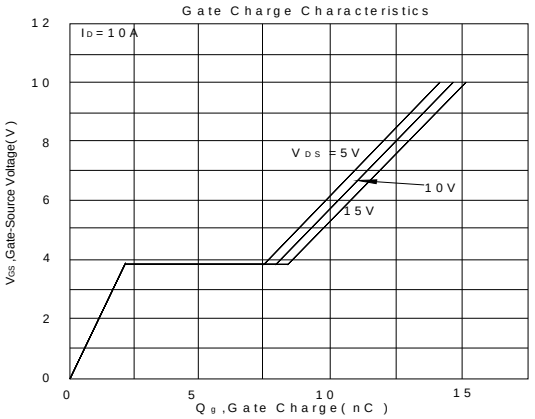

On-Resistance Variation with Drain Current and Gate Voltage
V_{GS} = 4.5V
5V
6V
7V
10V
$R_{DS(ON)}$,Normalized
Drain-Source On-Resistance
I_D ,Drain Current(A)

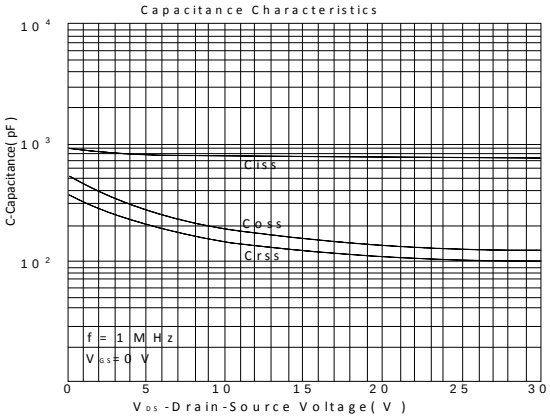

On-Resistance Variation with Temperature
I_D = 10A
V_{GS} = 10V
$R_{DS(ON)}$,Normalized
Drain-Source On-Resistance
T_j ,Junction Temperature(°C)

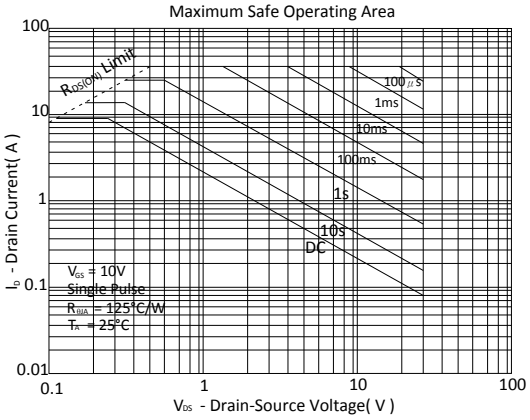

On-Resistance Variation with Gate-Source Voltage
I_D = 5A
T_A = 125°C
T_A = 25°C
$R_{DS(ON)}$,On-Resistance(ohm)
V_{GS} ,Gate-Source Voltage(V)

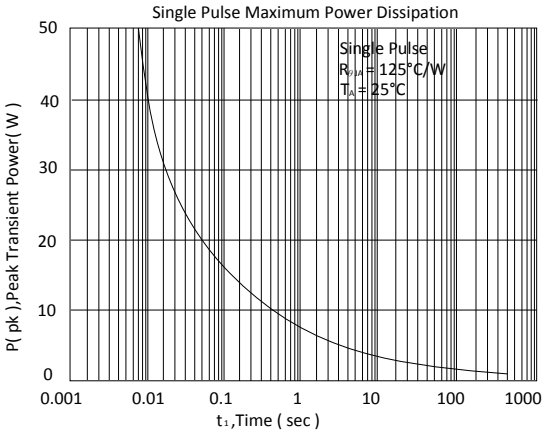

Transfer Characteristics
V_{DS} = 10V
T_A = -55 °C
25 °C
125 °C
I_D,Drain Current(A)
V_{GS} ,Gate-Source Voltage(V)

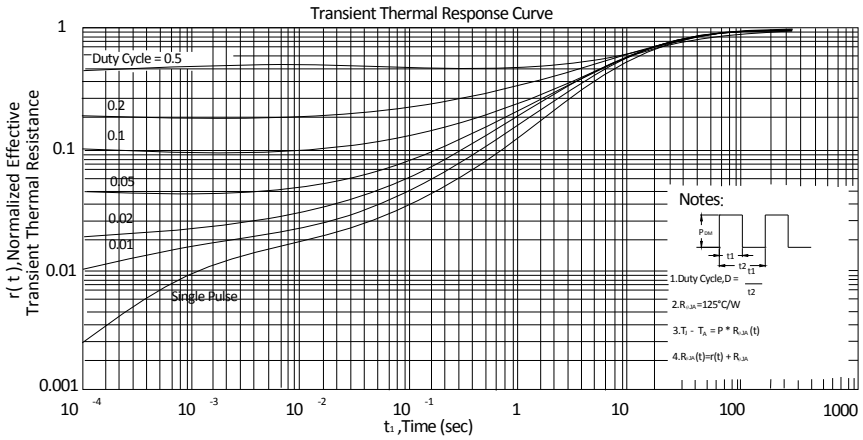

Body Diode Forward Voltage Variation with
Source Current and Temperature
V_{GS} = 0V
T_A = 125°C
25°C
-55°C
I_S ,Reverse Drain Current(A)
V_{SD} ,Body Diode Forward Voltage(V)


Gate Charge Characteristics
ID = 10A
VDS = 5V
10V
15V
VGS ,Gate-Source Voltage(V)
Qg ,Gate Charge(nC)


Capacitance Characteristics
Ciss
Coss
Crss
f = 1 MHz
VGS = 0 V
C-Capacitance(pF)
VDS -Drain-Source Voltage(V)


Maximum Safe Operating Area
RDS(ON) Limit
100μs
1ms
10ms
100ms
1s
10s
DC
VGS = 10V
Single Pulse
RθJA = 125°C/W
TA = 25°C
ID - Drain Current(A)
VDS - Drain-Source Voltage(V)


Single Pulse Maximum Power Dissipation
Single Pulse
RθJA = 125°C/W
TA = 25°C
P(pk),Peak Transient Power(W)
t1 ,Time (sec)


Transient Thermal Response Curve
Duty Cycle = 0.5
0.2
0.1
0.05
0.02
0.01
Single Pulse
Notes:
1.Duty Cycle,D =
2.RθJA=125°C/W
3.TJ - TA = P * RθJA (t)
4.RθJA(t)=r(t) + RθJA
r(t),Normalized Effective Transient Thermal Resistance
t1 ,Time (sec)