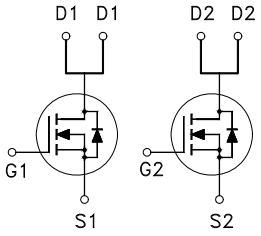
Dual N-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

	N-CH-Q1	N-CH-Q2
BV_{DSS}	30V	30V
$R_{DSON\ (MAX.)}$	12mΩ	17mΩ
I_D	12A	10A



UIS, Rg 100% Tested

Pb-Free Lead Plating & Halogen Free

GP
GREEN PRODUCT

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS		UNIT
			Q1	Q2	
Gate-Source Voltage		V_{GS}	±20	±20	V
Continuous Drain Current	T_A = 25 °C	I_D	12	10	A
	T_A = 100 °C		8.5	7	
Pulsed Drain Current[1]		I_{DM}	48	40	
Avalanche Current		I_{AS}	12	12	
Avalanche Energy	L = 0.1mH, ID=12A, RG=25Ω	E_{AS}	7.2	7.2	mJ
Repetitive Avalanche Energy[2]	L = 0.05mH	E_{AR}	3.6	3.6	
Power Dissipation	T_A = 25 °C	P_D	2.00	2.00	W
	T_A = 100 °C		0.8	0.8	
Operating Junction & Storage Temperature Range		T_j, T_{stg}	-55 to 150		°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	$R_{\theta JC}$		25	°C / W
Junction-to-Ambient[3]	$R_{\theta JA}$		62.5	

[1]Pulse width limited by maximum junction temperature.

[2]Duty cycle ≤ 1%

[3]62.5°C / W when mounted on a 1 in^2 pad of 2 oz copper.

ELECTRICAL CHARACTERISTICS (T_C = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS		LIMITS			UNIT
				MIN	TYP	MAX	
STATIC							
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = 250μA	Q1	30			V
			Q2	30			
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250μA	Q1	1	1.5	3	
			Q2	1	1.5	3	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0V, V_{GS} = ±20V	Q1			±100	nA
			Q2			±100	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 24V, V_{GS} = 0V	Q1			1	μA
			Q2			1	
		V_{DS} = 20V, V_{GS} = 0V, T_J = 125 °C	Q1			25	
			Q2			25	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 10V, V_{GS} = 10V	Q1	12			A
			Q2	10			
Drain-Source On-State Resistance[1]	$R_{DS(ON)}$	V_{GS} = 10V, I_D = 12A	Q1		11.5	12.5	mΩ
		V_{GS} = 10V, I_D = 10A	Q2		14.5	17	
		V_{GS} = 4.5V, I_D = 7A	Q1		16.5	20	
		V_{GS} = 4.5V, I_D = 6A	Q2		21	26	
Forward Transconductance[1]	g_{fs}	V_{DS} = 5V, I_D = 12A	Q1		20		S
		V_{DS} = 5V, I_D = 10A	Q2		18		
DYNAMIC							
Input Capacitance	C_{iss}	V_{GS} = 0V, V_{DS} = 15V, f = 1MHz	Q1		762		pF
			Q2		597		
Output Capacitance	C_{oss}		Q1		150		
			Q2		111		
Reverse Transfer Capacitance	C_{rss}		Q1		130		
			Q2		96		
Gate Resistance	R_g	V_{GS} = 15mV, V_{DS} = 0V, f = 1MHz	Q1		2.0		Ω
			Q2		2.0		

Total Gate Charge[1,2]	Q_g(V_{GS}=10V)	Q1: V_{DS} = 15V, V_{GS} = 10V, I_D = 12A	Q1		15.2		nC
			Q2		14		
	Q_g(V_{GS}=4.5V)	Q2: V_{DS} = 15V, V_{GS} = 10V, I_D = 10A	Q1		10		
			Q2		7.8		
Gate-Source Charge[1,2]	Q_{gs}		Q1		2.1		
			Q2		1.8		
Gate-Drain Charge[1,2]	Q_{gd}		Q1		6.5		
			Q2		4.7		
Turn-On Delay Time[1,2]	$t_{d(on)}$	V_{DS} = 15V, I_D = 1A, V_{GS} = 10V, R_{GS} = 6Ω	Q1		15		nS
			Q2		10		
Rise Time[1,2]	t_r		Q1		12		
			Q2		8		
Turn-Off Delay Time[1,2]	$t_{d(off)}$		Q1		25		
			Q2		20		
Fall Time[1,2]	t_f		Q1		15		
			Q2		10		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25 °C)							
Continuous Current	I_S		Q1			2.3	A
			Q2			2.3	
Pulsed Current[3]	I_{SM}		Q1			9.2	
			Q2			9.2	
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0V	Q1			1.2	V
			Q2			1.2	
Reverse Recovery Time	t_{rr}	I_F = I_S, dI_F/dt = 100A / μS	Q1		18		nS
			Q2		15		
Peak Reverse Recovery Current	$I_{RM(REC)}$		Q1		40		A
			Q2		30		
Reverse Recovery Charge	Q_{rr}		Q1		12		nC
			Q2		10		

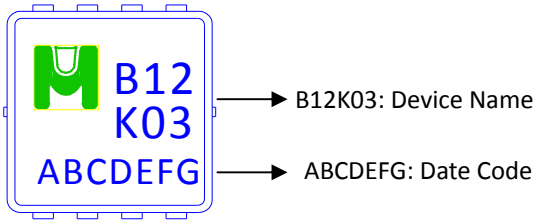
[1]Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.

[2]Independent of operating temperature.

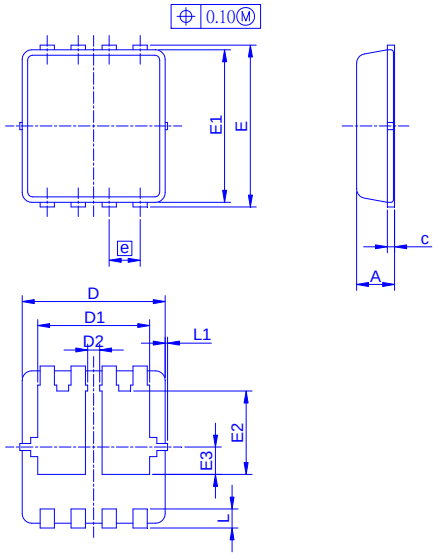
[3]Pulse width limited by maximum junction temperature.

Ordering & Marking Information:

Device Name: EMB12K03V for EDFN 3 x 3



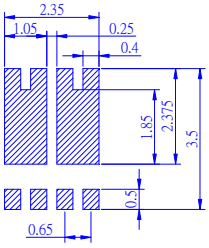
Outline Drawing



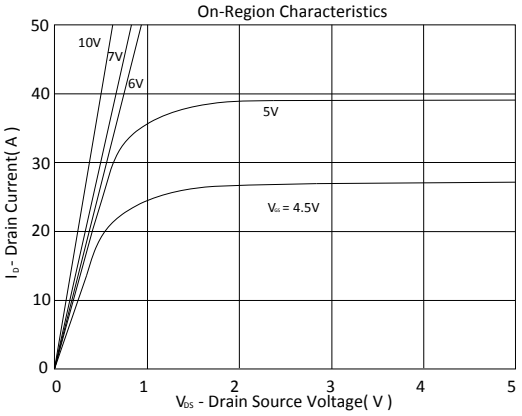
Dimension in mm

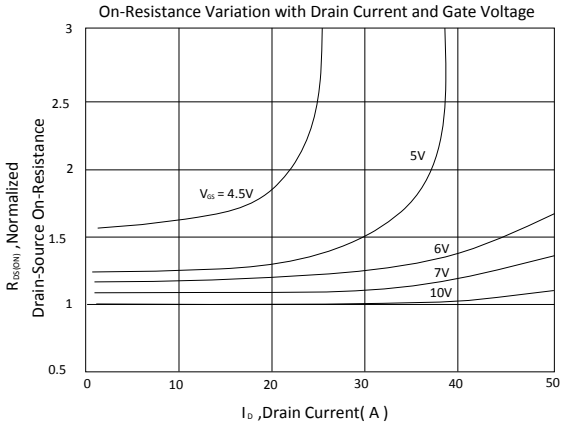
Dimension	A	A1	b	c	D	D1	D2	E	E1	E2	E3	e	L	L1	Θ1
Min.	0.70	0	0.24	0.10	2.95	2.25		3.15	2.95	1.65			0.30	0	0°
Typ.	0.80		0.30	0.152	3.00	2.35	0.225	3.20	3.00	1.75	0.575	0.65	0.40		10°
Max.	0.90	0.05	0.35	0.25	3.05	2.45		3.25	3.05	1.85			0.50	0.10	12°

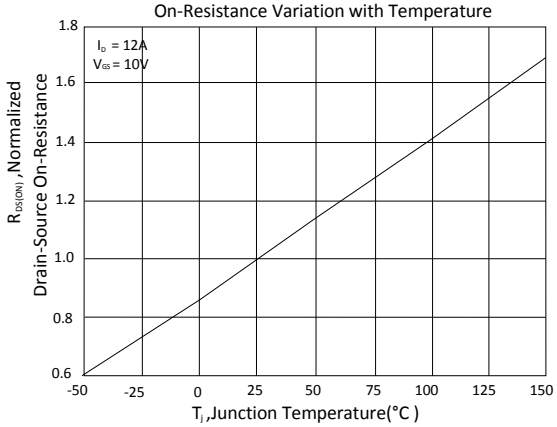
Recommended minimum pads

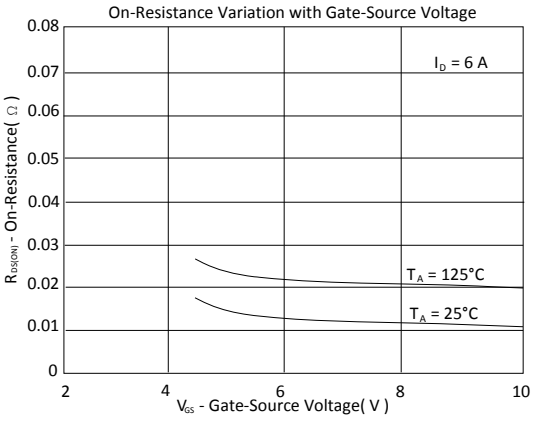


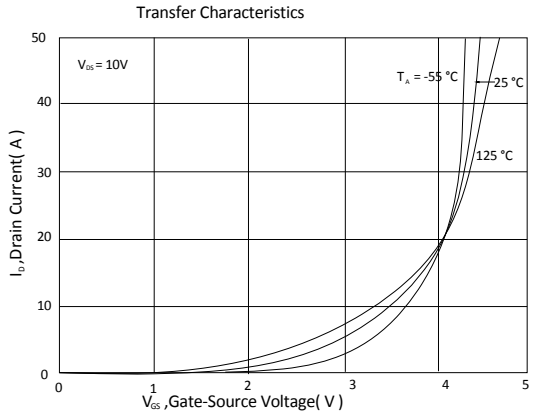
TYPICAL CHARACTERISTICS

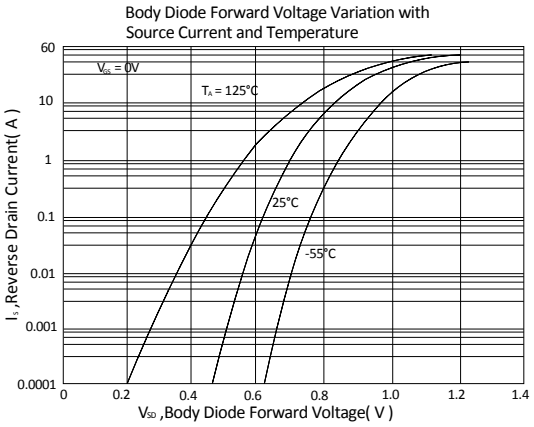


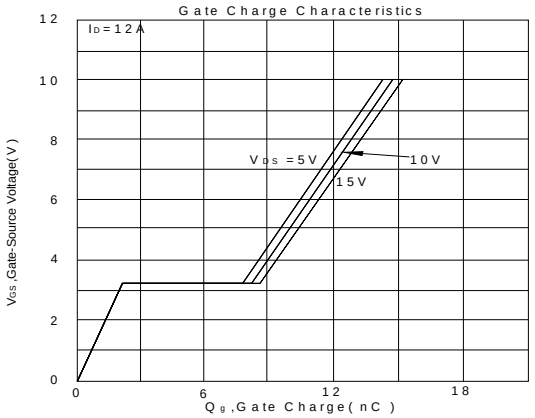


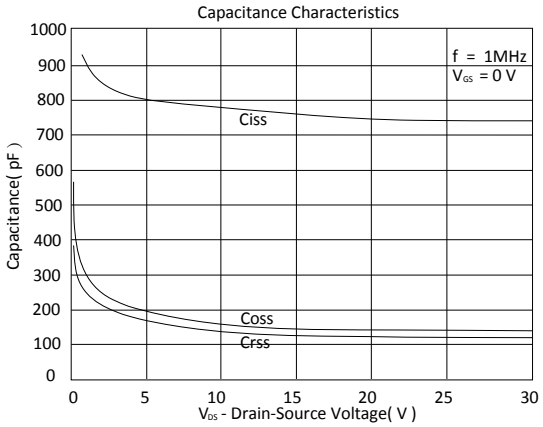


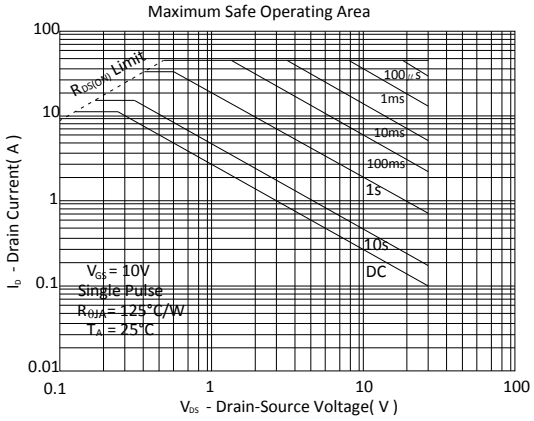


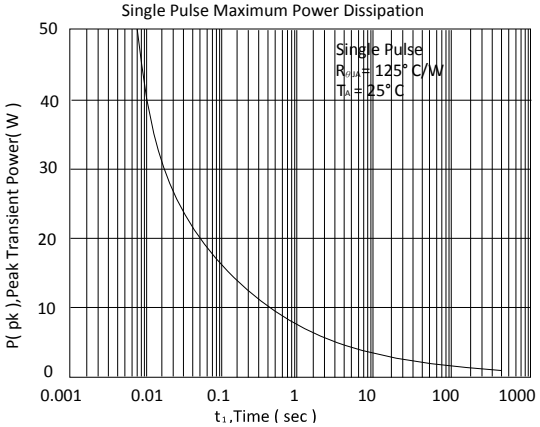


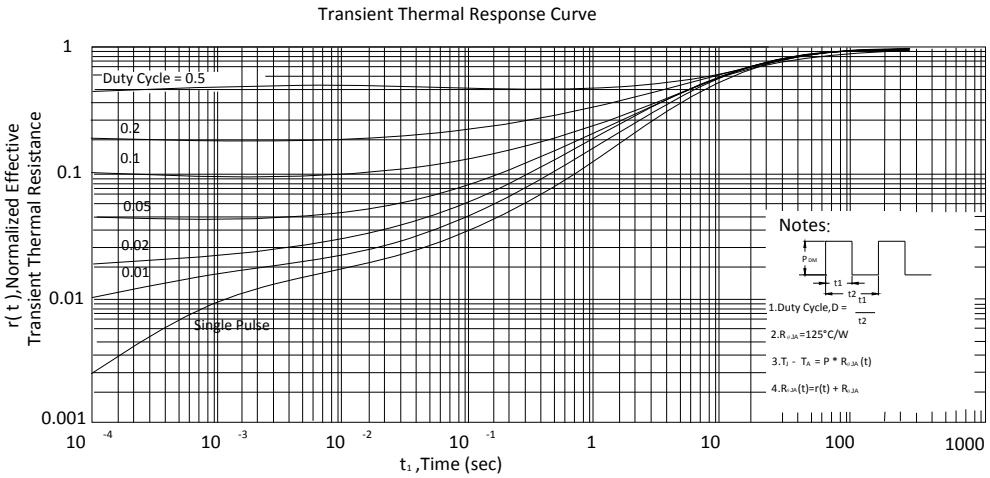



Gate Charge Characteristics
ID = 12 A
VDS = 5 V
10 V
15 V
VGS ,Gate-Source Voltage(V)
Qg ,Gate Charge(nC)

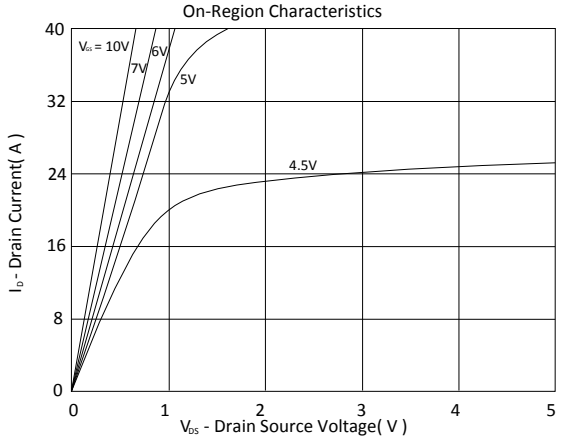

Capacitance Characteristics
f = 1MHz
VGS = 0 V
Ciss
Coss
Crss
Capacitance(pF)
VDS - Drain-Source Voltage(V)


Maximum Safe Operating Area
RDS(ON) Limit
100μs
1ms
10ms
100ms
1s
10s
DC
VGS = 10V
Single Pulse
RθJA = 125°C/W
TA = 25°C
Id - Drain Current(A)
VDS - Drain-Source Voltage(V)

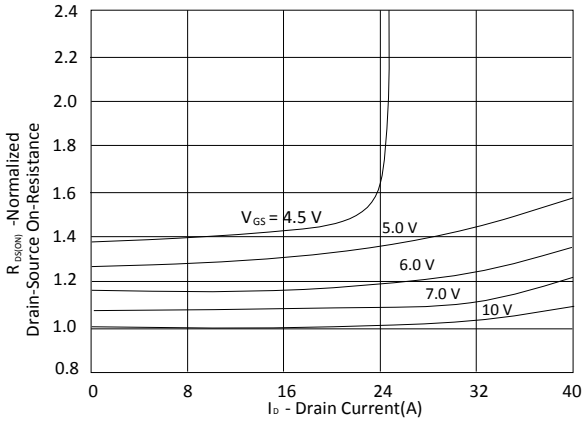

Single Pulse Maximum Power Dissipation
Single Pulse
RθJA = 125° C/W
TA = 25° C
P(pk),Peak Transient Power(W)
t1 ,Time (sec)


Transient Thermal Response Curve
Duty Cycle = 0.5
0.2
0.1
0.05
0.02
0.01
Single Pulse
Notes:
1.Duty Cycle,D =
2.RθJA=125°C/W
3.TJ - TA = P * RθJA (t)
4.RθJA(t)=r(t) + RθJA
r(t),Normalized Effective Transient Thermal Resistance
t1 ,Time (sec)

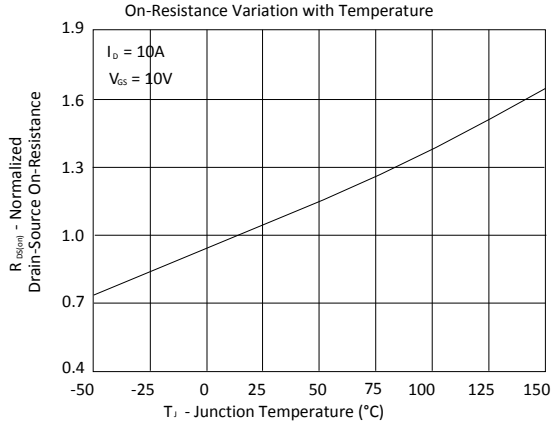
On-Region Characteristics



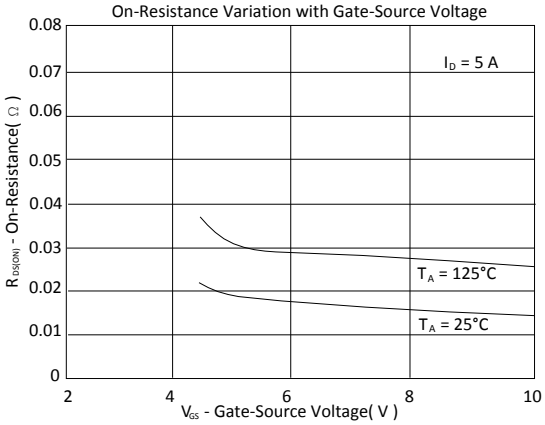
On-Resistance Variation with Drain Current and Gate Voltage



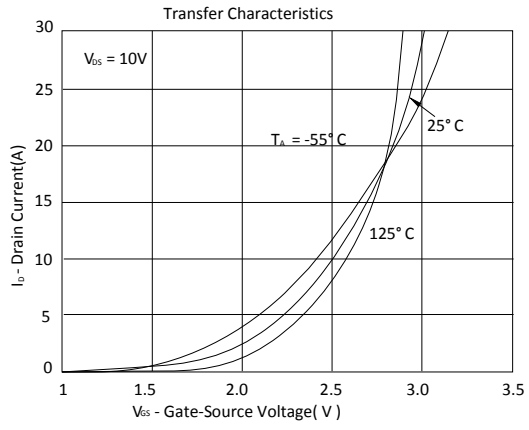
On-Resistance Variation with Temperature



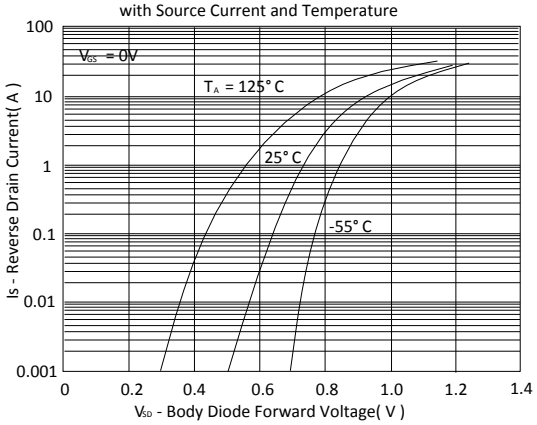
On-Resistance Variation with Gate-Source Voltage



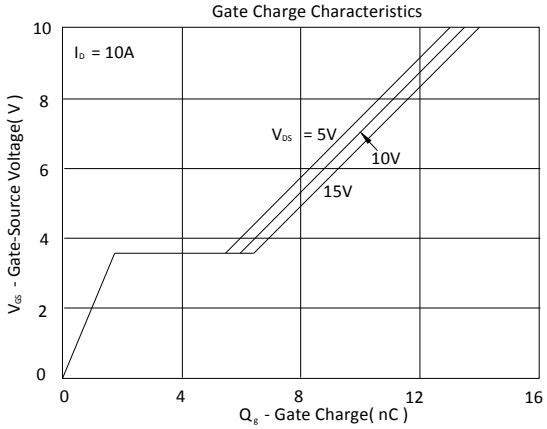
Transfer Characteristics



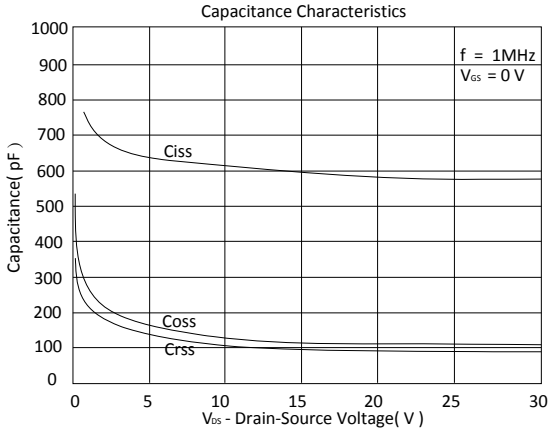
Body Diode Forward Voltage Variation
with Source Current and Temperature



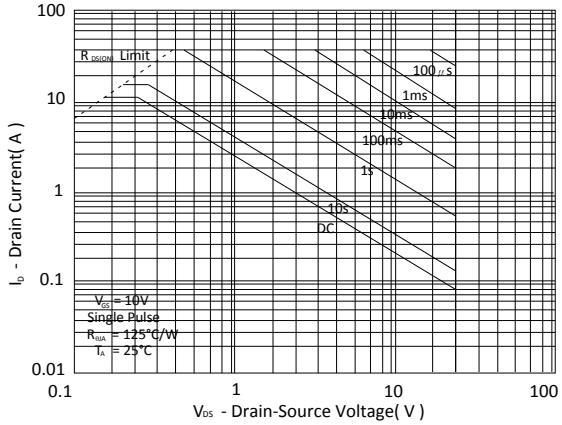
Gate Charge Characteristics



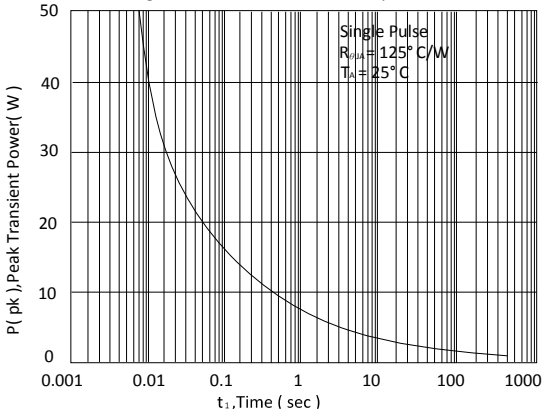
Capacitance Characteristics



Maximum Safe Operating Area



Single Pulse Maximum Power Dissipation



Transient Thermal Response Curve