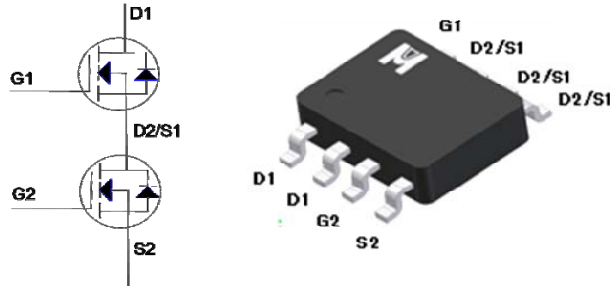


Dual Asymmetric N-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

	N-CH-Q1	N-CH-Q2
BV _{DSS}	30V	30V
RD _{SON (MAX.)}	22mΩ	15.5mΩ
I _D	8A	9A



UIS, R_g 100% Tested

Pb-Free Lead Plating & Halogen Free

ABSOLUTE MAXIMUM RATINGS (T_c = 25 °C Unless Otherwise Noted)



PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS		UNIT
Gate-Source Voltage		V _{GS}	±20	±20	V
Continuous Drain Current	T _c = 25 °C	I _D	8	9	A
	T _c = 100 °C		5.5	6	
Pulsed Drain Current ¹		I _{DM}	32	36	
Avalanche Current		I _{AS}	10	10	
Avalanche Energy	L = 0.1mH, I _D =10A, R _G =25Ω	E _{AS}	5	5	mJ
Repetitive Avalanche Energy ²	L = 0.05mH	E _{AR}	2.5	2.5	
Power Dissipation	T _c = 25 °C	P _D	2		W
	T _c = 100 °C		1.1		
Operating Junction & Storage Temperature Range		T _j , T _{stg}	-55 to 150		°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	R _{θJC}		25	°C / W
Junction-to-Ambient ³	R _{θJA}		62.5	

¹Pulse width limited by maximum junction temperature.

²Duty cycle ≤ 1%

³62.5°C / W when mounted on a 1 in² pad of 2 oz copper.

ELECTRICAL CHARACTERISTICS ($T_c = 25\text{ }^\circ\text{C}$, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT	
			MIN	TYP	MAX		
STATIC							
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	Q1	30		V	
			Q2	30			
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	Q1	1	1.5	3	
			Q2	1	1.7	3	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0V, V_{GS} = \pm 20V$	Q1			± 100	nA
			Q2			± 100	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 24V, V_{GS} = 0V$	Q1			1	μA
			Q2			1	
		$V_{DS} = 20V, V_{GS} = 0V, T_J = 125\text{ }^\circ\text{C}$	Q1			25	
			Q2			25	
On-State Drain Current ¹	$I_{D(ON)}$	$V_{DS} = 10V, V_{GS} = 10V$	Q1	8			A
			Q2	9			
Drain-Source On-State Resistance ¹	$R_{DS(ON)}$	$V_{GS} = 10V, I_D = 8A$ $V_{GS} = 10V, I_D = 9A$	Q1		19	22	m Ω
			Q2		13.5	15.5	
		$V_{GS} = 4.5V, I_D = 5A$ $V_{GS} = 4.5V, I_D = 6A$	Q1		29	36	
			Q2		21	26	
Forward Transconductance ¹	g_{fs}	$V_{DS} = 5V, I_D = 8A$ $V_{DS} = 5V, I_D = 9A$	Q1		12		S
			Q2		15		
DYNAMIC							
Input Capacitance	C_{iss}	$V_{GS} = 0V, V_{DS} = 15V, f = 1MHz$	Q1		520		pF
			Q2		597		
Output Capacitance	C_{oss}		Q1		88		
			Q2		111		
Reverse Transfer Capacitance	C_{rss}		Q1		62		
			Q2		96		
Gate Resistance	R_g	$V_{GS} = 15mV, V_{DS} = 0V, f = 1MHz$	Q1		2.0		Ω
			Q2		2.0		

Total Gate Charge ^{1,2}	$Q_g(V_{GS}=10V)$	$V_{DS} = 15V, V_{GS} = 10V,$ $I_D = 8A$	Q1	11.5	nC
	$Q_g(V_{GS}=4.5V)$		Q2	14	
Q_{gs}			Q1	5	
	Gate-Source Charge ^{1,2}		Q_{gd}	Q2	
Q1		1.6			
Gate-Drain Charge ^{1,2}	$t_{d(on)}$	$V_{DS} = 15V,$ $I_D = 1A, V_{GS} = 10V, R_{GS} = 6\Omega$	Q2	1.8	nS
			Turn-On Delay Time ^{1,2}	t_r	
Rise Time ^{1,2}	$t_{d(off)}$				
			Turn-Off Delay Time ^{1,2}	t_f	
Fall Time ^{1,2}					
			SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS ($T_C = 25^\circ C$)		
Continuous Current	I_S		Q1	2.3	A
			Q2	2.5	
Pulsed Current ³	I_{SM}		Q1	9.2	
			Q2	10	
Forward Voltage ¹	V_{SD}	$I_F = I_S, V_{GS} = 0V$	Q1	1.2	V
			Q2	1.2	
Reverse Recovery Time	t_{rr}	$I_F = I_S, dI_F/dt = 100A / \mu S$	Q1	15	nS
			Q2	18	
Reverse Recovery Charge	Q_{rr}		Q1	3	nC
			Q2	5	

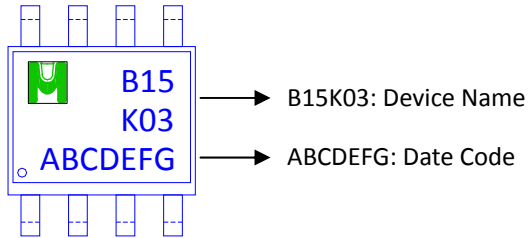
¹Pulse test : Pulse Width $\leq 300 \mu sec$, Duty Cycle $\leq 2\%$.

²Independent of operating temperature.

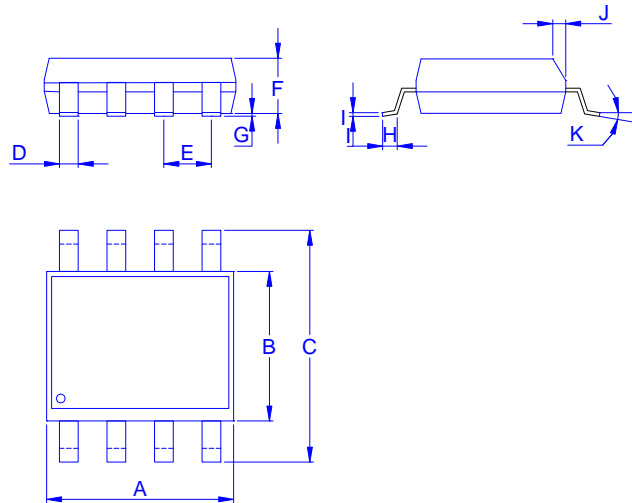
³Pulse width limited by maximum junction temperature.

Ordering & Marking Information:

Device Name: EMB15K03GP for Asymmetric SOP-8



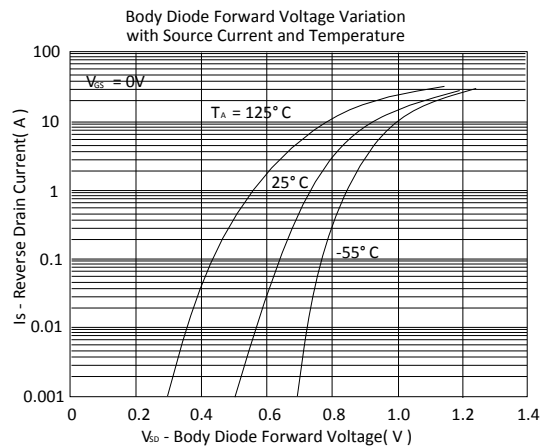
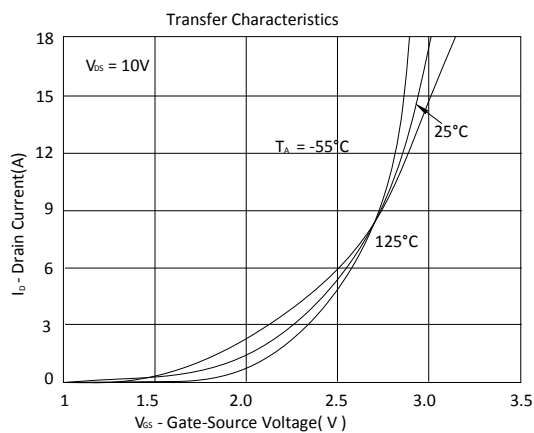
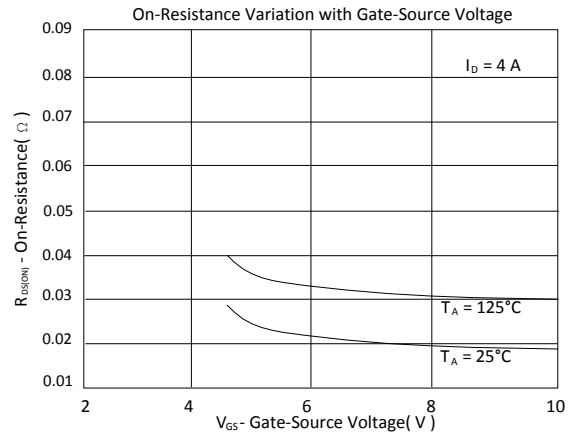
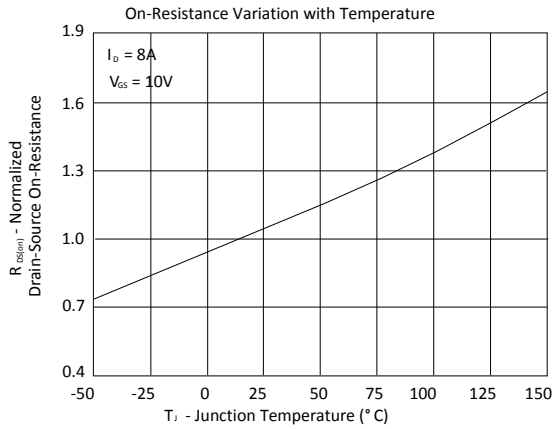
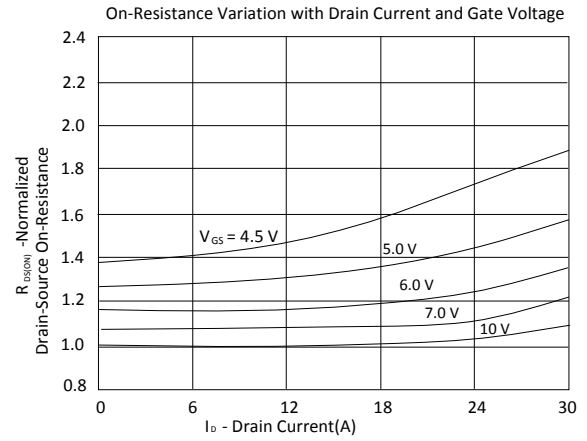
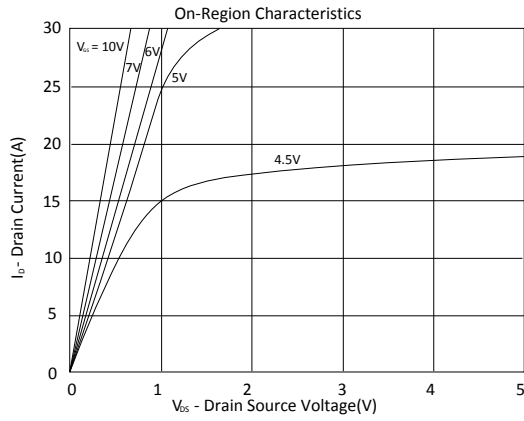
Outline Drawing

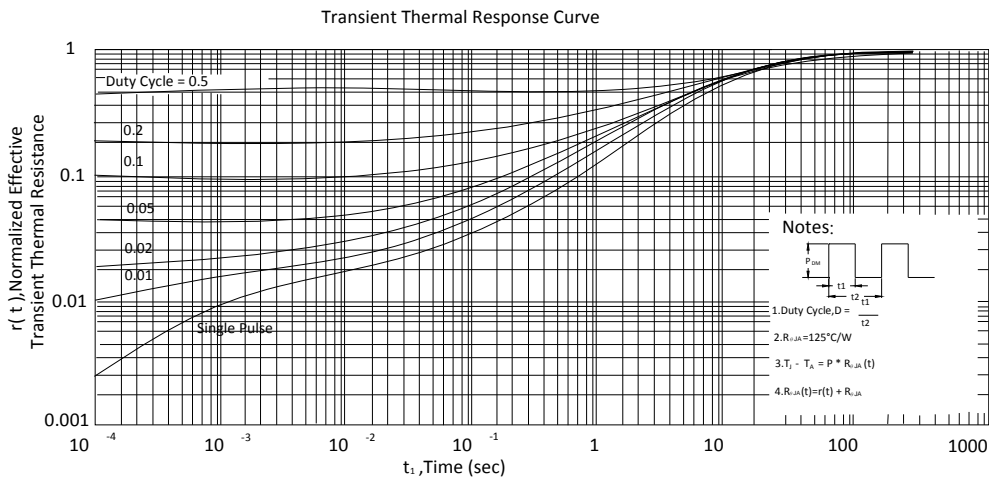
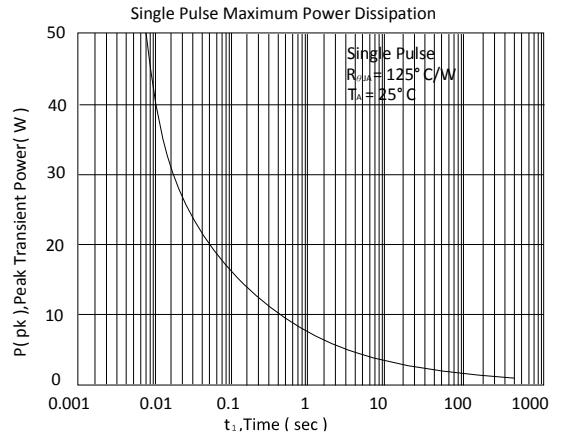
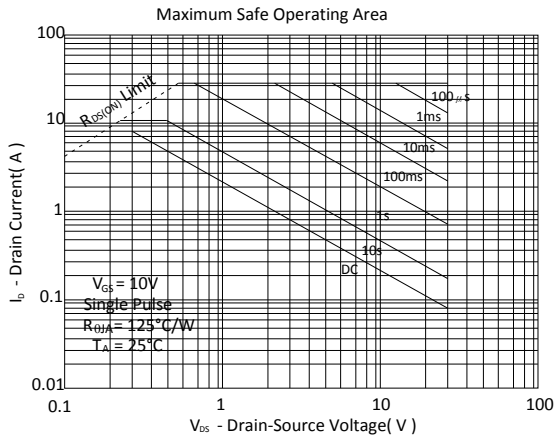
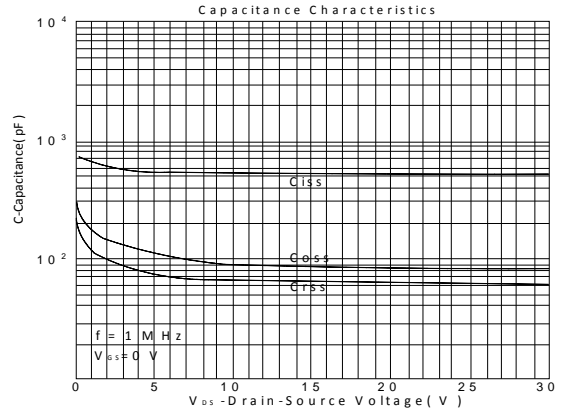
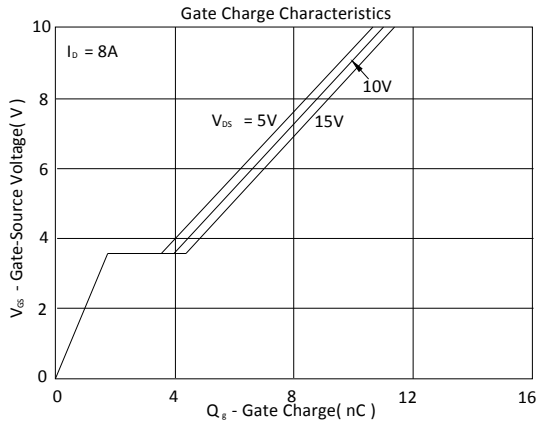


Dimension in mm

Dimension	A	B	C	D	E	F	G	H	I	J	K
Min.	4.70	3.70	5.80	0.33		1.20	0.08	0.40	0.19	0.25	0°
Typ.					1.27						
Max.	5.10	4.10	6.20	0.51		1.62	0.28	0.83	0.26	0.50	8°

N-Channel-Q1





N-Channel-Q2

