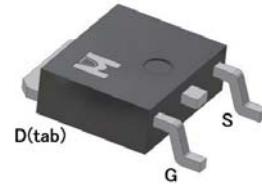


N-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

BV _{DSS}	30V
R _{DSON} (MAX.)	14mΩ
I _D	25A



UIS, R_G 100% Tested

Pb-Free Lead Plating & Halogen Free



ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V _{GS}	±20	V
Continuous Drain Current	T _C = 25 °C	I _D	25	A
	T _C = 100 °C		20	
Pulsed Drain Current ¹		I _{DM}	100	
Avalanche Current		I _{AS}	20	
Avalanche Energy	L = 0.1mH, ID=20A, RG=25Ω	E _{AS}	20	mJ
Repetitive Avalanche Energy ²	L = 0.05mH	E _{AR}	10	
Power Dissipation	T _C = 25 °C	P _D	35	W
	T _C = 100 °C		14	
Operating Junction & Storage Temperature Range		T _j , T _{stg}	-55 to 150	°C

100% UIS testing in condition of V_D=15V, L=0.1mH, V_G=10V, I_L=15A, Rated V_{DS}=25V N-CH

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	R _{θJC}	3.5	62	°C / W
Junction-to-Ambient ³	R _{θJA}			

¹Pulse width limited by maximum junction temperature.

²Duty cycle ≤ 1%

³62°C / W when mounted on a 1 in² pad of 2 oz copper.

ELECTRICAL CHARACTERISTICS ($T_c = 25^\circ\text{C}$, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(\text{BR})\text{DSS}}$	$V_{GS} = 0V, I_D = 250\mu\text{A}$	30			V
Gate Threshold Voltage	$V_{GS(\text{th})}$	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$	1	1.7	3	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0V, V_{GS} = \pm 20V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 24V, V_{GS} = 0V$			1	μA
		$V_{DS} = 20V, V_{GS} = 0V, T_J = 125^\circ\text{C}$			25	
On-State Drain Current ¹	$I_{D(\text{ON})}$	$V_{DS} = 5V, V_{GS} = 10V$	25			A
Drain-Source On-State Resistance ¹	$R_{DS(\text{ON})}$	$V_{GS} = 10V, I_D = 15A$		12.5	14	$\text{m}\Omega$
		$V_{GS} = 4.5V, I_D = 10A$		20	25	
Forward Transconductance ¹	g_{fs}	$V_{DS} = 5V, I_D = 15A$		15		S
DYNAMIC						
Input Capacitance	C_{iss}	$V_{GS} = 0V, V_{DS} = 15V, f = 1\text{MHz}$		597		pF
Output Capacitance	C_{oss}			111		
Reverse Transfer Capacitance	C_{rss}			96		
Gate Resistance	R_g	$V_{GS} = 15\text{mV}, V_{DS} = 0V, f = 1\text{MHz}$		2.0		Ω
Total Gate Charge ^{1,2}	$Q_g(V_{GS}=10V)$	$V_{DS} = 15V, V_{GS} = 10V, I_D = 15A$		14		nC
	$Q_g(V_{GS}=4.5V)$			7.2		
Gate-Source Charge ^{1,2}	Q_{gs}			1.8		
Gate-Drain Charge ^{1,2}	Q_{gd}			4.7		
Turn-On Delay Time ^{1,2}	$t_{d(on)}$	$V_{DS} = 15V, I_D = 1A, V_{GS} = 10V, R_{GS} = 2.7\Omega$		10		ns
Rise Time ^{1,2}	t_r			8		
Turn-Off Delay Time ^{1,2}	$t_{d(off)}$			20		
Fall Time ^{1,2}	t_f			10		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS ($T_c = 25^\circ\text{C}$)						
Continuous Current	I_S	$I_F = I_S, V_{GS} = 0V$			25	A
Pulsed Current ³	I_{SM}				100	
Forward Voltage ¹	V_{SD}				1.3	
Reverse Recovery Time	t_{rr}			18		
Peak Reverse Recovery Current	$I_{RM(\text{REC})}$			100		
Reverse Recovery Charge	Q_{rr}			10		

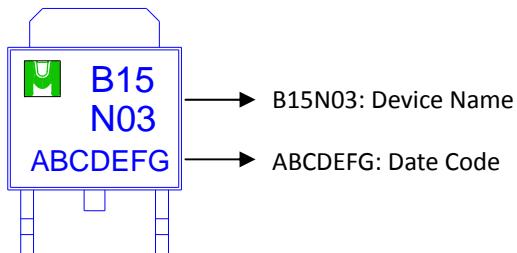
¹Pulse test : Pulse Width \leq 300 μ sec, Duty Cycle \leq 2%.

²Independent of operating temperature.

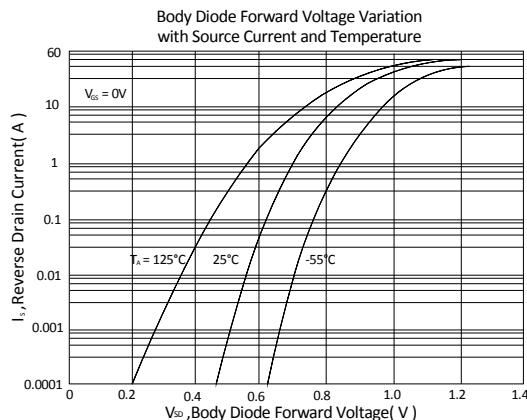
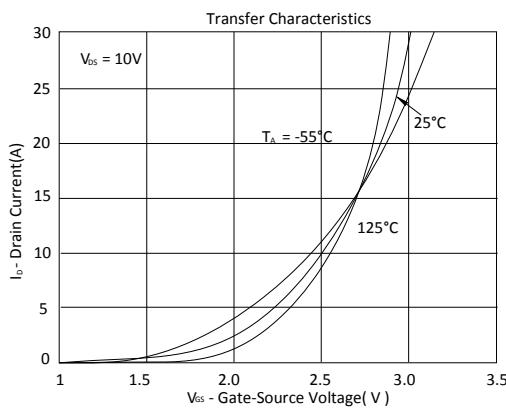
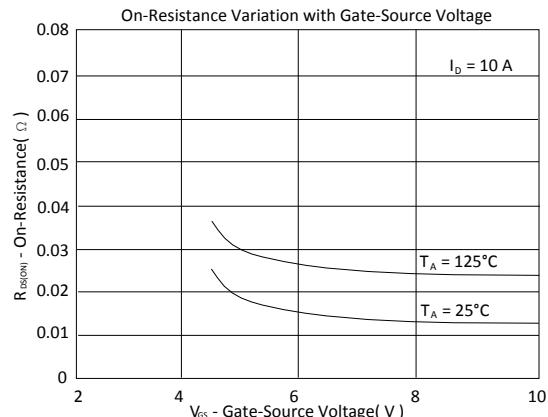
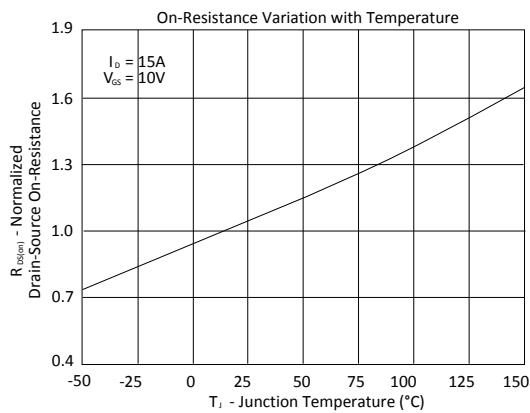
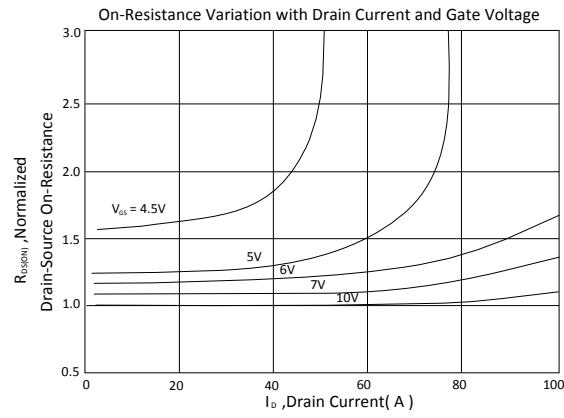
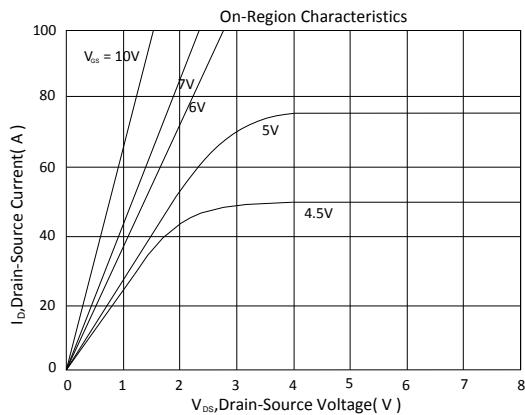
³Pulse width limited by maximum junction temperature.

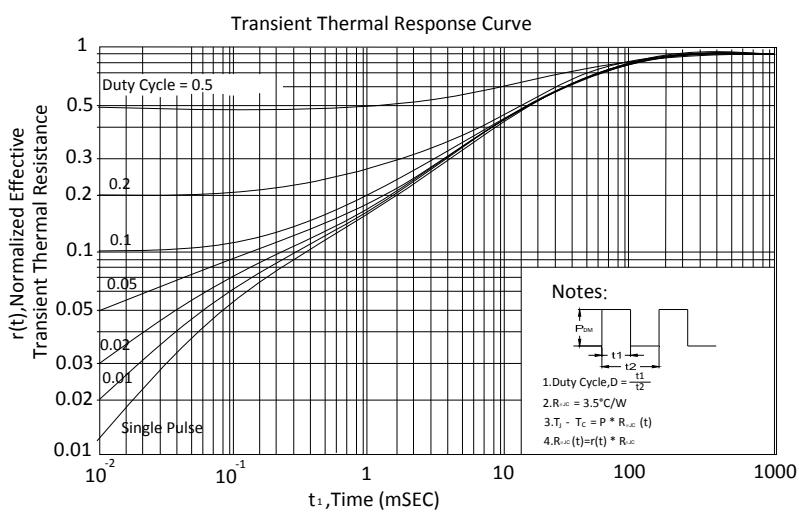
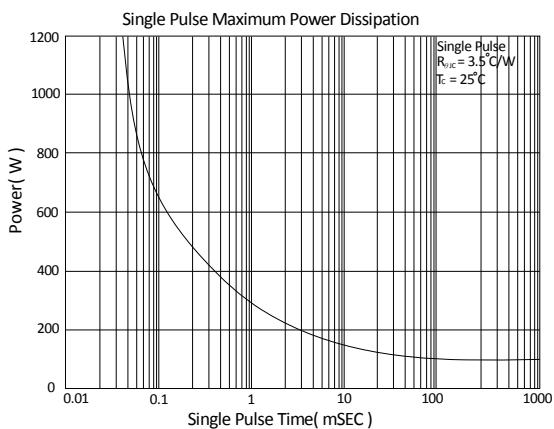
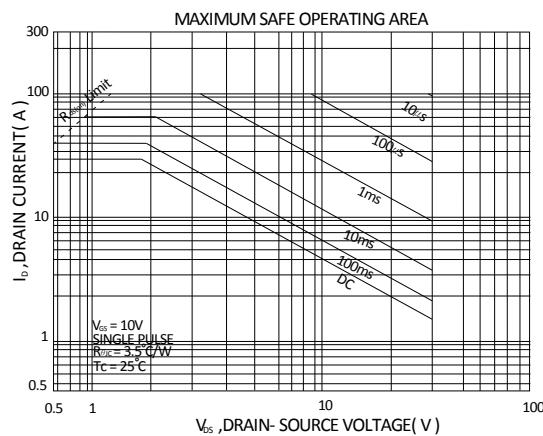
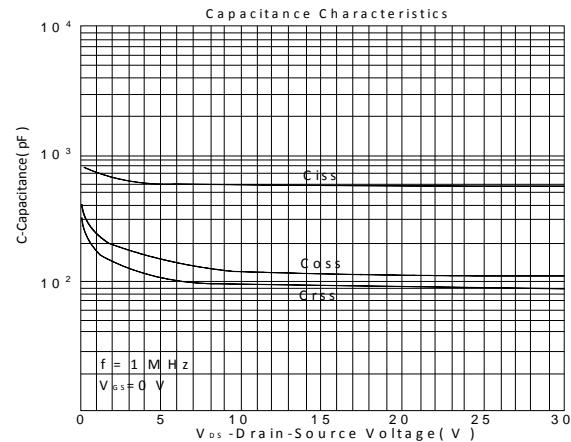
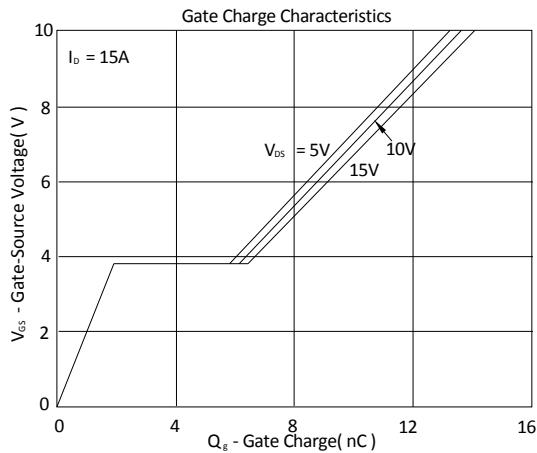
Ordering & Marking Information:

Device Name: EMB15N03A for DPAK (TO-252)

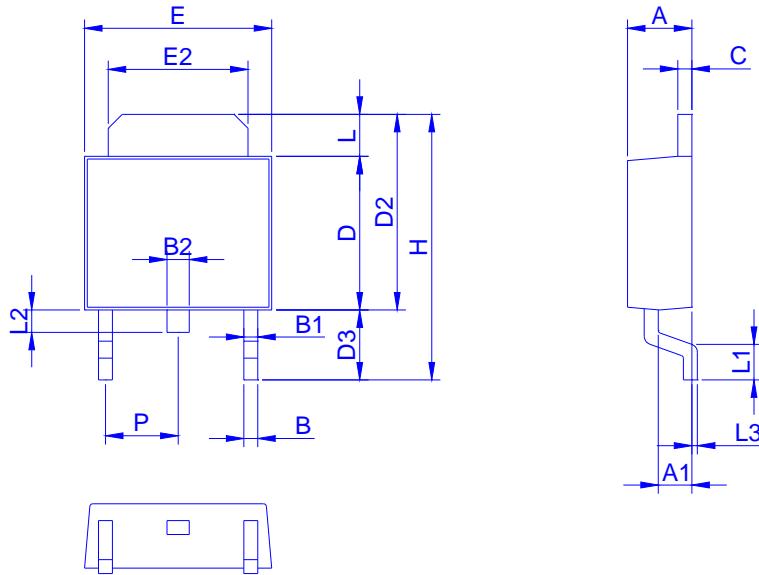


TYPICAL CHARACTERISTICS





Outline Drawing



Dimension in mm

Dimension	A	A1	B	B1	B2	C	D	D2	D3	E	E2	H	L	L1	L2	L3	P
Min.	2.10	0.95	0.30	0.40	0.60	0.40	5.30	6.70	2.20	6.40	4.80	9.20	0.89	0.90	0.50	0.00	2.10
Max.	2.50	1.30	0.85	0.94	1.00	0.60	6.20	7.30	3.00	6.70	5.45	10.15	1.70	1.65	1.10	0.30	2.50

Footprint

