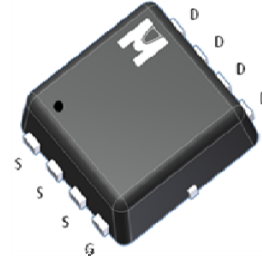


N-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

BV _{DSS}	30V
R _{DS(on)} (MAX.)	15mΩ
I _D	16A



UIS, Rg 100% Tested

Pb-Free Lead Plating & Halogen Free

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V _{GS}	±20	V
Continuous Drain Current	T _C = 25 °C	I _D	16	A
	T _A = 25 °C		9.8	
	T _C = 100 °C		11.6	
Pulsed Drain Current ¹		I _{DM}	64	
Avalanche Current		I _{AS}	10	
Avalanche Energy	L = 0.1mH, I _{AS} =10A, R _G =25Ω	E _{AS}	5	mJ
Repetitive Avalanche Energy ²	L = 0.05mH	E _{AR}	2.5	
Power Dissipation	T _C = 25 °C	P _D	21	W
	T _C = 100 °C		8.3	
Power Dissipation	T _A = 25 °C	P _D	2.5	W
	T _A = 100 °C		1	
Operating Junction & Storage Temperature Range		T _J , T _{stg}	-55 to 150	°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	R _{θJC}		6	°C / W
Junction-to-Ambient ³	R _{θJA}		50	

¹Pulse width limited by maximum junction temperature.

²Duty cycle ≤ 1%

³50°C / W when mounted on a 1 in² pad of 2 oz copper.



ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0V, I _D = 250μA	30			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250μA	1	1.5	3	
Gate-Body Leakage	I _{GSS}	V _{DS} = 0V, V _{GS} = ±20V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 24V, V _{GS} = 0V			1	μA
		V _{DS} = 20V, V _{GS} = 0V, T _J = 125 °C			25	
On-State Drain Current ¹	I _{D(ON)}	V _{DS} = 10V, V _{GS} = 10V	16			A
Drain-Source On-State Resistance ¹	R _{DS(ON)}	V _{GS} = 10V, I _D = 10A		12	15	mΩ
		V _{GS} = 4.5V, I _D = 6A		18	24	
Forward Transconductance ¹	g _{fs}	V _{DS} = 5V, I _D = 10A		18		S
DYNAMIC						
Input Capacitance	C _{iss}	V _{GS} = 0V, V _{DS} = 15V, f = 1MHz		730		pF
Output Capacitance	C _{oss}			112		
Reverse Transfer Capacitance	C _{rss}			96		
Gate Resistance	R _g	V _{GS} = 15mV, V _{DS} = 0V, f = 1MHz		1.8		Ω
Total Gate Charge ^{1,2}	Q _g (V _{GS} =10V)	V _{DS} = 15V, V _{GS} = 10V, I _D = 10A		14.8		nC
	Q _g (V _{GS} =4.5V)			7.6		
Gate-Source Charge ^{1,2}	Q _{gs}			2.9		
Gate-Drain Charge ^{1,2}	Q _{gd}			4.2		
Turn-On Delay Time ^{1,2}	t _{d(on)}	V _{DS} = 15V, I _D = 1A, V _{GS} = 10V, R _{GS} = 6Ω		10		nS
Rise Time ^{1,2}	t _r			12		
Turn-Off Delay Time ^{1,2}	t _{d(off)}			20		
Fall Time ^{1,2}	t _f			15		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25 °C)						
Continuous Current	I _S				16	A
Pulsed Current ³	I _{SM}				64	
Forward Voltage ¹	V _{SD}	I _F = I _S , V _{GS} = 0V			1.2	V
Reverse Recovery Time	t _{rr}	I _F = I _S , dI _F /dt = 100A / μS		10		nS
Peak Reverse Recovery Current	I _{RM(REC)}			35		A
Reverse Recovery Charge	Q _{rr}			12		nC

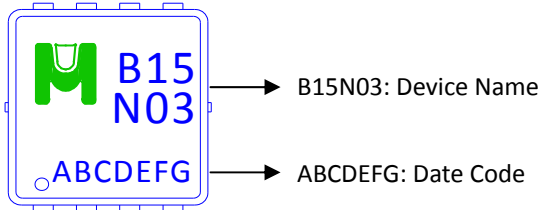
¹Pulse test : Pulse Width $\leq 300 \mu\text{sec}$, Duty Cycle $\leq 2\%$.

²Independent of operating temperature.

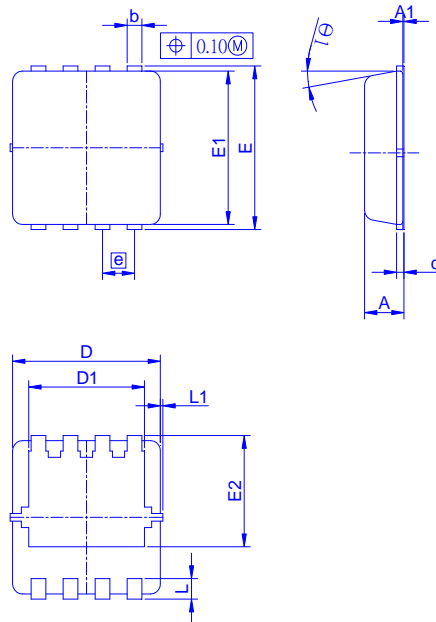
³Pulse width limited by maximum junction temperature.

Ordering & Marking Information:

Device Name: EMB15N03V for EDFN 3 x 3



Outline Drawing



Dimension in mm

Dimension	A	A1	b	c	D	D1	E	E1	E2	e	L	L1	θ
Min.	0.65	0	0.20	0.10	2.90	2.15	3.10	2.90	1.53	0.55	0.25	-	0°
Typ.	0.75	-	0.30	0.15	3.00	2.45	3.20	3.00	1.97	0.65	0.40	0.075	10°
Max.	0.90	0.05	0.40	0.25	3.30	2.74	3.50	3.30	2.59	0.75	0.60	0.150	14°

Recommended minimum pads

