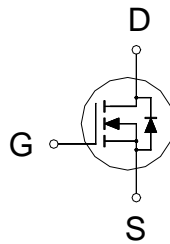


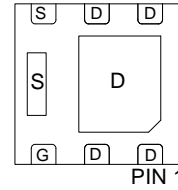
N-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

$BV_{DSS}$	30V
$R_{DS(on)} (MAX.)$	15m $\Omega$
$I_D$	8A



Bottom View



UIS, Rg 100% Tested

Pb-Free Lead Plating & Halogen Free



ABSOLUTE MAXIMUM RATINGS ( $T_A = 25\text{ }^\circ\text{C}$  Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		$V_{GS}$	$\pm 20$	V
Continuous Drain Current	$T_A = 25\text{ }^\circ\text{C}$	$I_D$	8	A
	$T_A = 100\text{ }^\circ\text{C}$		6	
Pulsed Drain Current <sup>1</sup>		$I_{DM}$	32	
Avalanche Current		$I_{AS}$	10	
Avalanche Energy	$L = 0.1\text{mH}, I_D = 10\text{A}, R_G = 25\Omega$	$E_{AS}$	5	mJ
Repetitive Avalanche Energy <sup>2</sup>	$L = 0.05\text{mH}$	$E_{AR}$	2.5	
Power Dissipation	$T_A = 25\text{ }^\circ\text{C}$	$P_D$	2.08	W
	$T_A = 100\text{ }^\circ\text{C}$		0.83	
Operating Junction & Storage Temperature Range		$T_{j}, T_{stg}$	-55 to 150	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	$R_{\theta JC}$		12	$^\circ\text{C} / \text{W}$
Junction-to-Ambient <sup>3</sup>	$R_{\theta JA}$		60	

<sup>1</sup>Pulse width limited by maximum junction temperature.

<sup>2</sup>Duty cycle  $\leq 1\%$

<sup>3</sup>60 $^\circ\text{C} / \text{W}$  when mounted on a 1 in<sup>2</sup> pad of 2 oz copper.



ELECTRICAL CHARACTERISTICS ( $T_A = 25\text{ }^\circ\text{C}$ , Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
<b>STATIC</b>						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	30			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	1	1.5	3	
Gate-Body Leakage	$I_{GSS}$	$V_{DS} = 0V, V_{GS} = \pm 20V$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 24V, V_{GS} = 0V$			1	$\mu A$
		$V_{DS} = 20V, V_{GS} = 0V, T_J = 125\text{ }^\circ\text{C}$			25	
On-State Drain Current <sup>1</sup>	$I_{D(ON)}$	$V_{DS} = 10V, V_{GS} = 10V$	8			A
Drain-Source On-State Resistance <sup>1</sup>	$R_{DS(ON)}$	$V_{GS} = 10V, I_D = 8A$		12	15	$m\Omega$
		$V_{GS} = 4.5V, I_D = 5A$		18	24	
Forward Transconductance <sup>1</sup>	$g_{fs}$	$V_{DS} = 5V, I_D = 8A$		18		S
<b>DYNAMIC</b>						
Input Capacitance	$C_{iss}$	$V_{GS} = 0V, V_{DS} = 15V, f = 1MHz$		597		$pF$
Output Capacitance	$C_{oss}$			111		
Reverse Transfer Capacitance	$C_{rss}$			96		
Gate Resistance	$R_g$	$V_{GS} = 15mV, V_{DS} = 0V, f = 1MHz$		2.0		$\Omega$
Total Gate Charge <sup>1,2</sup>	$Q_g(V_{GS}=10V)$	$V_{DS} = 15V, V_{GS} = 10V, I_D = 8A$		13.3		nC
	$Q_g(V_{GS}=4.5V)$			7.0		
Gate-Source Charge <sup>1,2</sup>	$Q_{gs}$			2.2		
Gate-Drain Charge <sup>1,2</sup>	$Q_{gd}$			3.9		
Turn-On Delay Time <sup>1,2</sup>	$t_{d(on)}$		$V_{DS} = 15V, I_D = 1A, V_{GS} = 10V, R_{GS} = 6\Omega$		10	
Rise Time <sup>1,2</sup>	$t_r$			8		
Turn-Off Delay Time <sup>1,2</sup>	$t_{d(off)}$			20		
Fall Time <sup>1,2</sup>	$t_f$			10		
<b>SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (<math>T_C = 25\text{ }^\circ\text{C}</math>)</b>						
Continuous Current	$I_S$				8	A
Pulsed Current <sup>3</sup>	$I_{SM}$				32	
Forward Voltage <sup>1</sup>	$V_{SD}$	$I_F = I_S, V_{GS} = 0V$			1.2	V
Reverse Recovery Time	$t_{rr}$	$I_F = I_S, di_F/dt = 100A / \mu S$		15		nS
Reverse Recovery Charge	$Q_{rr}$			12		nC

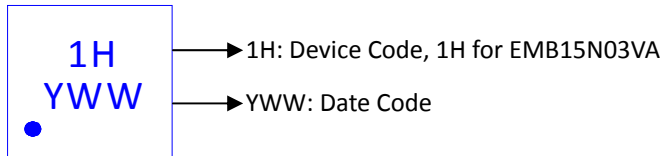
<sup>1</sup>Pulse test : Pulse Width  $\leq 300\text{ }\mu\text{sec}$ , Duty Cycle  $\leq 2\%$ .

<sup>2</sup>Independent of operating temperature.

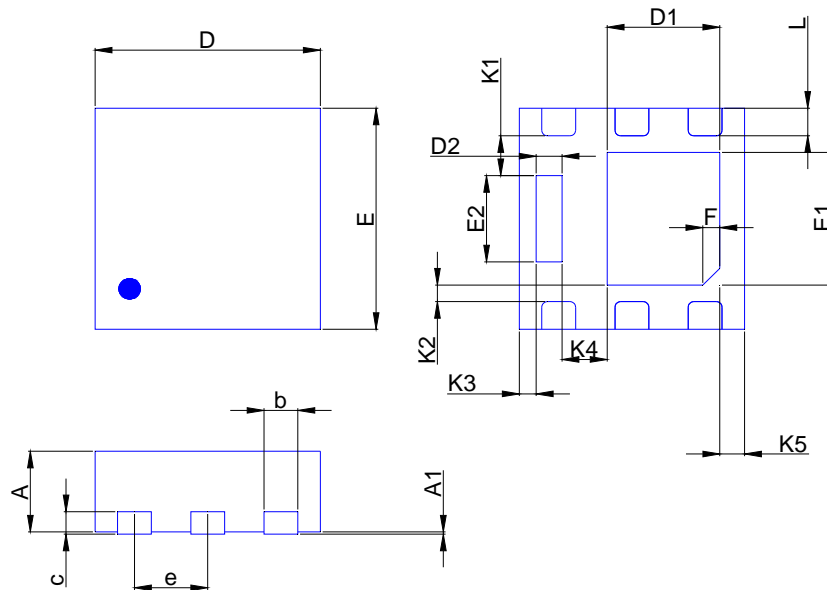
<sup>3</sup>Pulse width limited by maximum junction temperature.

### Ordering & Marking Information:

Device Name: EMB15N03VA for EDFN 2 x 2



### Outline Drawing



Dimension in mm

Dimension	A	A1	b	c	D	D1	D2	E	E1	E2	e	F	f	K1	K2	L	K3	K4	K5
Min.	0.70	0.00	0.25		1.9	0.9	0.13	1.9	1.1	0.68				0.306	0.10	0.2	0.10	0.35	0.17
Typ.	0.75	0.02	0.30	0.203	2.0	1.0	0.23	2.0	1.2	0.78	0.65	0.15	45°	0.356	0.15	0.25	0.15	0.40	0.22
Max.	0.80	0.05	0.35		2.1	1.1	0.33	2.1	1.3	0.88				0.406	0.20	0.3	0.20	0.45	0.27

### Recommended minimum pads

