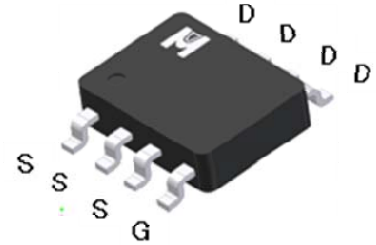


N-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

BV <sub>DSS</sub>	30V
R <sub>DS(on)</sub> (MAX.)	17mΩ
I <sub>D</sub>	12A



UIS, R<sub>g</sub> 100% Tested

Pb-Free Lead Plating & Halogen Free



ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub> = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V <sub>GS</sub>	±20	V
Continuous Drain Current	T <sub>A</sub> = 25 °C	I <sub>D</sub>	12	A
	T <sub>A</sub> = 100 °C		8	
Pulsed Drain Current <sup>1</sup>		I <sub>DM</sub>	48	
Avalanche Current		I <sub>AS</sub>	12	
Avalanche Energy	L = 0.1mH, I <sub>D</sub> =10A, R <sub>G</sub> =25Ω	E <sub>AS</sub>	5	mJ
Repetitive Avalanche Energy <sup>2</sup>	L = 0.05mH	E <sub>AR</sub>	2.5	
Power Dissipation	T <sub>A</sub> = 25 °C	P <sub>D</sub>	2.5	W
	T <sub>A</sub> = 100 °C		1	
Operating Junction & Storage Temperature Range		T <sub>j</sub> , T <sub>stg</sub>	-55 to 150	°C

100% UIS testing in condition of V<sub>D</sub>=15V, L=0.1mH, V<sub>G</sub>=10V, I<sub>L</sub>=10A, Rated V<sub>DS</sub>=30V N-CH

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	R <sub>θJC</sub>		25	°C / W
Junction-to-Ambient <sup>3</sup>	R <sub>θJA</sub>		50	

<sup>1</sup>Pulse width limited by maximum junction temperature.

<sup>2</sup>Duty cycle ≤ 1%

<sup>3</sup>50°C / W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper.



ELECTRICAL CHARACTERISTICS ( $T_c = 25\text{ }^\circ\text{C}$ , Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
<b>STATIC</b>						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	30			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	1	1.5	3	
Gate-Body Leakage	$I_{GSS}$	$V_{DS} = 0V, V_{GS} = \pm 20V$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 24V, V_{GS} = 0V$			1	$\mu A$
		$V_{DS} = 20V, V_{GS} = 0V, T_J = 125\text{ }^\circ\text{C}$			25	
On-State Drain Current <sup>1</sup>	$I_{D(ON)}$	$V_{DS} = 10V, V_{GS} = 10V$	12			A
Drain-Source On-State Resistance <sup>1</sup>	$R_{DS(ON)}$	$V_{GS} = 10V, I_D = 12A$		14.5	17	$m\Omega$
		$V_{GS} = 4.5V, I_D = 6A$		21	26	
Forward Transconductance <sup>1</sup>	$g_{fs}$	$V_{DS} = 5V, I_D = 12A$		18		S
<b>DYNAMIC</b>						
Input Capacitance	$C_{iss}$	$V_{GS} = 0V, V_{DS} = 15V, f = 1MHz$		597		$pF$
Output Capacitance	$C_{oss}$			111		
Reverse Transfer Capacitance	$C_{rss}$			96		
Gate Resistance	$R_g$	$V_{GS} = 15mV, V_{DS} = 0V, f = 1MHz$		2.0		$\Omega$
Total Gate Charge <sup>1,2</sup>	$Q_g(V_{GS}=10V)$	$V_{DS} = 15V, V_{GS} = 10V, I_D = 12A$		14		nC
	$Q_g(V_{GS}=4.5V)$			7.8		
Gate-Source Charge <sup>1,2</sup>	$Q_{gs}$			1.8		
Gate-Drain Charge <sup>1,2</sup>	$Q_{gd}$			4.7		
Turn-On Delay Time <sup>1,2</sup>	$t_{d(on)}$		$V_{DS} = 15V, I_D = 1A, V_{GS} = 10V, R_{GS} = 6\Omega$		11	
Rise Time <sup>1,2</sup>	$t_r$			16		
Turn-Off Delay Time <sup>1,2</sup>	$t_{d(off)}$			36		
Fall Time <sup>1,2</sup>	$t_f$			20		
<b>SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (<math>T_c = 25\text{ }^\circ\text{C}</math>)</b>						
Continuous Current	$I_S$				2.3	A
Pulsed Current <sup>3</sup>	$I_{SM}$				9.2	
Forward Voltage <sup>1</sup>	$V_{SD}$	$I_F = I_S, V_{GS} = 0V$			1.2	V
Reverse Recovery Time	$t_{rr}$	$I_F = I_S, di_F/dt = 100A / \mu S$		50		nS
Peak Reverse Recovery Current	$I_{RM(REC)}$			30		A
Reverse Recovery Charge	$Q_{rr}$			2		nC

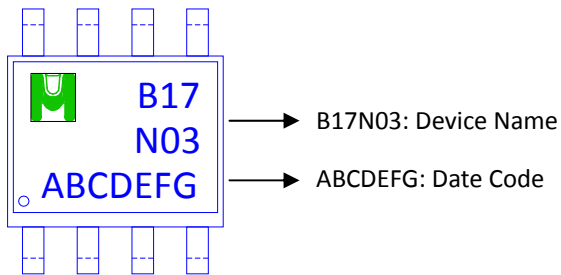
<sup>1</sup>Pulse test : Pulse Width  $\leq 300 \mu\text{sec}$ , Duty Cycle  $\leq 2\%$ .

<sup>2</sup>Independent of operating temperature.

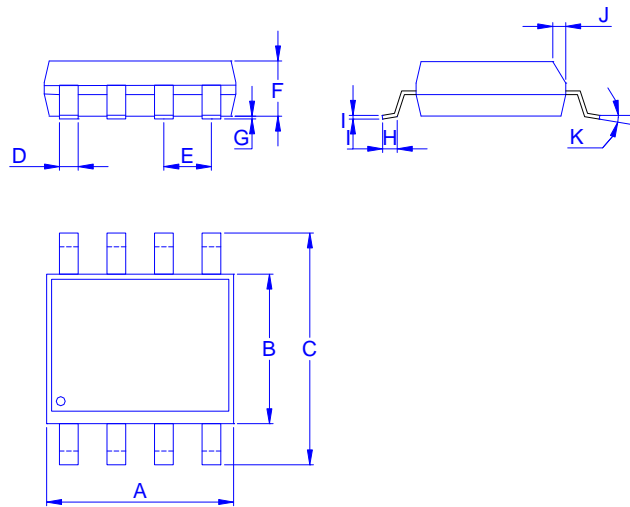
<sup>3</sup>Pulse width limited by maximum junction temperature.

Ordering & Marking Information:

Device Name: EMB17N03G for SOP-8



Outline Drawing



Dimension in mm

Dimension	A	B	C	D	E	F	G	H	I	J	K
Min.	4.70	3.70	5.80	0.33		1.20	0.08	0.40	0.19	0.25	0°
Typ.					1.27						
Max.	5.10	4.10	6.20	0.51		1.62	0.28	0.83	0.26	0.50	8°

