杰力科技股份有限公司
Excelliance MOS Corporation

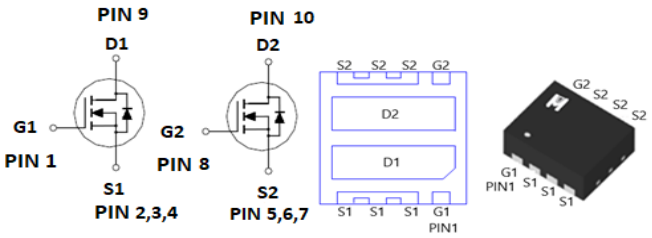
EMB18A04VB

Dual N-Channel Logic Level Enhancement Mode Field Effect Transistor

▪Product Summary:

	Q1	Q2
BVDSS	40V	40V
$R_{DSON\ (MAX.)}$@V_{GS}=10V	18mΩ	18mΩ
$R_{DSON\ (MAX.)}$@V_{GS}=4.5V	25mΩ	25mΩ
I_D @T_C=25°C	28A	28A
I_D @T_A=25°C	10A	10A

▪ Pin Description:



DFN3.0X3.0A-08

Dual N Channel MOSFET
UIS, Rg 100% Tested
Pb-Free Lead Plating & Halogen Free

▪ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS		UNIT
			Q1	Q2	
Gate-Source Voltage		V_{GS}	20/-20	20/-20	V
Continuous Drain Current	T_C = 25 °C	I_D	28	28	A
	T_C = 100 °C		18	18	
Continuous Drain Current	T_A = 25 °C	I_D	10	10	
	T_A = 70 °C		8	8	
Pulsed Drain Current[1]		I_{DM}	95	95	
Avalanche Current		I_{AS}	25	25	
Avalanche Energy	L = 0.1mH	EAS	31	31	mJ
	L = 0.01mH	EAS	3	3	
Repetitive Avalanche Energy[2]	L = 0.05mH	EAR	16	16	
Power Dissipation	T_C = 25 °C	P_D	24	24	W
	T_C = 100 °C		9.6	9.6	
Power Dissipation	T_A = 25 °C	P_D	3.1	3.1	W
	T_A = 70 °C		2	2	
Operating Junction & Storage Temperature Range		T_j, T_{stg}	-55 to 150		°C

▪ 100% UIS testing in condition of VD=35V, L=0.1mH, VG=10V, IL= 15A, Rated VDS=40V N-CH_Q1

▪ 100% UIS testing in condition of VD=35V, L=0.1mH, VG=10V, IL= 15A, Rated VDS=40V N-CH_Q2

▪THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE		SYMBOL	TYPICAL	MAXIMUM		UNIT
				Q1	Q2	
Junction-to-Case		$R_{\theta JC}$		5.2	5.2	°C/W
Junction-to-Ambient[3]	t≦10s	$R_{\theta JA}$		40	40	
	Steady-State	$R_{\theta JA}$		60	60	

[1]Pulse width limited by maximum junction temperature.
[2]Duty cycle < 1%
[3]60°C / W when mounted on a 1 in^2 pad of 2 oz copper.
[4]Guarantee by Engineering test

▪ **Q1_ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)**

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage[4]	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = 250uA	40			V
Gate Threshold Voltage[4]	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250uA	1.2	1.8	2.5	
Gate-Body Leakage[4]	I_{GSS}	V_{DS} = 0V, V_{GS} = +20V/-20V			±100	nA
Zero Gate Voltage Drain Current[4]	I_{DSS}	V_{DS} = 40V, V_{GS} = 0V			1	uA
		V_{DS} =32V, V_{GS} =0V, T_J = 125 °C			25	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 10V, V_{GS} = 10V	28			A
Drain-Source On-State Resistance[1,4]	$R_{DS(ON)}$	V_{GS} = 10V, I_D = 17A		15	18	mΩ
		V_{GS} = 4.5V, I_D = 10A		19	25	
DYNAMIC						
Input Capacitance[5]	C_{iss}	V_{GS} = 0V, V_{DS} = 20V, f = 1MHz		619		pF
Output Capacitance[5]	C_{oss}			77		
Reverse Transfer Capacitance[5]	C_{rss}			50		
Gate Resistance[4,5]	R_g	f = 1MHz		0.7		Ω
Total Gate Charge[1,2,5]	Q_g(V_{GS}=10V)	V_{DS} = 20V, V_{GS} = 10V, I_D = 7A		12		nC
	Q_g(V_{GS}=4.5V)			5.6		
Gate-Source Charge[1,2,5]	Q_{gs}			2.5		
Gate-Drain Charge[1,2,5]	Q_{gd}			2.1		
Turn-On Delay Time[1,2,5]	$t_{d(on)}$	V_{DS} = 20V, V_{GS} = 10V, I_D = 5A , Rg = 3Ω		5.6		nS
Rise Time[1,2,5]	t_r			8		
Turn-Off Delay Time[1,2,5]	$t_{d(off)}$			13		
Fall Time[1,2,5]	t_f			6.6		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS						
Continuous Current	I_S				28	A
Pulsed Current[3]	I_{SM}				95	
Forward Voltage[1,4]	V_{SD}	I_F = 7A, V_{GS} = 0V			1.3	V
Reverse Recovery Time[5]	t_{rr}	I_F = 7A, di/dt = 100A / uS		7.5		nS
Peak Reverse Recovery Current[5]	$I_{RM(REC)}$			0.6		A
Reverse Recovery Charge[5]	Q_{rr}			2.4		nC

[1]Pulse test : Pulse Width ≦ 300 usec, Duty Cycle ≦ 2%.

[2]Independent of operating temperature.

[3]Pulse width limited by maximum junction temperature.

[4]Guarantee by FT test Item

[5]Guarantee by Engineering test

EMC will review datasheet by quarter, and update new version.

▪Q1_TYPICAL CHARACTERISTICS

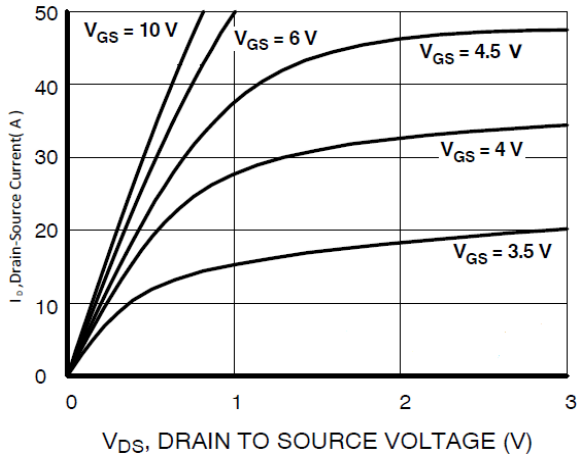


Fig.1 Typical Output Characteristics

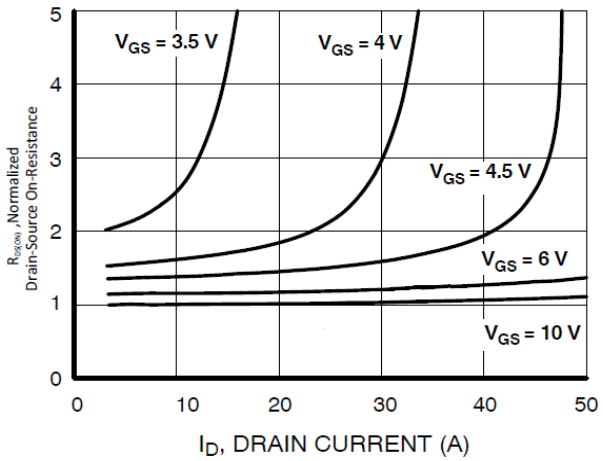


Fig.2 On-Resistance Variation with Drain Current and Gate Voltage

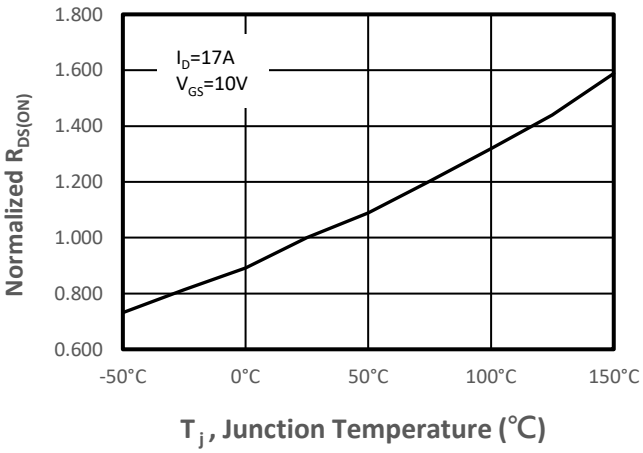


Fig.3 Normalized On-Resistance v.s. Junction Temperature

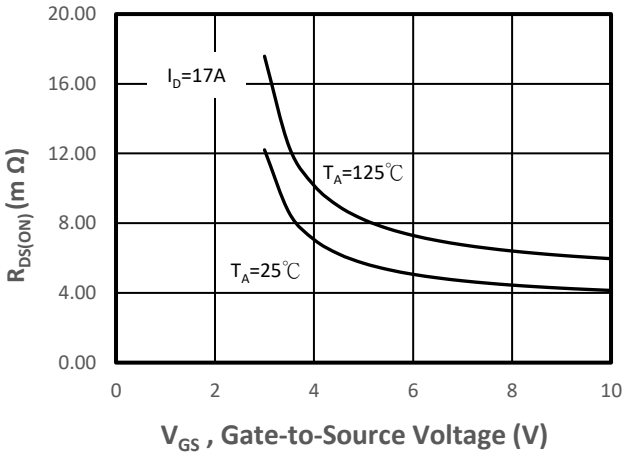


Fig.4 On-Resistance v.s. Gate Voltage

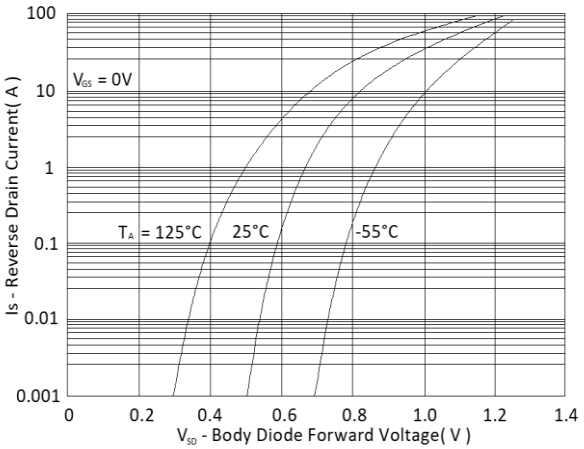


Fig.5 Forward Characteristic of Reverse Diode

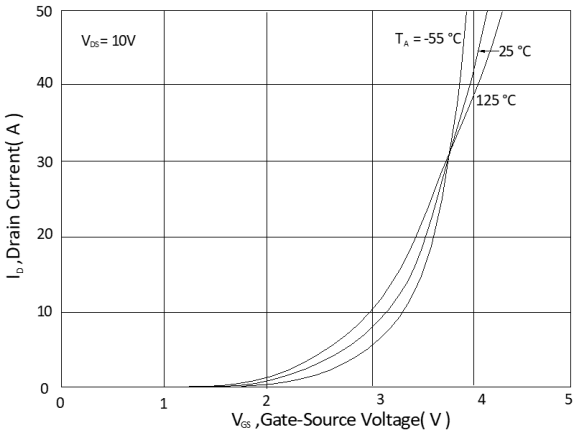


Fig.6 Transfer Characteristics

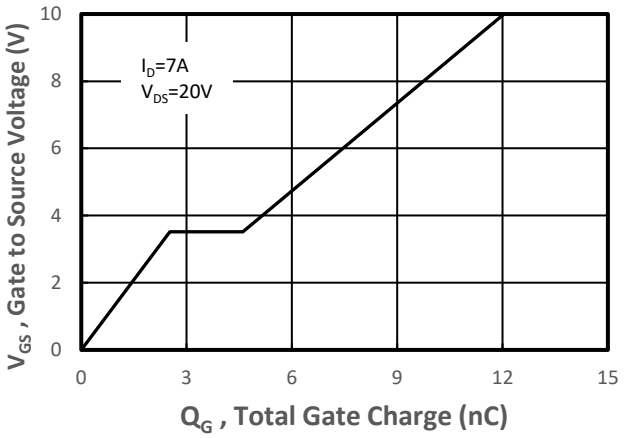


Fig.7 Gate Charge Characteristics

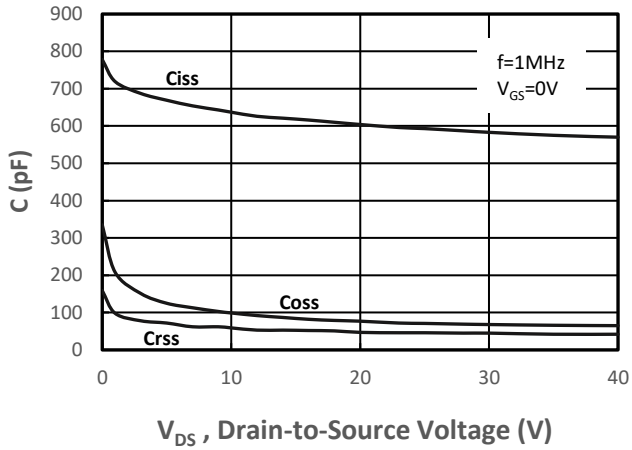


Fig.8 Typical Capacitance Characteristics

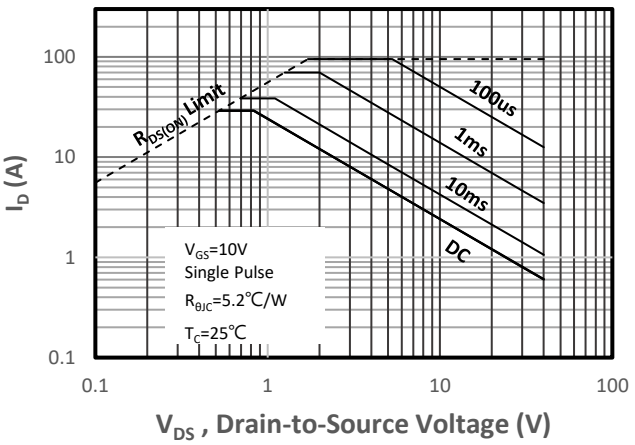


Fig 9. Maximum Safe Operating Area

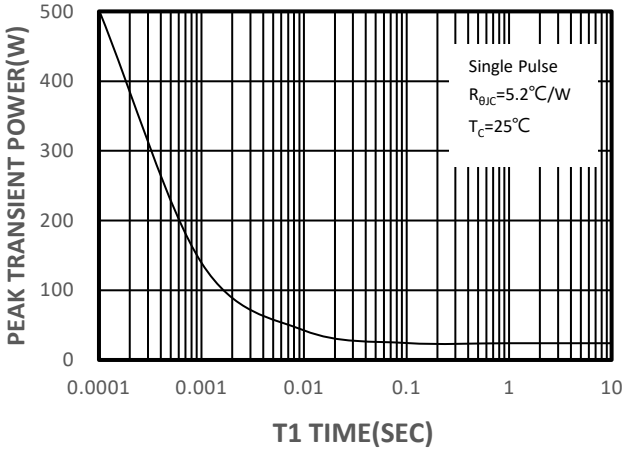


Fig 10. Single Pulse Maximum Power Dissipation

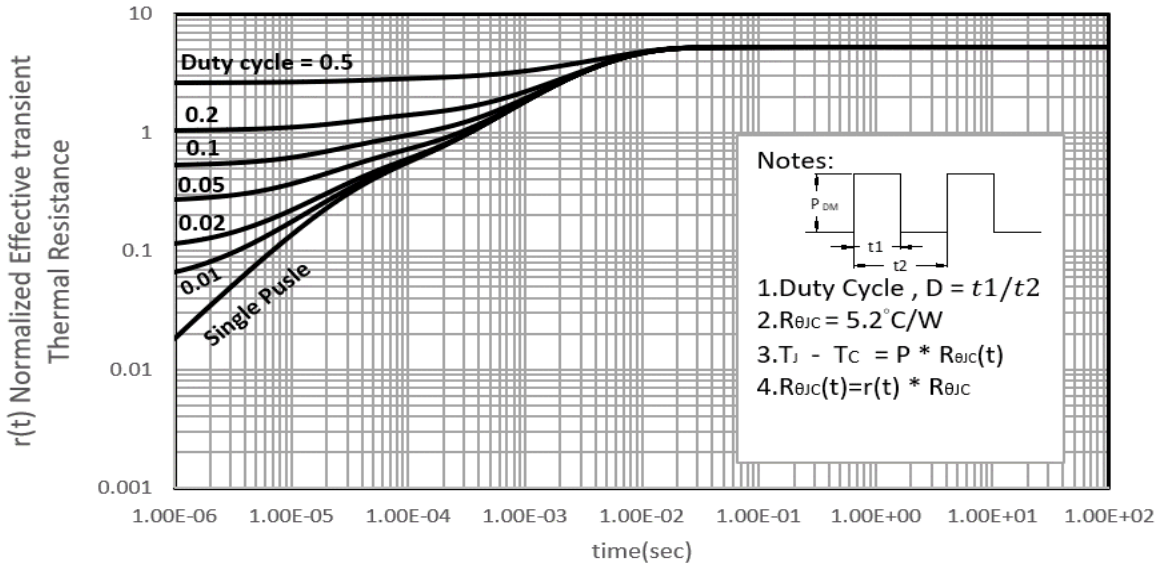


Fig 11. Effective Transient Thermal Impedance

▪ **Q2_ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)**

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage[4]	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = 250uA	40			V
Gate Threshold Voltage[4]	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250uA	1.2	1.8	2.5	
Gate-Body Leakage[4]	I_{GSS}	V_{DS} = 0V, V_{GS} = +20V/-20V			±100	nA
Zero Gate Voltage Drain Current[4]	I_{DSS}	V_{DS} = 40V, V_{GS} = 0V			1	uA
		V_{DS} =32V, V_{GS} =0V, T_J = 125 °C			25	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 10V, V_{GS} = 10V	28			A
Drain-Source On-State Resistance[1,4]	$R_{DS(ON)}$	V_{GS} = 10V, I_D = 17A		15	18	mΩ
		V_{GS} = 4.5V, I_D = 10A		19	25	
DYNAMIC						
Input Capacitance[5]	C_{iss}	V_{GS} = 0V, V_{DS} = 20V, f = 1MHz		628		pF
Output Capacitance[5]	C_{oss}			77		
Reverse Transfer Capacitance[5]	C_{rss}			50		
Gate Resistance[4,5]	R_g	f = 1MHz		1.0		Ω
Total Gate Charge[1,2,5]	Q_g(V_{GS}=10V)	V_{DS} = 20V, V_{GS} = 10V, I_D = 7A		12		nC
	Q_g(V_{GS}=4.5V)			5.6		
Gate-Source Charge[1,2,5]	Q_{gs}			2.6		
Gate-Drain Charge[1,2,5]	Q_{gd}			2		
Turn-On Delay Time[1,2,5]	$t_{d(on)}$	V_{DS} = 20V, V_{GS} = 10V, I_D = 5A , Rg = 3Ω		6.6		nS
Rise Time[1,2,5]	t_r			8.1		
Turn-Off Delay Time[1,2,5]	$t_{d(off)}$			15		
Fall Time[1,2,5]	t_f			2.4		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS						
Continuous Current	I_S				28	A
Pulsed Current[3]	I_{SM}				95	
Forward Voltage[1,4]	V_{SD}	I_F =7A, V_{GS} = 0V			1.3	V
Reverse Recovery Time[5]	t_{rr}	I_F = 7A, di/dt = 100A / uS		7.9		nS
Peak Reverse Recovery Current[5]	$I_{RM(REC)}$			0.6		A
Reverse Recovery Charge[5]	Q_{rr}			2.5		nC

[1]Pulse test : Pulse Width ≦ 300 usec, Duty Cycle ≦ 2%.

[2]Independent of operating temperature.

[3]Pulse width limited by maximum junction temperature.

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▪Q2_TYPICAL CHARACTERISTICS

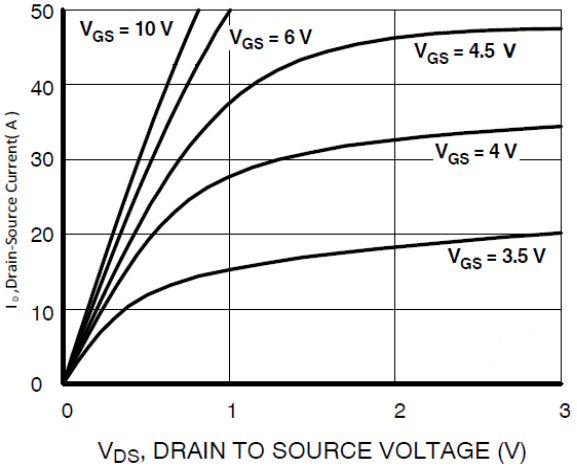


Fig.1 Typical Output Characteristics

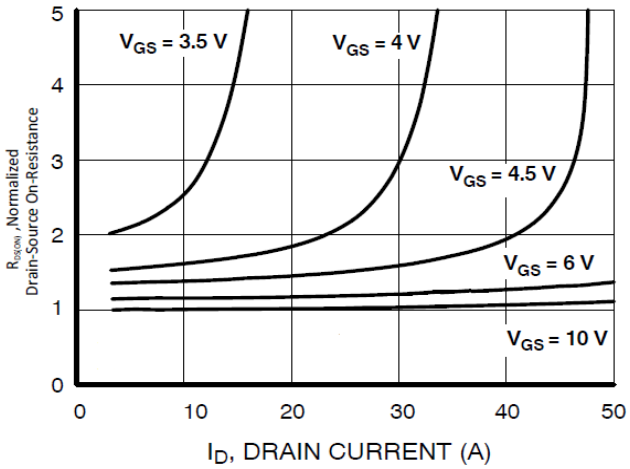


Fig.2 On-Resistance Variation with Drain Current and Gate Voltage

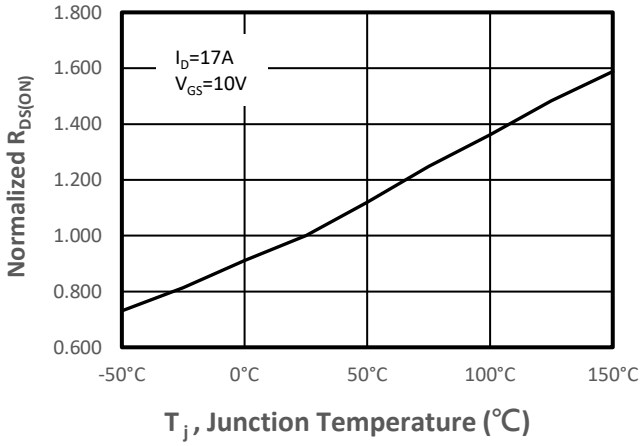


Fig.3 Normalized On-Resistance v.s. Junction Temperature

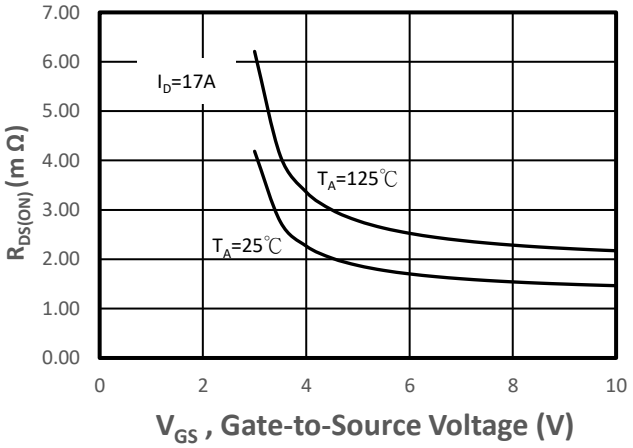


Fig.4 On-Resistance v.s. Gate Voltage

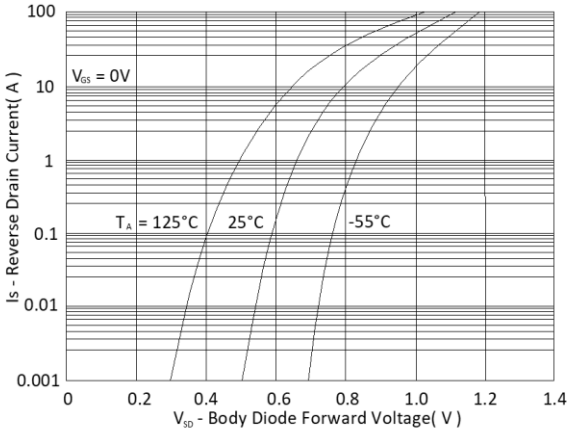


Fig.5 Forward Characteristic of Reverse Diode

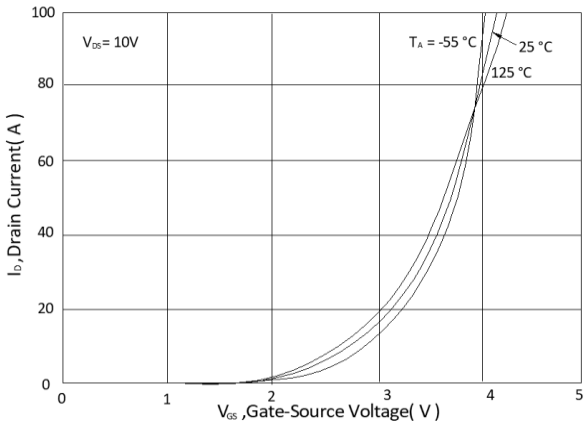


Fig.6 Transfer Characteristics

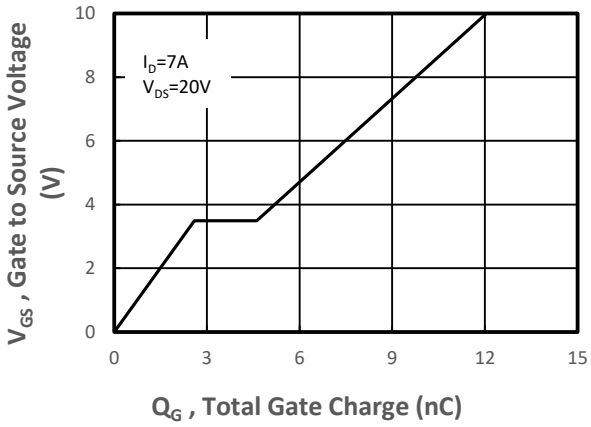


Fig.7 Gate Charge Characteristics

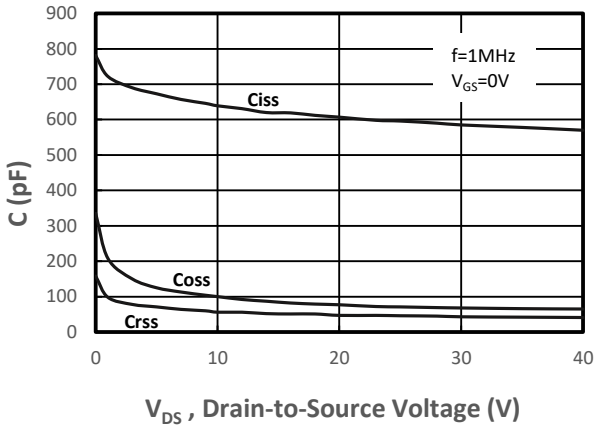


Fig.8 Typical Capacitance Characteristics

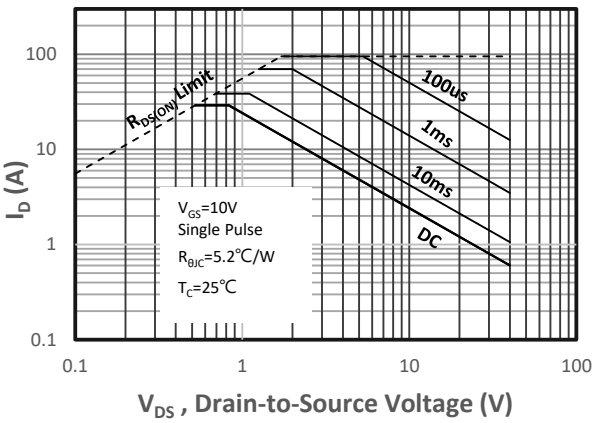


Fig 9. Maximum Safe Operating Area

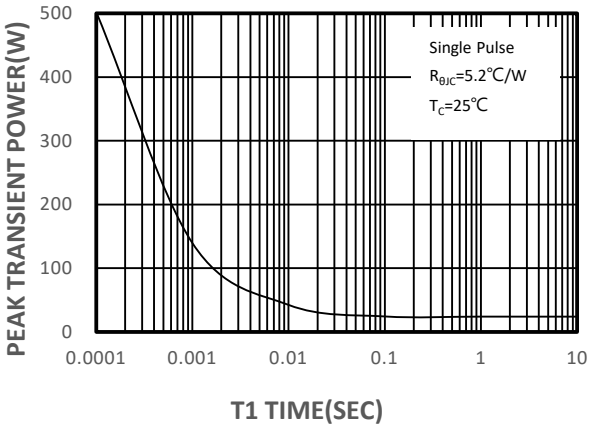


Fig 10. Single Pulse Maximum Power Dissipation

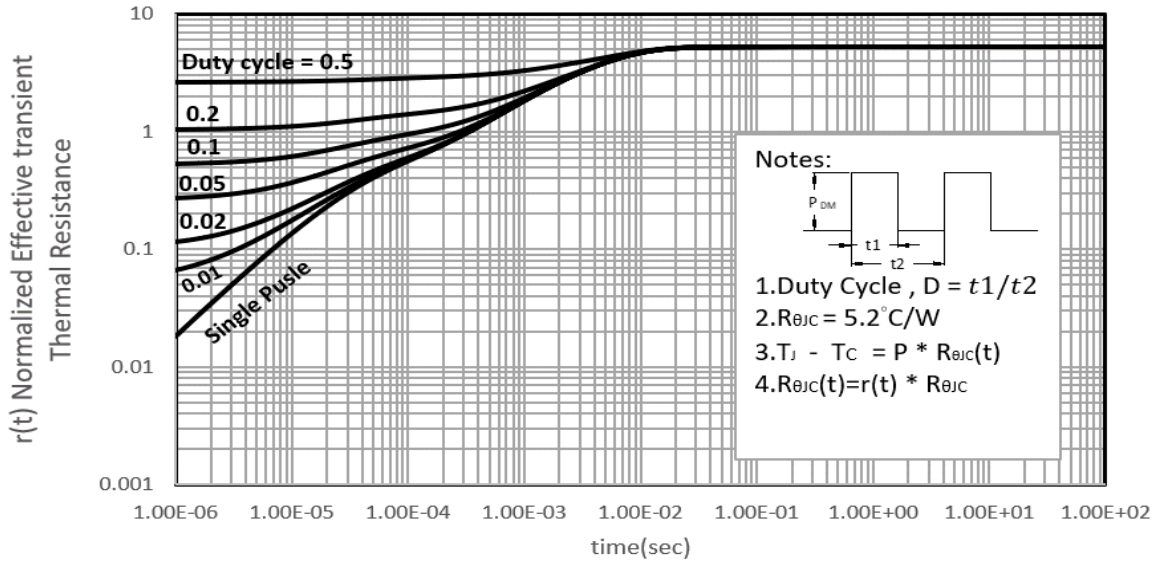


Fig 11. Effective Transient Thermal Impedance

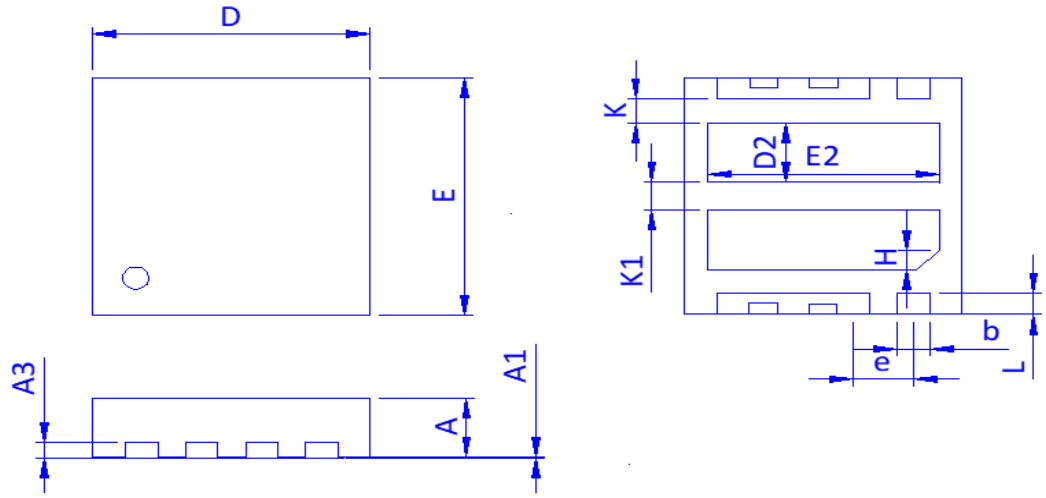
Ordering & Marking Information:

Device Name:EMB18A04VB for DFN3.0X3.0A-08

B18A04 : Device Name

ABCDEFG: Date Code
A: Assembly House
B: Year(A:2008 B:2009 C:2010….)
C: Month(A:01 B:02 C:03 D:04 E:05 F:06 G:07 H:08 I:09 J:10 K:11 L:12)
DEFG: Serial No.

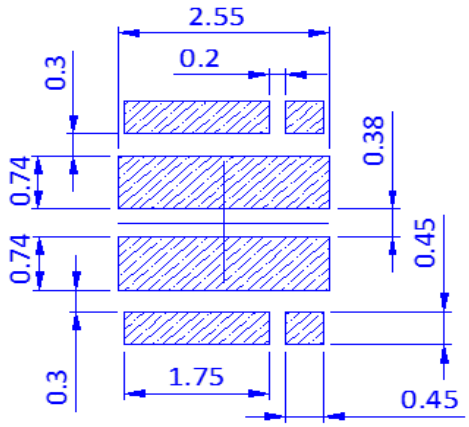
Outline Drawing



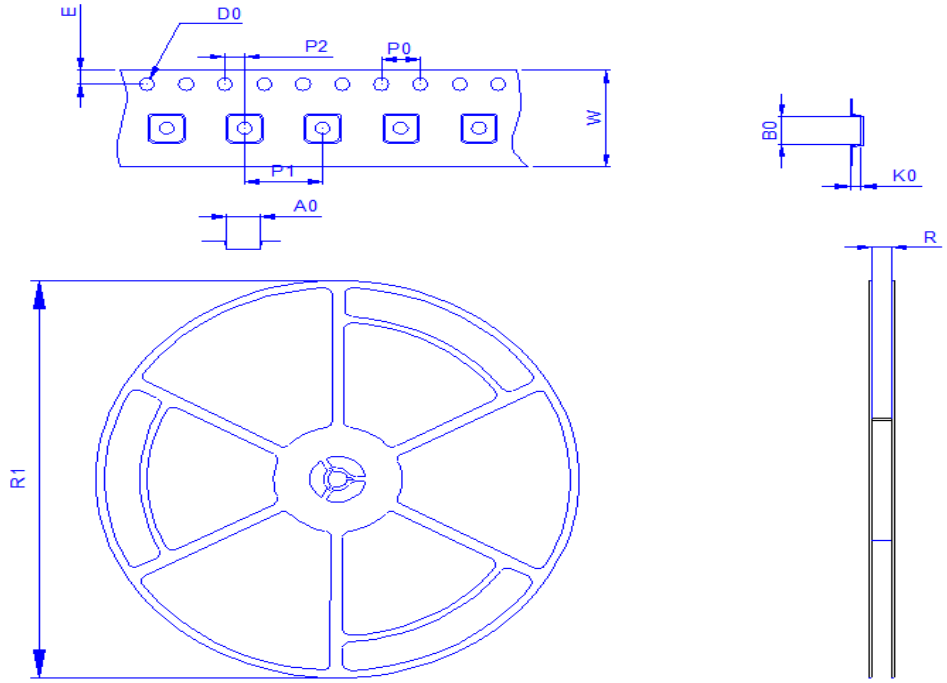
Dimension in mm

Dimension	A	A1	A3	b	D	E	D2	E2	e	H	K	K1	L
Min.	0.7	0		0.3	2.9	2.9	0.655	2.4	0.55				0.33
Typ.	0.75	0.02	0.2	0.35	3	3	0.755	2.5	0.65	0.25	0.3	0.35	0.27
Max.	0.8	0.05		0.4	3.1	3.1	0.855	2.6	0.75				0.32

Recommended minimum pads



◆ **Tape&Reel Information:5000pcs/Reel**



產品別	DFN3.0X3.0A-8L
Reel尺寸	13”
編帶方式	FEED DIRECTION

Dimension in mm

Dimension	Carrier tape									Reel	
	A0	B0	D0	E	K0	P0	P1	P2	W	R	R1
Typ.	3.30	3.30	1.50	1.75	1.10	4.00	8.00	2.00	12.00	12.40	330.00
±	0.30	0.20	0.20	0.20	0.40	0.20	0.20	0.20	0.50	REF	REF