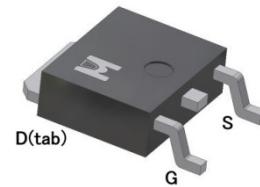
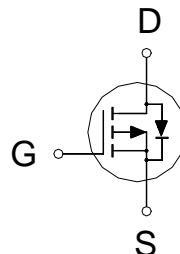


P-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

BV _{DSS}	-60V
R _{DSON} (MAX.)	15mΩ
I _D	-40A



UIS, R_G 100% Tested

Pb-Free Lead Plating & Halogen Free



ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V _{GS}	±20	V
Continuous Drain Current	T _C = 25 °C	I _D	-40	A
	T _C = 100 °C		-27	
Pulsed Drain Current ¹		I _{DM}	-100	
Avalanche Current		I _{AS}	-40	
Avalanche Energy	L = 0.1mH, ID=-40A, RG=25Ω	E _{AS}	80	mJ
Repetitive Avalanche Energy ²	L = 0.05mH	E _{AR}	40	
Power Dissipation	T _C = 25 °C	P _D	50	W
	T _C = 100 °C		25	
Operating Junction & Storage Temperature Range		T _j , T _{stg}	-55 to 150	°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	R _{θJC}	2.5	2.5	°C / W
Junction-to-Ambient	R _{θJA}		50	

¹Pulse width limited by maximum junction temperature.

²Duty cycle ≤ 1%

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$, Unless Otherwise Noted)

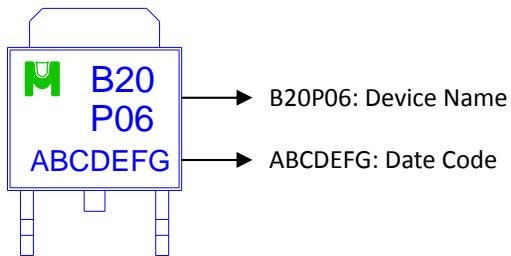
PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(\text{BR})\text{DSS}}$	$V_{GS} = 0V, I_D = -250\mu\text{A}$	-60			V
Gate Threshold Voltage	$V_{GS(\text{th})}$	$V_{DS} = V_{GS}, I_D = -250\mu\text{A}$	-1.0	-2.0	-3.0	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0V, V_{GS} = \pm 20V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -48V, V_{GS} = 0V$			-1	μA
		$V_{DS} = -40V, V_{GS} = 0V, T_J = 125^\circ\text{C}$			-25	
On-State Drain Current ¹	$I_{D(\text{ON})}$	$V_{DS} = -5V, V_{GS} = -10V$	-40			A
Drain-Source On-State Resistance ¹	$R_{DS(\text{ON})}$	$V_{GS} = -10V, I_D = -20\text{A}$		12	15	$\text{m}\Omega$
		$V_{GS} = -4.5V, I_D = -10\text{A}$		15	22	
Forward Transconductance ¹	g_{fs}	$V_{DS} = -5V, I_D = -20\text{A}$		36		S
DYNAMIC						
Input Capacitance	C_{iss}	$V_{GS} = 0V, V_{DS} = -30V, f = 1\text{MHz}$		6478		pF
Output Capacitance	C_{oss}			353		
Reverse Transfer Capacitance	C_{rss}			328		
Gate Resistance	R_g	$V_{GS} = 15\text{mV}, V_{DS} = 0V, f = 1\text{MHz}$		3.5		Ω
Total Gate Charge ^{1,2}	Q_g	$V_{DS} = -30V, V_{GS} = -10V, I_D = -20\text{A}$		111		nC
Gate-Source Charge ^{1,2}	Q_{gs}			24.7		
Gate-Drain Charge ^{1,2}	Q_{gd}			15.6		
Turn-On Delay Time ^{1,2}	$t_{d(\text{on})}$	$V_{DS} = -10V, I_D = -1\text{A}, V_{GS} = -10V, R_{GS} = 6\Omega$		20		nS
Rise Time ^{1,2}	t_r			25		
Turn-Off Delay Time ^{1,2}	$t_{d(\text{off})}$			70		
Fall Time ^{1,2}	t_f			30		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS ($T_C = 25^\circ\text{C}$)						
Continuous Current	I_S	$I_F = I_S, V_{GS} = 0V$			-40	A
Pulsed Current ³	I_{SM}				-100	
Forward Voltage ¹	V_{SD}				1.3	V
Reverse Recovery Time	t_{rr}			50		nS
Reverse Recovery Charge	Q_{rr}			80		

¹Pulse test : Pulse Width $\leq 300\ \mu\text{sec}$, Duty Cycle $\leq 2\%$.²Independent of operating temperature.

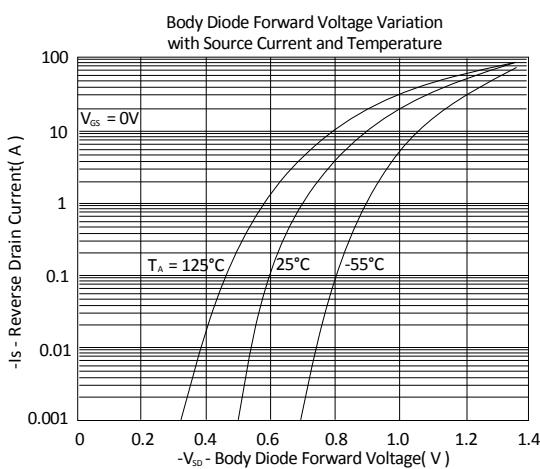
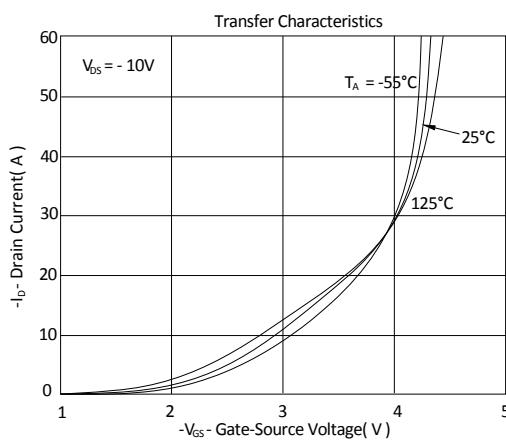
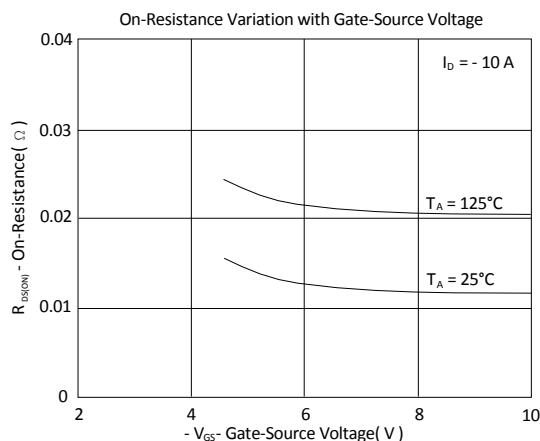
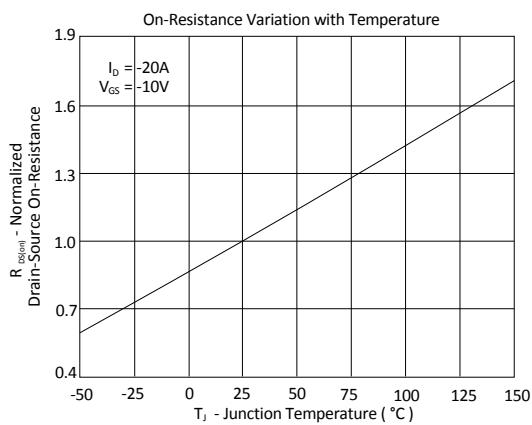
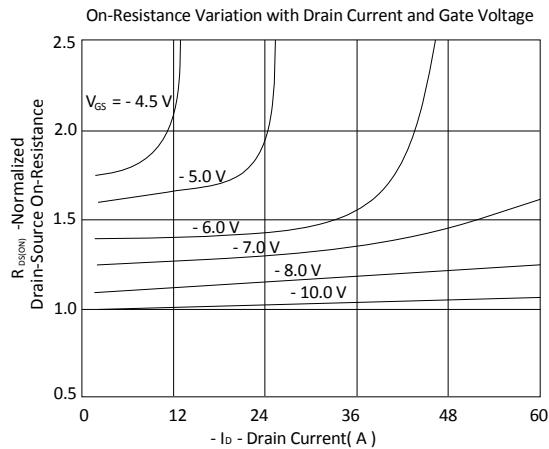
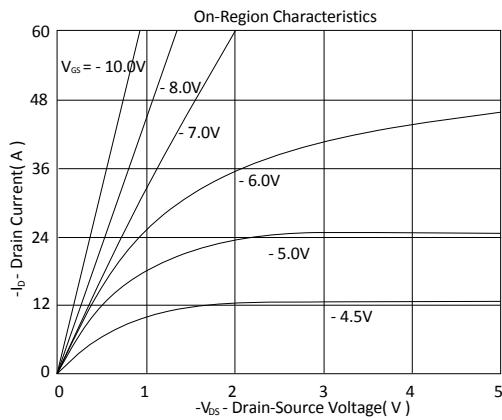
³Pulse width limited by maximum junction temperature.

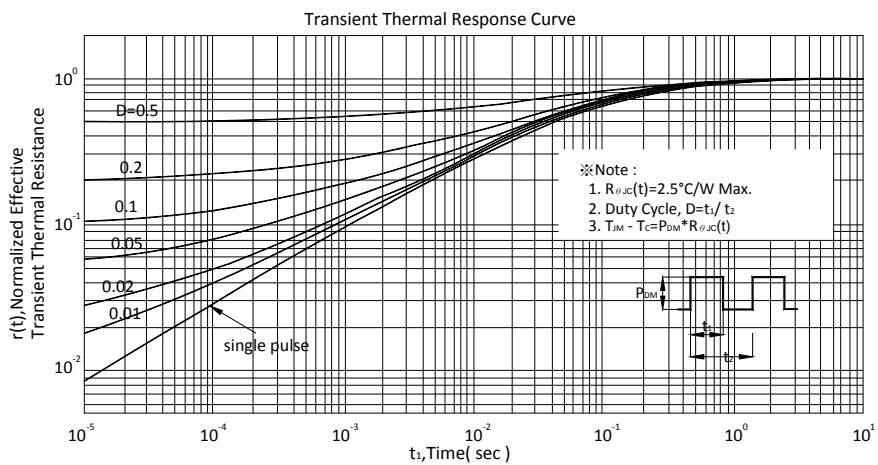
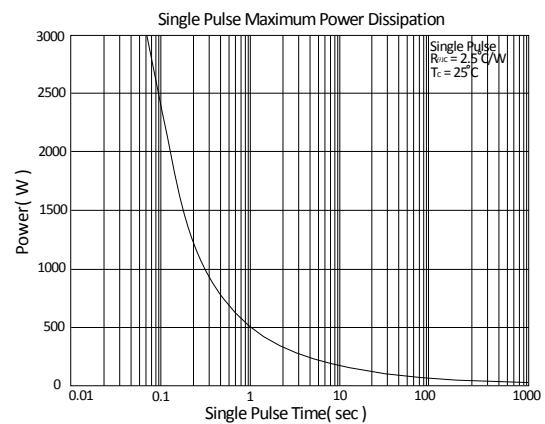
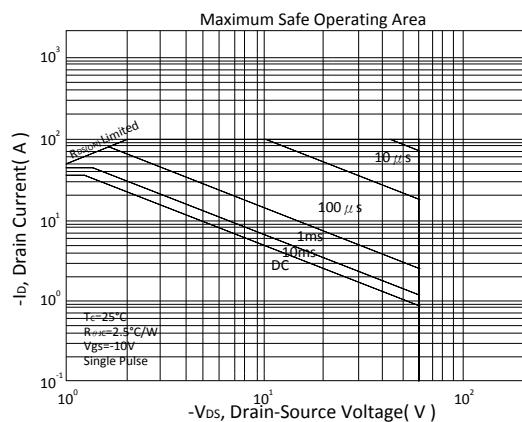
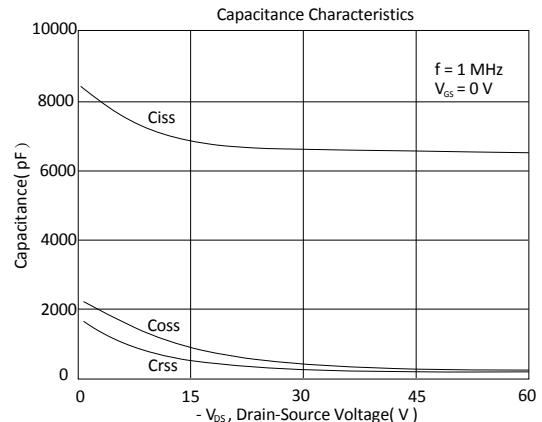
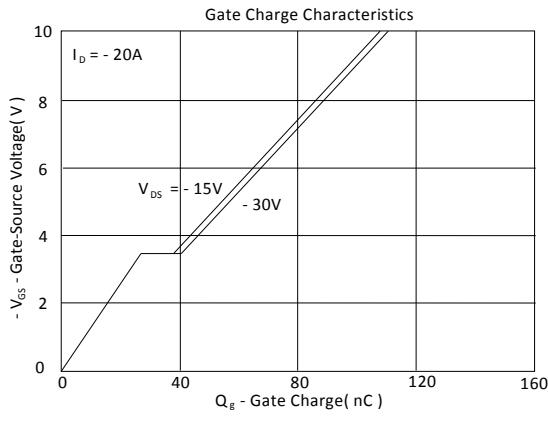
Ordering & Marking Information:

Device Name: EMB20P06A for DPAK (TO-252)

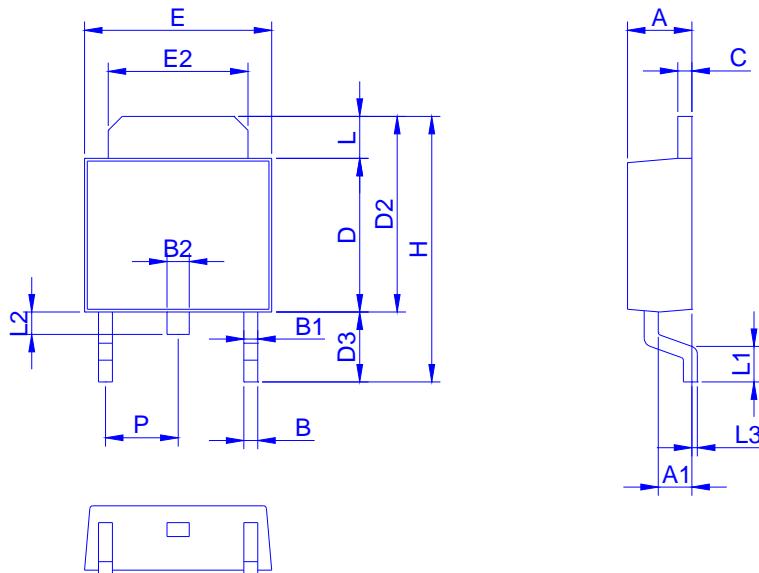


TYPICAL CHARACTERISTICS





Outline Drawing



Dimension	A	A1	B	B1	B2	C	D	D2	D3	E	E2	H	L	L1	L2	L3	P
Min.	2.10	0.95	0.30	0.40	0.60	0.40	5.30	6.70	2.20	6.40	4.80	9.20	0.89	0.90	0.50	0.00	2.10
Max.	2.50	1.30	0.85	0.94	1.00	0.60	6.20	7.30	3.00	6.70	5.45	10.15	1.70	1.65	1.10	0.30	2.50

Footprint

