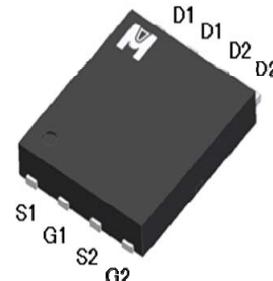
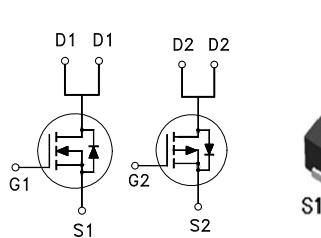


N & P-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

	N-CH	P-CH
BV <sub>DSS</sub>	40V	-40V
R <sub>DSON</sub> (MAX.)	22mΩ	50mΩ
I <sub>D</sub>	33A	-22A



UIS, Rg 100% Tested

Pb-Free Lead Plating & Halogen Free



**ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub> = 25 °C Unless Otherwise Noted)**

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS		UNIT
Gate-Source Voltage		V <sub>GS</sub>	N-CH	P-CH	V
			±20	±20	
Continuous Drain Current	T <sub>C</sub> = 25 °C	I <sub>D</sub>	33	-22	A
	T <sub>C</sub> = 100 °C		21	-14	
Pulsed Drain Current <sup>1</sup>		I <sub>DM</sub>	48	-36	
Avalanche Current		I <sub>AS</sub>	25	-20	
Avalanche Energy		E <sub>AS</sub>	11.25	5	mJ
L = 0.1mH, I <sub>AS</sub> =15A, RG=25Ω (N) L = 0.1mH, I <sub>AS</sub> =-10A, RG=25Ω (P)					
Repetitive Avalanche Energy <sup>2</sup>		E <sub>AR</sub>	5.6	2.5	
Power Dissipation	T <sub>C</sub> = 25 °C	P <sub>D</sub>	41		W
	T <sub>C</sub> = 100 °C		16		
Power Dissipation	T <sub>A</sub> = 25 °C	P <sub>D</sub>	2		W
	T <sub>A</sub> = 70 °C		1.28		
Operating Junction & Storage Temperature Range		T <sub>j</sub> , T <sub>stg</sub>	-55 to 150		°C

**THERMAL RESISTANCE RATINGS**

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	R <sub>θJC</sub>		3	°C / W
Junction-to-Ambient <sup>3</sup>	R <sub>θJA</sub>		62.5	

<sup>1</sup>Pulse width limited by maximum junction temperature.

<sup>2</sup>Duty cycle ≤ 1%

<sup>3</sup>62.5°C / W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper.

**ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25 °C, Unless Otherwise Noted)**

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT	
			MIN	TYP	MAX		
<b>STATIC</b>							
Drain-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA	N-CH	40		V	
		V <sub>GS</sub> = 0V, I <sub>D</sub> = -250μA	P-CH	-40			
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA	N-CH	1	1.8	3	
		V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250μA	P-CH	-1	-1.8	-3	
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0V, V <sub>GS</sub> = ±20V	N-CH			±100	
		V <sub>DS</sub> = 0V, V <sub>GS</sub> = ±20V	P-CH			±100	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 32V, V <sub>GS</sub> = 0V	N-CH			1	
		V <sub>DS</sub> = -32V, V <sub>GS</sub> = 0V	P-CH			-1	
		V <sub>DS</sub> = 30V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 125 °C	N-CH			25	
		V <sub>DS</sub> = -30V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 125 °C	P-CH			-25	
On-State Drain Current <sup>1</sup>	I <sub>D(ON)</sub>	V <sub>DS</sub> = 10V, V <sub>GS</sub> = 10V	N-CH	33		A	
		V <sub>DS</sub> = -5V, V <sub>GS</sub> = -10V	P-CH	-22			
Drain-Source On-State Resistance <sup>1</sup>	R <sub>DS(ON)</sub>	V <sub>GS</sub> = 10V, I <sub>D</sub> = 12A	N-CH		19	22	
		V <sub>GS</sub> = -10V, I <sub>D</sub> = -12A	P-CH		45	50	
		V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 10A	N-CH		33	40	
		V <sub>GS</sub> = -4.5V, I <sub>D</sub> = -10A	P-CH		70	85	
Forward Transconductance <sup>1</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 5V, I <sub>D</sub> = 12A	N-CH		20	S	
		V <sub>DS</sub> = -5V, I <sub>D</sub> = -12A	P-CH		10		
<b>DYNAMIC</b>							
Input Capacitance	C <sub>iss</sub>	N-CH V <sub>GS</sub> = 0V, V <sub>DS</sub> = 15V, f = 1MHz P=CH V <sub>GS</sub> = 0V, V <sub>DS</sub> = -15V, f = 1MHz	N-CH		536		
			P-CH		810		
Output Capacitance	C <sub>oss</sub>		N-CH		83		
			P-CH		94		
Reverse Transfer Capacitance	C <sub>rss</sub>		N-CH		66		
			P-CH		72		

Gate Resistance	R <sub>g</sub>	V <sub>GS</sub> = 15mV, V <sub>DS</sub> = 0V, f = 1MHz	N-CH		1.5		Ω
			P-CH		6.5		
Total Gate Charge <sup>1,2</sup>	Q <sub>g</sub>	N-CH V <sub>DS</sub> = 20V, V <sub>GS</sub> = 10V, I <sub>D</sub> = 12A P-CH	N-CH		14.5		
Gate-Source Charge <sup>1,2</sup>	Q <sub>gs</sub>	V <sub>DS</sub> = -20V, V <sub>GS</sub> = -10V, I <sub>D</sub> = -12A	P-CH		15		nC
Gate-Drain Charge <sup>1,2</sup>	Q <sub>gd</sub>		N-CH		2.1		
			P-CH		2.6		
Turn-On Delay Time <sup>1,2</sup>	t <sub>d(on)</sub>	N-CH V <sub>DS</sub> = 20V, I <sub>D</sub> = 1A, V <sub>GS</sub> = 10V, R <sub>GS</sub> = 6Ω P-CH	N-CH		4.3		
Rise Time <sup>1,2</sup>	t <sub>r</sub>		P-CH		3.1		
Turn-Off Delay Time <sup>1,2</sup>	t <sub>d(off)</sub>	V <sub>DS</sub> = -20V, I <sub>D</sub> = -1A, V <sub>GS</sub> = -10V, R <sub>GS</sub> = 6Ω	N-CH		10		
Fall Time <sup>1,2</sup>	t <sub>f</sub>		P-CH		12		
			N-CH		15		
			P-CH		25		
			N-CH		15		
			P-CH		15		
<b>SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T<sub>C</sub> = 25 °C)</b>							
Continuous Current	I <sub>S</sub>		N-CH			33	A
			P-CH			-22	
Pulsed Current <sup>3</sup>	I <sub>SM</sub>		N-CH			48	
			P-CH			-36	
Forward Voltage <sup>1</sup>	V <sub>SD</sub>	I <sub>F</sub> = 12A, V <sub>GS</sub> = 0V I <sub>F</sub> = -12A, V <sub>GS</sub> = 0V	N-CH			1.2	V
			P-CH			-1.2	

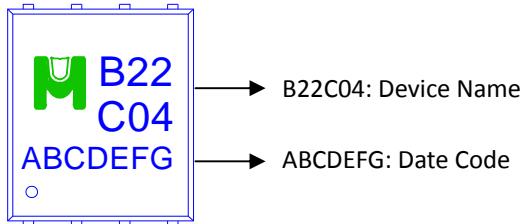
<sup>1</sup>Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.

<sup>2</sup>Independent of operating temperature.

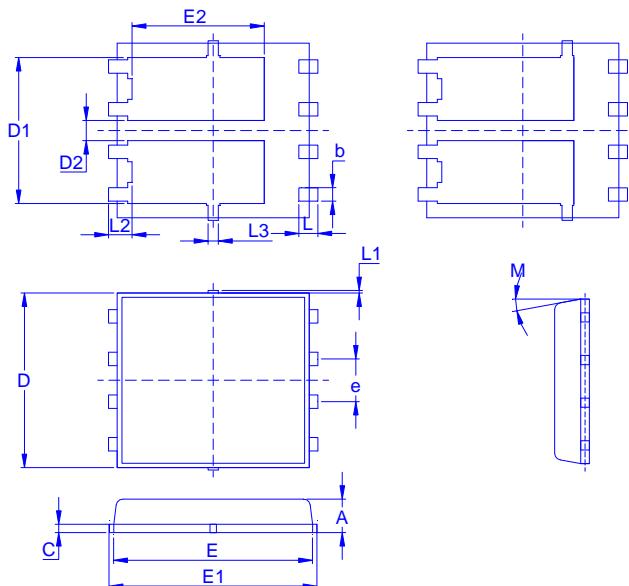
<sup>3</sup>Pulse width limited by maximum junction temperature.

Ordering & Marking Information:

Device Name: EMB22C04H for EDFN 5 x 6



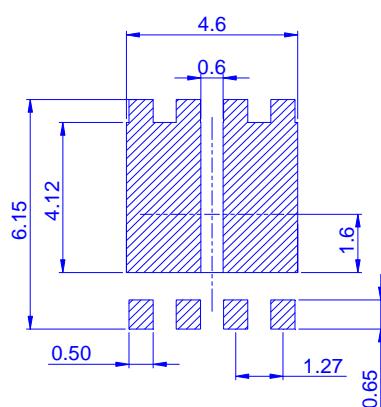
Outline Drawing



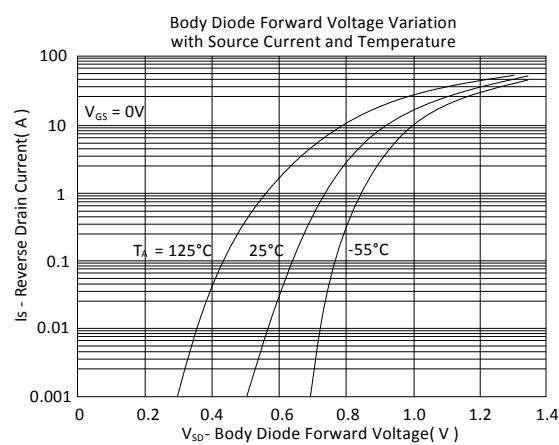
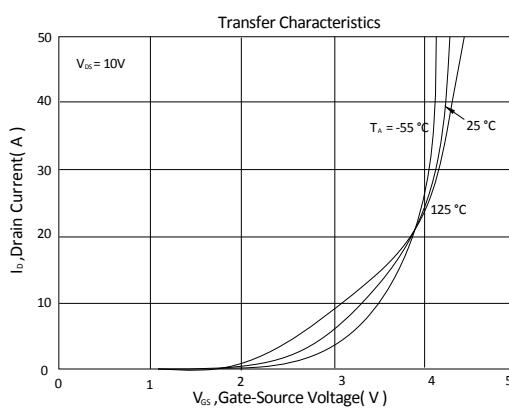
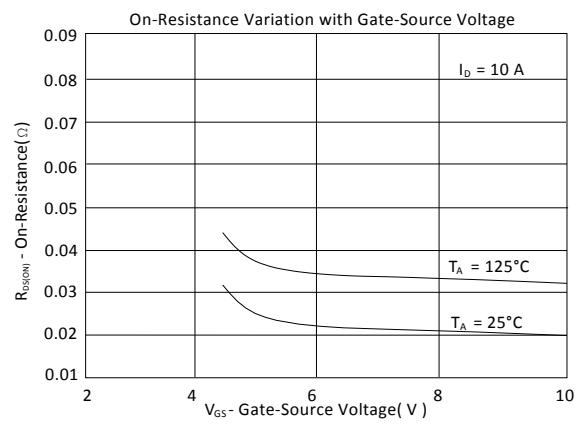
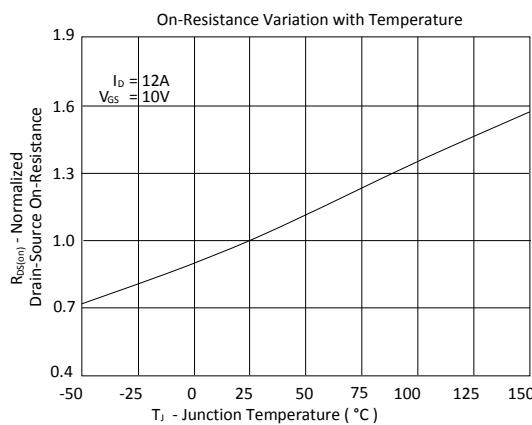
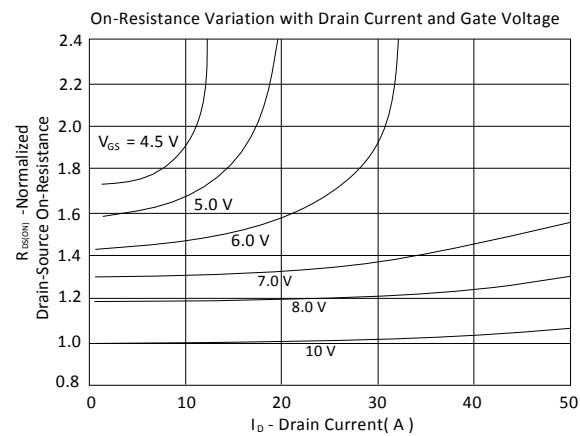
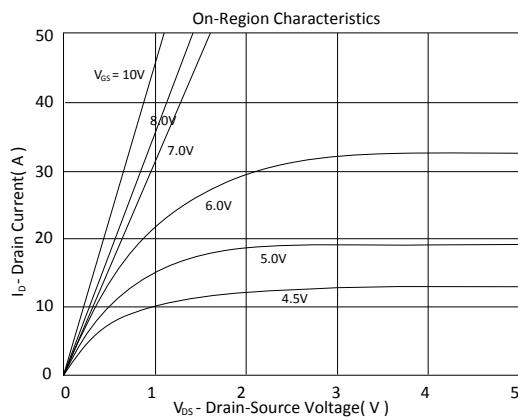
Dimension in mm

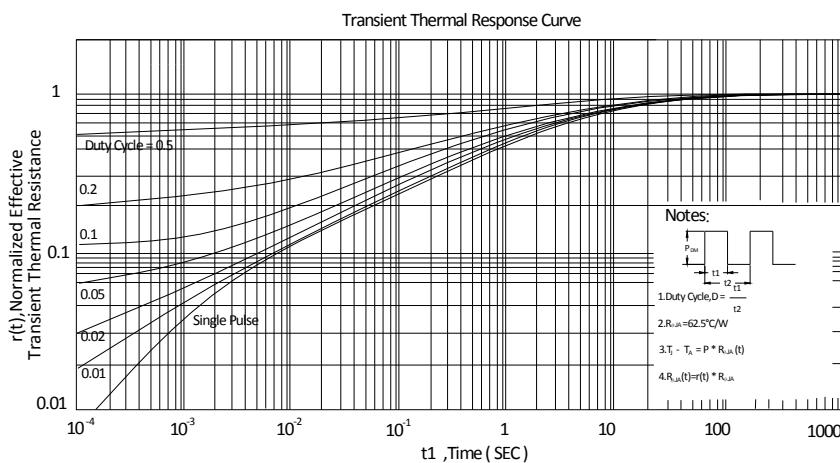
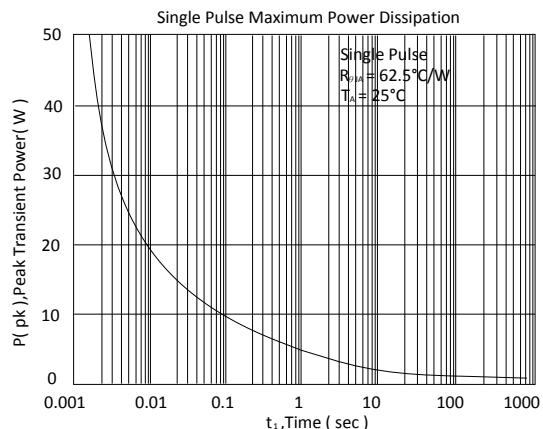
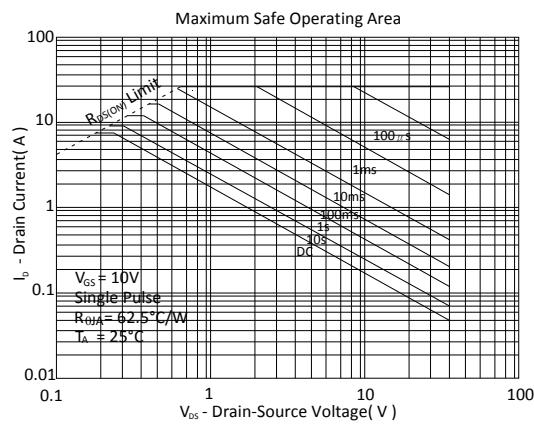
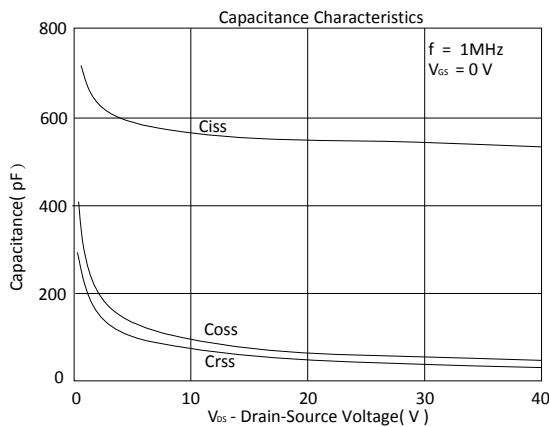
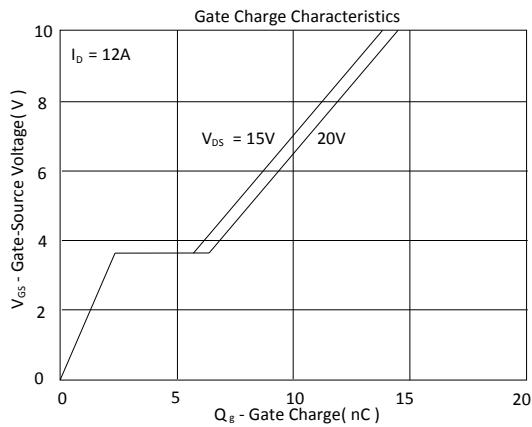
Dimension	A	b	c	D	D1	D2	E	E1	E2	e	L	L1	L2	M
Min.	0.85	0.3	0.15	4.8	3.41	0.47	5.65	5.95	3.30		0.38	0	0.38	0°
Typ.	1.01	0.4	0.2	5	4.01	0.67	5.75	6.05	3.43	1.27	0.55	0.09	0.48	
Max.	1.17	0.5	0.25	5.2	4.61	0.87	5.85	6.15	3.58		0.71	0.18	0.58	12°

Recommended minimum pads



## N-Channel





P-Channel

