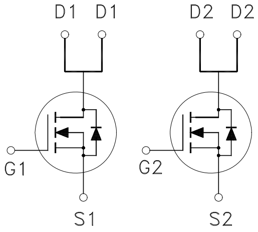
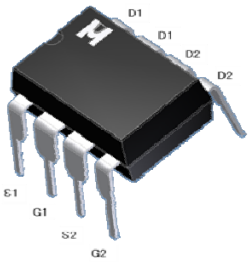
Dual N-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

BV_{DSS}	60V
$R_{DSON\,(MAX.)}$	30mΩ
I_D	7A





UIS, 100% Tested

Pb-Free Lead Plating

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_C = 25 °C	I_D	7	A
	T_C = 100 °C		5	
Pulsed Drain Current[1]		I_{DM}	28	
Avalanche Current		I_{AS}	12	
Avalanche Energy	L = 0.1mH, ID=12A, RG=25Ω	E_{AS}	7.2	mJ
Repetitive Avalanche Energy[2]	L = 0.05mH	E_{AR}	3.6	
Power Dissipation	T_C = 25 °C	P_D	5	W
	T_C = 100 °C		2	
Operating Junction & Storage Temperature Range		T_j, T_{stg}	-55 to 150	°C

100% UIS testing in condition of V_D=30V, L=0.1mH, V_G=10V, I_L=7A, Rated V_{DS}=60V N-CH

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	$R_{\theta JC}$		25	°C / W
Junction-to-Ambient[3]	$R_{\theta JA}$		62.5	

[1] Pulse width limited by maximum junction temperature.

[2] Duty cycle ≤ 1%

[3] 62.5°C / W when mounted on a 1 in^2 pad of 2 oz copper.

ELECTRICAL CHARACTERISTICS (T_C = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = 250μA	60			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250μA	1.0	2.0	3.2	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0V, V_{GS} = ±20V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 48V, V_{GS} = 0V			1	μA
		V_{DS} = 40V, V_{GS} = 0V, T_J = 125 °C			25	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 5V, V_{GS} = 10V	7			A
Drain-Source On-State Resistance[1]	$R_{DS(ON)}$	V_{GS} = 10V, I_D = 7A		25	30	mΩ
		V_{GS} = 5V, I_D = 6A		38	48	
Forward Transconductance[1]	g_{fs}	V_{DS} = 5V, I_D = 7A		25		S
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS} = 0V, V_{DS} = 30V, f = 1MHz		2240		pF
Output Capacitance	C_{oss}			172		
Reverse Transfer Capacitance	C_{rss}			145		
Total Gate Charge[1,2]	Q_g	V_{DS} = 30V, V_{GS} = 10V, I_D = 7A		43		nC
Gate-Source Charge[1,2]	Q_{gs}			7.2		
Gate-Drain Charge[1,2]	Q_{gd}			11		
Turn-On Delay Time[1,2]	$t_{d(on)}$	V_{DS} = 30V, I_D = 1A, V_{GS} = 10V, R_{GS} = 6Ω		20		nS
Rise Time[1,2]	t_r			12		
Turn-Off Delay Time[1,2]	$t_{d(off)}$			50		
Fall Time[1,2]	t_f			25		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25 °C)						
Continuous Current	I_S				2.3	A
Pulsed Current[3]	I_{SM}				9.2	
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0V			1.2	V

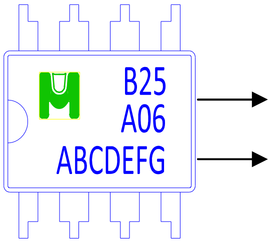
[1] Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.

[2] Independent of operating temperature.

[3] Pulse width limited by maximum junction temperature.

Ordering & Marking Information:

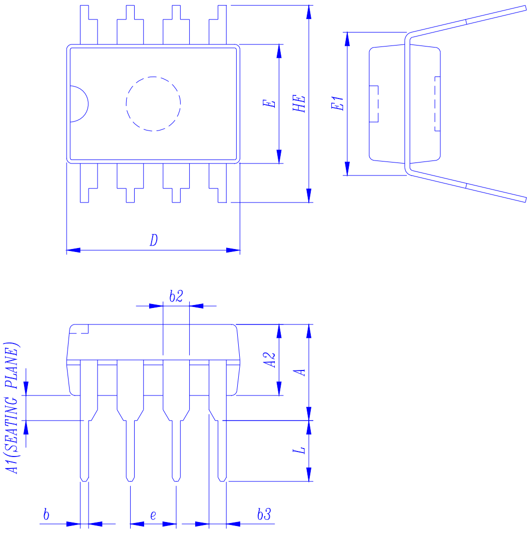
Device Name: EMB25A06S for DIP-8



B25A06: Device Name

ABCDEFG: Date Code

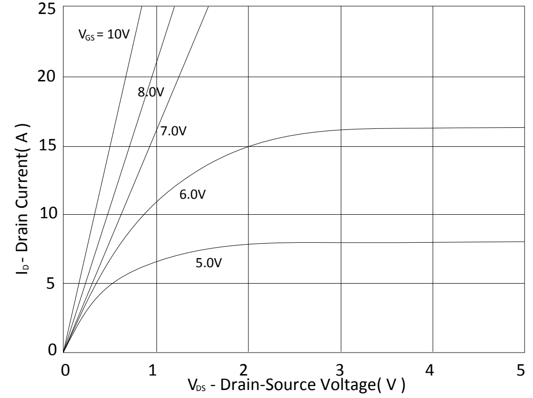
Outline Drawing



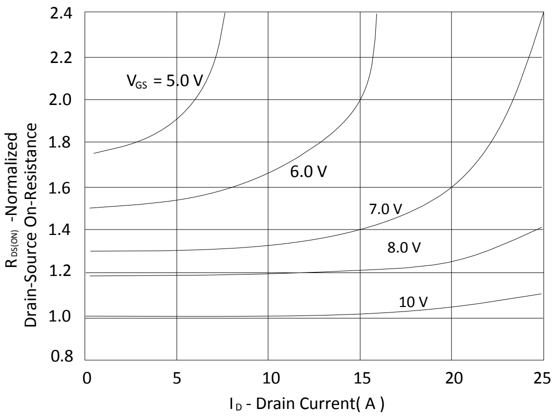
Dimension in mm

Dimension	A	A1	A2	b	b2	b3	c	D	E	E1	e	HE	L
in.		0.38	2.92	0.25	1.14	0.76	0.20	9.01	6.09	7.62			2.92
Typ.											2.54		
Max.	5.34		4.96	0.56	1.78	1.15	0.36	10.16	7.12	8.26		10.92	3.81

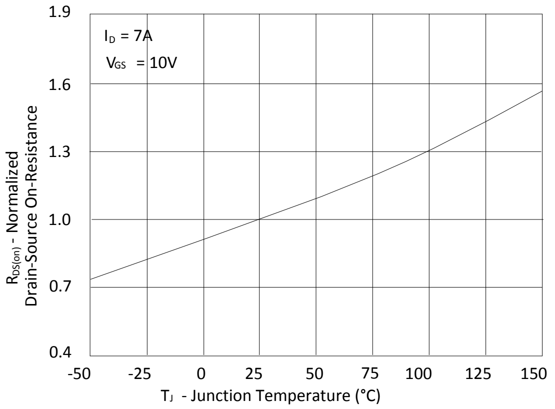
On-Region Characteristics



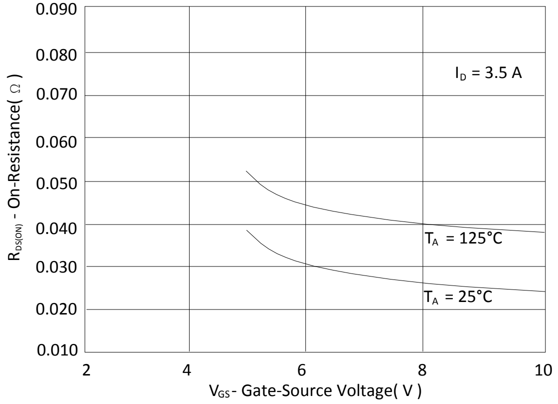
On-Resistance Variation with Drain Current and Gate Voltage



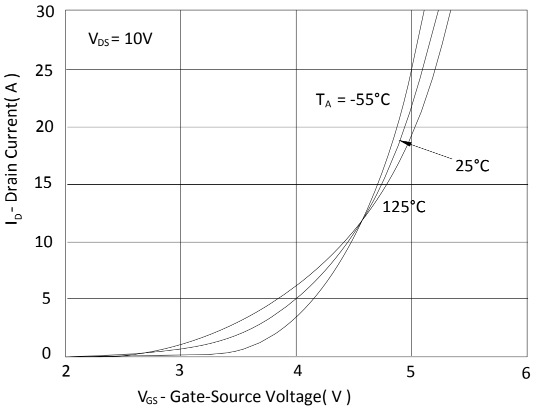
On-Resistance Variation with Temperature



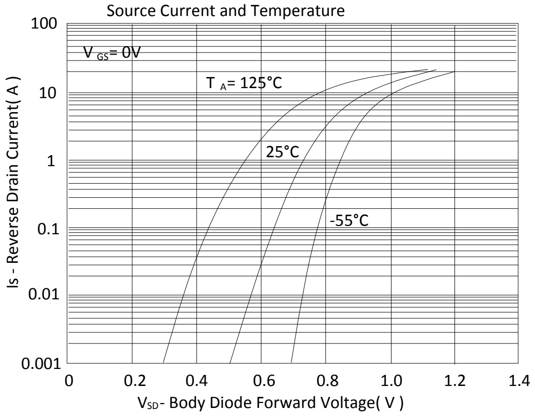
On-Resistance Variation with Gate-Source Voltage

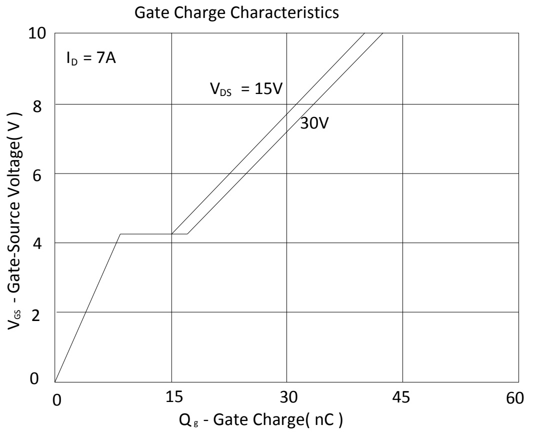


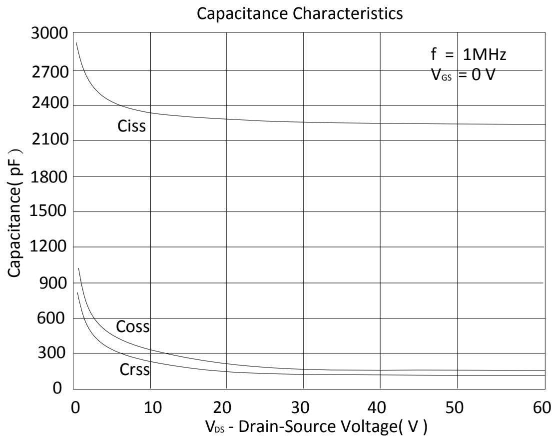
Transfer Characteristics

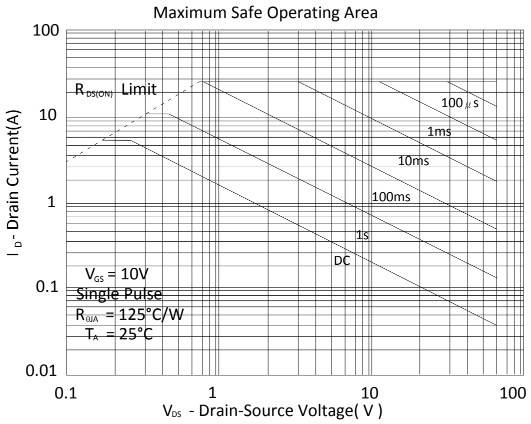


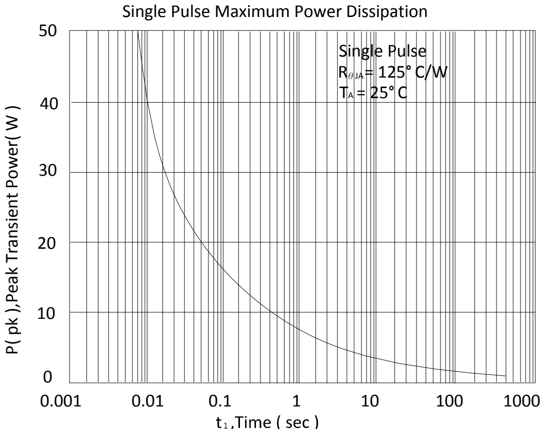
Body Diode Forward Voltage Variation with Source Current and Temperature

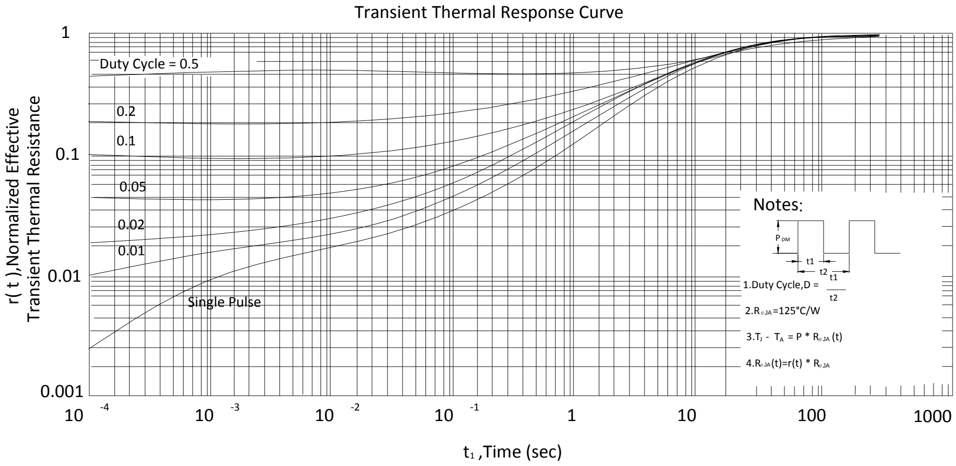



Gate Charge Characteristics


Capacitance Characteristics


Maximum Safe Operating Area


Single Pulse Maximum Power Dissipation


Transient Thermal Response Curve