杰力科技股份有限公司
Excelliance MOS Corporation

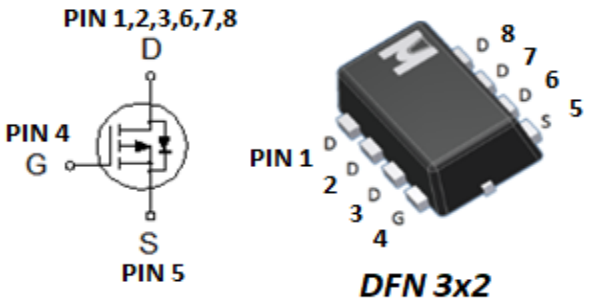
EMB28P03L

Single P-Channel Logic Level Enhancement Mode Field Effect Transistor

▪Product Summary:

	P-CH
BVDSS	-30V
$R_{DSON\ (MAX.)}$@V_{GS}=-10V	26.0mΩ
$R_{DSON\ (MAX.)}$@V_{GS}=-4.5V	34.0mΩ
I_D @T_A=25°C	-5.0A

▪ Pin Description:



Single P Channel MOSFET
UIS, Rg 100% Tested
Pb-Free Lead Plating & Halogen Free

▪ ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V_{GS}	±25	V
Continuous Drain Current	T_C = 25 °C	I_D	-10	A
	T_C = 100 °C		-6	
Continuous Drain Current	T_A = 25 °C	I_D	-5	
	T_A = 70 °C		-4	
Pulsed Drain Current[1]		I_{DM}	-40	
Avalanche Current		I_{AS}	-14	
Avalanche Energy	L = 0.1mH	EAS	9.8	mJ
Repetitive Avalanche Energy[2]	L = 0.05mH	EAR	4.9	
Power Dissipation	T_C = 25 °C	P_D	4.2	W
	T_C = 100 °C		1.7	
Power Dissipation	T_A = 25 °C	P_D	2.5	W
	T_A = 70 °C		1.6	
Operating Junction & Storage Temperature Range		T_j, T_{stg}	-55 to 150	°C

▪THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE		SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case		$R_{\theta JC}$		30	°C/W
Junction-to-Ambient[3]	t≦10s	$R_{\theta JA}$		50	
	Steady-State	$R_{\theta JA}$		90	

[1]Pulse width limited by maximum junction temperature.
[2]Duty cycle < 1%
[3]The power dissipation P_D is based on $T_{J(MAX)}$=150°C, using ≦10s junction-to-ambient thermal resistance.
[4]The value of $R_{\theta JA}$ is measured with mounted on a 1 in^2 pad of 2 oz copper.

▪ **ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)**

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage[4]	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = -250uA	-30			V
Gate Threshold Voltage[4]	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -250uA	-0.8	-1.3	-1.9	
Gate-Body Leakage[4]	I_{GSS}	V_{DS} = 0V, V_{GS} = ±20V			±30	uA
Zero Gate Voltage Drain Current[4]	I_{DSS}	V_{DS} = -24V, V_{GS} = 0V			1	uA
		V_{DS} = -20V, V_{GS} = 0V, T_J = 125 °C			25	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = -5V, V_{GS} = -10V	-10			A
Drain-Source On-State Resistance[1,4]	$R_{DS(ON)}$	V_{GS} = -10V, I_D = -5A		22	26	mΩ
		V_{GS} = -4.5V, I_D = -4A		30	34	
Forward Transconductance[1]	g_{fs}	V_{DS} = -5V, I_D = -5A		12		S
DYNAMIC						
Input Capacitance[5]	C_{iss}	V_{GS} = 0V, V_{DS} = -15V, f = 1MHz		779		pF
Output Capacitance[5]	C_{oss}			124		
Reverse Transfer Capacitance[5]	C_{rss}			97		
Gate Resistance[4,5]	R_g	f = 1MHz		5.6		Ω
Total Gate Charge[1,2,5]	Q_g(V_{GS}=10V)	V_{DS} = -15V, V_{GS} = -10V, I_D = -8A		14.9		nC
	Q_g(V_{GS}=4.5V)			8		
Gate-Source Charge[1,2,5]	Q_{gs}			1.7		
Gate-Drain Charge[1,2,5]	Q_{gd}			3.3		
Turn-On Delay Time[1,2,5]	$t_{d(on)}$	V_{DS} = -15V, V_{GS} = -10V, I_D = -5A , Rg = 6Ω		5.6		nS
Rise Time[1,2,5]	t_r			11.8		
Turn-Off Delay Time[1,2,5]	$t_{d(off)}$			33.5		
Fall Time[1,2,5]	t_f			30.5		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS						
Continuous Current	I_S				-10	A
Pulsed Current[3]	I_{SM}				-40	
Forward Voltage[1,4]	V_{SD}	I_F = I_S, V_{GS} = 0V			-1.2	V
Reverse Recovery Time[5]	t_{rr}	I_F = I_S, dI_F/dt = 400A / uS		11.6		nS
Reverse Recovery Charge[5]	Q_{rr}			9.4		nC

[1]Pulse test : Pulse Width ≦ 300 usec, Duty Cycle ≦ 2%.

[2]Independent of operating temperature.

[3]Pulse width limited by maximum junction temperature.

[4]Guarantee by FT test Item

[5]Guarantee by Engineering test

EMC will review datasheet by quarter, and update new version.

▪TYPICAL CHARACTERISTICS

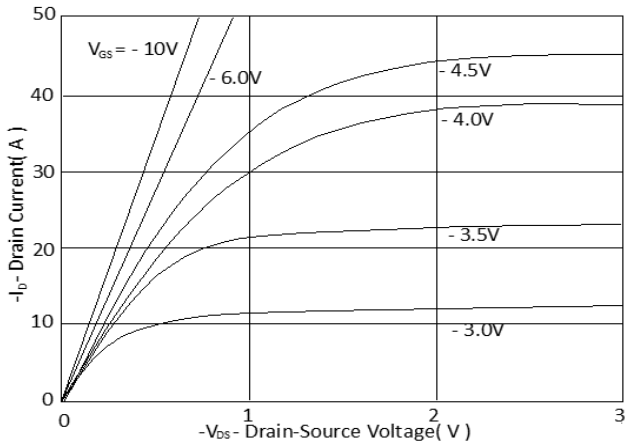


Fig.1 Typical Output Characteristics

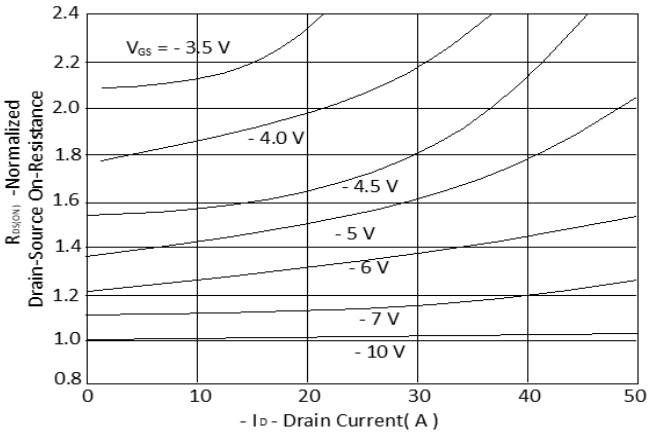


Fig.2 On-Resistance Variation with Drain Current and Gate Voltage

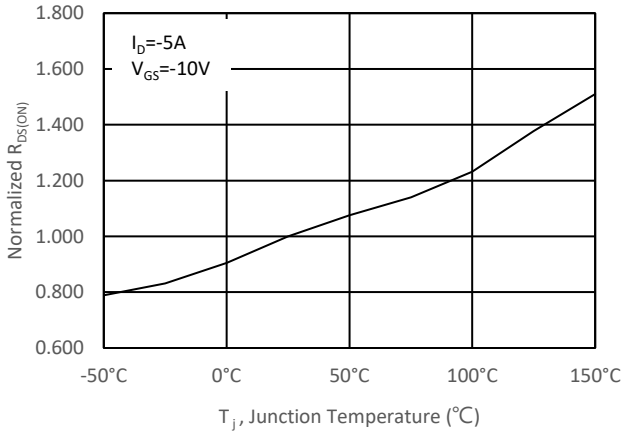


Fig.3 Normalized On-Resistance v.s. Junction Temperature

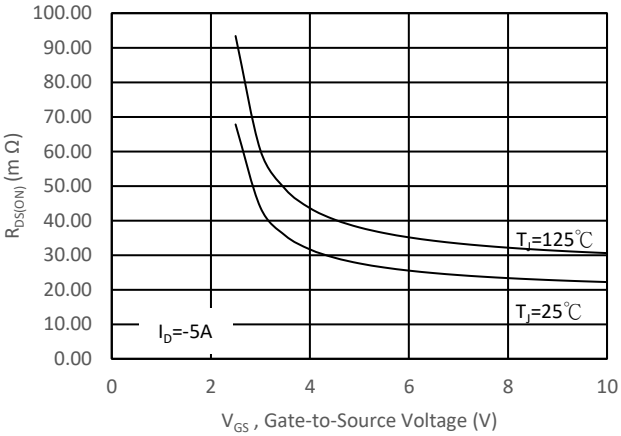


Fig.4 On-Resistance v.s. Gate Voltage

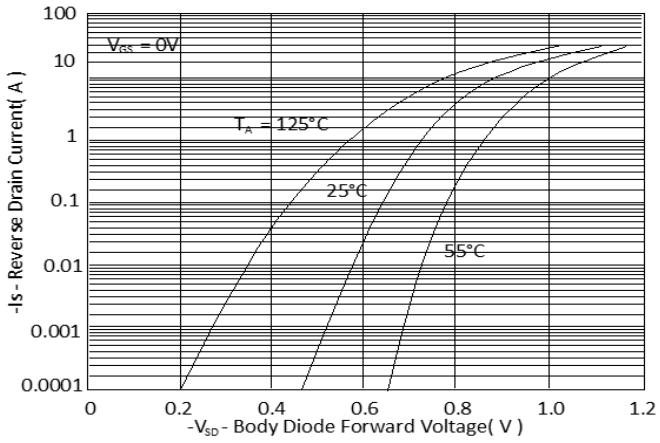


Fig.5 Forward Characteristic of Reverse Diode

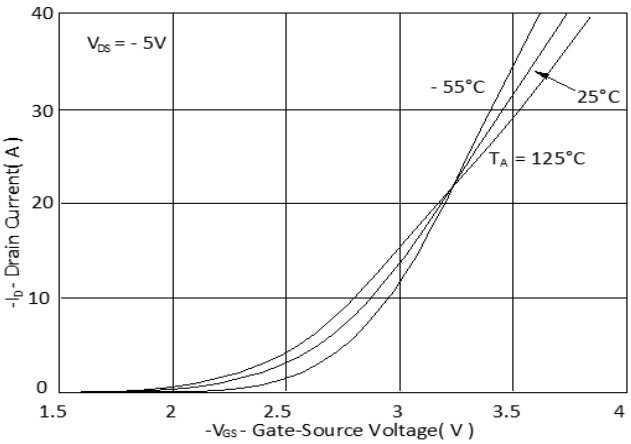


Fig.6 Transfer Characteristics

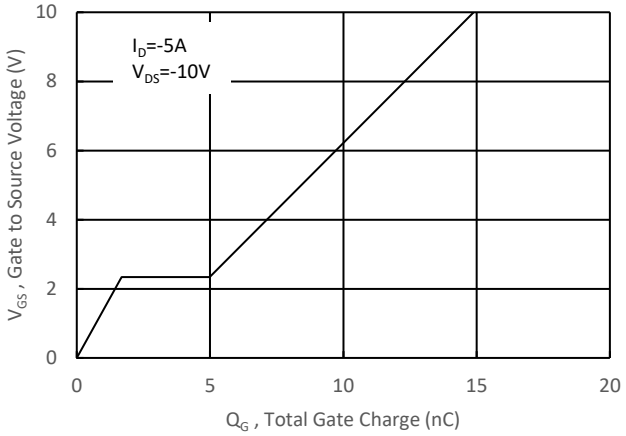


Fig.7 Gate Charge Characteristics

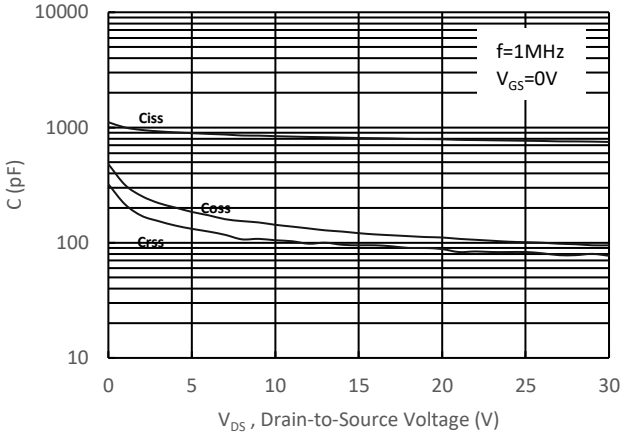


Fig.8 Typical Capacitance Characteristics

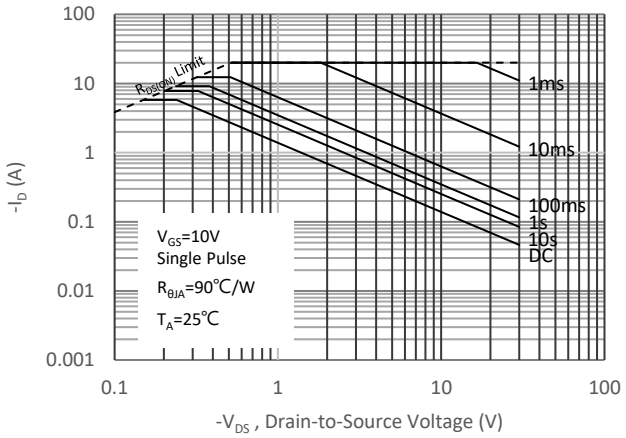


Fig 9. Maximum Safe Operating Area

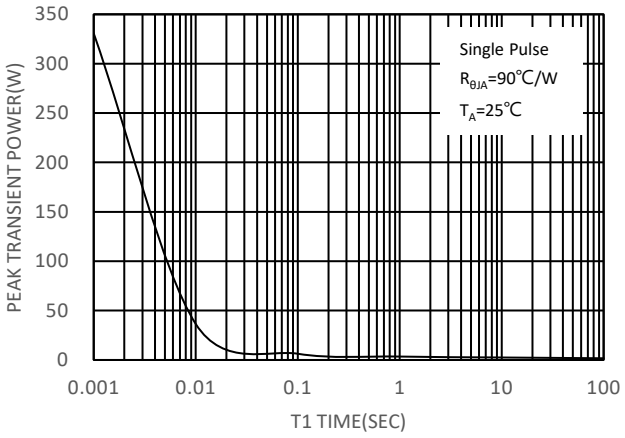


Fig 10. Single Pulse Maximum Power Dissipation

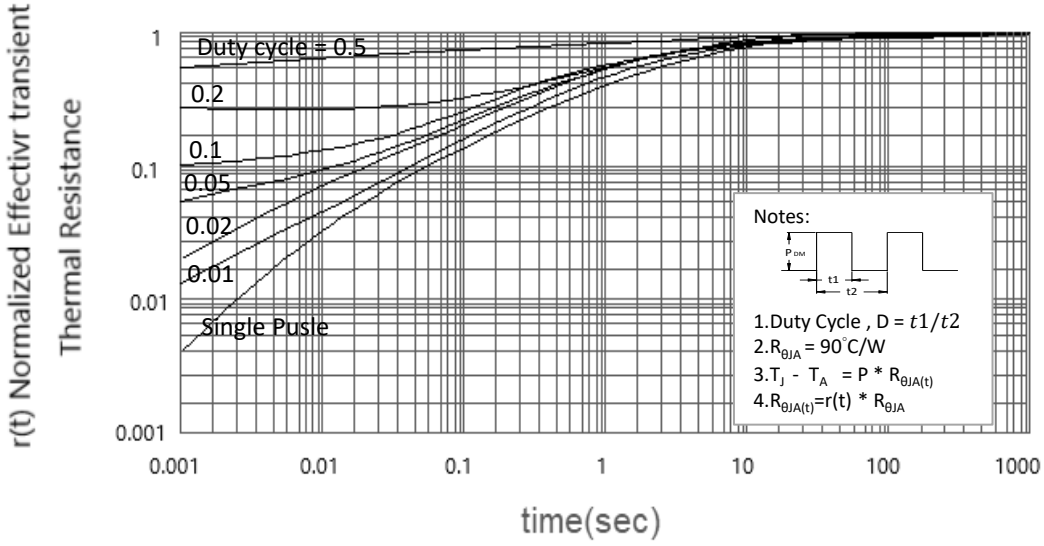
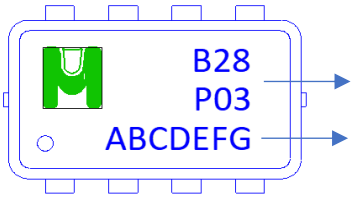


Fig 11. Effective Transient Thermal Impedance

Ordering & Marking Information:

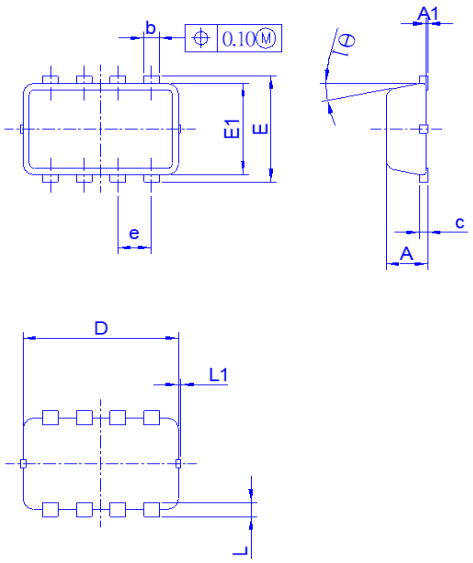
Device Name: EMB28P03L for DFN 3x2



B28P03: Device Name

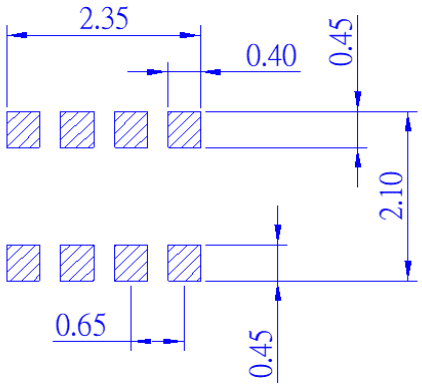
ABCDEFG: Date Code
A: Assembly House
B: Year(A:2008 B:2009 C:2010….)
C: Month(A:01 B:02 C:03 D:04 E:05 F:06 G:07 H:08 I:09 J:10 K:11 L:12)
DEFG: Serial No.

Outline Drawing

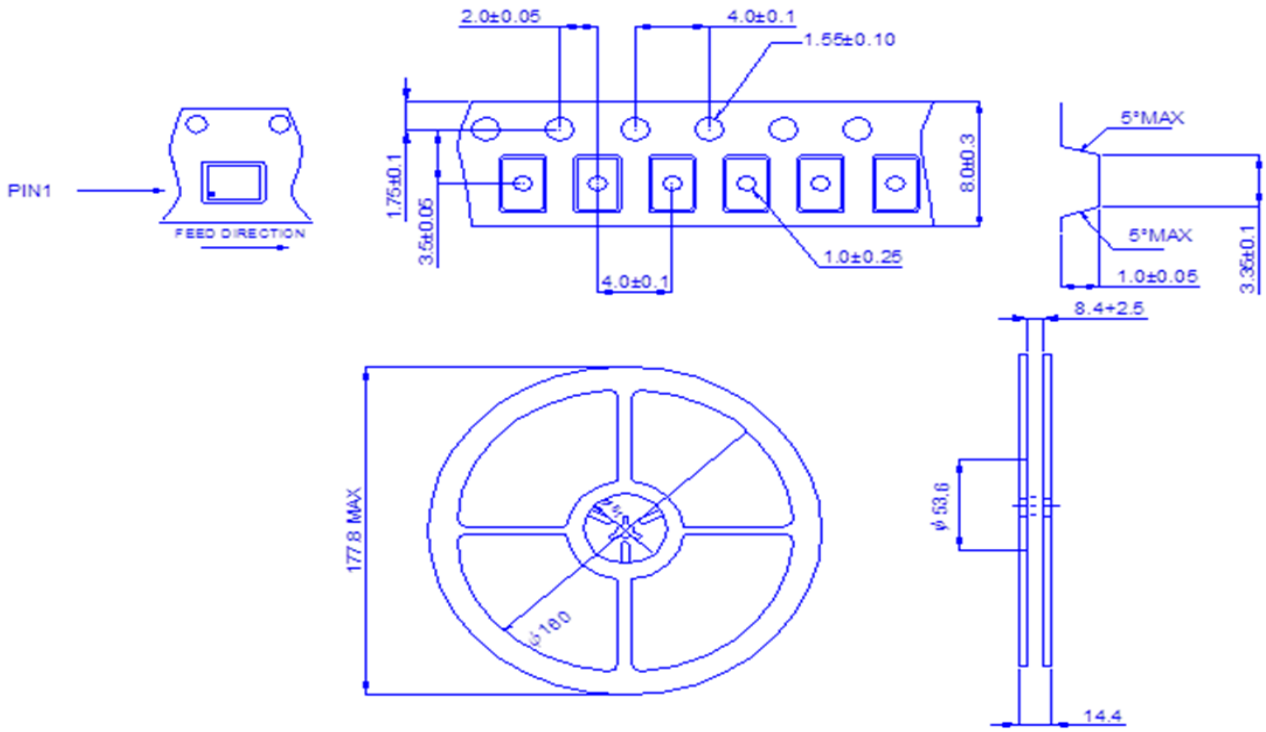


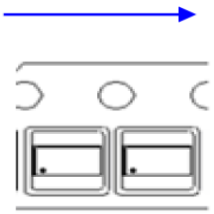
Dimension	A	A1	b	c	D	E	E1	e	L	L1	θ1
Min.	0.7	0	0.24	0.08					0.2	0	0°
Typ.					3	2	1.7	0.65			
Max.	0.9	0.05	0.35	0.25					0.4	0.1	12°

Footprint



◆ **Tape&Reel Information:3000pcs/Reel**
(Dimension in millimeter)



產品別	DFN3.0X2.0-08
Reel 尺寸	7”
編帶方式	FEED DIRECTION 
前空格	50
後空格	50
裝箱數	
滿捲數量	3K
捲/內盒比	5 : 1
內盒滿箱數	15K
內/外箱比	12 : 1
外箱滿箱數	180K

★Datasheet Latest version specification :

	Revision History	Prepared	Approved	Date
A.0	Initial Datasheet	Johnson	Sam	2020/7/8
A.1	Update Tape&Reel information	Johnson	Sam	2020/7/28