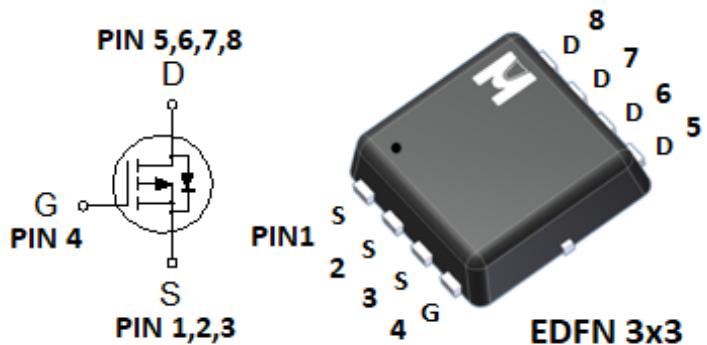


Single P-Channel Logic Level Enhancement Mode Field Effect Transistor

• Product Summary:

	P-CH
BV_{DSS}	-60V
$R_{DSON (MAX.)}@V_{GS}=-10V$	25m Ω
$R_{DSON (MAX.)}@V_{GS}=-4.5V$	33m Ω
$I_D @T_C=25^\circ C$	-33A

• Pin Description:



Single P Channel MOSFET

UIS, Rg 100% Tested

Pb-Free Lead Plating & Halogen Free



• ABSOLUTE MAXIMUM RATINGS ($T_C = 25^\circ C$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current ¹	$T_C = 25^\circ C$	I_D	-33	A
	$T_C = 100^\circ C$		-21	
	$T_A = 25^\circ C$		-7	
	$T_A = 70^\circ C$		-5	
Pulsed Drain Current ¹		I_{DM}	-53	mJ
Avalanche Current ¹		I_{AS}	-45	
Avalanche Energy ¹		E_{AS}	101	
Repetitive Avalanche Energy ²		E_{AR}	50.6	
Power Dissipation ¹	$T_C = 25^\circ C$	P_D	41.7	W
	$T_C = 100^\circ C$		16.7	
Power Dissipation	$T_A = 25^\circ C$	P_D	2.1	W
	$T_A = 70^\circ C$		1.3	
Operating Junction & Storage Temperature Range		T_j, T_{stg}	-55 to 150	$^\circ C$

¹ 100% UIS testing in condition of $V_D=-30V, L=0.1mH, V_G=10V, I_L=28A, \text{Rated } V_{DS}=-60V \text{ P-CH}$

• THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	$R_{\theta JC}$		3	$^\circ C / W$
Junction-to-Ambient ³	$R_{\theta JA}$		60	

¹ Pulse width limited by maximum junction temperature.

² Duty cycle $\leq 1\%$

³ $60^\circ C / W$ when mounted on a 1 in^2 pad of 2 oz copper.

▪ ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0V, I _D = -250uA	-60			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -250uA	-1	-2	-3	
Gate-Body Leakage	I _{GSS}	V _{DS} = 0V, V _{GS} = ±20V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = -48V, V _{GS} = 0V			-1	uA
		V _{DS} = -40V, V _{GS} = 0V, T _J = 125 °C			-25	
On-State Drain Current ¹	I _{D(ON)}	V _{DS} = -5V, V _{GS} = -10V	-33			A
Drain-Source On-State Resistance ¹	R _{DS(ON)}	V _{GS} = -10V, I _D = -10A		21	25	mΩ
		V _{GS} = -4.5V, I _D = -8A		26	33	
Forward Transconductance ¹	g _{fs}	V _{DS} = -5V, I _D = -10A		4		S
DYNAMIC						
Input Capacitance	C _{iss}	V _{GS} = 0V, V _{DS} = -30V, f = 1MHz		3334		pF
Output Capacitance	C _{oss}			175		
Reverse Transfer Capacitance	C _{rss}			137		
Gate Resistance	R _g	f = 1MHz		3.0		Ω
Total Gate Charge ^{1,2}	Q _g (V _{GS} =10V)	V _{DS} = -30V, V _{GS} = -10V, I _D = -10A		66.7		nC
	Q _g (V _{GS} =4.5V)			33.7		
Gate-Source Charge ^{1,2}	Q _{gs}			6.8		
Gate-Drain Charge ^{1,2}	Q _{gd}			14.5		
Turn-On Delay Time ^{1,2}	t _{d(on)}		V _{DS} = -30V, V _{GS} = -10V, I _D = -1A, R _g = 6Ω		9	
Rise Time ^{1,2}	t _r			9		
Turn-Off Delay Time ^{1,2}	t _{d(off)}			130		
Fall Time ^{1,2}	t _f			41		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS						
Continuous Current	I _S				-33	A
Pulsed Current ³	I _{SM}				-53	
Forward Voltage ¹	V _{SD}	I _F = I _S , V _{GS} = 0V			-1.2	V
Reverse Recovery Time	t _{rr}	I _F = I _S , dI _F /dt = 100A / uS		24.6		nS
Peak Reverse Recovery Current	I _{RM(REC)}			2.57		A
Reverse Recovery Charge	Q _{rr}			28.8		nC

¹Pulse test : Pulse Width ≤ 300 usec, Duty Cycle ≤ 2%.

²Independent of operating temperature.

³Pulse width limited by maximum junction temperature.

EMC will review datasheet by quarter, and update new version.

▪ TYPICAL CHARACTERISTICS

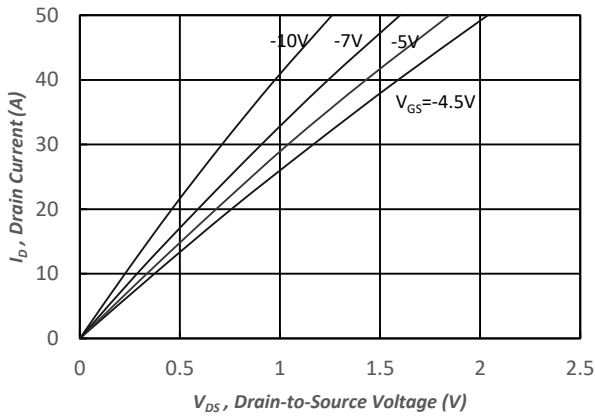


Fig.1 Typical Output Characteristics

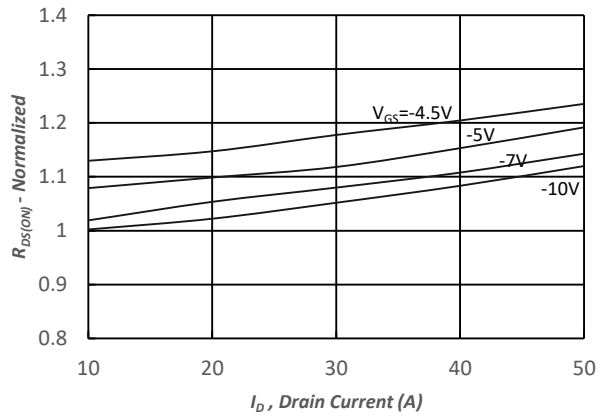


Fig.2 On-Resistance Variation with Drain Current and Gate Voltage

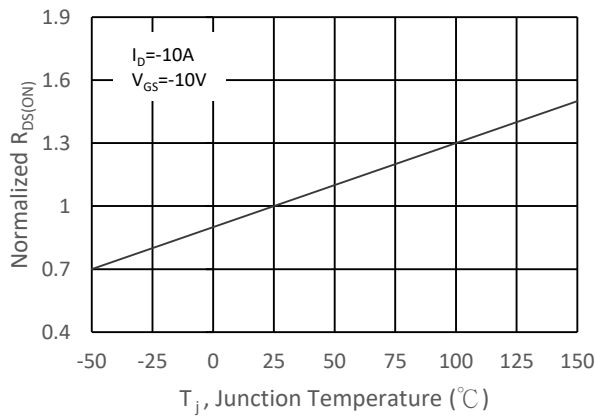


Fig.3 Normalized On-Resistance v.s. Junction Temperature

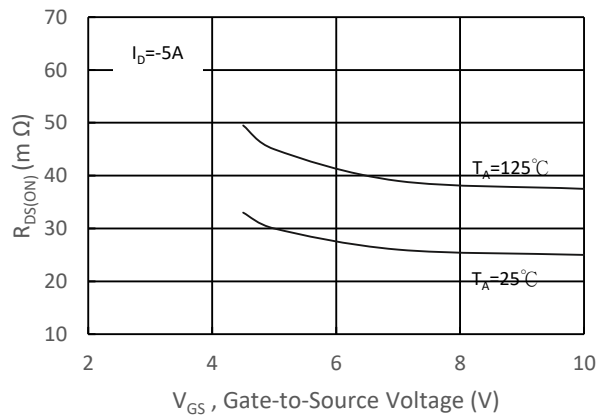


Fig.4 On-Resistance v.s. Gate Voltage

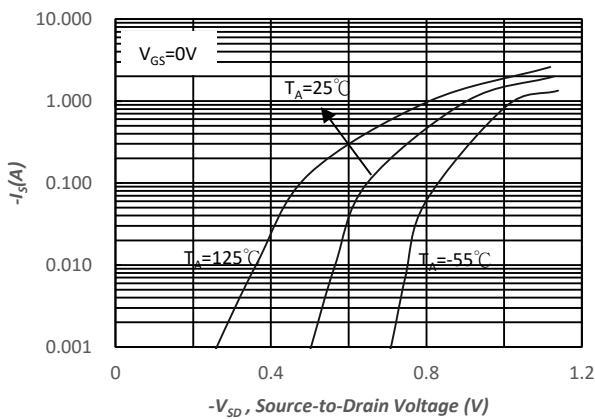


Fig.5 Forward Characteristic of Reverse Diode

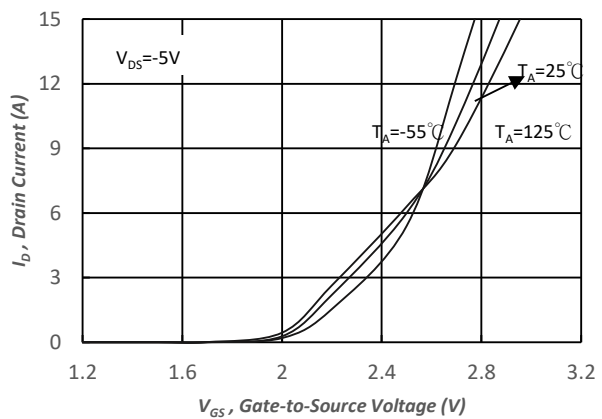


Fig.6 Transfer Characteristics

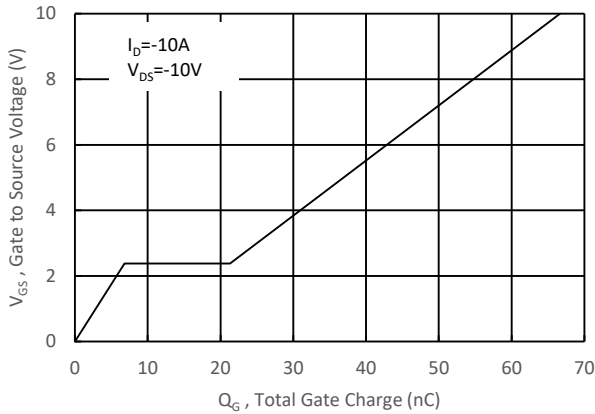


Fig.7 Gate Charge Characteristics

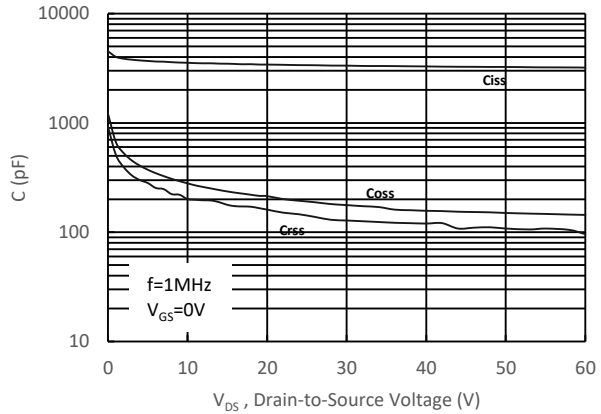


Fig.8 Typical Capacitance Characteristics

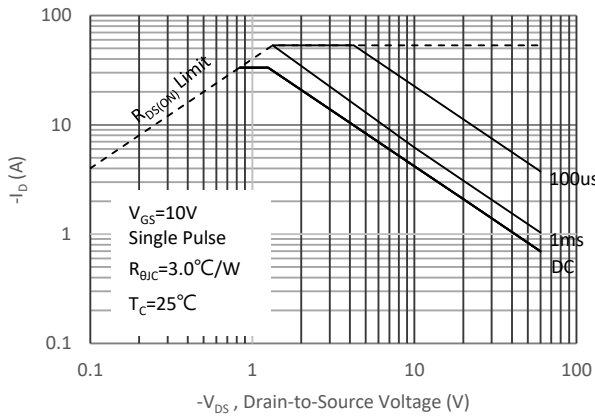


Fig.9. Maximum Safe Operating Area

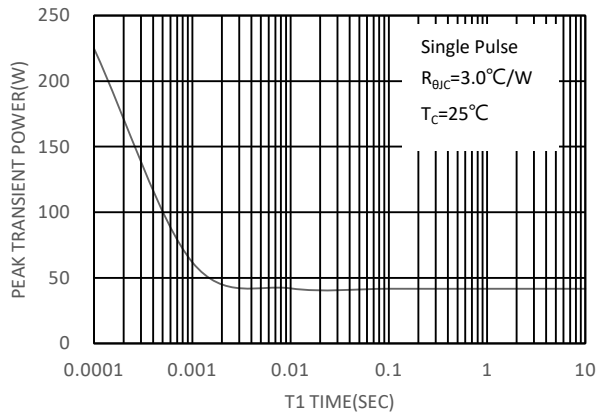


Fig.10. Single Pulse Maximum Power Dissipation

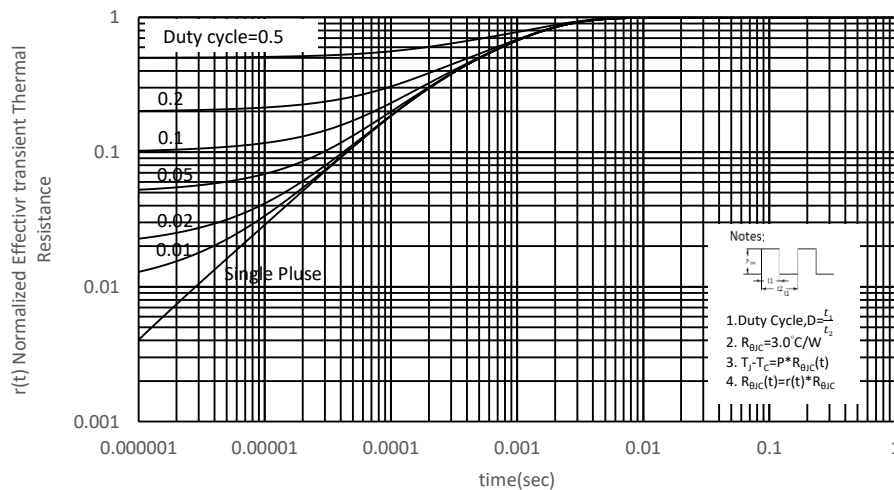


Fig.11. Effective Transient Thermal Impedance

Ordering & Marking Information:

Device Name: EMB28P06V for EDFN 3x3



B28P06: Device Name

ABCDEFGH: Date Code

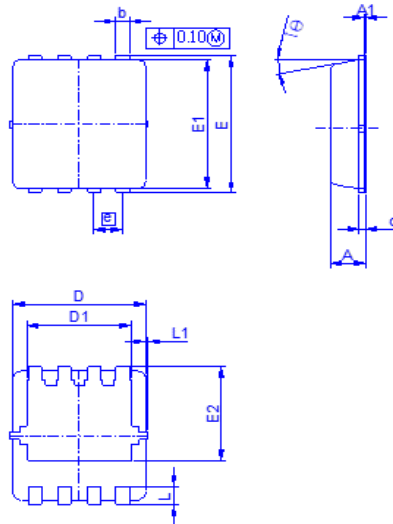
A: Assembly House

B: Year(A:2008 B:2009 C:2010....)

C: Month(A:01 B:02 C:03 D:04 E:05 F:06 G:07 H:08 I:09 J:10 K:11 L:12)

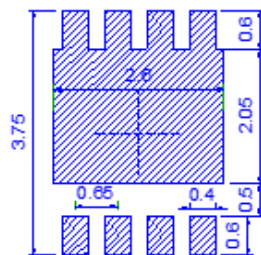
DEFG: Serial No.

Outline Drawing

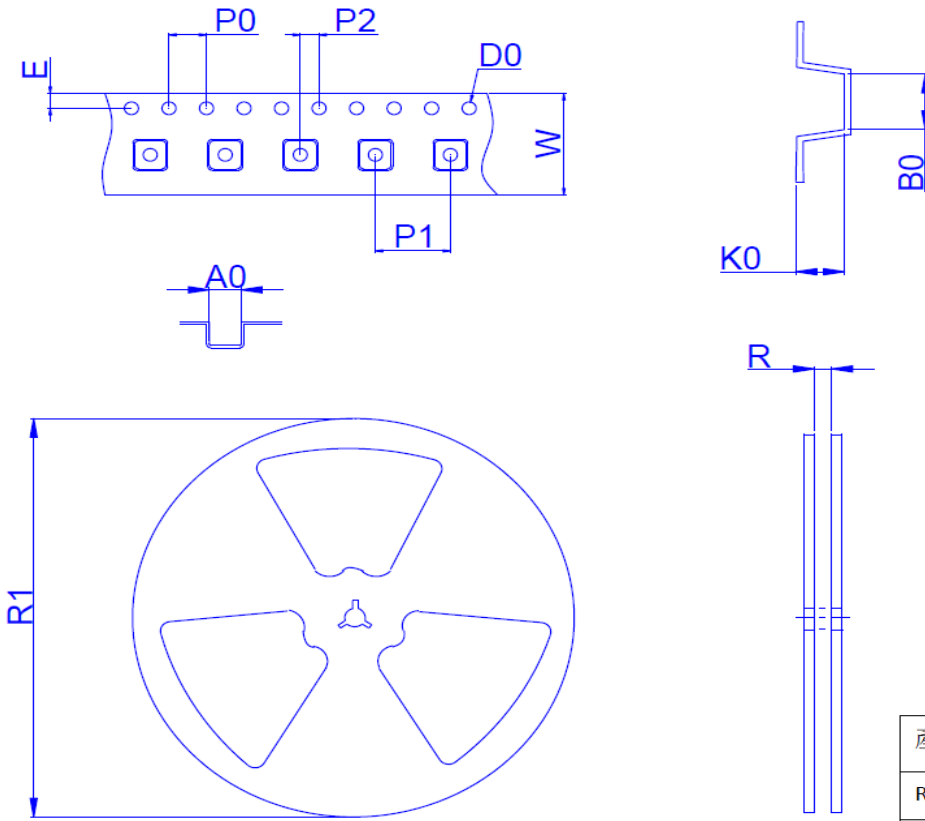


Dimension	A	A1	b	c	D	D1	E	E1	E2	e	L	L1	θ1
Min	0.65	0	0.2	0.1	2.9	2.15	3.1	2.9	1.53	0.55	0.25	-	0°
Typ.	0.75	-	0.3	0.15	3	2.45	3.2	3	1.97	0.65	0.4	0.075	10°
Max	0.9	0.05	0.4	0.25	3.3	2.74	3.5	3.3	2.59	0.75	0.6	0.15	14°

Footprint



◆ **Tape&Reel Information:5000pcs/Reel**
 (Dimension in millimeter)



產品別	EDFN3X3
Reel 尺寸	13"
編帶 方式	<p>FEED DIRECTION</p> <p>→</p>

Dimension in mm

Dimension	Carrier tape									Reel	
	A0	B0	D0	E	K0	P0	P1	P2	W	R	R1
Typ.	3.6	3.5	1.55	1.7	1.2	4	8	2	12	14	330
±	0.3	0.3	0.2	0.2	0.2	0.1	0.1	0.1	1	2	2



★Datasheet Latest version specification :

	Revision History	Prepared	Approved	Date
A.0	Initial Datasheet	Jannie	Andy	2015/10/1
A.1	Update thermal resistance coefficient and related information	Johnson	Sam	2020/3/3
A.2	Update Tape&Reel Information	Johnson	Sam	2020/11/12